NS486SXF

NS486(TM)SXF Optimized 32-Bit 486-Class Controller with On-Chip Peripherals for Embedded Systems

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NS486™SXF Optimized 32-Bit 486-Class Controller with On-Chip Peripherals for Embedded Systems

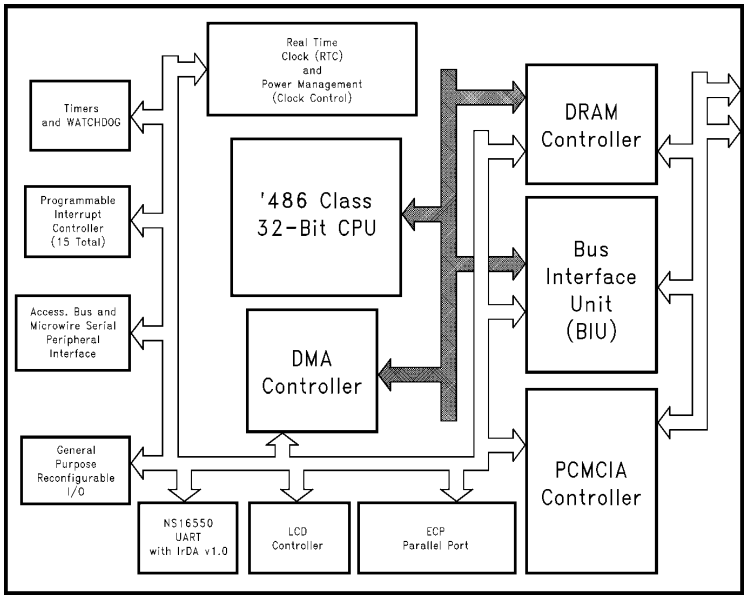
General Description

The NS486SXF is a highly integrated embedded system controller incorporating an Intel486™-class 32-bit processor, all of the necessary System Service Elements, and a set of peripheral I/O controllers tailored for embedded control systems. It is ideally suited for a wide variety of applications running in a segmented protect-mode environment.

Key Features

- 100% compatible with VxWorks®, VRTX®, QNX® Neutrino, pSOS+™, and other popular real-time executives and operating system kernels
- Intel486 instruction set compatible (protected mode only) with optimized performance
- CPU includes a 1 Kbyte Instruction Cache
- Operation at 25 MHz with 5V supply
- Low cost 160-pin PQFP package
- Industry standard interrupt controller, timers, real time clock, UART with IrDA v1.0 (Infrared Data Association) port
- Intel 82365 compatible PCMCIA interface
- Protected WATCHDOG™ timer
- Optimized DRAM Controller (supports two banks, up to 8 Mbytes each)
- Up to nine versatile, programmable chip selects
- Glueless interface to ISA peripherals
- Arbitration support for auxiliary processor
- Four external DMA channels (max. transfer rate of 25 MByte/sec @ 25 MHz) support many transfer modes
- High performance IEEE 1284 (ECP) Bidirectional Parallel Port
- MICROWIRE™/Access.bus synchronous serial interfaces
- LCD Controller for an up to 4 grey scale supertwist Liquid Crystal Displays up to 480 X 320
- Reconfigurable I/O: Up to 29 I/O pins can be used as general purpose bidirectional I/O lines
- Flexible, programmable, multilevel power saving modes maximize power savings

NS486SXF Single-Chip Embedded Controller



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NS486SXF Optimized 32-Bit 486-Class Controller with On-Chip Peripherals for Embedded Systems

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1.0 System Overview

1.1 NS486SXF SYSTEM OVERVIEW

The **NS486SXF** is a highly integrated embedded system controller. It includes an Intel486-class 32-bit processor, all resources required for the System Service Elements of a Real-Time Executive, and a generous set of peripherals. This ''system-on-a-chip'' is ideal for implementing a wide variety of embedded applications. These include (but are not limited to) fax machines, multifunction peripherals (fax, scanners, printers) mobile companions (both organizer and communicator), television set-top boxes, and telephones (mobile and desktop).

The 32-bit processor core executes all of the Intel486 instructions with a similar number of clocks per instruction. An on-board 1 kbyte instruction cache provides for efficient execution from ROM. Intel486 debug features are supported. The processor has been optimized for operating system kernels such as VRTX, VxWorks, pSOS+ and QNX. These environments only need the '486 protected mode operation (no real mode or virtual 8086 support), flat or linear memory addressing (no virtual memory paging), and floating point execution in software only (no co-processor interface).

In fact, the **NS486SXF** includes all of the System Service Elements required by a typical kernel, including an efficient DRAM controller that supports page-mode DRAMs for data cache-like performance; a six-channel DMA controller with two channels supporting data transfers from on-chip peripherals (the IEEE 1284 ECP or Extended Capabilities Port, and the LCD controller), and four channels supporting external devices such as scanners, and print engines; three timer channels (including one configured as a protected WATCHDOG Timer); two programmable 8259 interrupt controllers provide 15 on-chip interrupt sources; an industry standard real time clock and calendar (RTC) with battery backup; and support for comprehensive power management schemes.

In addition, the **NS486SXF** also incorporates the key I/O peripherals required for implementing a wide variety of embedded applications: an IEEE 1284 Bidirectional Parallel Port that includes both Host and Slave modes, an Intel 82365-compatible PCMCIA controller for one card slot, an industry standard high-performance NS16550-compatible UART with HP-SIR and IrDA v1.0 infrared option, an LCD panel interface with DMA supported refresh for many of the standard resolutions, an 8254 timer, and a general purpose 2- or 3-wire synchronous serial interface for easy interface to low-cost EEPROMs and other serial peripherals. System expansion is supported with nine programmable Chip Select (CS) signals and a generic ISA-type bus interface for external devices and memory.

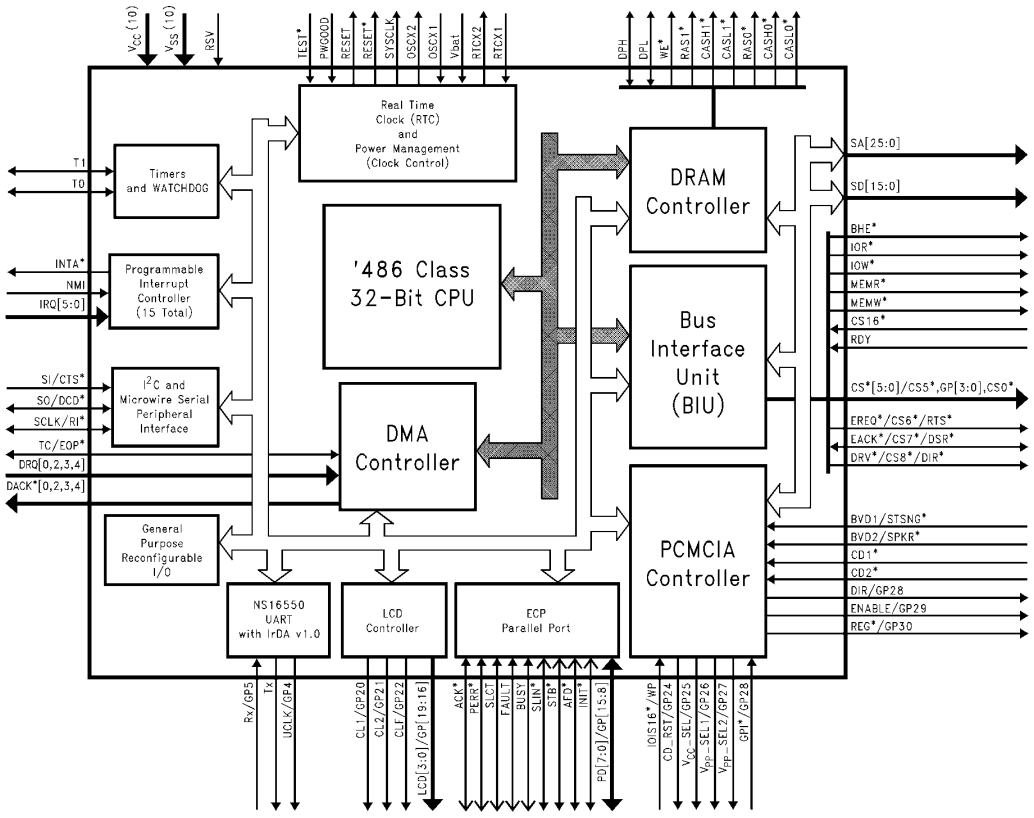

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FIGURE 1-1. NS486SXF Internal Resource to Pins Map

1.0 System Overview (Continued)

Certain I/O lines not being used by disabled peripherals can be reconfigured for use as general purpose bidirectional I/O lines (up to 29 pins). This gives the designer maximum flexibility in designing various systems using the **NS486SXF** device. It is expected that an **NS486SXF** system will minimally include the **NS486SXF** system controller with on-board processor and I/O devices, boot ROM, and working RAM memory. Many applications will not require any additional I/O support.

Finally, the **NS486SXF** implements a very flexible power management scheme that permits selective control of individual I/O subsystems, with varying levels of power consumption.

NS486SXF provides a cost-effective hardware platform for the design and implementation of a wide range of office automation and communication systems. With its powerful embedded '486-class processor, comprehensive set of on-chip peripheral controllers, flexible power management structure and reconfigurable I/O lines, NS486SXF makes possible a variety of end-user systems based on the same hardware. Because of its optimized design and on-board resources, a very cost effective system can be achieved.

1.2 32-BIT PROCESSOR CORE

The NS486SXF processor core is an implementation of the protected mode '486 instruction set architecture, optimized using a RISC-like design philosophy for embedded applications. Using this approach, the most frequently used instructions are optimized, and on an average execute in a lower number of clock cycles than a '486.

The NS486SXF features a three stage pipeline, efficient instruction prefetching mechanism, and single cycle instruction decoding for most instructions. Additionally, a 1 kbyte instruction cache and single cycle DRAM access provide higher memory performance than a larger unified cache implementation.

The NS486SXF processor provides the same programming model and register set as the standard '486 except that real mode, virtual memory, and floating point support have been eliminated. These features have little or no impact in embedded applications and save significant silicon real estate. At reset, unlike the standard '486, the NS486SXF starts up in protected mode instead of real mode. All '486 instructions appropriate to protected mode and our hardware configuration are supported, including debug instructions.

The NS486SXF is initially available to run 25 MHz at 5V. The processor clock is obtained by dividing the crystal frequency by two. For example, a 25 MHz NS486SXF runs with a 50 MHz crystal oscillator as the master clock.

As a result of our innovative design, the NS486SXF achieves performance equivalent to a standard '486 with less circuitry. This translates into reduced power consumption and a lower overall system cost. It also makes the NS486SXF ideal for ''green'' systems and battery operated systems.

1.3 SYSTEM SERVICE ELEMENTS

The **NS486SXF** controller provides the basic hardware resources required for the O/S-defined System Service Elements. These include a DRAM controller, a DMA controller, programmable interval timer, a protected WATCHDOG timer, a programmable interrupt controller, a real-time clock and calendar, and comprehensive power management features.

1.3.1 DRAM Controller

The **NS486SXF** DRAM controller supports one or two adjustable-sized banks of dynamic RAM using a 16-bit data path. Support is provided for byte parity (if desired), requiring the DRAM banks to be 18 bits wide when parity is enabled. Banks can be up to 8 Mbytes in size. The DRAM controller supports page mode read and write operations and can also support both byte and word accesses. All access control signals for read, write and parity checking are generated as well as an automatic and programmable CAS-before-RAS refresh. If self-refresh DRAMs are used, refresh can be disabled, saving power.

NS486SXF provides flexible support for use of a number of different DRAM configurations, using popular DRAM devices. Access is optimized for fast page mode DRAMs, and they will provide the highest performance with contiguous data. When accessing data bytes or words in the same DRAM page, the data access is in one cycle. This performance provides fast data access times without the overhead of a separate data cache. Page sizes can be 512, 1024, 2048 or 4096 bytes. Flexibility for DRAM timing is provided through programming of the DRAM controller registers: 3 or 4 cycle page miss accesses and extended CAS cycles can be selected.

Memory bank 0 starts at address 0h; memory bank 1 can start at any address in the 128 Mbyte address map that is a multiple of its size.

1.3.2 DMA Controller

The **NS486SXF** Direct Memory Access (DMA) controller is a high speed 16-bit controller that improves system performance by off-loading from the processor the task of managing data transfers to and from memory and external devices. Data transfers are done independently from the processor at a maximum data rate of 2 bytes per 2 clock cycles. (A 25 MHz clock yields a 25 megabyte per second transfer rate.)

There are six independent DMA channels. Requestor and target addresses have a maximum addressable memory range of 64 Mbytes. Three standard transfer modes, single, block and demand, are provided giving the designer a wide range of DMA options. A special transfer type, cascade-master, allows an external master to access the **NS486SXF** ISA-like bus. Normal transfers can be from memory to memory, memory to I/O and I/O to memory. DMA transfers are controlled by DMA control registers in the **NS486SXF** control register I/O map.

1.3.3 Programmable Interval Timer

The **NS486SXF** programmable interval timer is compatible with the Intel 8254 programmable interval timer and contains three identical timers (CH0–CH2). CH0 and CH1 can be used to generate accurate timing delays under software control. CH2 may be configured to provide a WATCHDOG timer function.

1.3.4 WATCHDOG Timer

The **NS486SXF** WATCHDOG timer, CH2, is a protected 16-bit timer that can be used to prevent system ''lockups or hangups.'' It uses a 1 kHz clock generated by the on-chip real-time clock circuit. If the WATCHDOG timer is enabled and times out, a reset or interrupt will be generated allowing graceful recovery from an unexpected system lockup.

1.0 System Overview (Continued)

1.3.5 Interrupt Controller

The **NS486SXF** interrupt controller consists of two cascaded programmable interrupt controllers that are compatible with the Intel 8259A Programmable Interrupt Controller. They provide a total of 15 (out of 16) programmable interrupts. Three interrupts are reserved for a real time clock-tick interrupt, a real time clock interrupt request, and a cascade interrupt channel. The remaining 13 interrupts can be used by internal or external sources. Additional external interrupt controllers can be cascaded as well.

1.3.6 Real Time Clock/Calendar

The **NS486SXF** Real Time Clock/Calendar is a low power clock that provides a time-of-day clock and 100-year calendar with alarm features and battery operation. Time is kept in BCD or binary format. It includes 50 bytes of general purpose CMOS RAM and 3 maskable interrupt sources. It is compatible with the DS1287 and MC146818 RTC/Calendar devices, except for the general purpose memory size.

1.3.7 Power Management Features

The **NS486SXF** power management structure includes a number of power saving mechanisms that can be combined to achieve comprehensive power savings under a variety of system conditions. First of all, the core processor power consumption can be controlled by varying the processor/system clock frequency. The internal CPU clock can be divided by 4, 8, 16, 32 or 64. In addition, in idle mode, the internal processor clock will be disabled. Finally, if an external crystal oscillator circuit is being used, it can be disabled. For maximum power savings, all internal clocks can be disabled (except for the real-time clock oscillator).

The clocks of the on-board peripherals can be individually or globally controlled. By setting bits in the power management control registers, the internal clocks to the DMA controller, the ECP port, the three-wire interface, the timer, the LCD controller, the DRAM controller, the PCMCIA controller and the UART can be disabled.

In addition to these internal clocks, the external SYSCLK can be disabled via a bit in the power management control registers.

Using various combinations of these power saving controls with the **NS486SXF** controller will result in excellent programmable power management for any application.

1.4 NS486SXF SYSTEM BUS

The **NS486SXF** system bus provides the interface to off-chip peripherals and memory. It offers an ISA-compatible interface and is therefore capable of directly interfacing to many ISA peripheral control devices. The interface is accomplished through the Bus Interface Unit (BIU). The BIU generates all of the access signals for both internal and external peripherals and memory. Depending upon whether the access is to internal peripherals, external peripherals or external memory, the BIU generates the timing and control signals to access those resources. The BIU is designed to support a glueless interface to many ISA-type peripherals.

For debug purposes, the **NS486SXF** can be set to generate external bus cycles at the same time as an internal peripheral access takes place. This gives logic analyzers or other debug tools the ability to track and capture internal peripheral accesses.

Access to internal peripherals is accomplished in three CPU T-states (clock cycles). The fastest access to off-chip I/O is also three T-states. When accessing off-chip memory and I/O, wait state generation is accomplished through a combination of **NS486SXF** chip select logic and off-chip peripheral feedback signals.

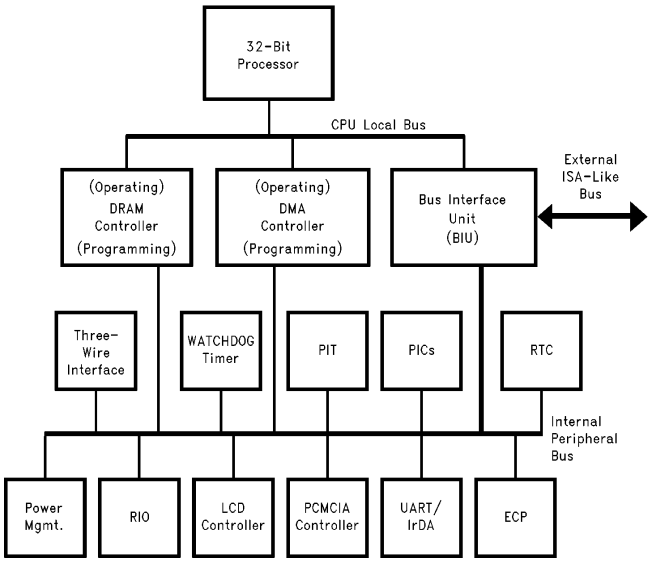

FIGURE 1-2. NS486SXF Internal Busses

1.0 System Overview (Continued)

When the CPU is in idle mode, the BIU is designed to mimic the CPU during DMA interchanges between memory and peripherals. By responding to DRQs and generating DACK, and HOLDA signals as required, the BIU eliminates the need to reactivate the CPU during such transfers as screen updates from memory to the LCD controller. This gives the designer added flexibility in conserving power while maintaining basic system functions.

1.5 OTHER ON-BOARD PERIPHERALS

In addition to those peripherals and system control elements needed for System Service Elements, the **NS486SXF** also includes a number of I/O controllers and resources that make implementing a complete embedded system possible with just a single-chip **NS486SXF** controller. These include an IEEE 1284 Extended Capabilities Port, a serial UART port, a LCD controller, a PCMCIA interface and a MICROWIRE or Access.bus synchronous serial bus interface. In addition, unused I/O controllers free up their I/O pins for general purpose use.

1.5.1 Reconfigurable I/O Lines

The **NS486SXF** supports reconfigurable I/O. For example, if the UART, ECP Parallel Port, LCD or PCMCIA functions are not being used, the I/O pins associated with them can be reconfigured as general purpose bidirectional I/O pins. Up to 29 pins can be reconfigured for this purpose. This capability makes the **NS486SXF** extremely versatile and ideal for supporting different end product configurations with a single **NS486SXF** device.

1.5.2 IEEE 1284 Bidirectional Port

The **NS486SXF** parallel port is a multifunction 8-bit parallel port that is compatible with the IEEE 1284 bidirectional parallel port standard. The operation of the parallel port is set by the content of the **NS486SXF** parallel port I/O control registers. The port can operate in one of two modes: a standard parallel port mode (PC compatible), or a full Extended Capabilities Port (ECP) mode. The **NS486SXF** ECP port can support both Host and Slave ECP mode. In slave mode, the **NS486SXF** becomes a versatile microprocessor for parallel I/O peripheral devices.

1.5.3 PCMCIA Interface

The **NS486SXF** PCMCIA interface supports the direct connection of a single PCMCIA 2.0 IC card. Exchange Card Architecture (ExCA release 1.50) compatibility and eXecute In Place (XIP) capability is also provided.

Accessing the PCMCIA interface switches the external bus automatically into the PCMCIA mode and permits Memory Window Mapping and Address Offset to be handled inside the **NS486SXF** device. Power management and ''hot'' card insertion/removal options can be implemented using external buffering, if required.

1.5.4 MICROWIRE/Access.bus Interface

The **NS486SXF** MICROWIRE/Access.bus interface provides for full support of either the three-wire MICROWIRE or the two-wire Access.bus serial interfaces. MICROWIRE has an alternate clock phasing option that supports the SPI bus protocol as well. These industry standard interfaces permit easy interfacing to a wide range of low-cost specialty memories and I/O devices. These include EEPROMs, SRAMs, timers, clock chips, A/D converters, D/A converters, and peripheral device drivers.

1.5.5 UART Serial Port

The **NS486SXF** UART provides complete NS16550 (PC standard) serial communications port compatibility including the performance enhancing 16-byte deep FIFO. It performs serial-to-parallel conversion from external devices to the **NS486SXF** and parallel-to-serial conversion from the **NS486SXF** to external peripherals. Full modem control can be supported.

A serial IrDA v1.0 and HP-SIR (infrared) mode is also supported, making possible low-cost wireless communications between an **NS486SXF**-based system and other wireless infrared systems.

1.5.6 LCD Controller

The **NS486SXF** LCD controller is capable of controlling a variety of monochrome supertwist LCD configurations including 320x240, 320x200 and 480x320 black and white or grayscale graphics LCD modules equipped with self-contained screen drivers. It uses a video frame buffer in system DRAM with either a 1- or 2-bit per pixel grayscale. A 60 Hz to 90 Hz frame refresh rate is supported. Special controls permit the fine tuning of display characteristics to precisely optimize visual display quality.

1.6 ICE SUPPORT

National Semiconductor has worked closely with Microtek International to provide hardware in-circuit emulator support for the **NS486SXF**. The Microtek product (PowerPack® EA-NS486) uses a special bondout version of the **NS486SXF** to deliver a full-featured hardware emulator that is capable of tracing on chip activity, including peripheral interrupt and I/O activity. The emulator runs at full speed, and supports overlay memory and multiple triggers.

1.7 OTHER ISSUES

NS486SXF provides a comprehensive set of on-board peripherals. Also, it is designed to easily interface to external peripherals. In addition to this ISA-like bus which supports ISA-compatible peripherals, the **NS486SXF** provides an interface to an external master with a shared memory space. The external master or auxiliary processor interface allows low cost interfacing to shared external memory belonging to other external masters (including another **NS486SXF** controller).

To program the resources of the **NS486SXF**, a set of internal control registers exists. These registers provide precise control over all internal resources and the setup of external **NS486SXF** control signals. It is the designer's responsibility to ensure the proper initialization of the registers in this I/O map.

In addition, the **NS486SXF** core processor itself requires several descriptor tables and initialization parameters that must be set by user-written start-up software.

The **NS486SXF** is designed from the ground up for optimum price/performance in embedded systems. This makes the **NS486SXF** the logical choice as the base hardware platform for executing an embedded operating system kernel such as those available from Microtec International, Wind River, ISI, QNX, and many others. Any Operating System or Real-Time Executive that will operate in a segmented or flat memory model protect mode environment is a suitable complement to the **NS486SXF**.

Also, there are many third party tool sets that will allow an executable application to be built to run directly on the target hardware without an O/S environment.

2.0 Pin Description Tables

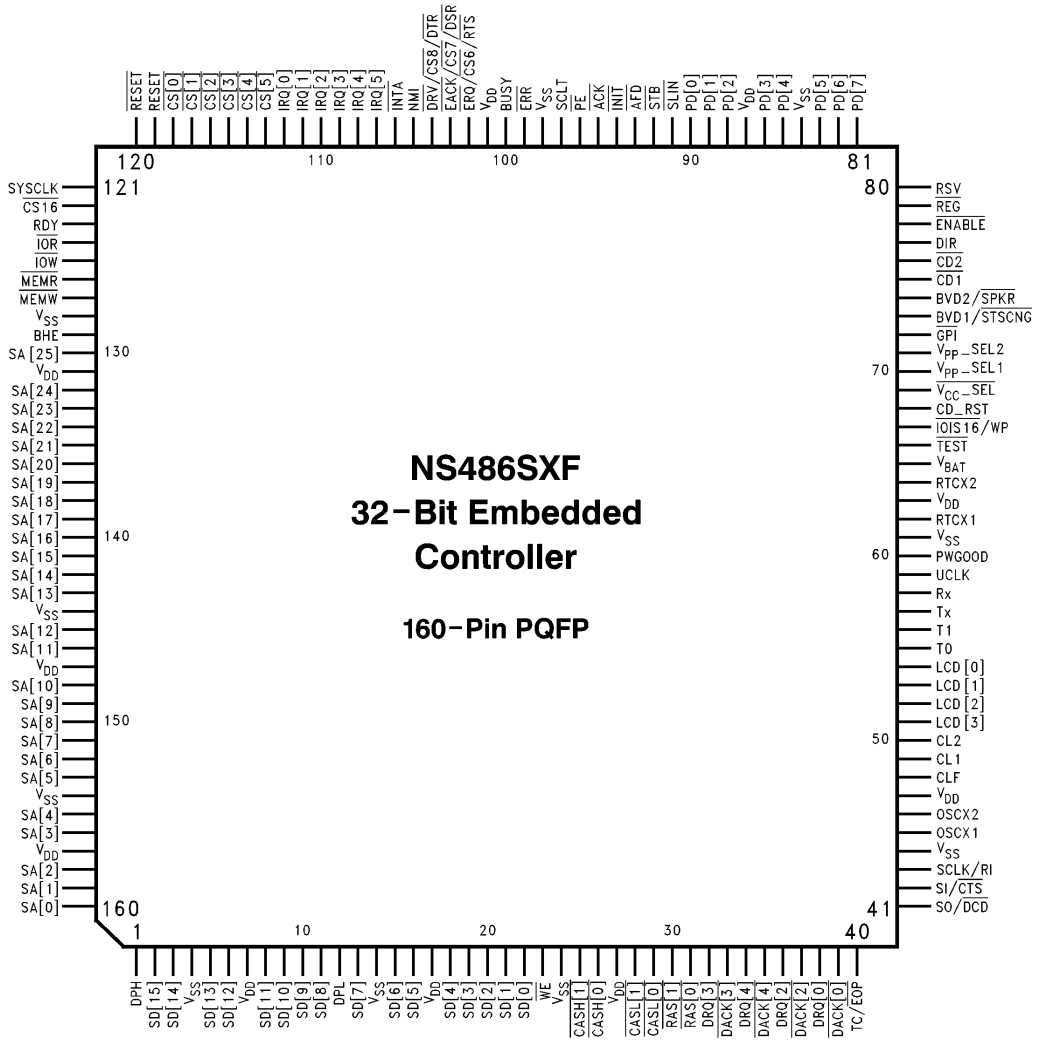

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FIGURE 2-1. NS486SXF Package Pinout Diagram

The **NS486SXF** single chip controller is provided in a compact 160-pin, industry standard JEDEC PQFP package. The following tables detail the Symbol, Type, and Description of each pin. The tables divide the pins into functional groups as follows: Bus Interface Unit Pins, DMA Control Pins, DRAM Control Pins, Power Pins, Reset Logic Pins, Auxiliary Processor Interface Pins, Test Pins, Interrupt Control Pins, Real Time Clock Pins, LCD Interface Pins, Oscillator Pins, UART/IrDA Pins, PCMCIA Pins, IEEE-1284 Port (ECP Mode) Pins, Timer Pins, 3-Wire Serial I/O Pins, General Purpose Chip Select Pins, and Reconfigurable I/O Pins. Twenty-nine I/O pins are multipurpose. In their standard modes, they perform specific I/O controller functions. When those particular I/O functions are not required in the system, however, those pins can be reprogrammed to become general purpose, bidirectional I/O lines.

Note: In the above figure and in the following tables, all active low signals are shown with an overbar.

2.0 Pin Description Tables (Continued)

TABLE 2-1. Bus Interface Unit Pins

Symbol	Pins	Type	Function
SA[25:0]	130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 145, 146, 148, 149, 150, 151, 152, 153, 155, 156, 158, 159, 160	O	**S**ystem **A**ddress bus. These output-only signals carry the latched address for the current access. DRAM accesses multiplex the row and column addresses for the DRAMs on the SA[12:1] pins. During Interrupt Acknowledge cycles, the internal master interrupt controller's cascade line signals, CAS[2:0], are driven onto SA[25:23], respectively. SA[0] is sampled at the end of reset to determine if the part will run normally or enter ICE TRI-STATE mode.
SD[15:0]	2, 3, 5, 6, 8, 9, 10, 11, 13, 15, 16, 18, 19, 20, 21, 22	I/O	**S**ystem **D**ata bus: This bi-directional data bus provides the data path for all memory and I/O accesses. During transfers with 8-bit devices, the upper data byte is not used (SD[15:8]).
$\overline{\text{SBHE}}$	129	O	**B**yte **H**igh **E**nable. This active-low signal indicates that the high byte (odd address byte) is being transferred. External 16-bit devices should use this signal to help them determine that a data byte is to be transferred on the upper byte of the System Data bus (SD[15:8]). 8-bit devices should ignore this signal. $\overline{\text{SBHE}}$ is sampled at the end of power good reset to determine if the boot ROM is 8- or 16-bit wide.
$\overline{\text{IOR}}$	124	O	**IO R**ead command. This active-low signal instructs an I/O device to place data onto the system data bus.
$\overline{\text{IOW}}$	125	O	**IO W**rite command. This active-low signal indicates to an I/O device that a write operation is in process on the system bus.
$\overline{\text{MEMR}}$	126	O	**MEM**ory **R**ead command. This active-low signal instructs a memory mapped device to place data onto the system data bus.
$\overline{\text{MEMW}}$	127	O	**MEM**ory **W**rite command. This active-low signal indicates to a memory mapped device that a write operation is in process on the system bus.
$\overline{\text{CS16}}$	122	I/O	**C**hip **S**elect **16**-bit. This active-low feedback signal indicates that the device being accessed is a 16-bit device. This signal should be driven by external devices with an open collector driver. If a chip select is programmed to force 16-bit accesses, this signal will be asserted (low) during the access.
RDY	123	I	**R**ea**DY**. An external device may drive this signal inactive low to insert wait states and extend the external bus cycle. This signal should be driven with an open collector or be TRI-STATE driven.

2.0 Pin Description Tables (Continued)

TABLE 2-2. DMA Control Pins

Symbol	Pins	Type	Function
DRQ[4], DRQ[3], DRQ[2], DRQ[0]	34, 32, 36, 38	I	**D**MA **R**e**Q**uest. A DRQn signal requests the internal DMA Controller to transfer data between the Requesting Device and memory.
$\overline{\text{DACK}}$[4], $\overline{\text{DACK}}$[3], $\overline{\text{DACK}}$[2], $\overline{\text{DACK}}$[0]	35, 33, 37, 39	O	**D**MA **ACK**nowledge: When the CPU has relinquished control of the bus to a requesting DMA channel, the appropriate active-low $\overline{\text{DACK}}$n signal acknowledges the winning DRQn.
TC/$\overline{\text{EOP}}$	40	I/O	**T**erminal **C**ount/**E**nd **O**f **P**rocess: This signal may operate either as a terminal count output or an active-low End of Process input. As TC, an active-high pulse occurs on this signal when the terminal count for any DMA channel has been reached. As $\overline{\text{EOP}}$, an external device may terminate the DMA transfer by driving this signal active-low.

TABLE 2-3. DRAM Control Pins

Symbol	Pins	Type	Function
$\overline{\text{RAS}}$[1:0]	30, 31	O	**R**ow **A**ddress **S**trobe. On the falling edge of these active-low signals, Bank 1 and Bank 0 respectively, should latch in the row address off of SA[12:1]. If only one bank of DRAMs are supported, $\overline{\text{RAS0}}$ will support that bank and $\overline{\text{RAS1}}$ will be unused.
$\overline{\text{CASH}}$[1:0]	25, 26	O	**C**olumn **A**ddress **S**trobe (**H**igh Byte). These active-low signals indicate when the column access is being made to the high byte of DRAM Bank 1 and DRAM Bank 0 respectively. If only one bank of DRAMs are supported, $\overline{\text{CASH0}}$ will support the high byte of that bank and $\overline{\text{CASH1}}$ will be unused.
$\overline{\text{CASL}}$[1:0]	28, 29	O	**C**olumn **A**ddress **S**trobe (**L**ow Byte). These active-low signals indicate when the column access is being made to the low byte of DRAM Bank 1 and DRAM Bank 0, respectively. If only one bank of DRAMs are supported, $\overline{\text{CASL0}}$ will support the low byte of that bank and $\overline{\text{CASL1}}$ will be unused.
$\overline{\text{WE}}$	23	O	**W**rite **E**nable. Active low signal for writing the data into the DRAM bank.
DPH, DPL	1, 12	I/O	DRAM **D**ata **P**arity. DRAM data parity may be enabled or disabled; if disabled these two pins will be unused. Otherwise, for DRAM writes the **NS486SXF**'s DRAM Controller will generate odd parity and drive the odd parity onto these two pins. For DRAM reads the **NS486SXF**'s DRAM Controller will read the values driven on these two pins and check it for odd parity in association with the appropriate data byte.

2.0 Pin Description Tables (Continued)

TABLE 2-4. Power Pins

Symbol	Pins	Type	Function
V_{DD}	7, 17, 27, 47, 63, 87, 101, 131, 147, 157	I	+5V power to core and I/O.
V_{SS}	4, 14, 24, 44, 61, 84, 98, 128, 144, 154	I	Ground to core and I/O.

TABLE 2-5. Reset Logic Pins

Symbol	Pins	Type	Function
RESET	119	O	**RESET** system output driver: This active high signal resets or initializes system peripheral logic during power up or during a low line voltage outage.
$\overline{\text{RESET}}$	120	O	Inverse of **RESET** for peripherals requiring active low reset.
PWGOOD	60	I	**P**o**W**er **GOOD**. This active-high (Schmitt Trigger) input will cause a hardware reset to the **NS486SXF** whenever this input goes low. This pin will typically be driven by the power supply and PWGOOD will remain low until the power supply determines that stable and valid voltage levels have been achieved.

TABLE 2-6. Auxiliary Processor Interface Pins

Symbol	Pins	Type	Function
$\overline{\text{EREQ}}$/CS6/$\overline{\text{RTS}}$	102	O	This pin has three programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. **E**xternal bus **REQ**uest (active-low) to an auxiliary processor. 2. **C**hip **S**elect **6** (active-low) pin. 3. **R**equest **T**o **S**end. When low, this signal informs the MODEM or data set that the UART is ready to exchange data. The $\overline{\text{RTS}}$ output signal can be set to an active low by programming bit 2 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{\text{EACK}}$/CS7/$\overline{\text{DSR}}$	103	I/O I O I	This pin has three possible programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. **E**xternal bus **ACK**nowledge (active-low) from an auxiliary processor. 2. **C**hip **S**elect **7** (active-low) pin. 3. **D**ata **S**et **R**eady. When low, it indicates that the MODEM or data set is ready to link with the UART. The $\overline{\text{DSR}}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{\text{DSR}}$ input has changed state since the previous reading of the MODEM Status Register. **Note:** Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{\text{DRV}}$/CS8/$\overline{\text{DTR}}$	104	O	This pin has three possible programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. DSP shared memory **DR**i**V**e control signal. 2. **C**hip **S**elect **8** (active-low) pin. 3. **D**ata **T**erminal **R**eady. When low, this signal informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{\text{DTR}}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

2.0 Pin Description Tables (Continued)

TABLE 2-7. Test Pins

Symbol	Pins	Type	Function
$\overline{\text{TEST}}$	66	I/O	Reserved for testing and development system support.

TABLE 2-8. Interrupt Control Pins

Symbol	Pins	Type	Function
NMI	105	I	**N**on-**M**askable **I**nterrupt. This active-high signal will generate a non-maskable interrupt to the CPU when it is active high. Normally this signal is used to indicate a serious system error.
$\overline{\text{INTA}}$	106	O	**INT**errupt **A**cknowledge. During each interrupt acknowledge cycle this signal will strobe low; it should be used by external cascaded interrupt controllers.
IRQ[5:0]	107, 108, 109, 110, 111, 112	I	**I**nterrupt **R**e**Q**uests. These inputs are either rising edge or low-level sensitive interrupt requests, depending on the configuration of the internal interrupt controllers. These interrupt requests may also be programmed to support externally cascaded interrupt controller(s). The IRQ pins are also used to select a particular test in test mode. If the PCMCIA controller is enabled, IRQ[5] becomes the $\overline{\text{IREQ}}$ signal.

TABLE 2-9. Real Time Clock Pins

Symbol	Pins	Type	Function
RTCX1	62	I	**R**eal **T**ime **C**lock crystal oscillator input: 32 kHz crystal.
RTCX2	64	O	**R**eal **T**ime **C**lock crystal oscillator output: 32 kHz crystal.
V_{bat}	65	I	External + battery input for real time clock.

TABLE 2-10. LCD Interface Pins

Symbol	Pins	Type	Function
LCD[3:0]	51, 52, 53, 54	O	**Data** Output Word to **LCD**, 1 = White, 0 = Blue/black.
CL2	50	O	Word **CL**ock to LCD.
CL1	49	O	Row **CL**ock to LCD.
CLF	48	O	**F**rame **CL**ock to LCD.

TABLE 2-11. Oscillator Pins

Symbol	Pins	Type	Function
SYSCLK	121	O	**SYS**tem **CL**oc**K**. This clock output pin will either be driven with a signal half the frequency of the OSCX1 input clock frequency or the CPU's clock frequency, which is determined in the Power Management Control Register 1. The source selection for this signal is determined by bit 1 of the Power Management Control Register 3.
OSCX1	45	I	**OSC**illator Crystal **1** input. This pin should either be driven by a TTL oscillator or be connected to an external crystal circuit. This signal is the fundamental clock source for all clocked elements in the **NS486SXF**, except the Real-Time Clock, which has its own crystal pins.
OSCX2	46	O	**OSC**illator Crystal **2** output. This is the output side of the **NS486SXF** on-chip circuitry provided to support an external crystal circuit. If a TTL oscillator drives OSCX1, this pin should be a no connect.

2.0 Pin Description Tables (Continued)

TABLE 2-12. HP-SIR/UART Pins

Symbol	Pins	Type	Function
Tx	57	O	UART Transmit data. In HP-SIR mode this pin is the UART output encoded for the serial infrared link. Otherwise it is the transmit output of the 16550 UART.
Rx	58	I	UART Receive data. In HP-SIR mode this pin is routed through the serial infrared decoder. Otherwise, it is the receive input to the 16550.
UCLK	59	O	**U**art **CL**oc**K**. Output of programmable rate UART/MODEM clock. Typically used for the Infrared Modulator.

TABLE 2-13. PCMCIA Pins

Symbol	Pins	Type	Function
CD__RST	68	O	**C**ar**D** **R**e**S**e**T**. This active high signal resets the PCMCIA card during a soft-reset.
$\overline{IOIS16}$/WP	67	I	**IO** port **IS 16** bits/**W**rite **P**rotect: When a PCMCIA card is configured as an IO card, this signal is asserted to indicate the currently addressed IO port is 16 bits wide. When a PCMCIA card is configured as a memory card, an active high signal indicates the card is currently write protected.
BVD2/$\overline{SPKR}$	74	I	**B**attery **V**oltage **D**etect bit **2**/ **SP**ea**K**e**R** output. When a PCMCIA card is configured as a memory card, this input along with BVD[1] will provide status information about the card's on-board battery condition. When a PCMCIA card is configured as an IO card, this pin will act as the audio output of the card to the system.
BVD1/$\overline{STSCNG}$	73	I	**B**attery **V**oltage **D**etect bit **1**/ **ST**atu**S** **C**ha**NG**e output. When a PCMCIA card is configured as a memory card, this input along with BVD[2] will provide status information about the card's on-board battery state. When a PCMCIA card is configured as an I/O card, the status change signal indicates one or more of the memory status signals (BVD[2:1], WP, RDY or $\overline{BSY}$) has changed states.
$\overline{V_{CC}}$—$\overline{SEL}$	69	O	PCMCIA **V_{CC} SEL**ect. When this signal is low, the V_{CC} power to the PCMCIA card should be enabled.
V_{PP}—SEL1, V_{PP}—SEL2	70, 71	O	PCMCIA **V_{PP} SEL**ect 1 and 2. These signals indicate the voltage with which the V_{PP} power to the PCMCIA card should be driven.
$\overline{GPI}$	72	I	**G**eneral **P**urpose **I**nput. This signal is a general purpose input signal used with a PCMCIA card to indicate a valid V_{PP} state, a pending card eject/insertion, or as an interrupt source.
$\overline{CD2}$, $\overline{CD1}$	76, 75	I	**C**ard **D**etect. Both signals are low when the PCMCIA card is correctly inserted.
DIR	77	O	**DIR**ection. Used to control the direction of the data line buffers to the PCMCIA interface.
$\overline{ENABLE}$	78	O	**$\overline{ENABLE}$** PCMCIA. Enables the buffer drivers to the PCMCIA interface. Low true signal.
$\overline{REG}$	79	O	**$\overline{REG}$**. PCMCIA card support.

Note: If PCMCIA is enabled, Chip Selects 1 and 2 become Card Enable 1 and 2. See Table 2-17, ''General Purpose Chip Select Pins''. Also, IRQ[5] becomes the PCMCIA $\overline{IREQ}$ signal.

2.0 Pin Description Tables (Continued)

TABLE 2-14. IEEE-1284 Port (ECP Mode)

Symbol	Pins	Type	Function
PD[7:0]	81, 82, 83, 85, 86, 88, 89, 90	O/I	**P**arallel **D**ata. Bi-directional data pins transfer data and address information to and from the parallel port.
$\overline{\text{SLIN}}$	91	O/I	**S**e**L**ect **IN**put: Used in a closed-loop handshake with $\overline{\text{BUSY}}$ to transfer data or address information from the host to the peripheral. Host driven.
$\overline{\text{STB}}$	92	O/I	data **ST**ro**B**e. Driven high by the host while in ECP Mode. Asserted low by host to terminate ECP Mode and return link to Compatibility Mode. Host driven.
$\overline{\text{AFD}}$	93	O/I	**A**utomatic **F**ee**D**. The host asserts this line low for flow control in the reverse direction. It is used in a interlocked handshake with $\overline{\text{ACK}}$. Provides command information in the forward direction. Host driven. Active low.
$\overline{\text{INIT}}$	94	O/I	**INIT**ialize.When this signal is asserted low to place the data channel in the reverse direction, the peripheral is allowed to drive the data bus. Host driven. Active low.
$\overline{\text{ACK}}$	95	I/O	**ACK**nowledge. Used in closed-loop handshake with $\overline{\text{AFD}}$ to transfer data to the host. Peripheral device drive. Active low.
$\overline{\text{PE}}$	96	I/O	**P**eripheral **E**rror. Asserted low to acknowledge $\overline{\text{INIT}}$, reverse request. Peripheral device drive.
SLCT	97	I/O	**S**e**L**e**CT**. Asserted high when selected or indicating an affirmative response for each respective extensibility byte. Peripheral device drive. Active high.
$\overline{\text{ERR}}$	99	I/O	**ERROR**. This input is asserted low by the peripheral to request host communications. Valid only in the forward direction. Peripheral device drive. Active low.
BUSY	100	I/O	**BUSY**. This is asserted low by the peripheral for flow control in the forward direction, de-asserted to acknowledge transfer of data or address completion. Peripheral device drive. Active low.

TABLE 2-15. Timer Pins

Symbol	Pins	Type	Function
T0	55	I/O	Programmable **T**imer pin **0**. This Bidirectional pin may be selected to control one of the following four functions via bits 1-0 of the Timer I/O Control Register: 1. The GATE input into Timer 0. 2. The GATE input into Timer 1. 3. The OUT output from Timer 0. 4. The CLK input into Timer 1.
T1	56	I/O	Programmable **T**imer pin **1**. This Bidirectional pin may be selected to control one of the following four functions via bits 3-2 of the Timer I/O Control Register: 1. The GATE input into Timer 0. 2. The GATE input into Timer 1. 3. The OUT output from Timer 1. 4. The CLK input into Timer 0.

2.0 Pin Description Tables (Continued)

TABLE 2-16. 3-Wire Serial I/O Pins

Symbol	Pins	Type	Function
SO/$\overline{DCD}$	41	I/O	This pin has two possible programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. The **S**erial data **O**utput signal for MICROWIRE. 2. **D**ata **C**arrier **D**etect. When low, this input signal indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. **Note:** Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
SI/$\overline{CTS}$	42	I/O	This pin has two possible programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. The **S**erial data **I**nput signal for MICROWIRE or the serial data I/O for Access.bus. 2. **C**lear **T**o **S**end. When low, this input signal indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. **Note:** Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
SCLK/$\overline{RI}$	43	I/O O I	This pin has two possible programmable options controlled by the Modem Signal Control Register (refer to the UART section): 1. The **S**erial **CL**oc**K** signal for MICROWIRE and Access.bus. 2. Ring Indicator. When low, this input signal indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to high state since the previous reading of the MODEM Status Register. **Note:** Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled. **Note:** Whenever the **RI bit** of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Note: For MICROWIRE Slave Mode, a pin must be selected to be the Chip Select Input.

2.0 Pin Description Tables (Continued)

TABLE 2-17. General Purpose Chip Select Pins

Symbol	Pins	Type	Function
$\overline{CS[0]}$	118	O	**C**hip **S**elect **0**: This output is used as the chip-select for the system boot ROM. It defaults to the upper 64 kbytes of memory.
$\overline{CS}$[5:1]	113, 114, 115, 116, 117	I/O	**C**hip **S**elect **1-5**. These pins can be programmed to be either memory or I/O mapped chip selects, which are used for glue-less connection to external peripherals. When the PCMCIA Controller is enabled $\overline{CS[1]}$ and $\overline{CS[2]}$ become PCMCIA Card Enable outputs 1 and 2 ($\overline{CE1}$ and $\overline{CE2}$, respectively).

TABLE 2-18. Summary of Reconfigurable I/O Pins

Symbol	Pins	Type	Pin #	Original Function	Power Up State
$\overline{REG}$	1	I/O	79	PCMCIA	TRI-STATE
$\overline{ENABLE}$	1	I/O	78	PCMCIA	1
DIR	1	I/O	77	PCMCIA	0
$\overline{GPI}$	1	I/O	72	PCMCIA	TRI-STATE
V_{PP}__SEL2	1	I/O	71	PCMCIA	0
V_{PP}__SEL1	1	I/O	70	PCMCIA	0
V_{CC}__$\overline{SEL}$	1	I/O	69	PCMCIA	1
CD__RST	1	I/O	68	PCMCIA	TRI-STATE
CLF	1	I/O	48	LCD	0
CL2	1	I/O	50	LCD	0
CL1	1	I/O	49	LCD	0
LCD [3:0]	4	I/O	51, 52, 53, 54	LCD	0, 0, 0, 0
PD [7:0]	8	I/O	81, 82, 83, 85, 86, 88, 89, 90	ECP	TRI-STATE
Rx	1	I/O	58	UART	TRI-STATE
UCLK	1	I/O	59	UART	Oscillating
$\overline{CS[4]}$	1	I/O	114	CS4	1
$\overline{CS[3]}$	1	I/O	115	CS3	1
$\overline{CS[2]}$	1	I/O	116	CS2	1
$\overline{CS[1]}$	1	I/O	117	CS1	1

These 29 pins, typically used for various I/O peripheral purposes, as defined in the above tables, can be reconfigured for use as general purpose I/O pins if the normally defined I/O function is not required.

3.0 Device Specifications

3.1 DC ELECTRICAL SPECIFICATIONS 5V ± 5%

3.1.1 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
T_A	Operating Temperature		0		+70	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 kΩ (Note 1)	2000			V

3.1.2 Absolute Maximum Ratings (Notes 2 and 3)

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}, V_{DDA}	Supply Voltage		−0.5	7.0	V
V_I	Input Voltage		−0.5	V_{DD} + 0.5	V
V_O	Output Voltage		−0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		−65	+165	°C
T_L	Lead Temperature Soldering (10 sec.)			+260	°C

3.1.3 Capacitance: T_A = 25°C, f = 1 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance			5	7	pF
C_{IN1}	Clock Input Capacitance			8	10	pF
C_{IO}	I/O Pin Capacitance			10	12	pF
C_O	Output Pin Capacitance			6	8	pF

3.0 Device Specifications (Continued)

3.1.4 DC Characteristics (Under Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
I_{CC}	V_{DD} Average Supply Current	V_{IL} = 0.5V V_{IH} = 2.4V No Load				mA

Note 1: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

Note 2: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

3.1.4.1 EXTERNAL BUS

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{OH}	Output High Voltage	I_{OH} = −6 mA (Nch Quiet-drive) or I_{OH} = −24 mA (High-drive) on: SA12–1, DP1–0, SD15–0 I_{OH} = −12 mA on: SA0, SA25–13 [SA0 − min. 10 kΩ pullup]	2.4		V	Max Load on SA12–1 is 100 pF, and SD0–15 is 50 pF
V_{OL}	Output Low Voltage	I_{OL} = 20 mA on: SA12–1, DP1–0, SD15–0 I_{OL} = 12 mA on: SA0, SA25–13, $\overline{BHE}$		0.4	V	

3.1.4.2 DMA CONTROL UNIT

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{OH}	Output High Voltage	I_{OH} = −6 mA on: TC/$\overline{EOP}$ I_{OH} = −4 mA on: $\overline{DACK4}$, $\overline{DACK3}$, $\overline{DACK2}$, $\overline{DACK0}$	2.4		V	
V_{OL}	Output Low Voltage	I_{OL} = 6 mA on: TC/$\overline{EOP}$ I_{OL} = 4 mA on: $\overline{DACK4}$, $\overline{DACK3}$, $\overline{DACK2}$, $\overline{DACK0}$		0.4	V	

3.1.4.3 DRAM CONTROL UNIT

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{OH}	Output High Voltage	I_{OH} = −6 mA(Nch Quiet-drive) or I_{OH} = −24 mA (High-drive) on: $\overline{RAS}$0–1, $\overline{CASH}$0–1, $\overline{CASL}$0–1, $\overline{WE}$	2.4		V	Max load on $\overline{RAS}$1–0, $\overline{CASH}$1–0, and $\overline{CASL}$1–0 is 63 pF
V_{OL}	Output Low Voltage	I_{OL} = 20 mA on: $\overline{RAS}$1–0, $\overline{CASH}$1–0, $\overline{CASL}$1–0, $\overline{WE}$		0.4	V	Max load on $\overline{WE}$ is 100 pF

3.0 Device Specifications (Continued)

3.1.4.4 AUXILIARY PROCESSOR INTERFACE

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -6$ mA on: $\overline{EACK}$ $I_{OH} = -4$ mA on: $\overline{DRV}$, $\overline{EREQ}$	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 6$ mA on: $\overline{EACK}$ $I_{OL} = 4$ mA on: $\overline{DRV}$, $\overline{EREQ}$		0.4	V	

3.1.4.5 HP-SIR/UART

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$ $I_{OH} = -6$ mA on: Tx, UCLK, Rx	$V_{CC} - 0.2$ 2.4		V V	
V_{OL}	Output Low Voltage	$I_{OL} = 100\ \mu A$ $I_{OL} = 6$ mA on: Tx, UCLK, Rx		0.2 0.4	V V	

3.1.4.6 EXTERNAL BUS CONTROL

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -12$ mA on: $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, RESET, $\overline{RESET}$, $\overline{CS16}$, $\overline{BHE}$ [$\overline{CS16}$ - min. 10 kΩ pullup]	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 12$mA on: $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, RESET, $\overline{RESET}$, $\overline{CS16}$, $\overline{BHE}$		0.4	V	

3.1.4.7 OSCILLATOR (CPUX1/CLK)

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -12$ mA on: SYSCLK	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA on: SYSCLK		0.4	V	
V_{IH}	OSCX1 Input High Voltage		2.4			OSCX2 is the output
V_{IL}	OSCX2 Input Low Voltage			0.4	V	

3.1.4.8 LCD INTERFACE

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -2.6$ mA on: LCD[3:0], CL1, CL2, CLF	$V_{CC} - 0.8$		V	CMOS Level
V_{OH}	Output High Voltage	$I_{OH} = -6$ mA on: LCD[3:0], CL1, CL2, CLF	2.4		V	TTI Level
V_{OL}	Output Low Voltage	$I_{OL} = 6$ mA on: LCD[3:0], CL1, CL2, CLF		0.4	V	

3.0 Device Specifications (Continued)

3.1.4.9 REAL TIME CLOCK (RTCX1/CLK)

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{IH}	RTCX1 Input High Voltage		2.0			RTCX2 is the output
V_{IL}	RTCX1 Input Low Voltage			0.4	V	
V_{BAT}	Battery Voltage		2.4		V	Lithium Battery
I_{BAT}	Battery Current	V_{BAT} = 3.0 V		3	μA	

3.1.4.10 PCMCIA (RIO8-15)

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	I_{OH} = −12 mA on: V_{CC}_SEL, V_{PP}_SEL1, V_{PP}_SEL2 I_{OH} = −6 mA on: DIR, ENABLE, $\overline{REG}$, CD_RST, BUSY_LED, $\overline{GPI}$, RSV (RSV is a reserved usage pin)	2.4		V	Power Switch 1 Card at a 50 pF Load
V_{OL}	Output Low Voltage	I_{OL} = 12 mA on: V_{CC}_SEL, V_{PP}_SEL, V_{PP}_SEL2 I_{OL} = 6 mA on: DIR, ENABLE, $\overline{REG}$, CD_RST, BUSY_LED, $\overline{GPI}$, RSV (RSV is a reserved usage pin)		0.4	V	

3.1.4.11 IEEE-1284 PORT (ECP MODE) AND (RIO16-31)

Symbol	Parameter	Condition	Min	Max	Unit	Notes
I_{CH}	High-Level Output Current (Note 4)	V_{OH} = 2.4V on: PD[7:0], $\overline{SLIN}$, $\overline{STB}$, $\overline{AFD}$, PE, $\overline{INIT}$, $\overline{ACK}$, SLCT $\overline{ERR}$, BUSY	14		mA	
I_{CL}	Low-Level Output Current	V_{OL} = 0.4V on: PD[7:0], $\overline{SLIN}$, $\overline{STB}$, $\overline{AFD}$, PE, $\overline{INIT}$, $\overline{ACK}$, SLCT $\overline{ERR}$, BUSY	14		mA	

Note 4: When ECP mode 0, or ECP mode 2 and bit 1 of PCR is 0 for the parallel port, are selected, pins AFD, INIT, SLIN, and STB are open drain supports. 4.7 kΩ resistors should be used. The ECP I/Os have over-voltage protection against being backdriven by higher external voltages when the I/Os are at TRI-STATE. The I/Os also isolate the NS486SXF power-rail from external voltages when the chip is powered down. The maximum power-down leakage is 1 mA to ground.

3.1.4.12 TIMER

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	I_{OH} = −6 mA on: T0, T1	2.4		V	
V_{OL}	Output Low Voltage	I_{OL} = 6 mA on: T0, T1		0.4	V	

3.0 Device Specifications (Continued)

3.1.4.13 GENERAL PURPOSE CHIP SELECTS

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -6$ mA on: $\overline{CS}5-0$	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 6$ mA on: $\overline{CS}5-0$		0.4	V	

3.1.4.14 INTERRUPT CONTROLLER

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -12$ mA on: $\overline{INTA}$	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA on: $\overline{INTA}$		0.4	V	

3.1.4.15 3-WIRE I/O (AND ACCESS.BUS)

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	$I_{OH} = -12$ mA on: SO, SI, SCLK	2.4		V	
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA on: SO, SI, SCLK		0.4	V	

3.0 Device Specifications (Continued)

3.2 GENERAL AC SPECIFICATIONS

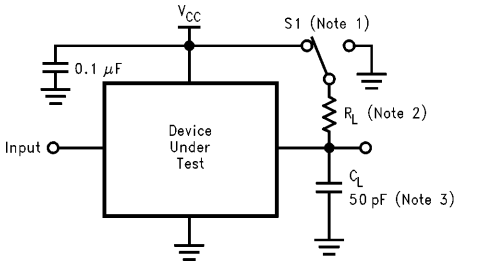
AC TEST CONDITIONS

Note 1: S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements
S_1 = GND for t_{PZL}, and t_{PHZ} measurements
S_1 = Open for push-pull outputs

Note 2: R_L = 1.1k

Note 3: C_L includes scope and jig capacitance

Test Circuit for Output Tests



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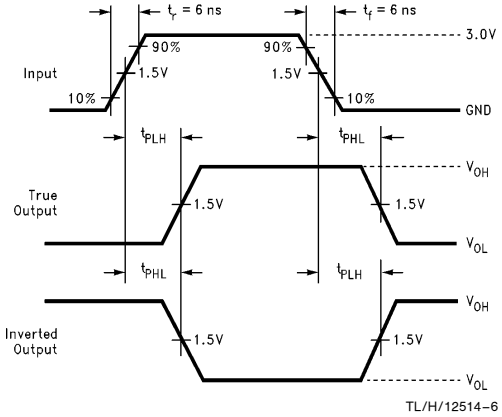
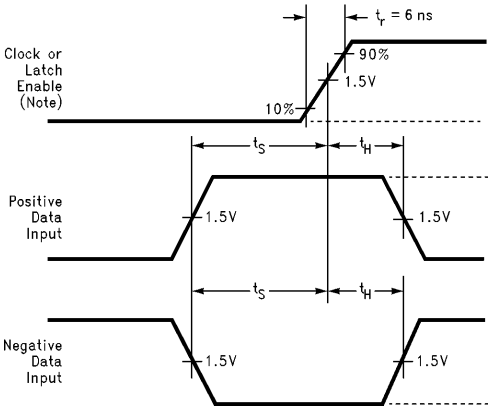
Propagation Delay Waveforms



TL/H/12514–6

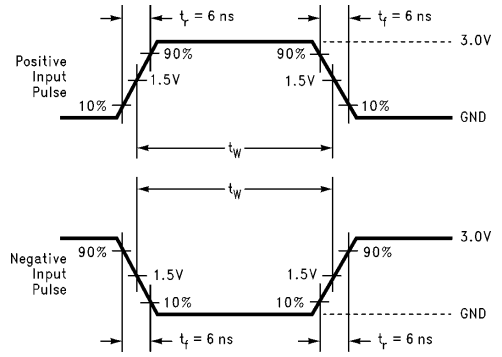
Setup and Hold Time Waveforms



TL/H/12514–7

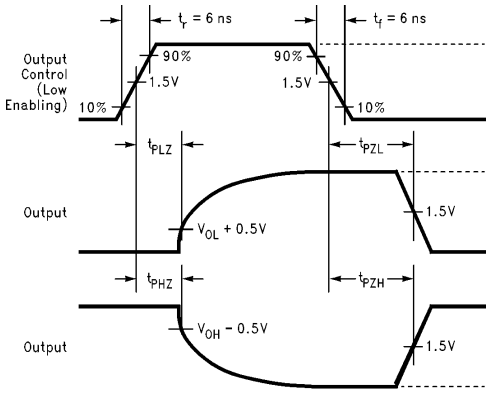
Note: Waveform for negative edge sensitive circuits will be invert.

Input Pulse Width Waveforms Except for Clock Pins



TL/H/12514–8

TRI-STATE Output Enable and Disable Waveforms

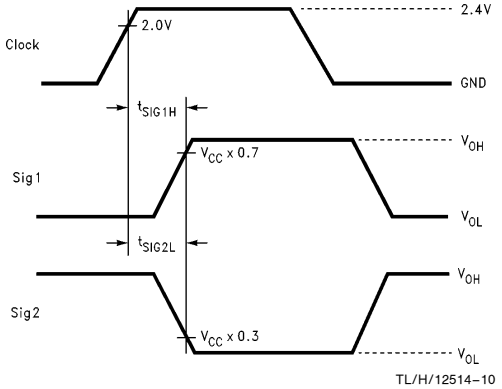


TL/H/12514–9

FIGURE 3-1. Switching Characteristic Measurement Waveforms

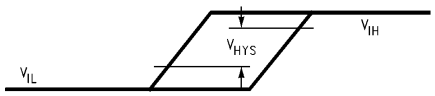
3.0 Device Specifications (Continued)

LCD Output Specification Standard



TL/H/12514–10

Hysteresis Input Specification Standard



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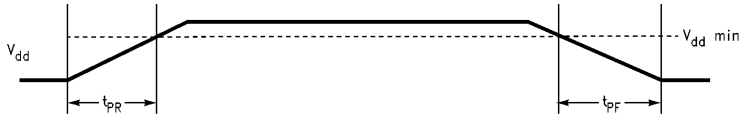
V_{HYS} = 200 mV
Switching thresholds not specified

FIGURE 3-2. More Switching Specifications

3.2.1 Power Ramp Times



TL/H/12514–12

FIGURE 3-3. Power Supply Rise and Fall

TABLE 3-1. V_{DD} Rise and Fall Times

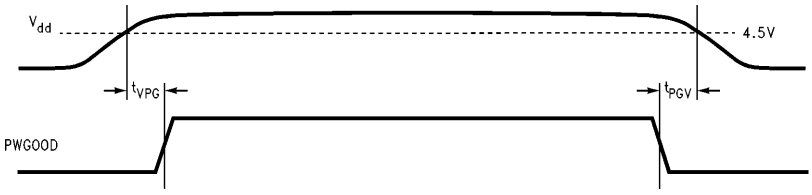
Symbol	Parameter	Min	Max	Unit
t_{PF}	V_{DD} Falling Time from 4.5V to 0V	5		ms
t_{PR}	V_{DD} Rising Time from 0V to 4.5V	5		ms

Note: The rising/falling rate is assumed linear.

3.2.2 PWRGOOD and Power Rampdown Timing

TABLE 3-2. V_{DD} Rampdown vs PWRGOOD

Symbol	Parameter	Min	Max	Unit
t_{VPG}	V_{DD} (4.5V) to PWGOOD High	1		μs
t_{PGV}	PWGOOD Falling to V_{DD} (4.5V)	1		μs



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Note: The rising/falling rate is assumed linear.

FIGURE 3-4. PWGOOD in Relation to V_{DD}

3.0 Device Specifications (Continued)

3.3 AC SWITCHING SPECIFICATIONS

The following pages list some of the preliminary AC Specifications for the NS486SXF. All parameters are listed in alphabetical order according to their Symbol.

The Tables consist of the following:

Parameter — A short description of the specification being documented.

Symbol — A quick reference between the timing diagram and the Table entries.

Formula — An equation, which in addition to the Minimum and Maximum Specifications can be used to determine the actual timing provided at any operating frequency.

Min. — Minimum Specification when added to the value produced by the formula.

Max. — Maximum Specification when added to the value produced by the formula.

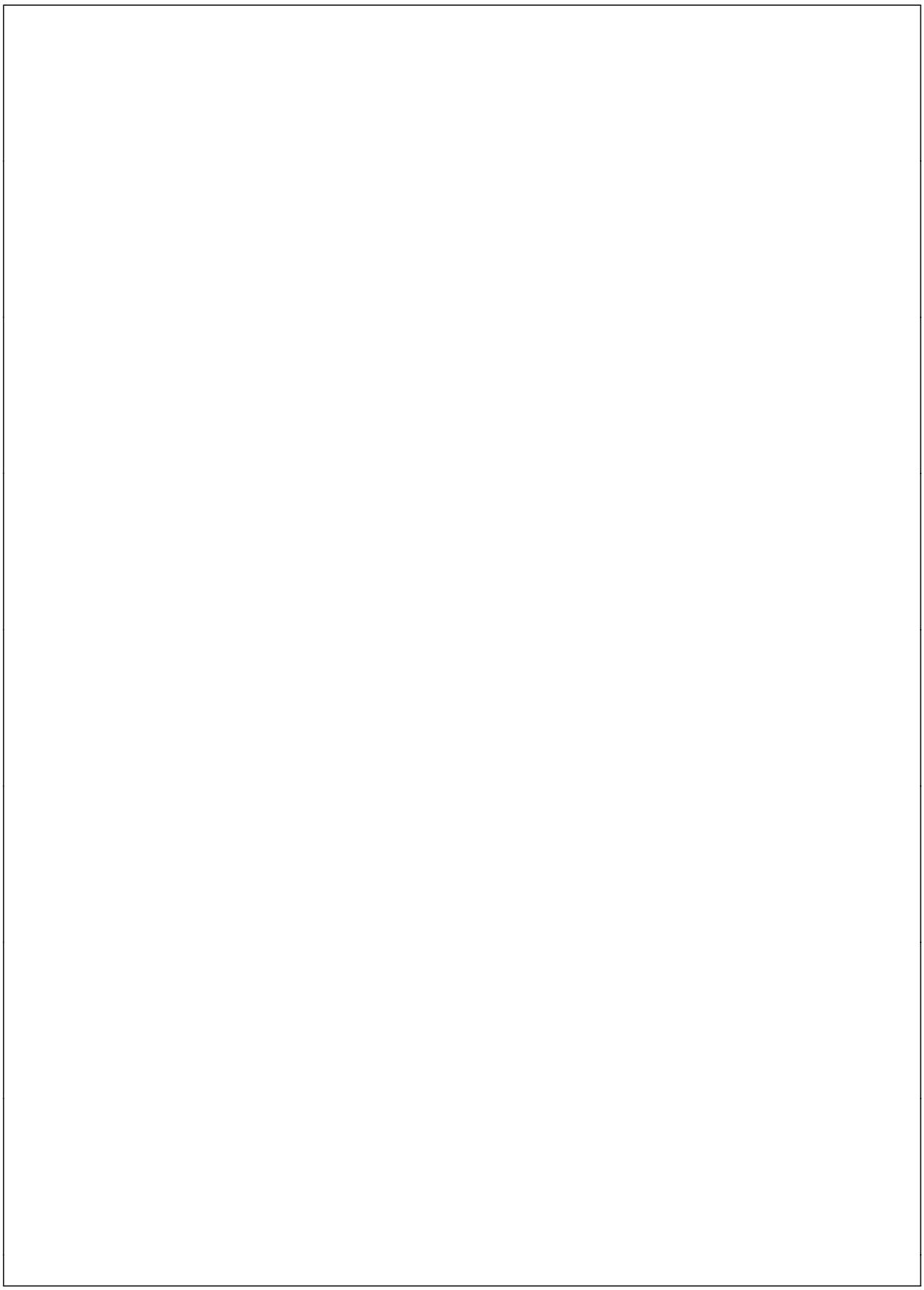
How to calculate the actual specification at a given frequency:

In the formula column, one will see many formulae, which contain the variable T. The T represents one period (or one T-state) of the CPU Clock. So if the CPU is running at 25 MHz, T is equivalent to 40 ns; similarly if the CPU is running at 20 MHz, T is equivalent to 50 ns.

EXAMPLE: Calculate the minimum guaranteed Column Address Setup Time

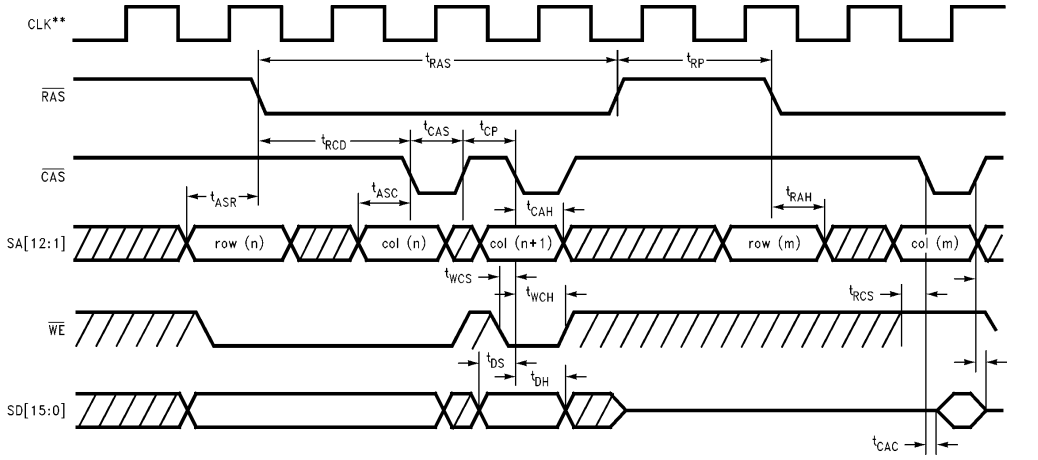
At 25 MHz:	Formula + Min. Spec.	=
	(0.5T) + (−20 ns)	=
	0.5 (40 ns) + (−20 ns)	=
	20 ns − 20 ns	= 0 ns
At 20 MHz:	Formula + Min. Spec.	=
	(0.5T) + (−20 ns)	=
	0.5 (50 ns) + (−20 ns)	=
	25 ns − 20 ns	= 5 ns

As the frequency varies, so will many of the specifications. One should always calculate the specification based on the CPU's operating frequency.



3.0 Device Specifications (Continued)

3.3.1 DRAM Interface Timing Specification



**The CLK signal is only included as a reference; no specifications are guaranteed to this signal.

FIGURE 3-5. DRAM Timing Diagram

TABLE 3-3. 4-Cycle Page Miss Preliminary Specifications

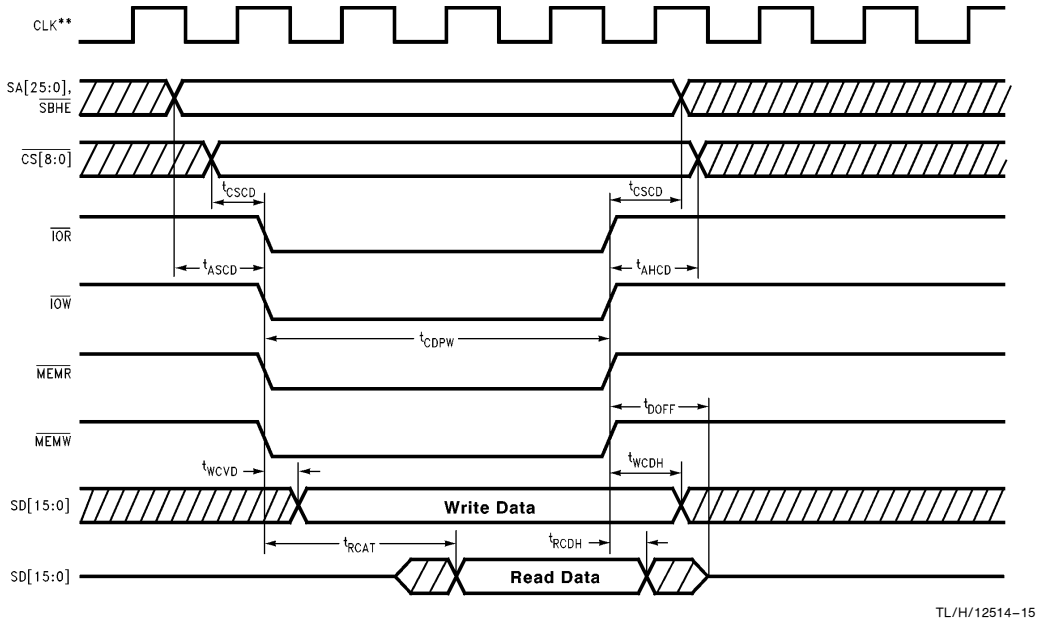
Symbol	Parameter	Formula	Min	Max
t_{ASC}	Column Address Setup Time	0.5T +	−20	
t_{ASR}	Row Address Setup Time	0.5T +	−20	
t_{CAC}	Access Time from CAS	0.5T +		−5
t_{CAH}	Column Address Hold Time	0.5T +	−5	
t_{CAS}	$\overline{CAS}$ Pulse Width	0.5T +	0	10
t_{CP}	Page Mode $\overline{CAS}$ Precharge	0.5T +	−10	
t_{DH}	Write Data Hold Time	0.5T +	−5	
t_{DS}	Write Data Setup Time	0.5T +	−20	
t_{OFF}	Read Data Valid Hold Time		0	
t_{RAS}	$\overline{RAS}$ Pulse Width	2.5T +	−15	Programmable
t_{RAH}	Row Address Hold Time	0.5T +	−10	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	1.5T +	−20	
t_{RCH}	Read Command Hold Time		0	
t_{RCS}	Read Command Setup Time	0.5T +	−20	
t_{RP}	$\overline{RAS}$ Precharge Time	1.5T +	−10	
t_{WCH}	Write Command Hold TIme	0.5T +	−5	
t_{WCS}	Write Command Setup Time	0.5T +	−20	

3.0 Device Specifications (Continued)

TABLE 3-4. 3 Cycle Miss Preliminary Specifications

Symbol	Parameter	Formula	Min	Max
t_{ASC}	Column Address Setup Time	0.5T +	−20	
t_{ASR}	Row Address Setup Time	0.5T +	−20	
t_{CAC}	Access Time From $\overline{CAS}$	0.5T +		−5
t_{CAH}	Column Address Hold Time	0.5T +	−5	
t_{CAS}	$\overline{CAS}$ Pulse Width	0.5T +	0	10
t_{CP}	Page Mode $\overline{CAS}$ Precharge	0.5T +	−10	
t_{DH}	Write Data Hold Time	0.5T +	−5	
t_{DS}	Write Data Setup Time	0.5T +	−20	
t_{OFF}	Read Data Valid Hold Time		0	
t_{RAS}	$\overline{RAS}$ Pulse Width	2.0T +	−15	PROG
t_{RAH}	Row Address Hold Time	0.5T +	−10	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	1.0T +	−20	
t_{RCH}	Read Command Hold Time		0	
t_{RCS}	Read Command Setup Time	0.5T +	−20	
t_{RP}	$\overline{RAS}$ Precharge Time	1.0T +	0	
t_{WCH}	Write Command Hold TIme	0.5T +	−5	
t_{WCS}	Write Command Setup Time	0.5T +	−20	

3.3.2 ISA-like Bus Cycles Timing Specification



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**The CLK signal is only included as a reference; no specifications are guaranteed to this signal.

FIGURE 3-6. ISA-like Bus Timing Diagram

3.0 Device Specifications (Continued)

TABLE 3-5. No Command Delay ISA-like Bus Specifications

Symbol	Parameter	Formula	Min	Max
t_{AHCD}	Address Hold Time from $\overline{CMD}$	1.0T +	−20	
t_{ASCD}	Address Setup TIme to $\overline{CMD}$	1.0T +	−20	
t_{CDPW}	Command Pulse Width	1.0T + (Wait)T +	−10	
t_{CHCD}	Chip Select Hold Time from $\overline{CMD}$	1.0T +	−25	
t_{CSCD}	Chip Select Setup Time to $\overline{CMD}$	1.0T +	−40	
t_{DOFF}	Read Data TRI-STATE	1.0T +		−25
t_{RCAT}	Read $\overline{CMD}$ Data Access TIme	1.0T + (Wait)T +		−30
t_{RCDH}	Read $\overline{CMD}$ Data Hold TIme		0	
t_{WCDH}	Write $\overline{CMD}$ Data Hold Time	1.0T +	−25	
t_{WCVD}	Write $\overline{CMD}$ to Valid Data			5
t_{WCS}	Write Command Setup Time	0.5T +	−20	

Note: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0−7).

TABLE 3-6. One Programmed Command Delay ISA-like Bus Specifications

Symbol	Parameter	Formula	Min	Max
t_{AHCD}	Address Hold Time from $\overline{CMD}$	1.0T +	−20	
t_{ASCD}	Address Setup TIme to $\overline{CMD}$	2.0T +	−20	
t_{CDPW}	Command Pulse Width	1.0T + (Wait)T +	−10	
t_{CHCD}	Chip Select Hold Time from $\overline{CMD}$	1.0T +	−25	
t_{CSCD}	Chip Select Setup Time to $\overline{CMD}$	2.0T +	−40	
t_{DOFF}	Read Data TRI-STATE	1.0T +		−25
t_{RCAT}	Read $\overline{CMD}$ Data Access TIme	1.0T + (Wait)T +		−30
t_{RCDH}	Read $\overline{CMD}$ Data Hold TIme		0	
t_{WCDH}	Write $\overline{CMD}$ Data Hold Time	1.0T +	−25	
t_{WCVD}	Write Valid Data to CMD (Note 2)	1.0T +	−5	
t_{WCS}	Write Command Setup Time	0.5T +	−20	

Note 1: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0−7).

Note 2: For this case Valid Write Data Sets-up to the leading edge of the Command Strobe.

3.0 Device Specifications (Continued)

3.3.3 Ready Feedback Timing Specifications

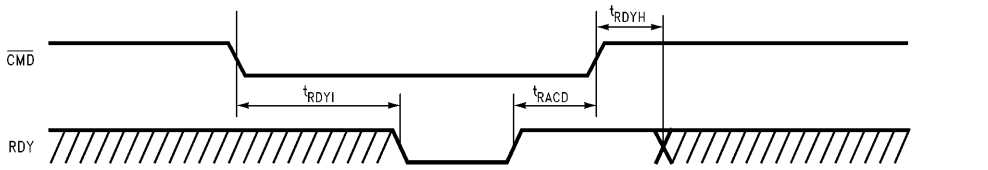

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FIGURE 3-7. Ready Feedback Timing Diagram

TABLE 3-7. Ready Signal Timing Specifications

Symbol	Parameter	Formula	Min	Max
t_{RACD}	RDY Active to $\overline{CMD}$ Rising	(E__RDY)T +	0	
t_{RDYH}	RDY Hold Time from $\overline{CMD}$		0	
t_{RDYI}	$\overline{CMD}$ to RDY Inactive Feedback	1.0T + (Wait)T +		−30

Note: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0–7). The value of (E__RDY) in the above formulae, is the number of programmed extended ready states associated with every access cycle (default number is 2, but may be programmed to 0–2).

3.3.4 OSCX1 AC Specification

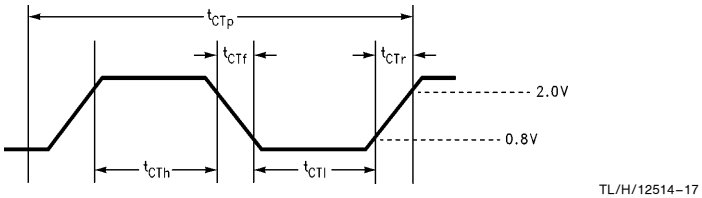

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FIGURE 3-8. TTL Clock Input Timing Diagram

TABLE 3-8. TTL Clock Input Specification

Symbol	Parameter	Min	Max	Unit
t_{CTp}	CTTL Clock Period	40	870	ns
t_{CTh}	CTTL High Time (Note)	(0.5 X t_{CTp}) − 4		ns
t_{CTl}	CTTL Low Time (Note)	(0.5 X t_{CTp}) − 4		ns
t_{CTr}	CTTL Rise Time		4	ns
t_{CTf}	CTTL Fall Time		4	ns

Note: Except for the cycle in which the core frequency is changed. In this cycle, t_{CTh} and t_{CTl} relate to different t_{CTp} cycles.

3.0 Device Specifications (Continued)

3.3.5 Peripheral Timing Specifications

3.3.5.1 DMA CONTROLLER

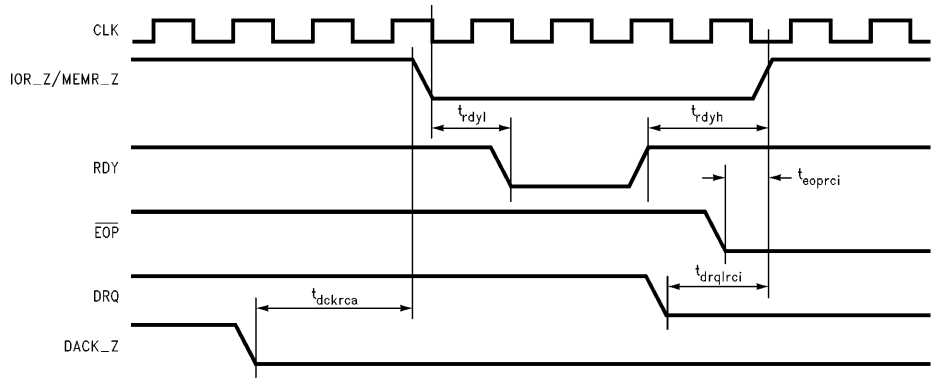

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FIGURE 3-9. DMA Controller Read Timing Diagram

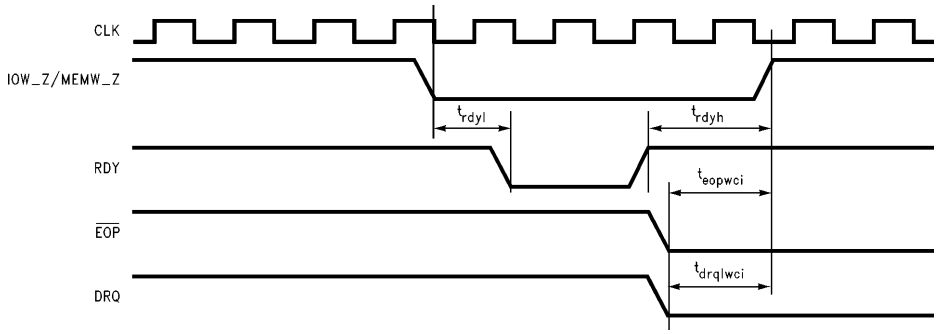

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FIGURE 3-10. DMA Controller Write Timing Diagram

TABLE 3-9. DMA Controller Specifications

Symbol	Parameter	Min	Typ	Max
t_{rdyl}	RDY Inactive Low Setup to CMD Active	−15 ns		
t_{rdyh}	RDY Active High Setup to CMD Inactive			2T + 15 ns
t_{eoprci}		45 ns		
t_{eopwci}		2T + 5 ns		
$t_{drqlwci}$		2T + 36 ns		
$t_{drqlrci}$		T + 40 ns		
t_{dckrca}		2T + 2.2 ns		

3.3.5.2 PIC AC SPECS

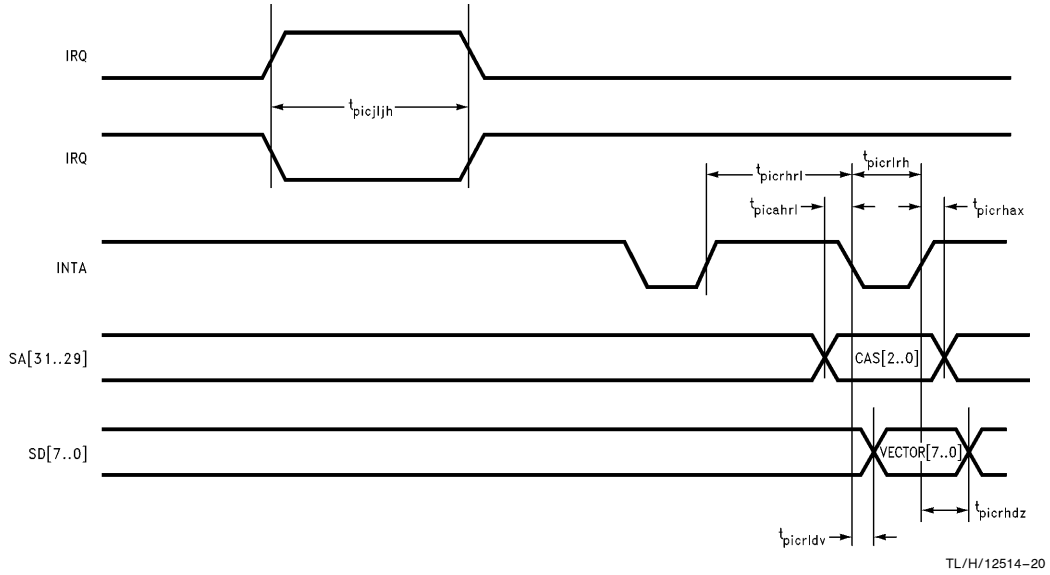

FIGURE 3-11. PIC Timing Diagram

TABLE 3-10. PIC Timing Specifications

Symbol	Parameter	Min	Typ	Max
$t_{picljlh}$		100		
$t_{picahrl}$		0		
$t_{picrlrh}$		235		
$t_{picrhax}$		0		
$t_{picrldv}$				200
$t_{picrhdz}$		10		
$t_{picrhrl}$		100		

3.0 Device Specifications (Continued)

3.3.5.3 PARALLEL PORT

TABLE 3-11. Parallel Port Compatibility Mode Handshake Timing Values

Symbol	Measured At	Measured From	Measured to	Value (min/max)	Compliance
T_{ready}	Host Output	Busy V_{IL}	$\overline{Strobe}$ V_{OH}	0 min	Compatible Hosts
T_{setup}(host)	Host Output	Data Stable	$\overline{Strobe}$ V_{OH}	750 ns min	Compatible Hosts
T_{setup} (peripheral)	Peripheral Input	Data Stable	$\overline{Strobe}$ V_{IH}	500 ns max*	Compatible Peripherals
T_{strobe}(host)	Host Output	$\overline{Strobe}$ V_{OL}	$\overline{Strobe}$ > V_{OL}	750 ns min 500 μs max	Compatible Hosts
T_{strobe} (peripheral)	Peripheral Input	$\overline{Strobe}$ V_{IL}	$\overline{Strobe}$ > V_{IL}	500 ns max	Compatible Peripherals
T_{hold}(host)	Host Output	$\overline{Strobe}$ V_{OH}	Data or $\overline{AutoFd}$ Change	750 ns min	Compatible Hosts
T_{hold} (peripheral)	Peripheral Input	$\overline{Strobe}$ V_{IL}	Data or $\overline{AutoFd}$ Change	500 ns max	Compatible Peripherals
T_{busy}	Peripheral Output	$\overline{Strobe}$ V_{IL}	Busy V_{OH}	500 ns max	Compliant Peripherals
T_{reply}	Peripheral Output	$\overline{Strobe}$ V_{IL}	$\overline{Ack}$ V_{OH}	0 min	Compatible Peripherals
T_{ack}	Peripheral Output	$\overline{Ack}$ V_{OL}	$\overline{Ack}$ V_{OL}	500 ns min 10 μs max	Compatible Peripherals
T_{nbusy}	Peripheral Output	$\overline{Ack}$ V_{OH}	Busy V_{OH}	0 min**	Compliant Peripherals
T_{next}	Host Output	$\overline{Ack}$ V_{IL}	$\overline{Strobe}$ V_{OH}	0 min	Compliant Hosts

Note 1: For more information on the history of Centronics Standard Parallel and PC-Compatible Parallel Interfaces, see annex Ca and in particular C.6.2 for Busy-to-Ack timing variations.

Note 2: V_{IL} is the low-level voltage input

V_{OL} is the low-level voltage output

V_{OH} is the high-level voltage output

V_{IH} is the high-level voltage input

*The maximum value stated for peripherals in this table are referenced to the peripheral. For example, the peripheral cannot require more than 500 ns data setup time.

**Recognize that complementary signal changes may have overlapping signal transistions. The zero minimum value cannot be guaranteed.

TABLE 3-12. Parallel Port IEEE 1284 Mode Handshake Timing Values

Symbol	Parameter	Min	Max
T_H	Host Response Time	0	1.0s
T_∞	Infinite Response Time	0	Infinite
T_L	Peripheral Response Time	0	35 ms
T_R	Peripheral Response Time (ECP Mode Only)	0	
T_S	Host Recovery Time (ECP Mode Only)	35 ms	
T_P	Minimum Setup or Pulse Width	0.5 μs	
T_D	Minimum Data Setup Time (ECP/EPP Modes Only)	0	
T_{ES}	Short Response Time (EPP Mode Only)	0	125 ms
T_{EL}	Long Response Time (EPP Mode Only)	0	10 μs
T_{ER}	Termination Pulse Width (EPP Mode Only)	50 μs	Infinite

3.0 Device Specifications (Continued)

3.3.5.4 PCMCIA CONTROLLER

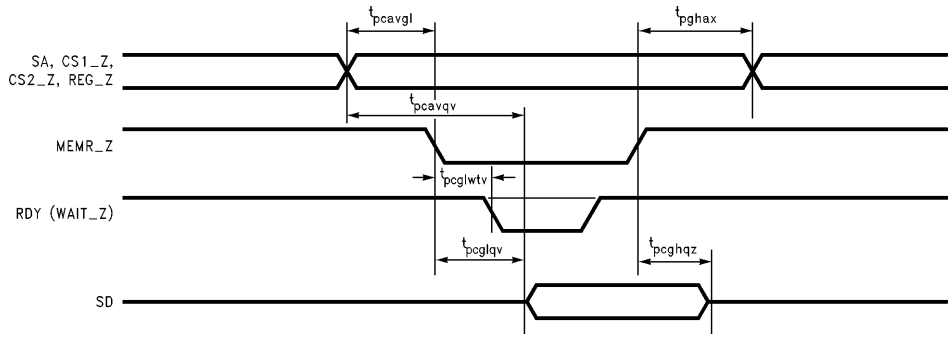

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FIGURE 3-12. Memory Read Timing

TABLE 3-13. PCMCIA Memory Read Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max
t_{pcavgl}			50 ns		
t_{pghax}			20 ns		
$t_{pcglwtv}$					35 ns
t_{pcavqv}					250 ns
t_{pcghqz}			0 ns		
t_{pcglqv}					125 ns

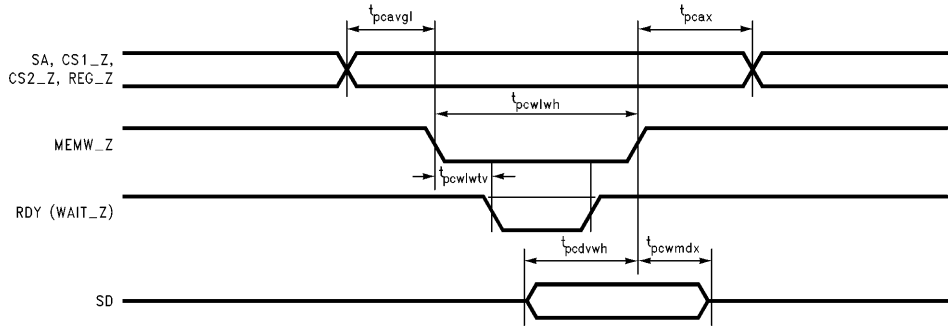

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FIGURE 3-13. Memory Write Timing Diagram

TABLE 3-14. Memory Write Timing Diagram

Symbol	Parameter	Condition	Min	Typ	Max
t_{pcavgl}			50 ns		
t_{pcax}			20 ns		
t_{pcwlwh}			60 ns + (t_{sysclk}) • (number of waitstates)		
t_{pcdvwh}			100 ns		
t_{pcwmdx}			30 ns		
$t_{pcwlwtv}$					35 ns

3.0 Device Specifications (Continued)

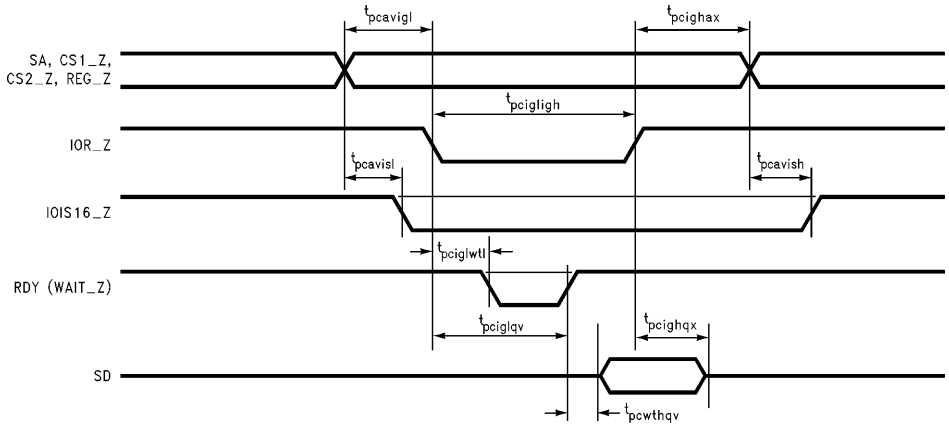

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FIGURE 3-14. I/O Read Timing

TABLE 3-15. PCMCIA I/O Read Specifications

Symbol	Parameter	Condition	Min	Typ	Max
$t_{pcavigl}$			100 ns		
$t_{pcighax}$			20 ns		
$t_{pcigligh}$			180 ns		
$t_{pcavisl}$					35 ns
$t_{pcavish}$					35 ns
$t_{pciglwtl}$					35 ns
$t_{pciglqv}$					120 ns
$t_{pcighqx}$			0 ns		
$t_{pcwthqv}$					35 ns

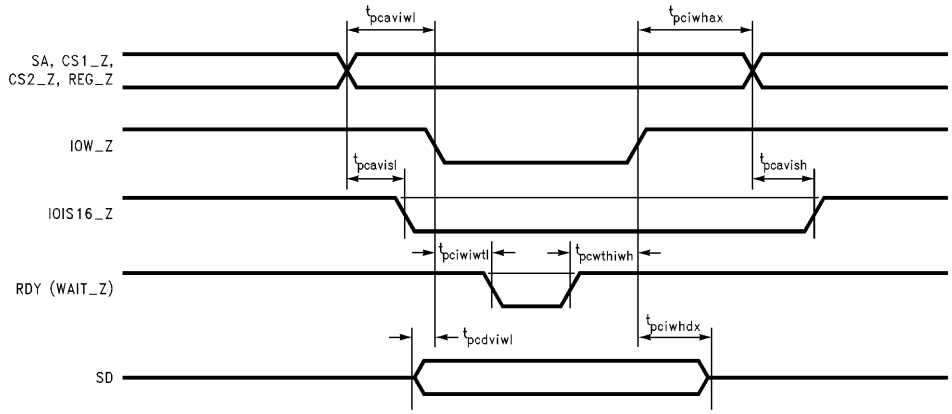

FIGURE 3-15. I/O Write Timing Diagram

TABLE 3-16. PCMCIA I/O Write Specifications

Symbol	Parameter	Condition	Min	Typ	Max
$t_{pcaviwl}$			100 ns		
$t_{pciwhax}$			20 ns		
$t_{pcavisl}$					35 ns
$t_{pcavish}$					35 ns
$t_{pciwlwtl}$					35 ns
$t_{pcdviwl}$			80 ns		
$t_{pcwthiwh}$			0 ns		
$t_{pciwhdx}$			30 ns		

3.0 Device Specifications (Continued)

3.3.5.5 MICROWIRE (3-WIRE) & ACCESS.BUS

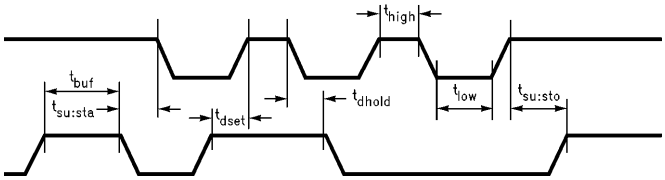

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FIGURE 3-16. Access.bus Timing Diagram

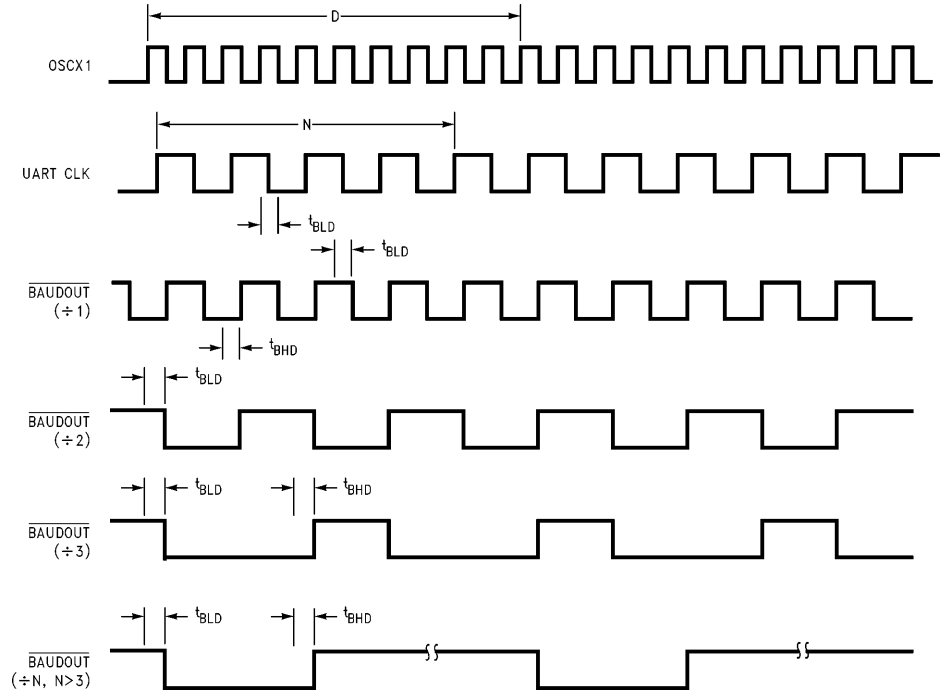
TABLE 3-17. Access.Bus Timing Specifications

Symbol	Parameter	Formula	Min	Max
f_{sclk}	SCLK Clock Frequency			100 kHz
t_{buf}	Bus Free Time between STOP and START Condition		4.7 μs	
t_{low}	Low Period of the SCLK Clock		4.7 μs	
t_{high}	High Period of the SCLK Clock		4.0 μs	
t_{dhold}	Data Hold Time		250	
t_{dset}	Data Setup Time		250	
$t_{su:sto}$	Setup Time for STOP Condition		4.0 μs	
$t_{su:sta}$	Hold Time for START Condition		4.7 μs	

3.0 Device Specifications (Continued)

3.3.5.6 FIFO UART

Symbol	Parameter	Condition	Min	Max	Units
D	OSC Clock Divider		1	63	CLKs
D	Baud Divisor		1	65535	CLKs
t_{BHD}	Baud Output Positive Edge Delay			56	ns
t_{BLD}	Baud Output Negative Edge Delay			56	ns



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Symbol	Parameter	Condition	Min	Max	Units
t_{IRTXW}	IRTX Pulse Width		1.6 μs	3/16	BAUD OUT Cycles
t_{IRRXW}	IRRX Pulse Width		1.6 μs	6/16	BAUD OUT Cycles

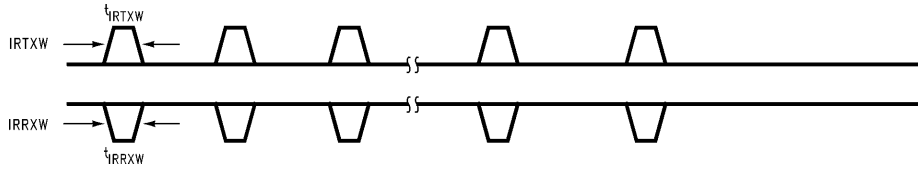

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FIGURE 3-17. UART Baud Rate and Infrared Clocks

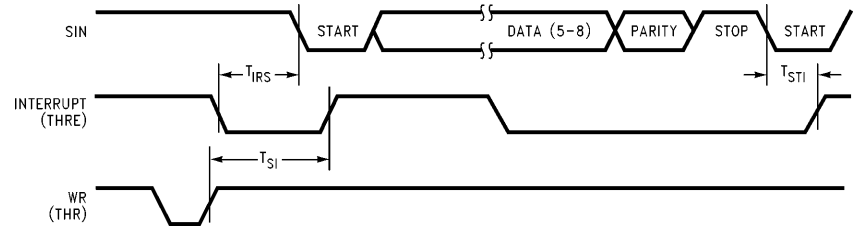
3.0 Device Specifications (Continued)

Symbol	Parameter	Min	Max	Units
t_{SINT}	Delay from Stop Bit to Set Interrupt		2	BAUDOUT Cycles
t_{STI}	Delay from Start Bit to IRQ		8	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to IRQ	16	24	BAUDOUT Cycles
t_{IRS}	Delay from IRQ Reset to Tx Start	8	24	BAUDOUT Cycles
t_{MDO}	Delay from Write to Output		40	ns
t_{RIM}	Delay to Reset IRQA from Read		78	ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns

$$\text{BAUDOUT Cycle} = \frac{\text{Input Clock Frequency}}{\text{16 x Baudrate Divisor}}$$

$$\text{Input Clock Frequency} = \frac{\text{OSCX1 Frequency}}{\text{UART Clock Divisor}}$$

Registers: Divisor Latch Holds Baudrate Divisor
EF70 holds UART Clock Divisor



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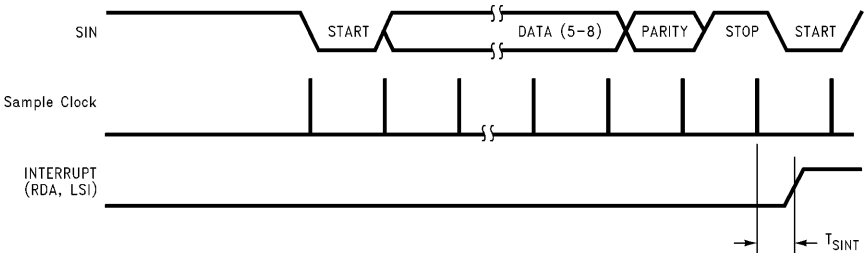

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FIGURE 3-18. UART IRQ Timing

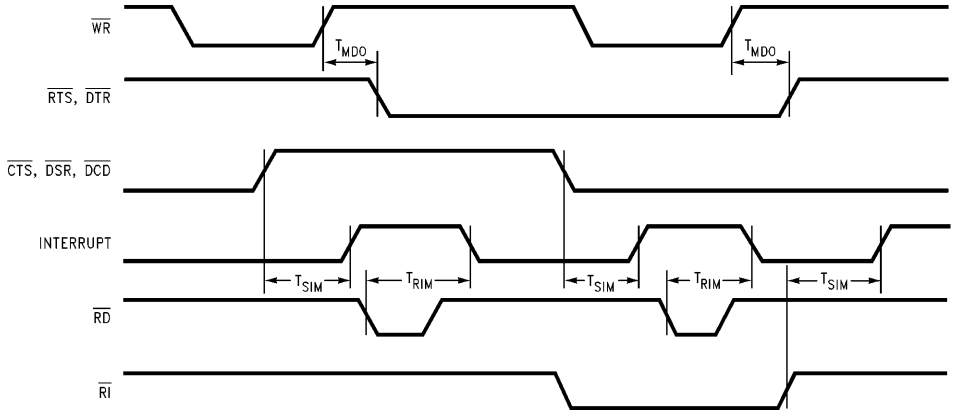

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FIGURE 3-19. UART Modem Control Timing

3.0 Device Specifications (Continued)

3.3.5.7 LCD CONTROLLER

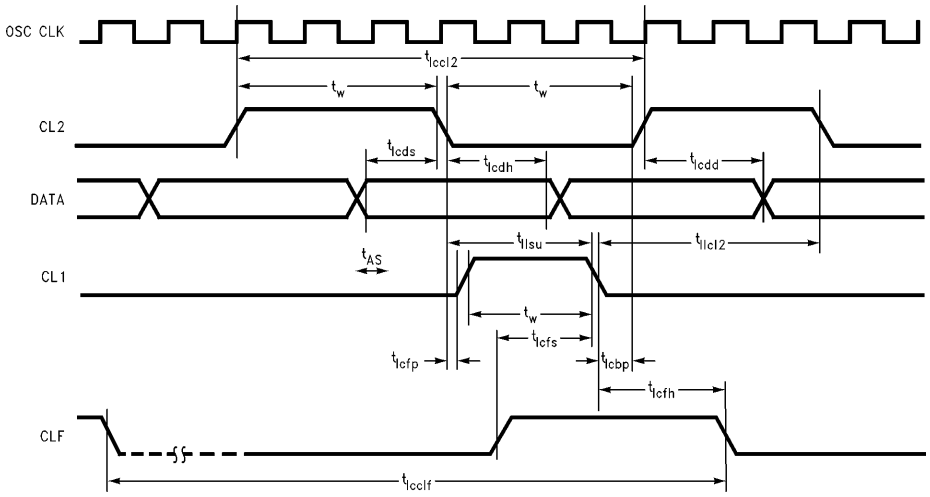

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FIGURE 3-20. LCD Controller Timing Diagram

TABLE 3-18. LCD Controller Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max
t_{lcclf}	Frame Period	Programmable		14.3 ms	
t_{lccl2}	Dot Clock Period	Programmable	Oscx1*6		
t_{lcds}	LCD Data Situp, CL2 Fall		$(t_{lccl2})/2$-50 ns		
t_{lcdh}	LCD Data Hold, CL2 Fall		$(t_{lccl2})/2$-50 ns		
t_{lcdd}	LCD Data Delay, CL2 Rise		$(t_{lccl2})/2$-50 ns		50 ns
t_{lcfp}	CL2 Falling to CL1 Rising		$(t_{lccl2})/2$-50 ns		
t_{lcbp}	CL1 Falling to CL2 Rising		$(t_{lccl2})/2$-50 ns		
t_{lcfs}	CLF Setup to CL1 Fall		t_{lccl2}		
t_{lcfh}	CLF Hold from CL1 Fall		$(t_{lccl2})/2$-20 ns		
t_{llsu}	CL1 Load Setup Time		$(t_{lccl2})/2$-50 ns		
t_{llcl2}	CL1 Falling to CL2 Falling		$(t_{lccl2})/2$-50 ns		
t_w	Pulse Width		$(t_{lccl2})/2$-50 ns		

3.3.5.8 SUPPORTED TESTMODES

Symbol	Parameter	Conditions	Min	Max	Units
t_{AND}	AND Function Result Delay			1	ms
t_{HILO}	HI/LO Function Drive Delay			1	ms
t_{TRI}	TRI-STATE Outputs Delay			1	ms
t_{TOG}	Toggle Function Delay			1	ms

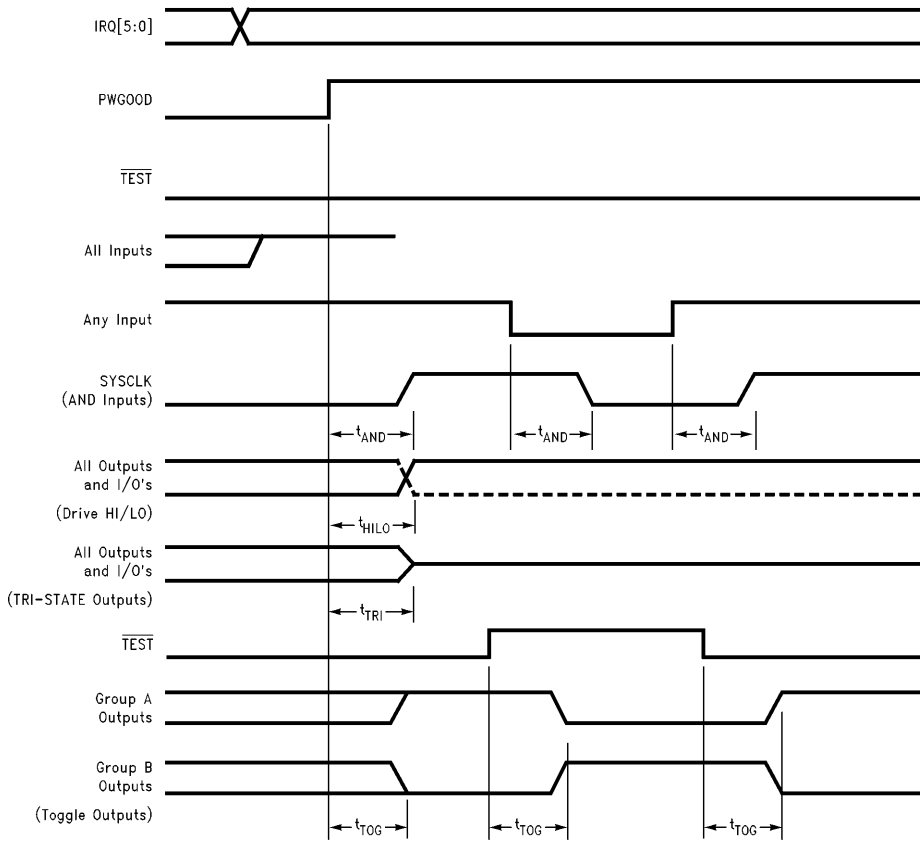

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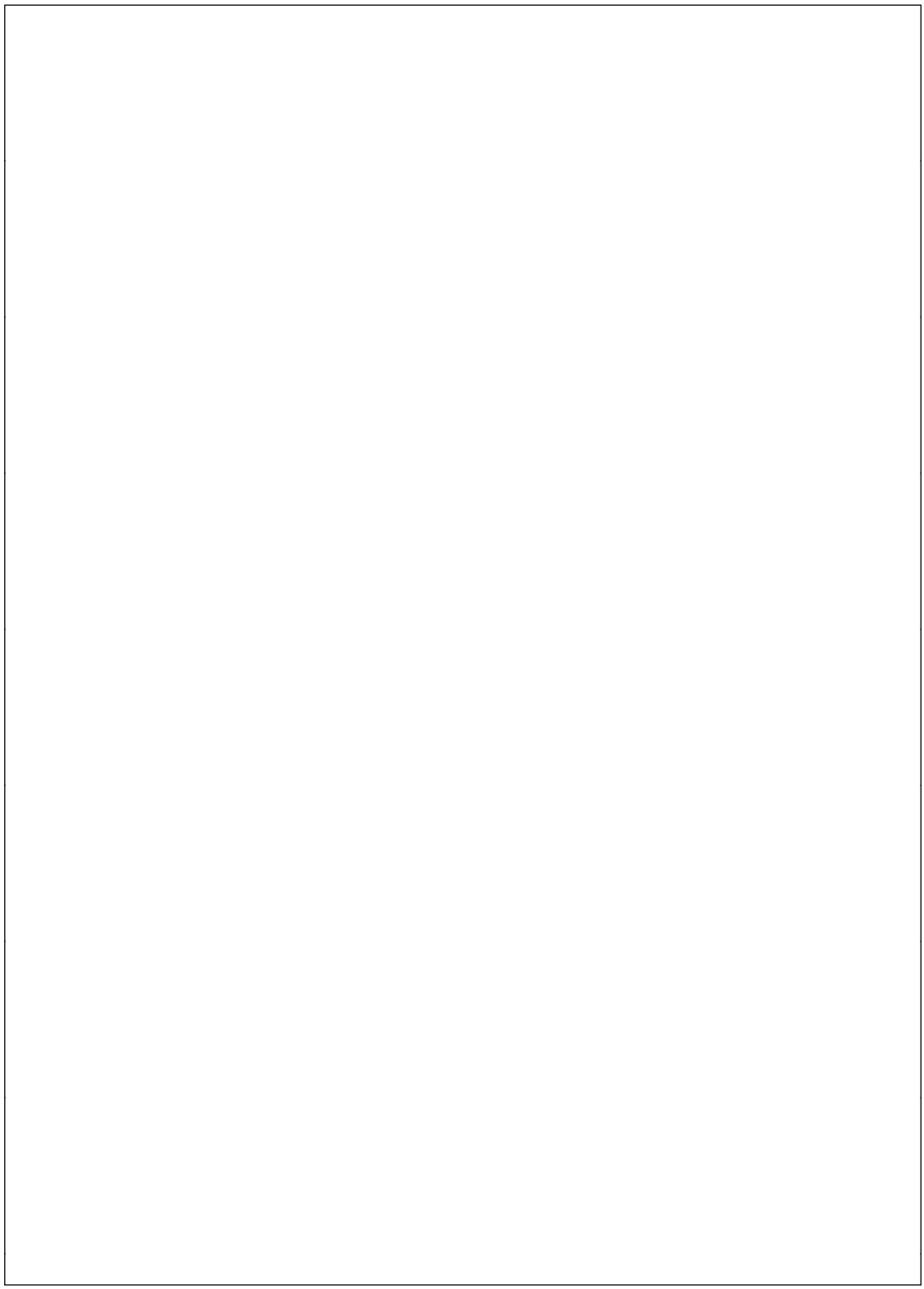
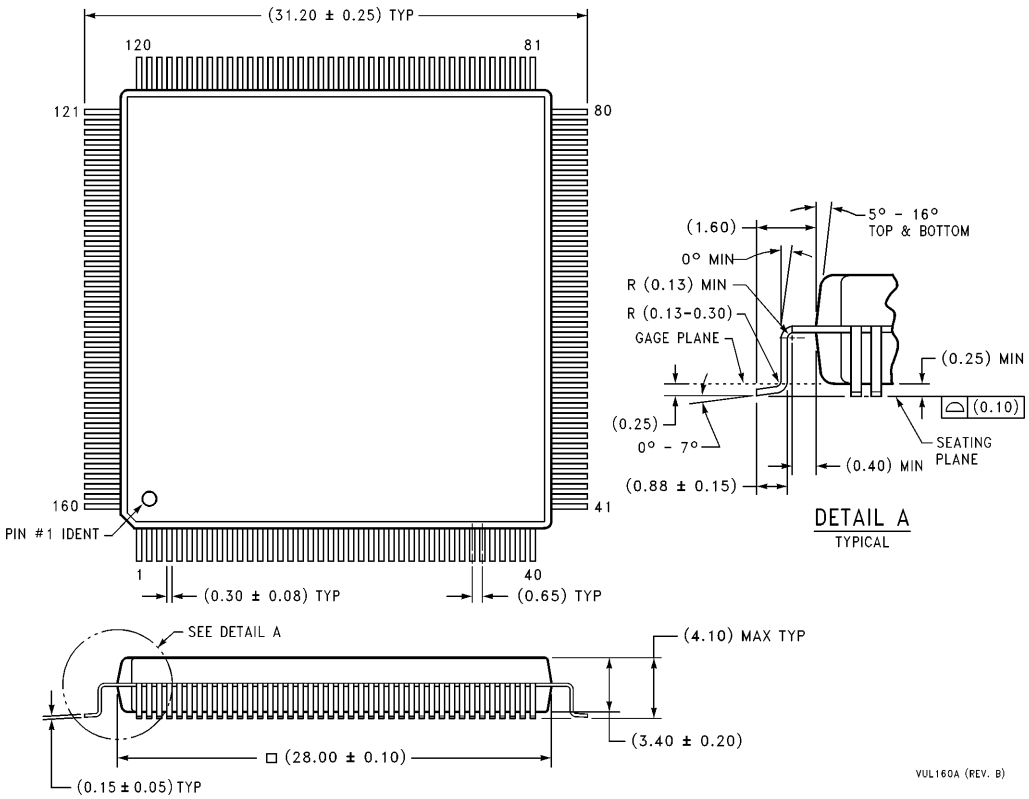
FIGURE 3-21. Testmode Timing Diagram



3.0 Device Specifications (Continued)

3.4 Physical Dimensions inches (millimeters)

The NS486SXF is provided in a 160-lead, 28mm x 28mm, PQFP package.



160-Lead Plastic Quad Flatpak JEDEC (VUL)
NS Package Number VUL160A

FIGURE 3-22. Plastic Package Specifications

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