LP324, LP2902 ULTRA-LOW-POWER QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS460A-MARCH 2005-REVISED MAY 2005

FEATURES

- Low Supply Current . . . 85 μA Typ
- Low Offset Voltage . . . 2 mV Typ
- Low Input Bias Current . . . 2 nA Typ
- Input Common Mode to GND
- Wide Supply Voltage . . . 3 V < V_{CC} < 32 V
- Pin Compatible With LM324
- Applications
 - LCD Displays
 - Portable Instrumentation
 - Sensor/Metering Equipment
 - Consumer Electronics (MP3 Players, Toys, Etc.)
 - Power Supplies

D, N, OR PW PACKAGE (TOP VIEW) 14 1 40UT 10UT [1IN- Π 13**∏** 4IN− 1IN+ [] 3 ∏ 4IN+ V_{CC} [] 4 GND 11 2IN+ [] 5 10 3IN+ 2IN- **1** 6 9∏ 3IN-20UT [1 30UT

DESCRIPTION/ORDERING INFORMATION

The LP324 and LP2902 are quadruple low-power operational amplifiers especially suited for battery-operated applications. Good input specifications and wide supply-voltage range still are achieved, despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes GND.

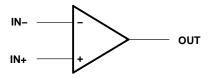
The LP324 and LP2902 are ideal in applications where wide supply voltage and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, etc.), and power supplies.

ORDERING INFORMATION

T _A	Р	ACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	LP324N	LP324N
	SOIC - D	Tube of 50	LP324D	LP324
0°C to 70°C	30IC - D	Reel of 2500	LP324DR	LF324
	TSSOP – PW	Tube of 90	LP324PW	LP324
	1330P – PW	Reel of 2000	LP324PWR	LP324
	PDIP – N	Tube of 25	LP2902N	LP2902N
	SOIC – D	Tube of 50	LP2902D	LP2902
–40°C to 85°C	30IC - D	Reel of 2500	LP2902DR	LP2902
	TSSOP – PW	Tube of 50	LP2902PW	LP2902
	1330F – PW	Reel of 2500	LP2902PWR	LF2902

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SYMBOL (EACH AMPLIFIER)

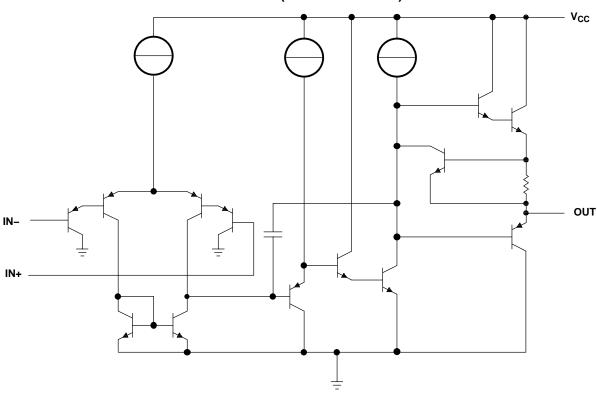




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SCHEMATIC (EACH AMPLIFIER)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽²⁾			±16 or 32	V
V_{ID}	Differential input voltage (3)			±32	V
VI	Input voltage (either input)		-0.3	32	V
	Duration of output short circuit (one amplifier)	to ground at (or below) $T_A = 25^{\circ}C$, $V_{CC} \le 15 V^{(4)}$		Unlimited	
		D package		86	
θ_{JA}	Package thermal impedance (5)(6)	N package		80	°C/W
	Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^{\circ}C$, $V_{CC} \le 15 \text{ V}^{(4)}$ Unlim Package thermal impedance (5) (6) PW package PW package	113			
TJ	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+, with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

ESD Protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	±2	kV



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Electrical Characteristics

 $\rm T_A$ = 25°C, $\rm V_{CC}$ = 5 V, $\rm V_{IC}$ = V $_{CC}/2,$ $\rm R_L$ = 100 k Ω to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T (2)	I	_P324		L	P2902		UNIT	
	PARAMETER	TEST CONDITIONS(1)	T _A ⁽²⁾	MIN	TYP ⁽³⁾	MAX	MIN	TYP ⁽³⁾	MAX	UNII	
V	Innut offeet valtage		25°C		2	4		2	4	m\/	
V_{IO}	Input offset voltage		Full range			9			10	mV	
_	Input bigg gurrent		25°C		2	10		2	20	nA	
I _{IB}	Input bias current		Full range			20			40	ΠA	
-	Innut offeet ourrent		25°C		0.2	2		0.5	4	nA	
I _{IO}	Input offset current		Full range			4			8	ΠA	
^	Large-signal	$R_L = 10 \text{ k}\Omega \text{ to GND},$	25°C	50	100		40	70		V/mV	
A_V	voltage gain	$V_{CC} = 30 \text{ V}$	Full range	40			30			V/IIIV	
CMRR	Common-mode	V _{CC} = 30 V,	25°C	80	90		80	90		dB	
CIVIKK	rejection ratio	$V_{IC} = 0 \text{ V to } V_{CC} - 1.5 \text{ V}$	Full range	75			75			uБ	
l _z	Power-supply	\/ - 5 \/ to 20 \/	25°C	80	90		80	90		V	
k _{VSR}	rejection ratio	$V_{CC} = 5 \text{ V to } 30 \text{ V}$	Full range	75			75			V	
	Supply current	R₁ = ∞	25°C		85	150		85	150	μΑ	
I _{CC}	Supply current	KL = ∞	Full range			250			275	μΑ	
V	V _{OH} Output voltage swing (high)	$I_L = 0.35 \text{ mA to GND},$	25°C	3.4	3.6		3.4	3.6		V	
VOH		$V_{IC} = 0 V$	Full range	V _{CC} – 1.9			V _{CC} – 1.9			V	
V	Output voltage	$I_L = 0.35 \text{ mA from } V_{CC}$	25°C	0.82	0.7		0.82	0.7		V	
V_{OL}	swing (low)	$V_{IC} = 0 V$	Full range	1			1			V 	
_	Output source	V _O = 3 V, V _{ID} = 1 V	25°C	7	10		7	10		mA	
I _O	current	$V_0 = 3 V$, $V_{ID} = 1 V$	Full range	4			4				
		V 45V V 4V	25°C	4	5		4	5			
	Output sink surrent	$V_{O} = 1.5 \text{ V}, V_{ID} = -1 \text{ V}$	Full range	3			3			A	
I _O	Output sink current	$V_{O} = 1.5 \text{ V}, V_{ID} = -1 \text{ V},$	25°C	2	4		2	4		mA	
		$V_{IC} = 0 V$	Full range	1			1				
	Outrout als and to CNID	V 4.V	25°C		20	35		20	35	A	
I _{OS,GND}	Output short to GND	$V_{ID} = 1 V$	Full range			40			40	mA	
	I Outrout about 4 - M	V _{ID} = -1 V	25°C		15	30		15	30	m^	
I _{os,vcc}	Output short to V _{CC}	v _{ID} = -1 v	Full range			45			45	mA	
∞V_{IO}	Input offset voltage drift		25°C		10			10		μV/°C	
∝I _{IO}	Input offset current drift		25°C		10			10		pA/°C	

⁽¹⁾ For full-range temperature limits: $V_{CC} = 3$ V to 32 V, $V_{ICR} = 0$ V to $V_{CC} - 1.5$ V (unless otherwise noted) (2) Full range is 0°C to 70°C for LP324 and -40°C to 85°C for LP2902. (3) All typical values are at $T_A = 25$ °C.

Operating Conditions

 $V_{CC} = \pm 15 \text{ V}, T_A = 25^{\circ}\text{C}$

GBW	Gain bandwidth product	100	kHz	
SR	Slew rate	50	V/ms	





10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LP2902D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	Samples
LP2902DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	Samples
LP2902N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LP2902N	Samples
LP2902PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	Samples
LP2902PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	Samples
LP2902PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	Samples
LP324D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LP324N	Samples
LP324NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LP324N	Samples
LP324PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples
LP324PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	Samples



PACKAGE OPTION ADDENDUM

10-Jun-2014

(1) The marketing status values are defined as follows:

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ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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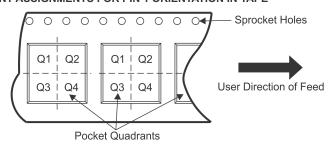
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902DR	SOIC	D	14	2500	333.2	345.9	28.6
LP2902PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LP324DR	SOIC	D	14	2500	364.0	364.0	27.0
LP324DR	SOIC	D	14	2500	333.2	345.9	28.6
LP324DRG4	SOIC	D	14	2500	333.2	345.9	28.6
LP324PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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