# LP2989 Micropower and Low-Noise, 500-mA Ultra Low-Dropout Regulator for Use With Ceramic Output Capacitors

## 1 Features

- 2.1-V to 16-V Input Voltage Range
- 2.5-V to 5-V Fixed Output Voltage Options
- Ultra-Low Dropout Voltage
- 500-mA Continuous Output Current
- Very Low Output Noise With External Capacitor
- < 0.8-µA Quiescent Current When Shutdown
- Low Ground Pin Current at All Loads
- 0.75% Output Voltage Accuracy (A Grade)
- High Peak Current Capability (800-mA typical)
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

## 2 Applications

- Notebooks and Desktop PCs
- PDAs and Palmtop Computers
- Wireless Communication Pins
- SMPS Post-Regulators

## 3 Description

The LP2989 is a fixed-output 500-mA precision LDO regulator designed for use with ceramic output capacitors.

Output noise can be reduced to 18 µV (typical) by connecting an external 10-nF capacitor to the bypass pin.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2989 delivers superior performance:

- **Dropout Voltage:** Typically 310 mV at 500-mA load, and 1 mV at 100-µA load.
- **Ground Pin Current:** Typically 3 mA at 500-mA load, and 110 µA at 100-µA load.
- **Sleep Mode:** The LP2989 draws less than 0.8-µA quiescent current when $\overline{\text{SHUTDOWN}}$ pin is pulled low.
- **Error Flag:** The built-in error flag goes low when the output drops approximately 5% below nominal.
- **Precision Output:** Output voltage accuracy is 0.75% (A grade) and 1.25% (standard grade) at room temperature.

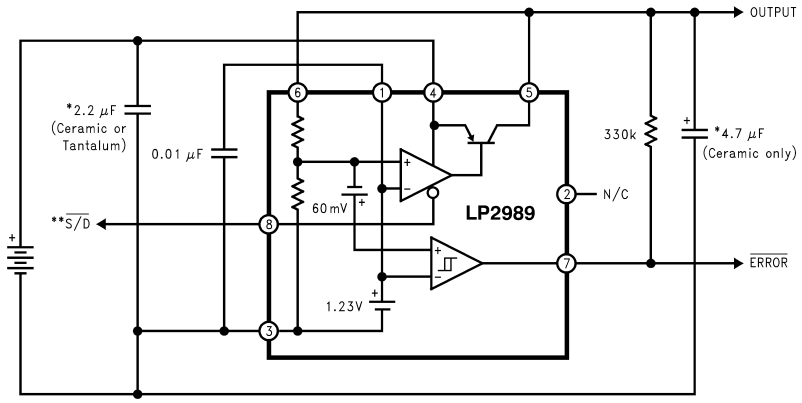
For output voltages < 2 V, see LP2989LV (SNVS086) data sheet.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LP2989 | WSON (8) | 4.00 mm x 4.00 mm |
| | SOIC (8) | 4.90 mm x 3.91 mm |
| | VSSOP (8) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application**




*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. See the *Output Capacitor* section.

**Shutdown must be actively terminated (see the *Shutdown Input Operation* section). Tie to IN (pin 4) if not use.

## Table of Contents



## 4 Revision History

**Changes from Revision N (December 2014) to Revision O** **Page**

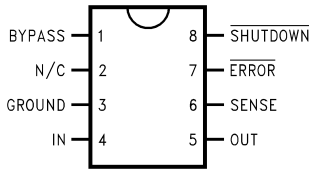
- Changed 30-V to 16-V ... 1
- Deleted trademark symbol from VIP which is no longer trademarked ... 1
- Changed pin names to TI nomenclature; references to National to TI; add notes to *Typical Application* on first page; fix errors in EC table reformat; replace *Handling Ratings* with *ESD Ratings*; take out *Output Voltage Options* and add graphic to *Mechanical* section; changed LLP package name references to WSON; added overbar to SHUTDOWN pin references; fix ulink for LP2989LV references. ... 1
- Changed description of N/C pin; add description of Thermal Pad; change "Ground" to "Thermal Pad" for NGN drawing ... 3
- Changed reference to National to TI ... 4
- Deleted "Operating" row from Input supply voltage; thermal values from footnote 2 ... 4
- Changed 1.6 to 16 in ROC input supply voltage ... 5
- Added word "OFF" ... 6
- Changed "high" to "low" ... 14
- Changed wording of "*Operation with Shutdown Control*" subsection ... 15
- Changed $V_{ON/OFF}$ to $V_{\overline{SD}}$ ... 15
- Changed "guaranteed" to "ensured" in "CAUTION". ... 15
- Changed $V_{ON/OFF}$ to $V_{\overline{SD}}$ ... 15
- Changed wording of last sentence of introductory *Detailed Design Procedure* paragraph ... 17
- Changed words "size" and "amount" for capacitors to "value" ... 17
- Changed wording of first sentence, second paragraph of *Noise Bypass Capacitor* subsection ... 18
- Added *Documentation Support* section ... 21

**Changes from Revision M (February 2005) to Revision N** **Page**

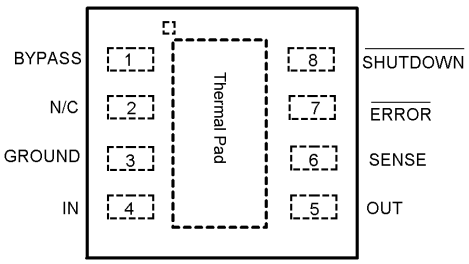
- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation section*, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; add updated *Thermal Information* values ... 1

# 5 Pin Configuration and Functions

**D/DGK Packages**
**8-Pin SOIC and VSSOP**
**Top View**




**NGN Package**
**8-Lead WSON**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BYPASS | 1 | I | Bypass capacitor input |
| $\overline{\text{ERROR}}$ | 7 | O | Error signal output |
| GROUND | 3 | — | GND |
| INPUT | 4 | I | Regulator power input |
| N/C | 2 | — | DO NOT CONNECT. Device pin 2 is reserved for post packaging test and calibration of the LP2989 $V_{OUT}$ accuracy. Device pin 2 must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 2 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 2 may activate the trim circuitry forcing $V_{OUT}$ to move out of tolerance. |
| OUTPUT | 5 | O | Regulated output voltage |
| SENSE | 6 | I | Feedback voltage sense input |
| $\overline{\text{SHUTDOWN}}$ | 8 | I | Shutdown input |
| Thermal Pad | — | — | The exposed thermal pad on the bottom of the WSON package should be connected to a copper thermal pad on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3. For additional information on using TI's Non Pull Back WSON package, see Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401). |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required contact the Texas Instruments Sales Office/Distributors for availability and specifications.(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Operating junction temperature | | –40 | 125 | °C |
| Power dissipation(2) | | Internally Limited | | |
| Input supply voltage | Survival | –0.3 | 16 | V |
| SENSE pin | | –0.3 | 6 | V |
| Output voltage | Survival(3) | –0.3 | 16 | V |
| $I_{OUT}$ (Survival) | | Short-circuit protected | | |
| Input-output voltage | Survival(4) | –0.3 | 16 | V |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$. The value $R_{\theta JA}$ for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2989 output must be diode-clamped to ground.
(4) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating junction temperature | –40 | 125 | °C |
| Operating input supply voltage | 2.1 | 16 | V |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LP2989 | | | UNIT |
|---|---|---|---|---|---|
| | | WSON (NGN) | SOIC (D) | VSSOP (DGK) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance, High-K | 34.8 | 114.5 | 156.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 28.4 | 61.1 | 51.0 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.0 | 55.6 | 76.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | 9.7 | 4.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 12.2 | 54.9 | 75.2 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.3 | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

| PARAMETER | | TEST CONDITIONS | LP2989AI-X.X[1] | | | LP2989I-X.X[1] | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OUT}$ | Output voltage tolerance | | −0.75 | | 0.75 | −1.25 | | 1.25 | $\%V_{NOM}$ |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V | −1.5 | | 1.5 | −2.5 | | 2.5 | |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | −4 | | 2.5 | −5 | | 3.5 | |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, −25°C ≤ $T_J$ ≤ 125°C | −3.5 | | 2.5 | −4.5 | | 3.5 | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Output voltage line regulation | $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V | | 0.005 | 0.014 | | 0.005 | 0.014 | %/V |
| | | $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.005 | 0.032 | | 0.005 | 0.032 | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | 1 mA < $I_{OUT}$ < 500 mA | | 0.4 | | | 0.4 | | $\%V_{NOM}$ |
| $V_{IN} - V_{OUT}$ | Dropout voltage[2] | $I_{OUT}$ = 100 µA | | 1 | 3 | | 1 | 3 | mV |
| | | $I_{OUT}$ = 100 µA, –40°C ≤ $T_J$ ≤ 125°C | | 1 | 4 | | 1 | 4 | |
| | | $I_{OUT}$ = 200 mA | | 150 | 200 | | 150 | 200 | mV |
| | | $I_{OUT}$ = 200 mA, –40°C ≤ $T_J$ ≤ 125°C | | 150 | 300 | | 150 | 300 | |
| | | $I_{OUT}$ = 500 mA | | 310 | 425 | | 310 | 425 | mV |
| | | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ 125°C | | 310 | 650 | | 310 | 650 | |

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

## Electrical Characteristics (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

| PARAMETER | | TEST CONDITIONS | LP2989AI-X.X(1) | | | LP2989I-X.X(1) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 100 µA | | 110 | 175 | | 110 | 175 | µA |
| | | $I_{OUT}$ = 100 µA, –40°C ≤ $T_J$ ≤ 125°C | | 110 | 200 | | 110 | 200 | |
| | | $I_{OUT}$= 200 mA | | 1 | 2 | | 1 | 2 | mA |
| | | $I_{OUT}$ = 200 mA, –40°C ≤ $T_J$ ≤ 125°C | | 1 | 3.5 | | 1 | 3.5 | |
| | | $I_{OUT}$ = 500 mA | | 3 | 6 | | 3 | 6 | mA |
| | | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ 125°C | | 3 | 9 | | 3 | 9 | |
| | | $V_{\overline{SD}}$ < 0.18 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 2 | | 0.5 | 2 | µA |
| | | $V_{\overline{SD}}$ < 0.4 V | | 0.05 | 0.8 | | 0.05 | 0.8 | |
| $I_{OUT(PK)}$ | Peak output current | $V_{OUT}$ ≥ $V_{OUT(NOM)}$ − 5% | 600 | 800 | | 600 | 800 | | mA |
| $I_{OUT(MAX)}$ | Short circuit current | $R_L$ = 0 (Steady State)(3) | | 1000 | | | 1000 | | mA |
| $e_n$ | Output noise voltage (RMS) | BW = 100 Hz to 100 kHz, $C_{OUT}$ = 10 µF, $C_{BYPASS}$ = .01 µF, $V_{OUT}$ = 2.5 V | | 18 | | | 18 | | $µV_{(RMS)}$ |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Ripple Rejection | f = 1 kHz, $C_{OUT}$ = 10 µF | | 60 | | | 60 | | dB |
| $\Delta V_{OUT}/\Delta T_D$ | Output voltage temperature coefficient | See(4), –40°C ≤ $T_J$ ≤ 125°C | | 20 | | | 20 | | ppm/°C |
| **$\overline{SHUTDOWN}$ INPUT** | | | | | | | | | |
| $V_{\overline{SD}}$ | $\overline{SD}$ Input voltage | $V_H$ = Output ON | | 1.4 | | | 1.4 | | V |
| | | $V_H$ = Output ON, –40°C ≤ $T_J$ ≤ 125°C | 1.6 | | | 1.6 | | | |
| | | $V_L$ = Output OFF | | 0.5 | | | 0.5 | | |
| | | $V_L$ = Output OFF, $I_{IN}$ ≤ 2 µA, –40°C ≤ $T_J$ ≤ 125°C | | | 0.18 | | | 0.18 | |
| $I_{\overline{SD}}$ | $\overline{SD}$ Input current | $V_{\overline{SD}}$ = 0 | | 0.001 | | | 0.001 | | µA |
| | | $V_{\overline{SD}}$ = 0, –40°C ≤ $T_J$ ≤ 125°C | | | −1 | | | −1 | |
| | | $V_{\overline{SD}}$ = 5 V | | 5 | | | 5 | | |
| | | $V_{\overline{SD}}$ = 5 V, –40°C ≤ $T_J$ ≤ 125°C | | | 15 | | | 15 | |
| **ERROR COMPARATOR** | | | | | | | | | |
| $I_{OH}$ | Output “HIGH” leakage | $V_{OH}$ = 16 V | | 0.001 | 1 | | 0.001 | 1 | µA |
| | | $V_{OH}$ = 16 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.001 | 2 | | 0.001 | 2 | |
| $V_{OL}$ | Output “LOW” voltage | $V_{IN}$ = $V_{OUT(NOM)}$ − 0.5 V, $I_{OUT(COMP)}$ = 150 µA | | 150 | 220 | | 150 | 220 | mV |
| | | $V_{IN}$ = $V_{OUT(NOM)}$ − 0.5 V, $I_{OUT(COMP)}$ = 150 µA, –40°C ≤ $T_J$ ≤ 125°C | | 150 | 350 | | 150 | 350 | |
| $V_{THR(MAX)}$ | Upper threshold voltage | | −6 | −4.8 | −3.5 | −6 | −4.8 | −3.5 | $\%V_{OUT}$ |
| | | –40°C ≤ $T_J$ ≤ 125°C | −8.3 | −4.8 | −2.5 | −8.3 | −4.8 | −2.5 | |
| $V_{THR(MIN)}$ | Lower threshold voltage | | −8.9 | −6.6 | −4.9 | −8.9 | −6.6 | −4.9 | $\%V_{OUT}$ |
| | | –40°C ≤ $T_J$ ≤ 125°C | −13 | −6.6 | −3 | −13 | −6.6 | −3 | |
| HYST | Hysteresis | | | 2 | | | | | |

(3) See the *Typical Characteristics* section.
(4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.

## 6.6 Typical Characteristics

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

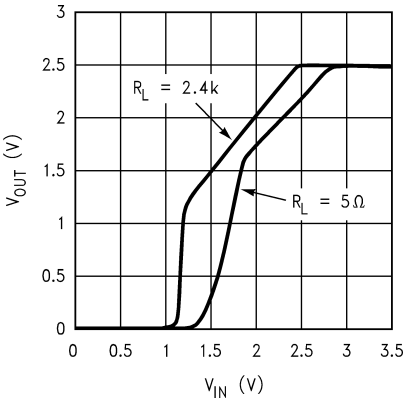



**Figure 1. Dropout Characteristics**

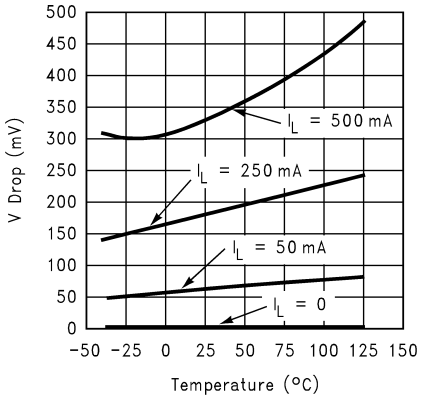



**Figure 2. Dropout Voltage vs Temperature**

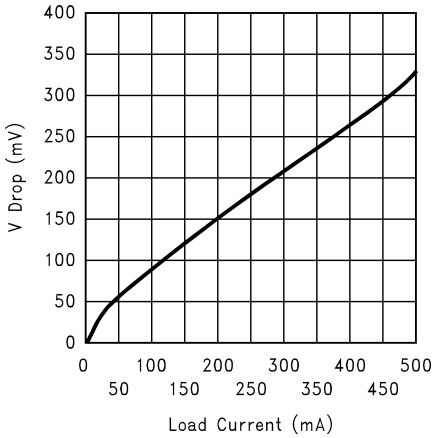



**Figure 3. Dropout Voltage vs Load Current**

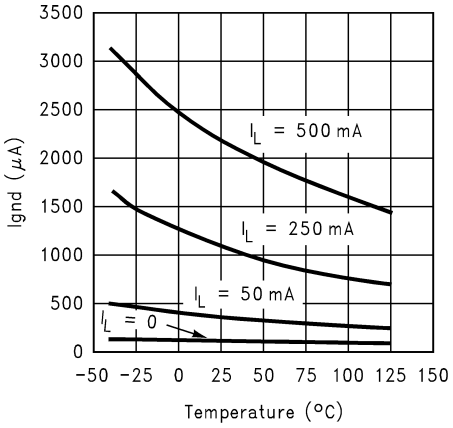



**Figure 4. GND Pin Current vs Temperature and Load**

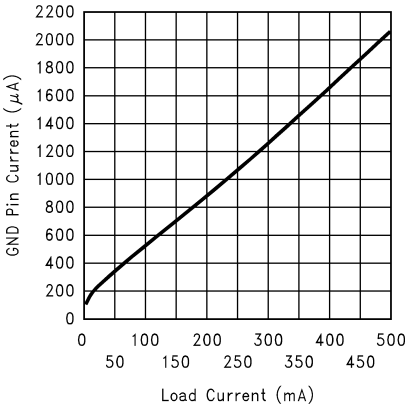



**Figure 5. Ground Pin Current vs Load Current**

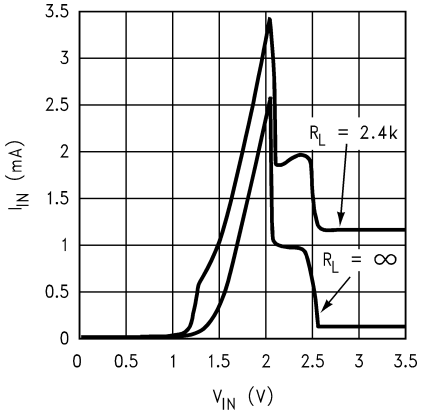



**Figure 6. Input Current vs $V_{IN}$**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

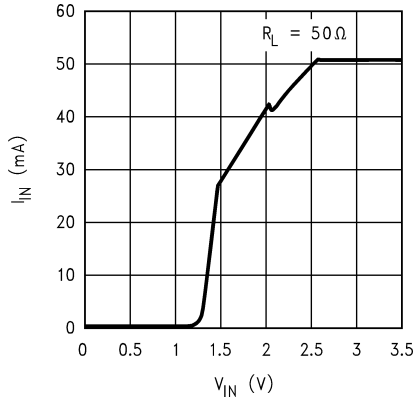



**Figure 7. Input Current vs $V_{IN}$**

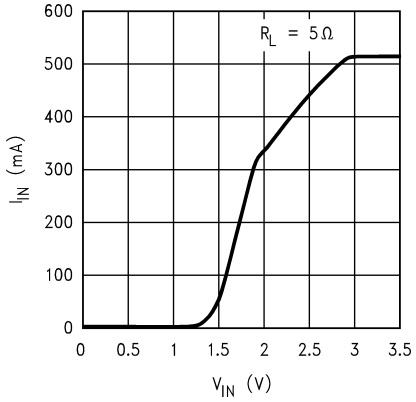



**Figure 8. Input Current vs $V_{IN}$**

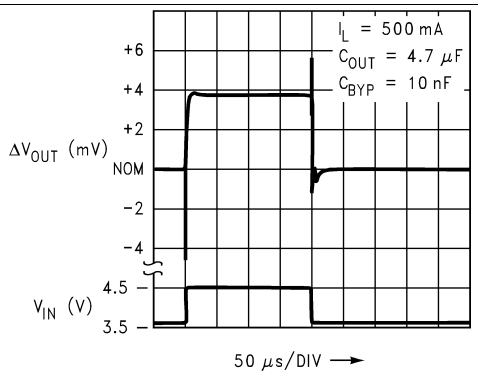



**Figure 9. Line Transient Response**

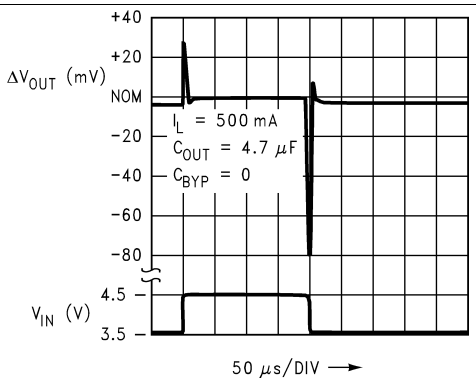



**Figure 10. Line Transient Response**

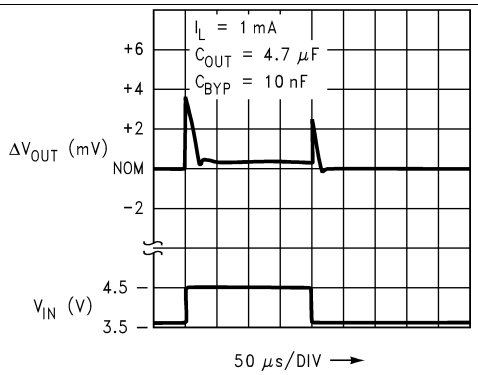



**Figure 11. Line Transient Response**

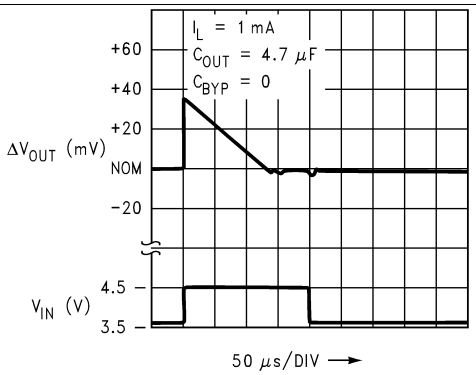



**Figure 12. Line Transient Response**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

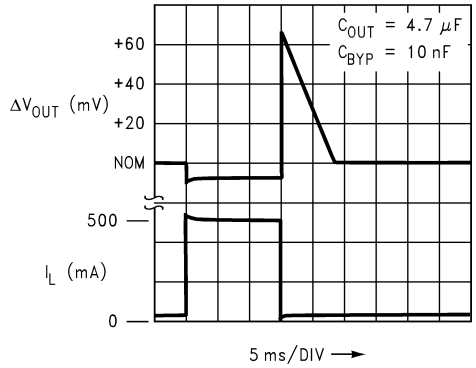



**Figure 13. Load Transient Response**

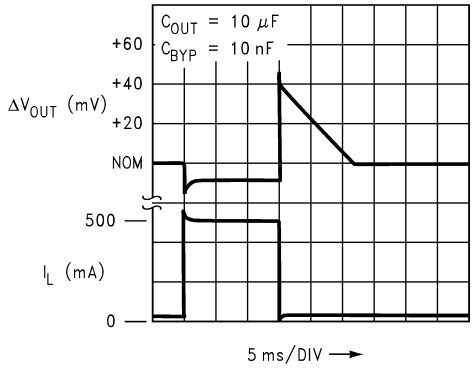



**Figure 14. Load Transient Response**

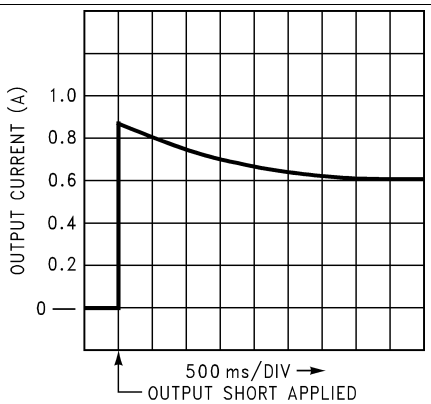



**Figure 15. Short Circuit Current**

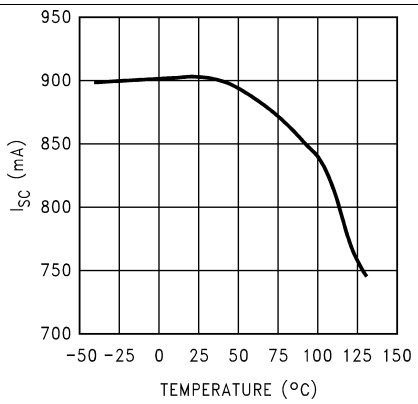



**Figure 16. Short Circuit Current vs Temperature**

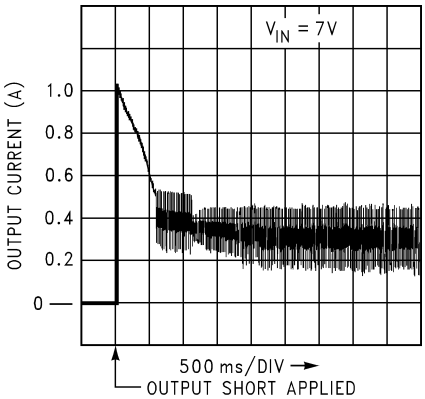



**Figure 17. Short Circuit Current**

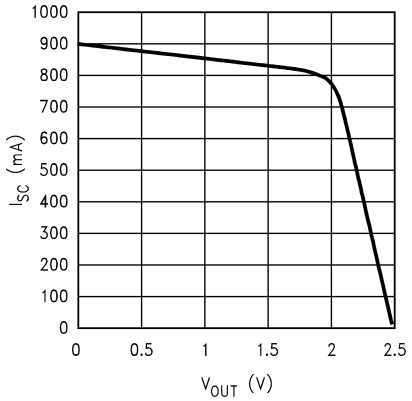



**Figure 18. Short Circuit Current vs $V_{OUT}$**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

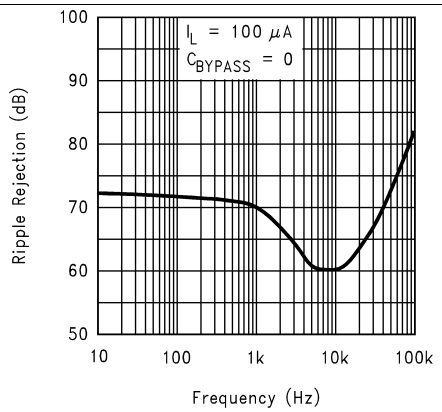



**Figure 19. Ripple Rejection**

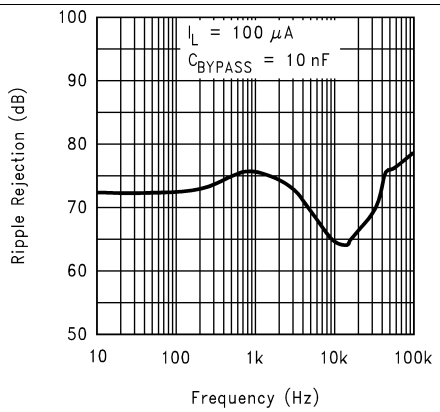



**Figure 20. Ripple Rejection**

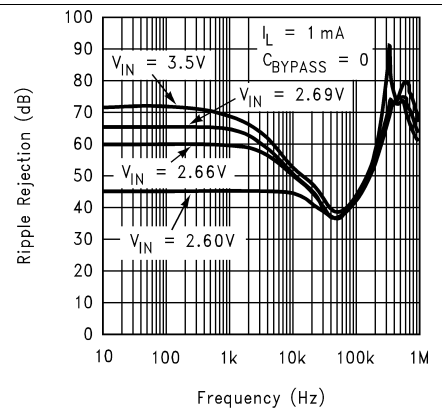



**Figure 21. Ripple Rejection**

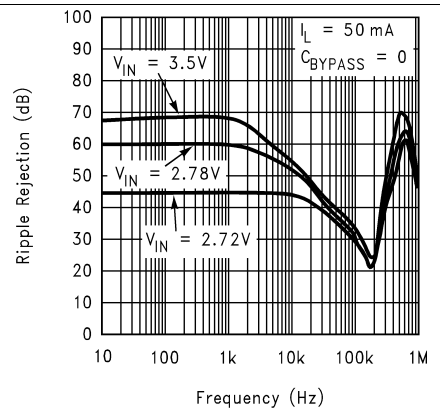



**Figure 22. Ripple Rejection**

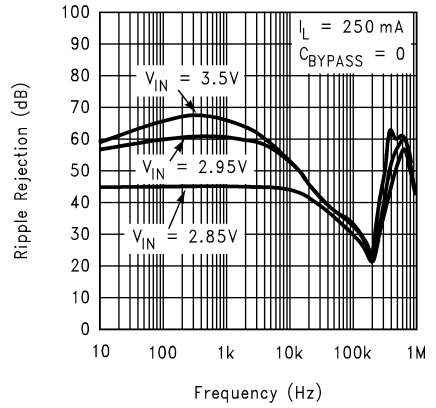



**Figure 23. Ripple Rejection**

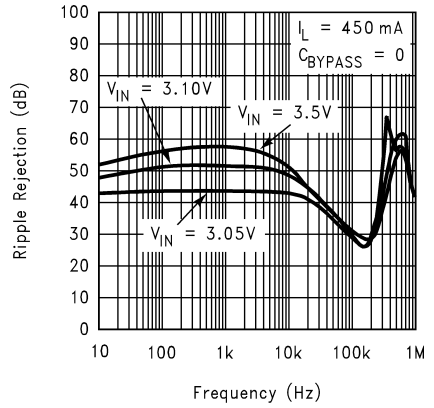



**Figure 24. Ripple Rejection**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

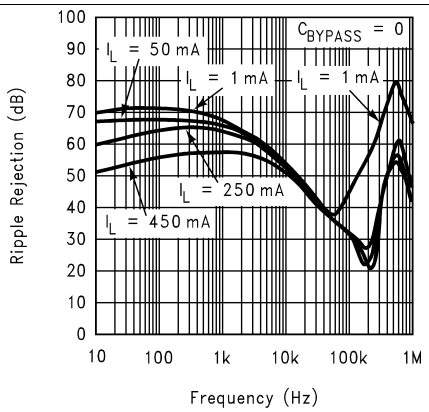



**Figure 25. Ripple Rejection**

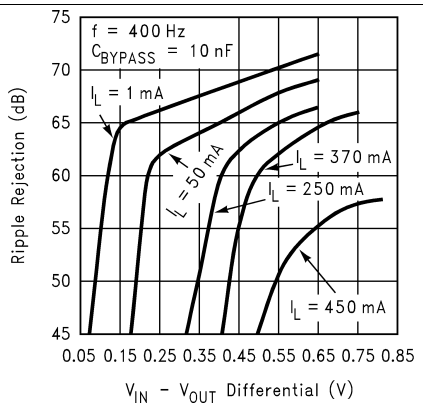



**Figure 26. Ripple Rejection in Dropout**

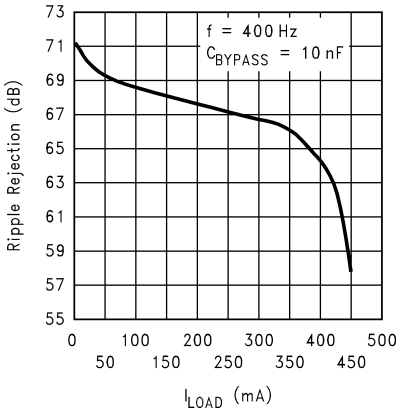



**Figure 27. Ripple Rejection vs Load**

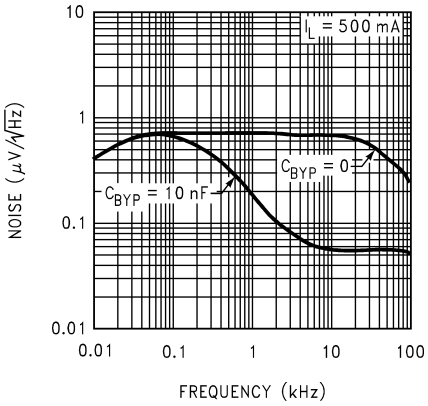



**Figure 28. Output Noise Density**

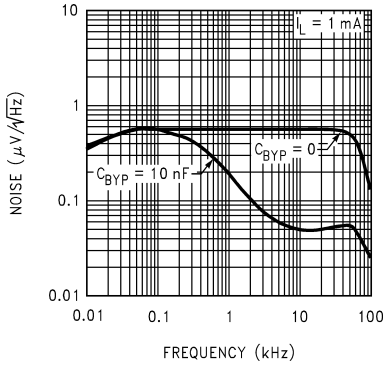



**Figure 29. Output Noise Density**

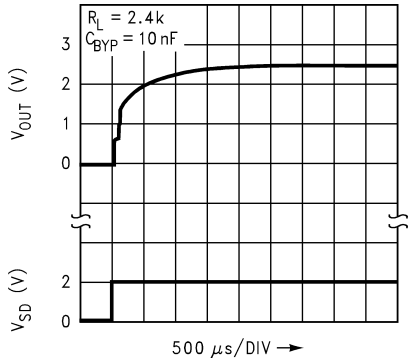



**Figure 30. Turn-ON Waveform**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

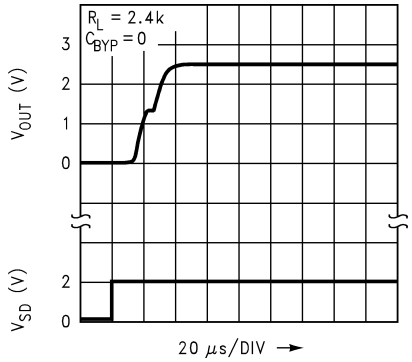



**Figure 31. Turn-ON Waveform**

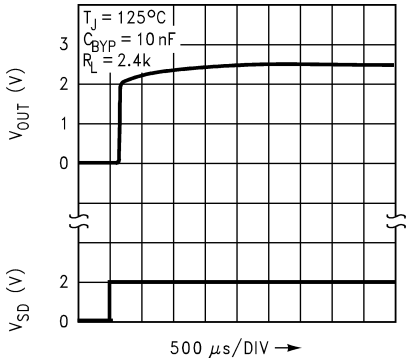



**Figure 32. Turn-ON Waveform**

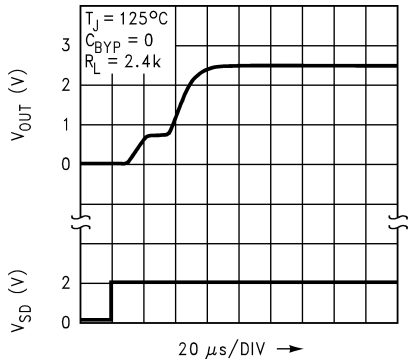



**Figure 33. Turn-ON Waveform**

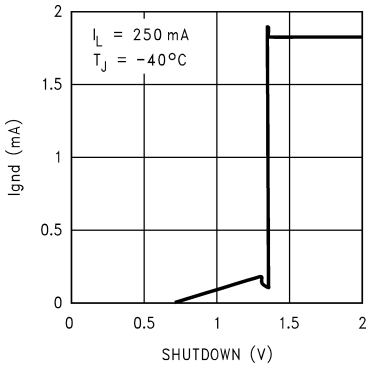



**Figure 34. $I_{GND}$ vs Shutdown**

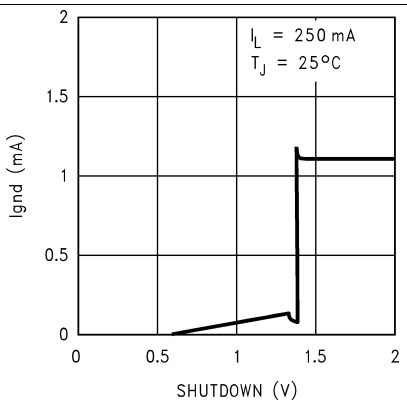



**Figure 35. $I_{GND}$ vs Shutdown**

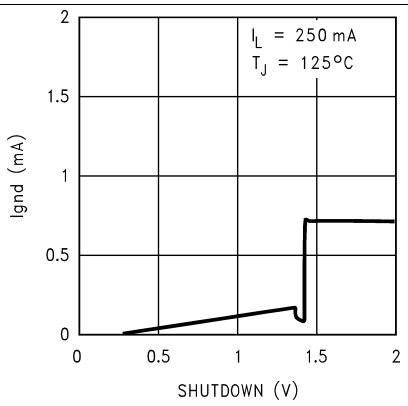



**Figure 36. $I_{GND}$ vs Shutdown**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

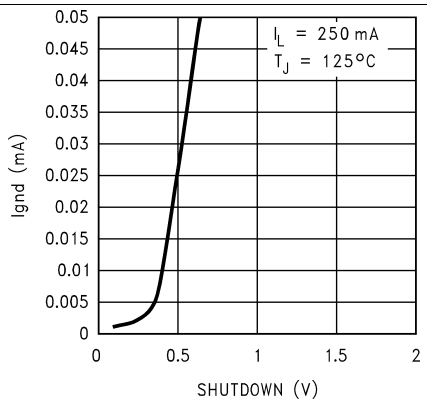



**Figure 37. $I_{GND}$ vs Shutdown**

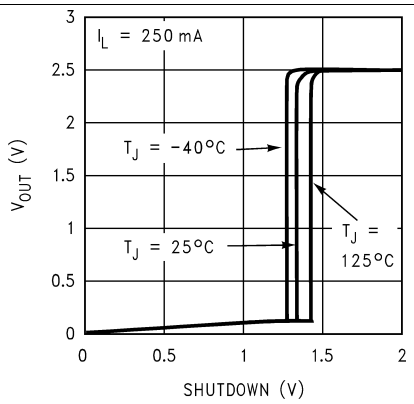



**Figure 38. $V_{OUT}$ vs Shutdown**

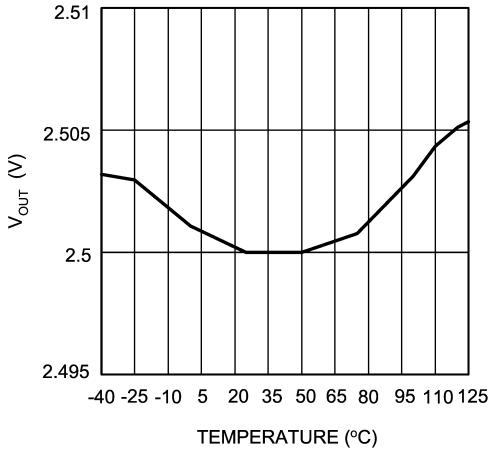



**Figure 39. Typical Temperature vs $V_{OUT}$ (LP2989-2.5)**

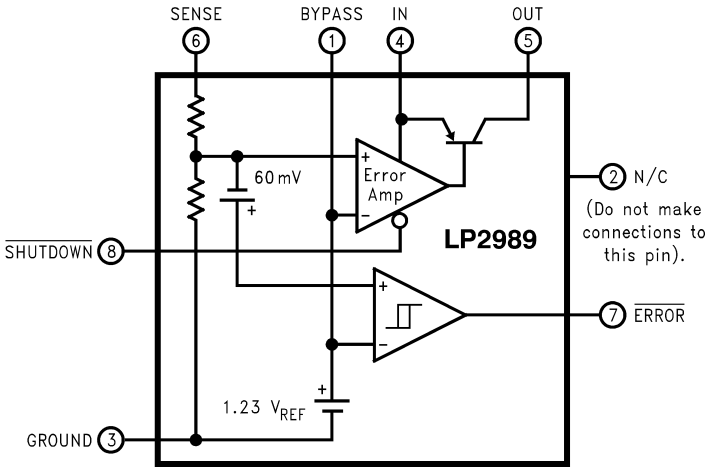
# 7 Detailed Description

## 7.1 Overview

The LP2989 device is a very high-accuracy micro-power voltage regulator with low quiescent current (75 µA typical) and low dropout voltage (typical 40 mV at light loads and 380 mV at 100 mA). It is ideally suited for use in battery-powered systems. The LP2989 block diagram contains several features, including:

- Very high-accuracy 1.23-V reference
- Fixed 2.5-V to 5-V versions
- Shutdown input
- Error flag output
- Internal protection circuitry, such as foldback current limit, and thermal shutdown

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2989 distinguishes itself as a very high output-voltage-accuracy micro-power LDO. This includes a tight initial tolerance (.75% typical, A grade), extremely good line regulation (.005%/V typical), and a very low output-noise voltage (10 $\mu_{VRMS}$ typical), making the device an ideal a low-power voltage reference.

### 7.3.2 Sleep Mode

When pulling $\overline{\text{SHUTDOWN}}$ pin to low levels, the LP2989 enters shutdown mode, and a very low quiescent current is consumed. This function is designed for applications which needs a shutdown mode to effectively enhance battery life cycle.

### 7.3.3 Error Detection Comparator Output

The LP2989 will generate a logic low output whenever its output falls out of regulation by more than approximately 5%. Refer to *Application and Implementation* for more details.

## Feature Description (continued)

### 7.3.4 Short Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device may not start correctly.

### 7.3.5 Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the device is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

## 7.4 Device Functional Modes

### 7.4.1 Operation With 16 V ≥ $V_{IN}$ > $V_{OUT(TARGET)}$ + 1 V

The device operates if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 1 V. At input voltages below the minimum $V_{IN}$ requirement, the devices does not operate correctly, and output voltage may not reach target value.

### 7.4.2 Operation with Shutdown Control

If the voltage on the $\overline{\text{SHUTDOWN}}$ pin is less than 0.18 V, the output is ensured to be OFF. When the voltage on the $\overline{\text{SHUTDOWN}}$ pin is more than 1.6 V the output is ensured to be ON. Operating with the $\overline{\text{SHUTDOWN}}$ pin voltage between 0.18 V and 1.6 V is strongly discouraged as the status of the output is not ensured.

### 7.4.3 Shutdown Input Operation

The LP2989 is shut off by driving the $\overline{\text{SHUTDOWN}}$ pin low, and turned on by pulling it high. If this feature is not to be used, the $\overline{\text{SHUTDOWN}}$ should be tied to $V_{IN}$ to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the *Electrical Characteristics* section under $V_{\overline{SD}}$.

To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the Shutdown input must have a slew rate which is ≥ 40 mV/µs.

**CAUTION**

The regulator output voltage **cannot** be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification $V_{\overline{SD}}$ (see the *Electrical Characteristics* table).

# 8 Application and Implementation

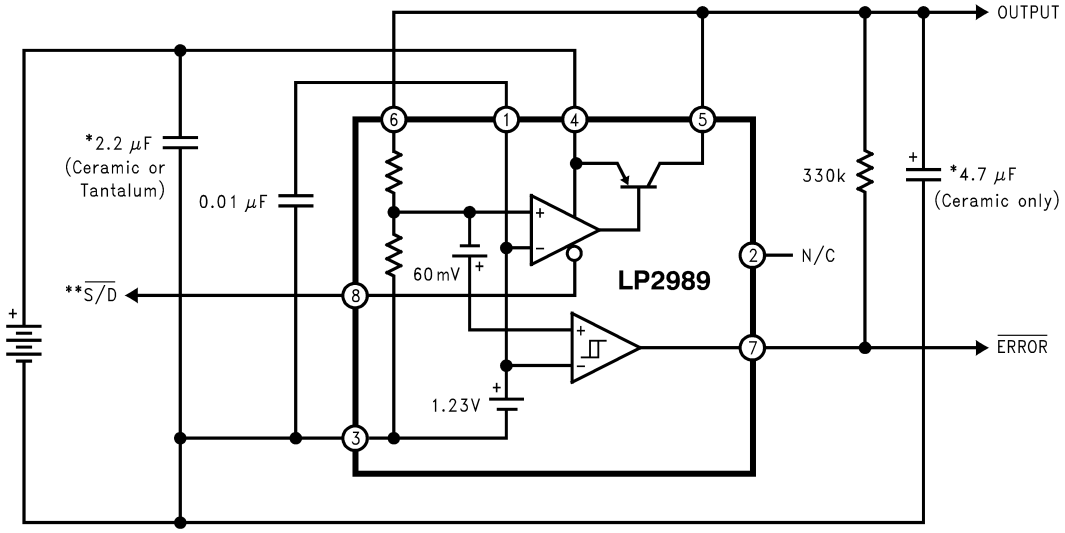
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LP2989 is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 2.5 V to 5 V with 0.75% accuracy and 500 mA maximum outputs current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2989 is a linear voltage regulator. To achieve high efficiency, the dropout voltage ($V_{IN} – V_{OUT}$) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, PSRR, or any other transient specification is required, the design becomes more challenging. This section discusses the implementation and behavior of the LP2989 LDO.

## 8.2 Typical Application




*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. See the *Output Capacitor* section.

**Shutdown must be actively terminated (see the *Shutdown Input Operation* section). Tie to IN (pin 4) if not use.

**Figure 40. Typical Application Schematic**

### 8.2.1 Design Requirements

| DESIGN PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 6.5 V, ±10%, |
| Output voltage | 5 V, ±1% |
| Output current | 500 mA (maximum), 1 mA (minimum) |
| RMS noise, 100 Hz to 100 kHz | 18 $\mu V_{RMS}$ typical |
| PSRR at 1 kHz | 60 dB typical |

### 8.2.2 Detailed Design Procedure

At 500-mA loading, the dropout of the LP2989 has 650-mV maximum dropout over temperature, thus an 1500-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2989 in this configuration is $V_{OUT}$ / $V_{IN}$ = 76.9%. To achieve the smallest form factor, the WSON package is selected. Input and output capacitors are selected in accordance with the capacitor recommendations. Ceramic capacitances of 2.2 µF for the input and one 4.7-µF capacitor for the output are selected. With an efficiency of 76.9% and a 500-mA maximum load, the internal power dissipation is 750 mW, which corresponds to a 26.1°C junction temperature rise for the WSON package. With an 85°C maximum ambient temperature, the junction temperature is at 111.1°C. To minimize noise, a bypass capacitance ($C_{BYPASS}$) of 0.01 µF is placed from the BYPASS pin (device pin 1) to device ground (device pin 3).

#### *8.2.2.1 WSON Package Devices*

The LP2989 is offered in the 8-lead WSON surface mount package to allow for increased power dissipation compared to the SOIC and VSSOP packages. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).

For output voltages < 2 V, see LP2989LV (SNVS086) data sheet.

#### *8.2.2.2 External Capacitors*

Like any low-dropout regulator, the LP2989 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

##### 8.2.2.2.1 Input Capacitor

An input capacitor whose value is at least 2.2 µF is required between the LP2989 input and ground (the amount of capacitance may be increased without limit).

Characterization testing performed on the LP2989 has shown that if the value of actual input capacitance drops below about 1.5 µF, an unstable operating condition may result. Therefore, the next larger standard size (2.2 µF) is specified as the minimum required input capacitance. Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see *Capacitor Characteristics* section) to assure the minimum requirement of 1.5 µF is met over all operating conditions.

The input capacitor must be located at a distance of not more than 0.5 inches from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor, assuming the minimum capacitance requirement is met.

##### 8.2.2.2.2 Output Capacitor

The LP2989 requires a ceramic output capacitor whose value is at least 4.7 µF. The actual amount of capacitance on the output must never drop below about 3.5 µF or unstable operation may result. For this reason, capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP2989 is designed specifically to work with ceramic output capacitors, using circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 4 mΩ. It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see the *Capacitor Characteristics* section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an equivalent series resistance (ESR) value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see Figure 41).

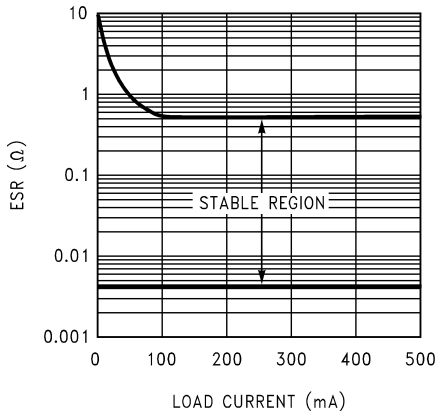



**Figure 41. Stable Region for Output Capacitor ESR**

**NOTE**

**Important:** The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

It is important to remember that capacitor tolerance and variation with temperature must be considered when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. (See the *Capacitor Characteristics* section.)

The output capacitor must be located not more than 0.5 inches from the OUT pin and returned to a clean analog ground.

#### 8.2.2.2.3 Noise Bypass Capacitor

Connecting a 10-nF capacitor to the BYPASS pin significantly reduces noise on the regulator output. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause the regulated output voltage to drop. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Ten-nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

### *8.2.2.3 Capacitor Characteristics*

#### 8.2.2.3.1 Ceramic

The LP2989 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 4.7 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 4.7-µF ceramic capacitor is in the range of 10 mΩ to 15 mΩ, which easily meets the ESR limits required for stability by the LP2989.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large-value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 4.7-µF capacitor were used on the output because it will drop down to approximately 2.4 µF at high ambient temperatures (which could cause the LP2989 to oscillate). Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

*For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP2989.*

#### 8.2.2.3.2 Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are typically more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics; while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

Tantalum capacitors may be used on the input as long as the requirement for minimum capacitance is met.

#### 8.2.2.3.3 Film

Polycarbonate and polypropelene film capacitors have excellent electrical performance: their ESR is the lowest of the three types listed, their capacitance is very stable with temperature, and DC leakage current is extremely low.

One disadvantage is that film capacitors are larger in physical size than ceramic or tantalum which makes film a poor choice for either input or output capacitors.

However, their low leakage makes them a good choice for the noise bypass capacitor. Because the required amount of capacitance is only 0.01 µF, small surface-mount film capacitors are available in this size.

### *8.2.2.4 Reverse Input-Output Voltage*

The PNP power transistor used as the pass element in the LP2989 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn on and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow high current to flow into $V_{IN}$ can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from $V_{IN}$ to $V_{OUT}$ (cathode on $V_{IN}$, anode on $V_{OUT}$), to limit the reverse voltage across the LP2989 to 0.3 V (see the *Absolute Maximum Ratings* table).

## 8.2.3 Application Curves

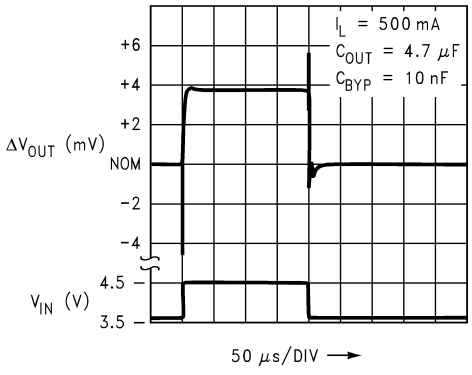



**Figure 42. Line Transient Response**

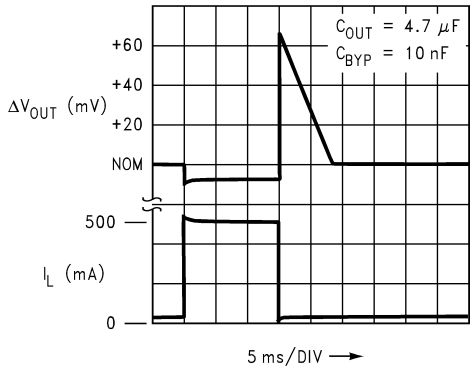



**Figure 43. Load Transient Response**

# 9 Power Supply Recommendations

The LP2989 is designed to operate from an input voltage supply range from 2.1 V to 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

# 10 Layout

## 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

## 10.2 Layout Example

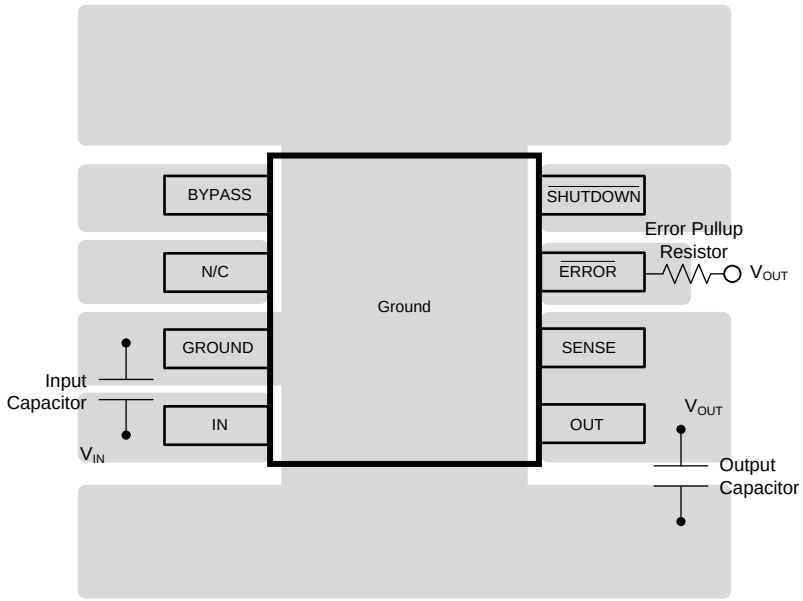



**Figure 44. Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

LP2989LV (SNVS086) data sheet

Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).

## 11.2 Trademarks

All trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

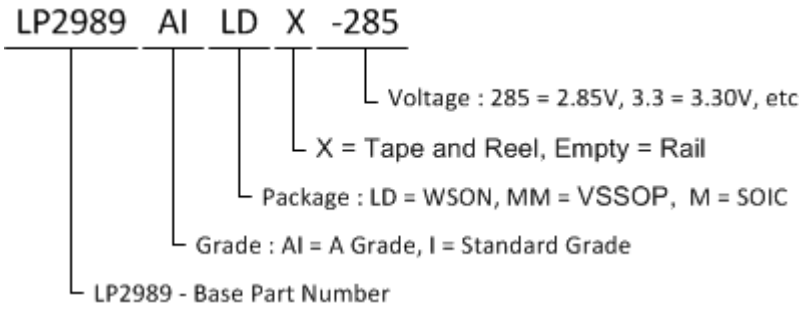



**Figure 45. POA Orderable Device Key**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2989AILD-3.0/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01HA | Samples |
| LP2989AILD-3.3/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01JA | Samples |
| LP2989AILD-5.0 | NRND | WSON | NGN | 8 | 1000 | TBD | Call TI | Call TI | -40 to 125 | L01KA | |
| LP2989AILD-5.0/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01KA | Samples |
| LP2989AILDX-2.8/NOPB | ACTIVE | WSON | NGN | 8 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L000A | Samples |
| LP2989AIM-2.5 | NRND | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 125 | 2989A IM2.5 | |
| LP2989AIM-2.5/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM2.5 | Samples |
| LP2989AIM-3.0/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM3.0 | Samples |
| LP2989AIM-3.3/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM3.3 | Samples |
| LP2989AIM-5.0 | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | 2989A IM5.0 | |
| LP2989AIM-5.0/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM5.0 | Samples |
| LP2989AIMM-2.5/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA0A | Samples |
| LP2989AIMM-3.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA1A | Samples |
| LP2989AIMM-3.3/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA2A | Samples |
| LP2989AIMM-5.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA4A | Samples |
| LP2989AIMMX-2.5/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA0A | Samples |
| LP2989AIMMX-3.3/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA2A | Samples |
| LP2989AIMMX-5.0 | NRND | VSSOP | DGK | 8 | | TBD | Call TI | Call TI | -40 to 125 | LA4A | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2989AIMMX-5.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA4A | Samples |
| LP2989AIMX-2.5/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM2.5 | Samples |
| LP2989AIMX-3.0/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM3.0 | Samples |
| LP2989AIMX-3.3/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM3.3 | Samples |
| LP2989AIMX-5.0/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989A IM5.0 | Samples |
| LP2989ILD-2.5/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01FA B | Samples |
| LP2989ILD-3.0/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01HA B | Samples |
| LP2989ILD-3.3 | NRND | WSON | NGN | 8 | | TBD | Call TI | Call TI | -40 to 125 | L01JA B | |
| LP2989ILD-3.3/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01JA B | Samples |
| LP2989ILD-5.0/NOPB | ACTIVE | WSON | NGN | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01KA B | Samples |
| LP2989ILDX-3.3 | NRND | WSON | NGN | 8 | | TBD | Call TI | Call TI | -40 to 125 | L01JA B | |
| LP2989ILDX-3.3/NOPB | ACTIVE | WSON | NGN | 8 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01JA B | Samples |
| LP2989ILDX-5.0/NOPB | ACTIVE | WSON | NGN | 8 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L01KA B | Samples |
| LP2989IM-2.5 | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | 2989 IM2.5 | |
| LP2989IM-2.5/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM2.5 | Samples |
| LP2989IM-3.0/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM3.0 | Samples |
| LP2989IM-3.3 | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | 2989 IM3.3 | |
| LP2989IM-3.3/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM3.3 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2989IM-5.0 | NRND | SOIC | D | 8 | 95 | TBD | Call TI | Call TI | -40 to 125 | 2989 IM5.0 | |
| LP2989IM-5.0/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM5.0 | Samples |
| LP2989IMM-2.8/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA6B | Samples |
| LP2989IMM-3.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA1B | Samples |
| LP2989IMM-3.3/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA2B | Samples |
| LP2989IMM-5.0 | NRND | VSSOP | DGK | 8 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LA4B | |
| LP2989IMM-5.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA4B | Samples |
| LP2989IMMX-2.8/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA6B | Samples |
| LP2989IMMX-5.0 | NRND | VSSOP | DGK | 8 | 3500 | TBD | Call TI | Call TI | -40 to 125 | LA4B | |
| LP2989IMMX-5.0/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LA4B | Samples |
| LP2989IMX-2.5/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM2.5 | Samples |
| LP2989IMX-3.0/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM3.0 | Samples |
| LP2989IMX-3.3 | NRND | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 125 | 2989 IM3.3 | |
| LP2989IMX-3.3/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM3.3 | Samples |
| LP2989IMX-5.0/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | 2989 IM5.0 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

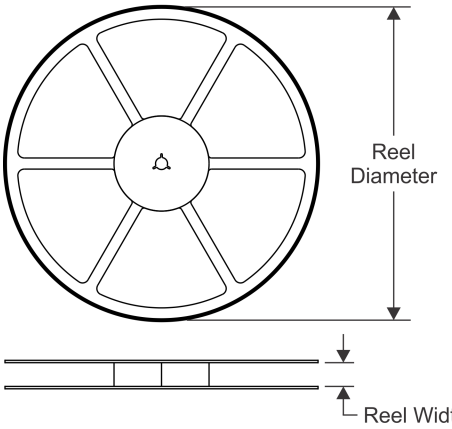
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

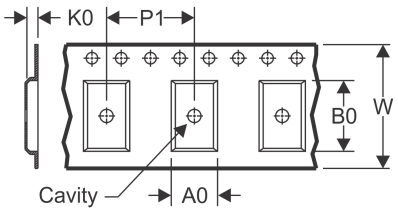
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

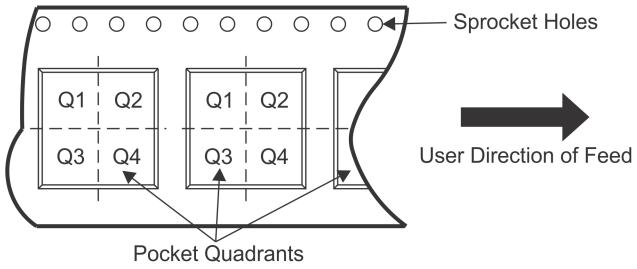



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

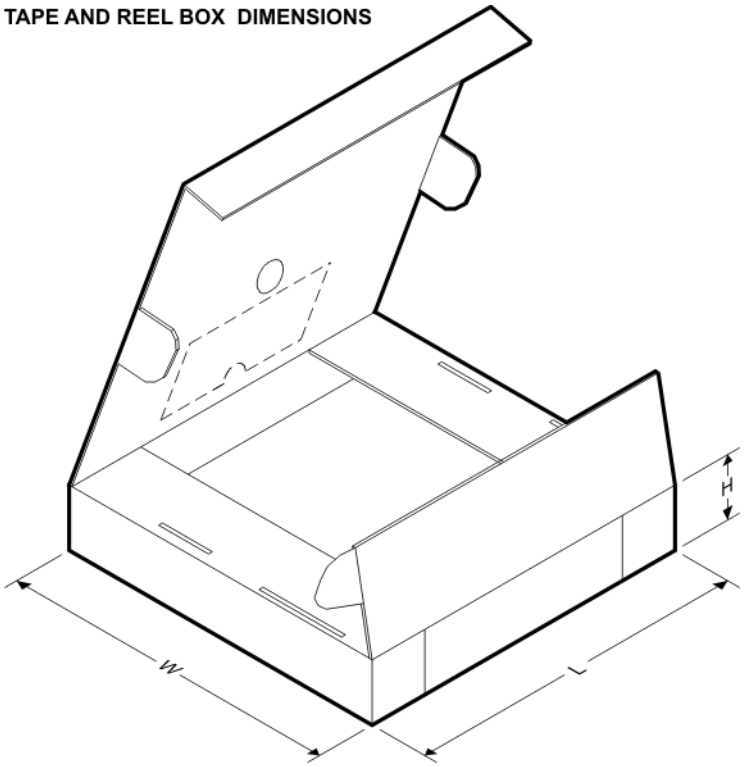



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2989AILD-3.0/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989AILD-3.3/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989AILD-5.0 | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989AILD-5.0/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989AILDX-2.8/NOPB | WSON | NGN | 8 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989AIMM-2.5/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMM-3.0/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMM-3.3/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMM-5.0/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMMX-2.5/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMMX-3.3/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMMX-5.0/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989AIMX-2.5/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989AIMX-3.0/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989AIMX-3.3/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989AIMX-5.0/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989ILD-2.5/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989ILD-3.0/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2989ILD-3.3/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989ILD-5.0/NOPB | WSON | NGN | 8 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989ILDX-3.3/NOPB | WSON | NGN | 8 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989ILDX-5.0/NOPB | WSON | NGN | 8 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LP2989IMM-2.8/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMM-3.0/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMM-3.3/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMM-5.0 | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMM-5.0/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMMX-2.8/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMMX-5.0 | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMMX-5.0/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LP2989IMX-2.5/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989IMX-3.0/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989IMX-3.3 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989IMX-3.3/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LP2989IMX-5.0/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

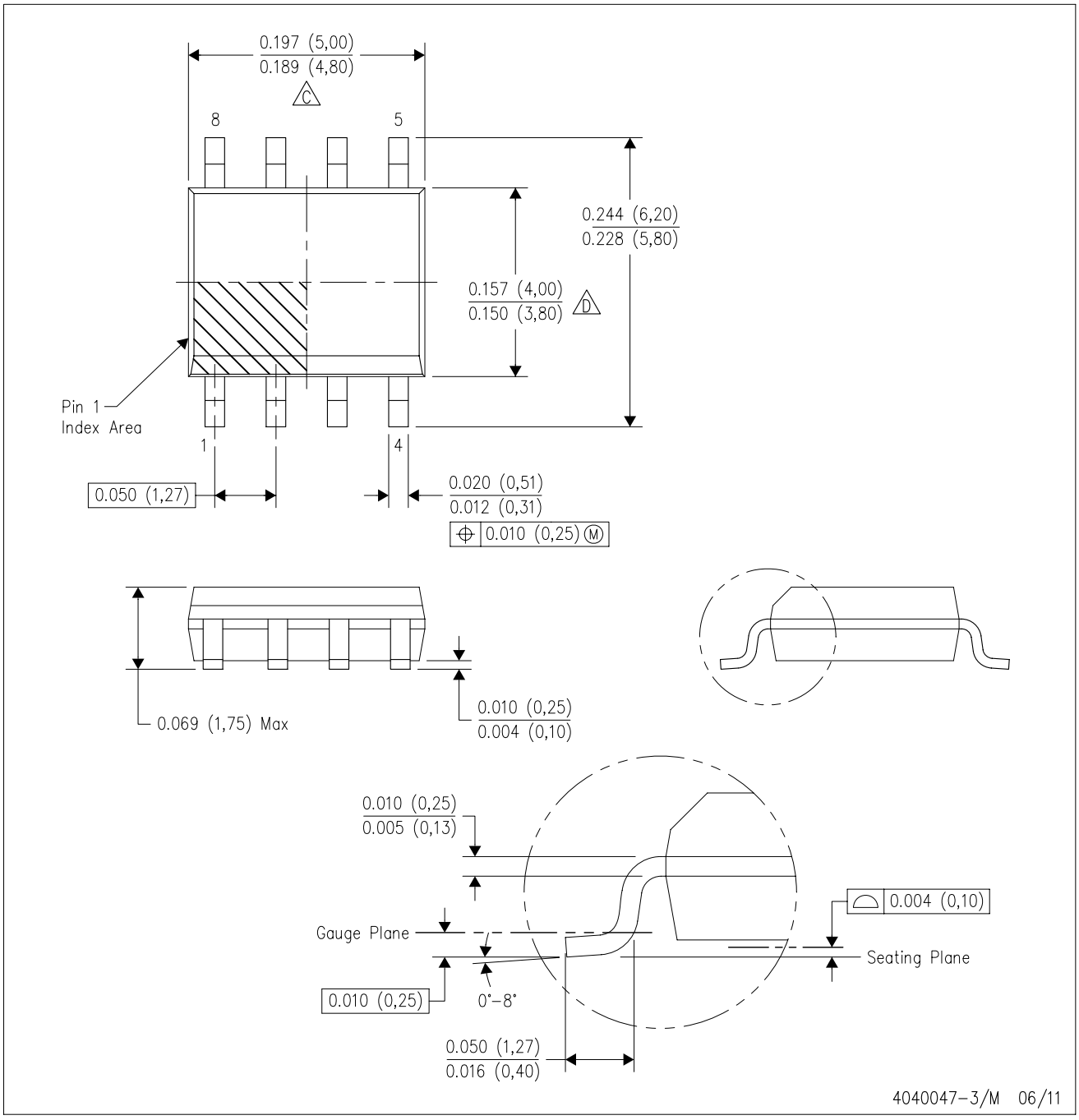
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

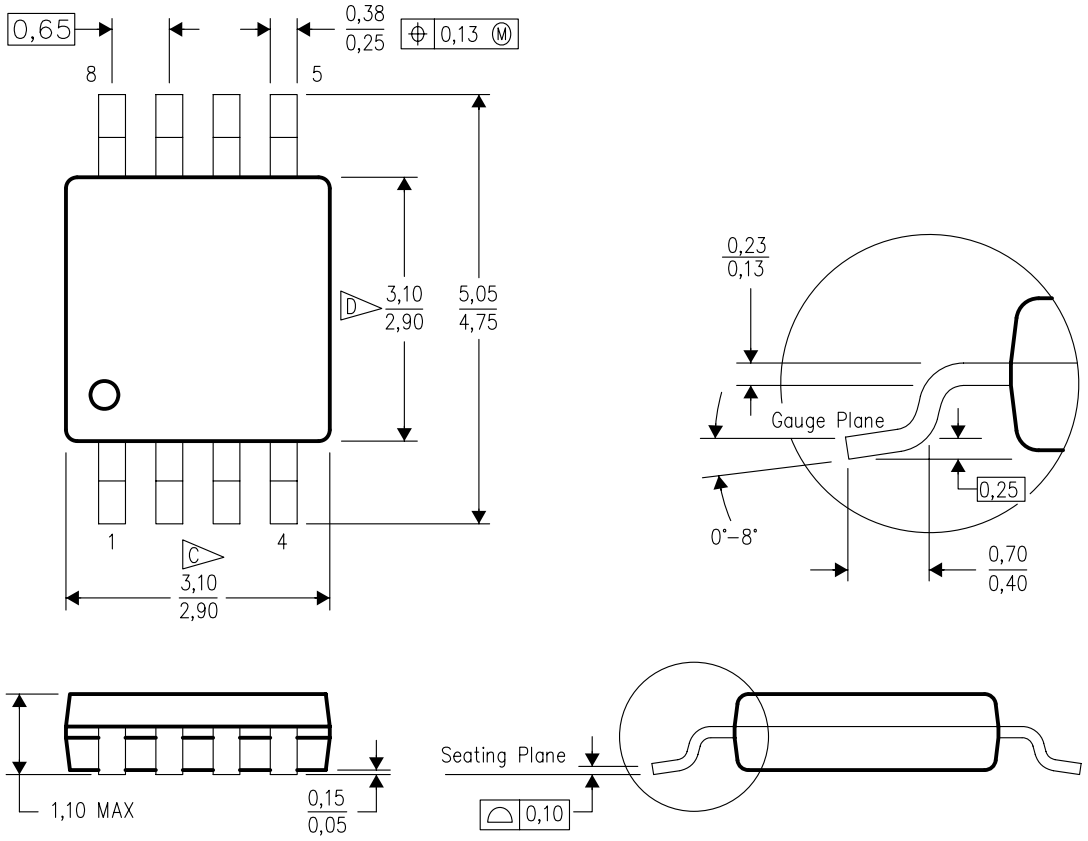
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2989AILD-3.0/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AILD-3.3/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AILD-5.0 | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AILD-5.0/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AILDX-2.8/NOPB | WSON | NGN | 8 | 4500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMM-2.5/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AIMM-3.0/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AIMM-3.3/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AIMM-5.0/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989AIMMX-2.5/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMMX-3.3/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMMX-5.0/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMX-2.5/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMX-3.0/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMX-3.3/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989AIMX-5.0/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989ILD-2.5/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989ILD-3.0/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989ILD-3.3/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989ILD-5.0/NOPB | WSON | NGN | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989ILDX-3.3/NOPB | WSON | NGN | 8 | 4500 | 367.0 | 367.0 | 35.0 |
| LP2989ILDX-5.0/NOPB | WSON | NGN | 8 | 4500 | 367.0 | 367.0 | 35.0 |
| LP2989IMM-2.8/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989IMM-3.0/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989IMM-3.3/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989IMM-5.0 | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989IMM-5.0/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2989IMMX-2.8/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989IMMX-5.0 | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989IMMX-5.0/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LP2989IMX-2.5/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989IMX-3.0/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989IMX-3.3 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989IMX-3.3/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LP2989IMX-5.0/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

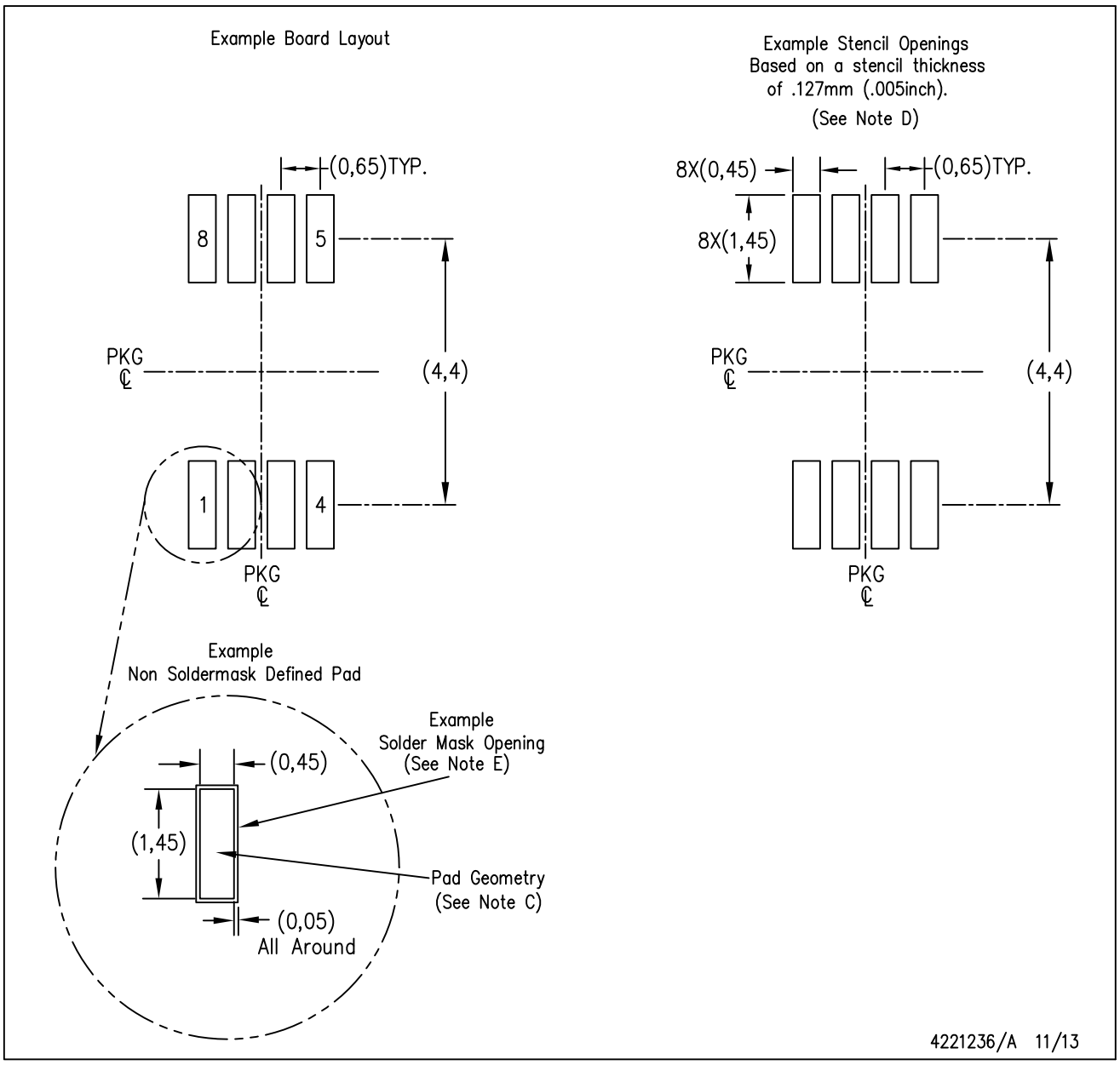
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

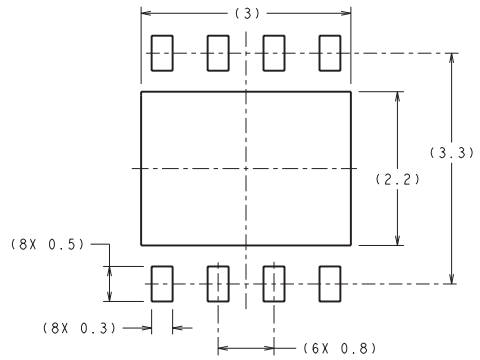
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



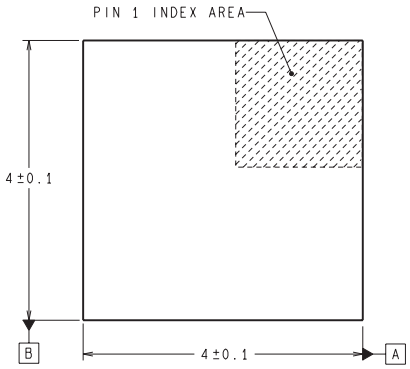

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

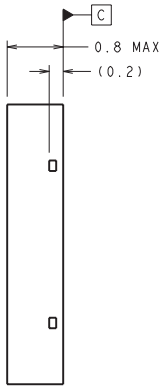
# NGN0008A

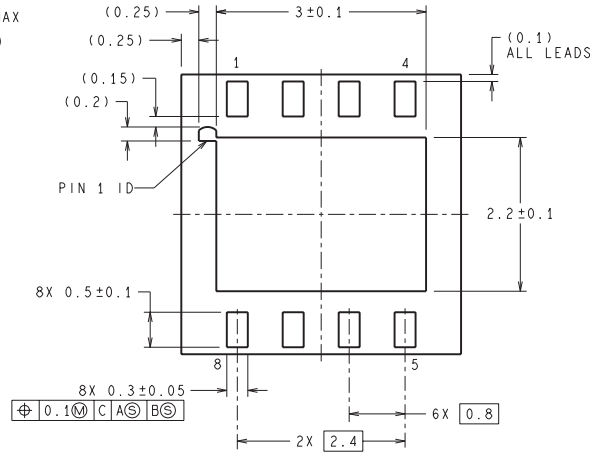



**RECOMMENDED LAND PATTERN**
1:1 RATION WITH PKG SOLDER PADS

**DIMENSIONS ARE IN MILLIMETERS**
DIMENSIONS IN ( ) FOR REFERENCE ONLY




LDC08A (Rev B)

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