

# REF50xx

## Low-Noise, Very Low Drift, Precision Voltage Reference

### 1 Features

- Low Temperature Drift:
  - High-Grade: 3 ppm/°C (Max)
  - Standard-Grade: 8 ppm/°C (Max)
- High Accuracy:
  - High-Grade: 0.05% (Max)
  - Standard-Grade: 0.1% (Max)
- Low Noise: 3  $\mu\text{V}_{\text{PP}}/\text{V}$
- Excellent Long-Term Stability:
  - 45 ppm/1000 hr (Typ) after 1000 Hours
- High-Output Current:  $\pm 10$  mA
- Temperature Range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### 2 Applications

- Precision Data Acquisition Systems
- ATE Equipment
- Industrial Process Controls
- Medical Instrumentation
- Pressure and Temperature Transmitters
- Seismic monitoring systems

### 3 Description

The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing current, and have excellent line and load regulation.

Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very low noise, make the REF50xx family ideal for use in high-precision data acquisition systems.

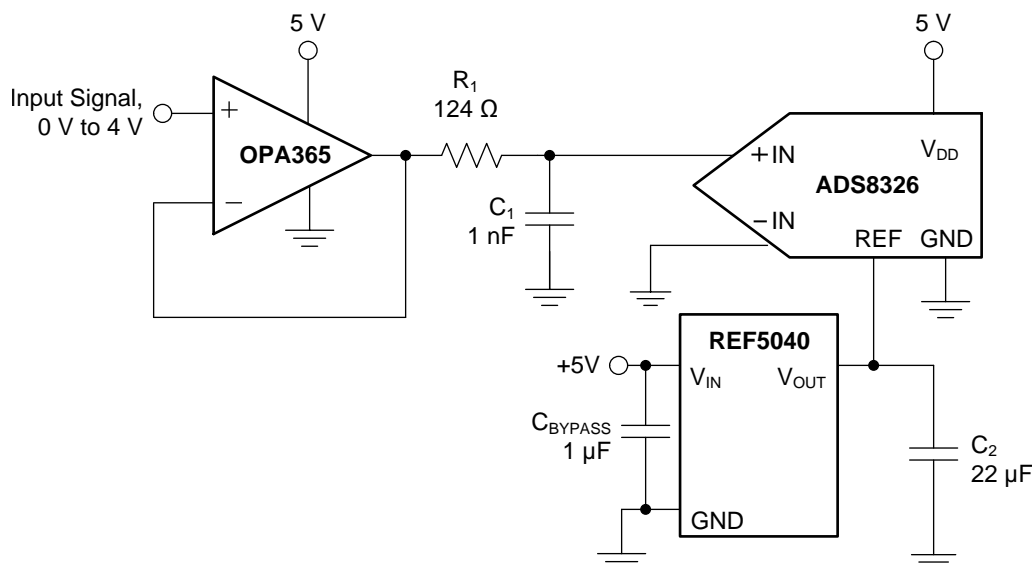
Each reference voltage is available in both high grade (REF50xxIDGK and REF50xxID) and standard grade (REF50xxAIDGK and REF50xxAID). The reference voltages are offered in 8-pin VSSOP and SOIC packages, and are specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF50xx	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.3 Feature Description .....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	9.4 Device Functional Modes .....	<b>18</b>
<b>3 Description</b> .....	<b>1</b>	<b>10 Applications and Implementation</b> .....	<b>19</b>
<b>4 Revision History</b> .....	<b>2</b>	10.1 Application Information .....	<b>19</b>
<b>5 Device Comparison Table</b> .....	<b>4</b>	10.2 Typical Applications .....	<b>19</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>11 Power Supply Recommendations</b> .....	<b>21</b>
<b>7 Specifications</b> .....	<b>5</b>	<b>12 Layout</b> .....	<b>21</b>
7.1 Absolute Maximum Ratings .....	<b>5</b>	12.1 Layout Guidelines .....	<b>21</b>
7.2 ESD Ratings .....	<b>5</b>	12.2 Layout Example .....	<b>21</b>
7.3 Recommended Operating Conditions .....	<b>5</b>	12.3 Power Dissipation .....	<b>21</b>
7.4 Thermal Information .....	<b>5</b>	<b>13 Device and Documentation Support</b> .....	<b>22</b>
7.5 Electrical Characteristics .....	<b>6</b>	13.1 Documentation Support .....	<b>22</b>
7.6 Typical Characteristics .....	<b>8</b>	13.2 Related Links .....	<b>22</b>
<b>8 Parameter Measurement Information</b> .....	<b>13</b>	13.3 Community Resources .....	<b>22</b>
8.1 Solder Heat Shift .....	<b>13</b>	13.4 Trademarks .....	<b>22</b>
<b>9 Detailed Description</b> .....	<b>15</b>	13.5 Electrostatic Discharge Caution .....	<b>22</b>
9.1 Overview .....	<b>15</b>	13.6 Glossary .....	<b>22</b>
9.2 Functional Block Diagram .....	<b>15</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>23</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision G (November 2015) to Revision H</b>	<b>Page</b>
• Changed all ( <i>Maximum</i> ) to ( <i>Max</i> ) in <i>Features</i> section .....	<b>1</b>
• Changed <i>MSOP</i> to <i>VSSOP</i> and <i>SO</i> to <i>SOIC</i> throughout document .....	<b>1</b>
• Added TI Design .....	<b>1</b>
• Changed first <i>Applications</i> bullet .....	<b>1</b>
• Changed last paragraph of <i>Description</i> section .....	<b>1</b>
• Changed <i>Simplified Schematic</i> .....	<b>1</b>
• Changed device name in <i>Recommended Operating Conditions</i> table footnote .....	<b>5</b>
• Added <i>Output Voltage</i> and <i>Noise</i> sections to <i>Electrical Characteristics</i> table .....	<b>6</b>
• Changed third bullet in <i>Layout Guidelines</i> section .....	<b>21</b>

<b>Changes from Revision F (December 2013) to Revision G</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

<b>Changes from Revision E (June 2010) to Revision F</b>	<b>Page</b>
• Changed <i>Excellent Long-Term Stability</i> feature bullet .....	1
• Changed <i>Thermal Hysteresis</i> typical values .....	6
• Changed <i>Long-Term Stability</i> typical values .....	6
• Added note 3 to <i>Electrical Characteristics</i> .....	6
• Changed <a href="#">Figure 22</a> .....	10
• Changed <a href="#">Figure 23</a> .....	10
• Changed <a href="#">Figure 24</a> .....	10
• Changed <a href="#">Figure 25</a> .....	11
• Changed <a href="#">Figure 26</a> .....	11
• Changed <a href="#">Figure 27</a> .....	11

<b>Changes from Revision D (April 2009) to Revision E</b>	<b>Page</b>
• Updated <i>Features</i> list; added <i>Excellent Long-Term Stability</i> bullet .....	1
• Added <i>Thermal Hysteresis</i> parameters and specifications .....	6
• Added <i>Long-Term Stability</i> parameters and specifications .....	6
• Added <a href="#">Figure 22</a> through <a href="#">Figure 24</a> .....	10
• Added <a href="#">Figure 25</a> through <a href="#">Figure 27</a> .....	11
• Added <i>Thermal Hysteresis</i> section.....	16
• Revised <i>Noise Performance</i> section; added paragraph with links to applications articles .....	17

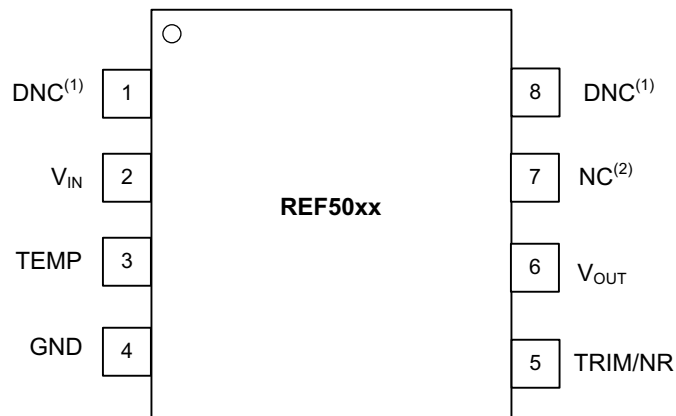
<b>Changes from Revision C (December 2008) to Revision D</b>	<b>Page</b>
• Removed all notes regarding MSOP-8 package status. MSOP-8 package released at time of document revision.....	1
• Changed <i>Storage Temperature Range</i> absolute minimum value from –55°C to –65°C.....	5
• Added <i>Load Regulation</i> test condition and <i>Over Temperature</i> specifications .....	6
• Added typical characteristic graph, <i>Quiescent Current vs Input Voltage</i> ( <a href="#">Figure 10</a> ) .....	8

## 5 Device Comparison Table

MODEL	OUTPUT VOLTAGE
REF5020	2.048 V
REF5025	2.5 V
REF5030	3 V
REF5040	4.096 V
REF5045	4.5 V
REF5050	5 V
REF5010	10 V

## 6 Pin Configuration and Functions

D, DGK Packages  
8-Pin SOIC, VSSOP  
Top View



NOTES: (1) DNC = Do not connect.  
(2) NC = No internal connection.

### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
DNC	1	Do not connect
VIN	2	Input supply voltage
TEMP	3	Temperature monitoring pin. Provides a temperature-dependent output voltage
GND	4	Ground
TRIM/NR	5	Output adjustment and noise reduction pin
VOUT	6	Reference voltage output
NC	7	No internal connection
DNC	8	Do not connect

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Input voltage	-0.2	18	V
Output short circuit	-30	30	mA
Operating temperature	-55	125	°C
Junction temperature (T <sub>J</sub> max)		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V <sub>IN</sub>	V <sub>OUT</sub> + 0.2 V <sup>(1)</sup>		18	V
I <sub>OUT</sub>	-10		10	mA

- (1) Except for the REF5020, where V<sub>IN</sub> (min) = 2.7 V.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		REF50xx		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	115	160.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	63.4	53.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	57.1	82.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	15.4	5.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.2	80.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $C_L = 1\ \mu\text{F}$ , and  $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\ \text{V})$  to 18 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT VOLTAGE</b>						
$V_{\text{OUT}}$	Output Voltage	REF5020 ( $V_{\text{OUT}} = 2.048\ \text{V}$ ) <sup>(1)</sup> , $2.7\ \text{V} < V_{\text{IN}} < 18\ \text{V}$		2.048		V
		REF5025		2.5		
		REF5030		3.0		
		REF5040		4.096		
		REF5050		5.0		
		REF5010		10.0		
	Initial Accuracy: High Grade	All voltage options <sup>(1)</sup>	-0.05%		0.05%	
	Initial Accuracy: Standard Grade	All voltage options <sup>(1)</sup>	-0.1%		0.1%	
<b>NOISE</b>						
	Output Voltage Noise	$f = 0.1\ \text{Hz}$ to 10 Hz		3		$\mu\text{V}_{\text{PP}}/\text{V}$
<b>OUTPUT VOLTAGE TEMPERATURE DRIFT</b>						
$dV_{\text{OUT}}/dT$	Output Voltage Temperature Drift					
	High-Grade			2.5	3	ppm/ $^\circ\text{C}$
	Standard-Grade			3	8	ppm/ $^\circ\text{C}$
<b>LINE REGULATION</b>						
$\Delta V_{\text{O}(\Delta\text{V})}$	Line Regulation	$V_{\text{IN}} = (V_{\text{OUT}} + 0.2)$ to 18 V <sup>(2)</sup>		0.1	1	ppm/V
		$V_{\text{IN}} = V_{\text{OUT}} + 0.2\ \text{V}$ , $T_A = -40^\circ\text{C}$ to 125 $^\circ\text{C}$ <sup>(2)</sup>		0.2	1	ppm/V
<b>LOAD REGULATION</b>						
$\Delta V_{\text{O}(\Delta\text{I})}$	Load Regulation	$-10\ \text{mA} < I_{\text{LOAD}} < 10\ \text{mA}$ , $V_{\text{IN}} = V_{\text{OUT}} + 0.75\ \text{V}$ <sup>(3)</sup>		20	30	ppm/mA
		$-10\ \text{mA} < I_{\text{LOAD}} < 10\ \text{mA}$ , $V_{\text{IN}} = V_{\text{OUT}} + 0.75\ \text{V}$ , $T_A = -40^\circ\text{C}$ to 125 $^\circ\text{C}$ <sup>(3)</sup>			50	ppm/mA
<b>SHORT-CIRCUIT CURRENT</b>						
$I_{\text{SC}}$	Short circuit current	$V_{\text{OUT}} = 0$		25		mA
<b>THERMAL HYSTERESIS<sup>(4)</sup> <sup>(5)</sup></b>						
	High-Grade	VSSOP-8	Cycle 1		50	ppm
	Standard-Grade	VSSOP-8	Cycle 1		70	ppm
	High-Grade	SOIC-8	Cycle 1		70	ppm
	Standard-Grade	SOIC-8	Cycle 1		90	ppm
	High-Grade	VSSOP-8	Cycle 2		40	ppm
	Standard-Grade	VSSOP-8	Cycle 2		40	ppm
	High-Grade	SOIC-8	Cycle 2		50	ppm
	Standard-Grade	SOIC-8	Cycle 2		50	ppm
<b>LONG-TERM STABILITY<sup>(5)</sup></b>						
		VSSOP-8	0 to 1000 hours		125	ppm/1000 hr
		VSSOP-8	1000 to 2000 hours		45	ppm/1000 hr
		SOIC-8	0 to 1000 hours		100	ppm/1000 hr
		SOIC-8	1000 to 2000 hours		50	ppm/1000 hr
<b>TEMP PIN</b>						
	Voltage Output	At $T_A = 25^\circ\text{C}$		575		mV
	Temperature Sensitivity	$T_A = -40^\circ\text{C}$ to 125 $^\circ\text{C}$		2.64		mV/ $^\circ\text{C}$
<b>TURNON SETTLING TIME</b>						
	Turnon Settling Time	To 0.1% with $C_L = 1\ \mu\text{F}$		200		$\mu\text{s}$

(1) For  $V_{\text{OUT}} \leq 2.5\ \text{V}$ , the minimum supply voltage is 2.7 V.

(2) Except for REF5020, where  $V_{\text{IN}} = 2.7\ \text{V}$  to 18 V.

(3) Except for REF5020, where  $V_{\text{IN}} = 3\ \text{V}$ .

(4) The thermal hysteresis procedure is explained in more detail in the [Thermal Hysteresis](#) section.

(5) Data collected using devices soldered onto the test board.

## Electrical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $C_L = 1\ \mu\text{F}$ , and  $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\ \text{V})$  to 18 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$V_S$	Supply Voltage	See Note <sup>(1)</sup>	$V_{\text{OUT}} + 0.2^{(1)}$		18	V
	Quiescent Current			0.8	1	mA
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			1.2	mA
<b>TEMPERATURE RANGE</b>						
	Specified Range		-40		125	$^\circ\text{C}$
	Operating Range		-55		125	$^\circ\text{C}$

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{ V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{ V}$ , the minimum supply voltage is 2.7 V.

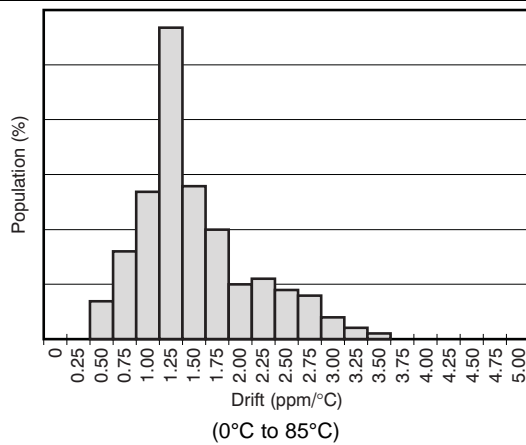


Figure 1. Temperature Drift

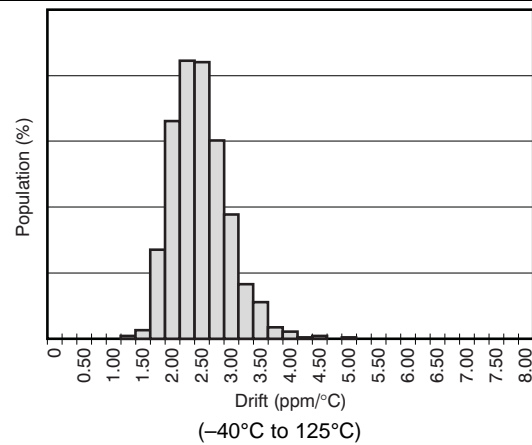


Figure 2. Temperature Drift

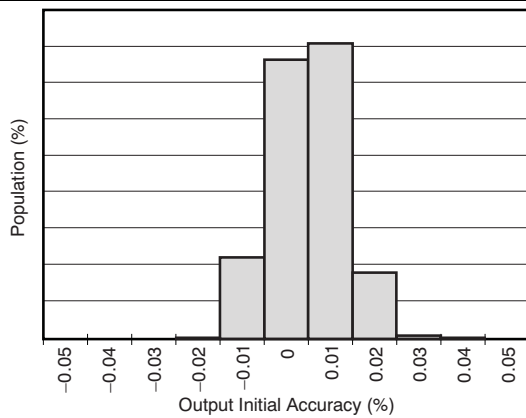


Figure 3. Output Voltage Initial Accuracy

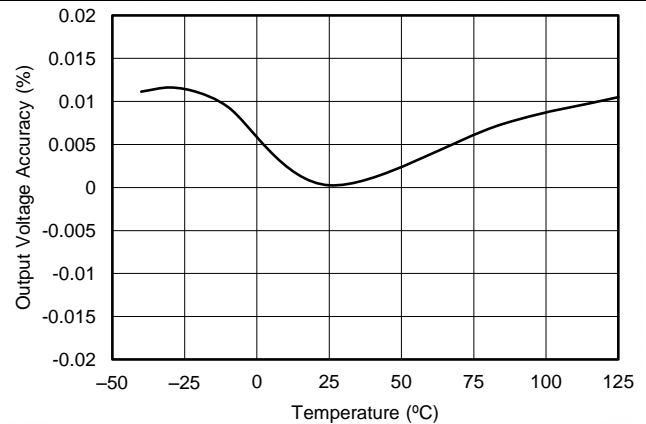


Figure 4. Output Voltage Accuracy vs Temperature

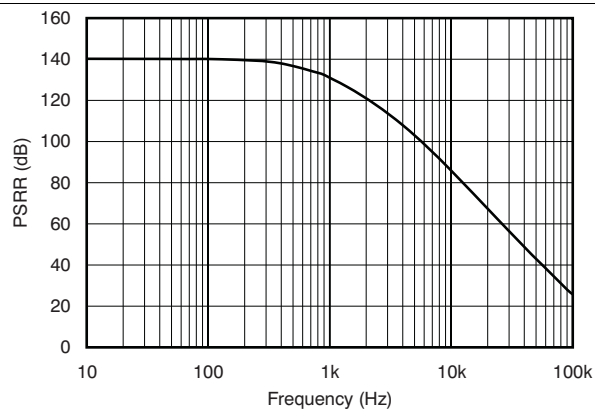


Figure 5. Power-Supply Rejection Ratio vs Frequency

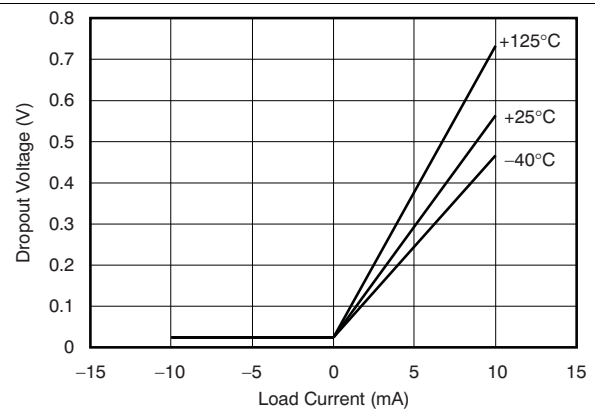


Figure 6. Dropout Voltage vs Load Current



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{ V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{ V}$ , the minimum supply voltage is 2.7 V.

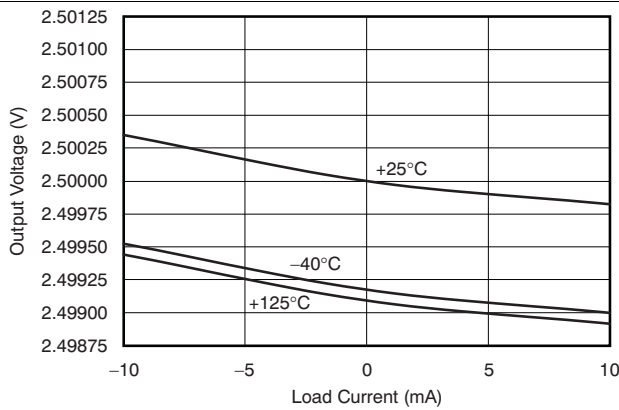


Figure 7. REF5025 Output Voltage vs Load Current

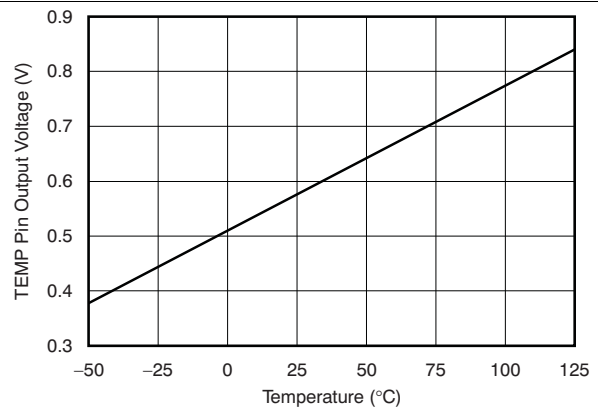


Figure 8. Temp Pin Output Voltage vs Temperature

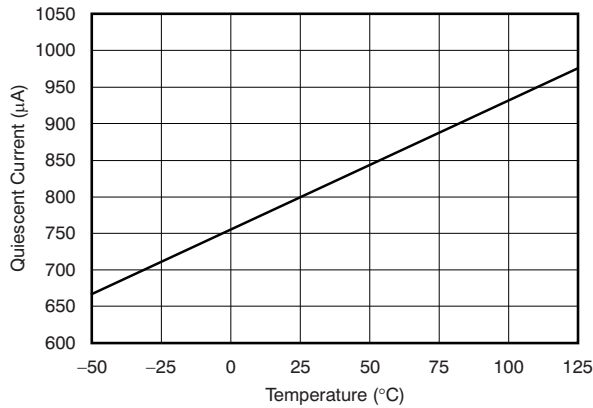


Figure 9. Quiescent Current vs Temperature

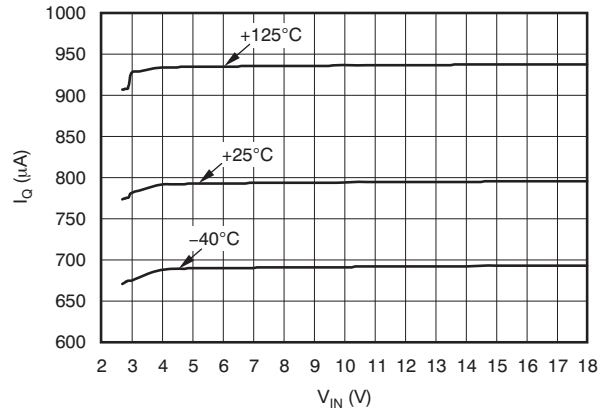


Figure 10. Quiescent Current vs Input Voltage

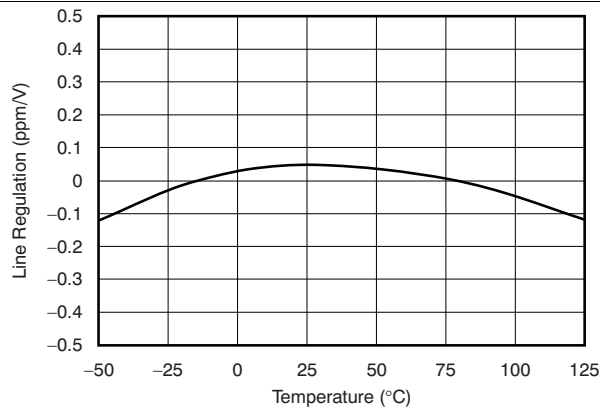


Figure 11. Line Regulation vs Temperature

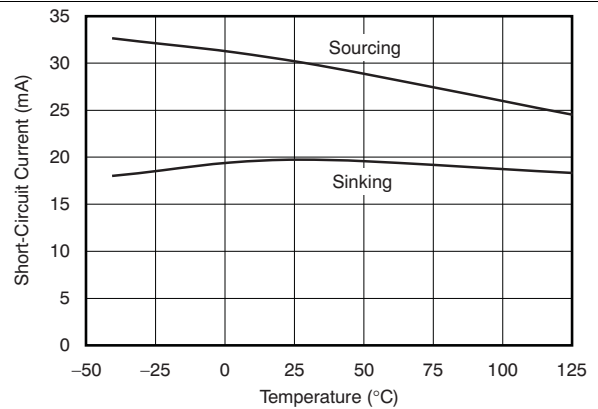


Figure 12. Short Circuit Current vs Temperature

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{ V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{ V}$ , the minimum supply voltage is 2.7 V.

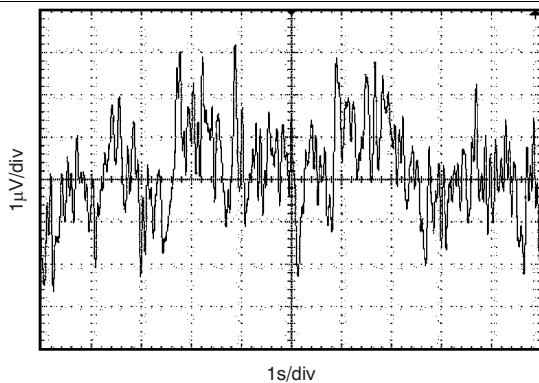


Figure 13. NOISE

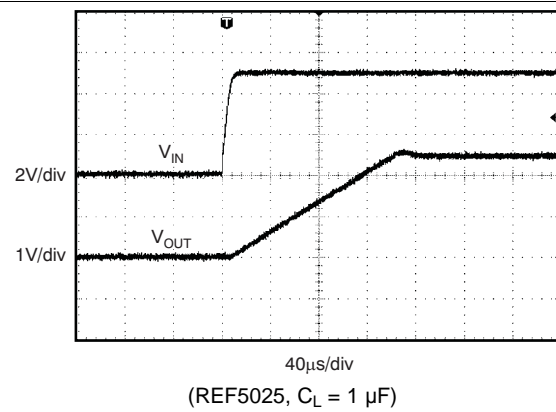


Figure 14. Start-Up

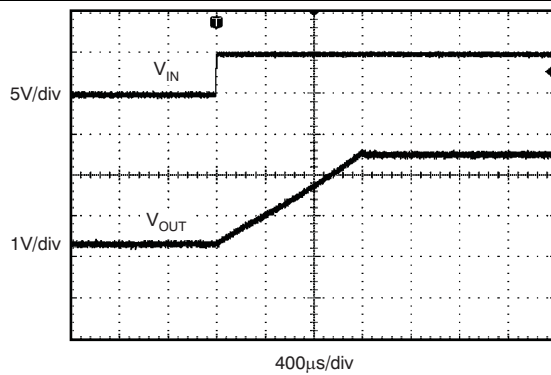


Figure 15. Start-Up

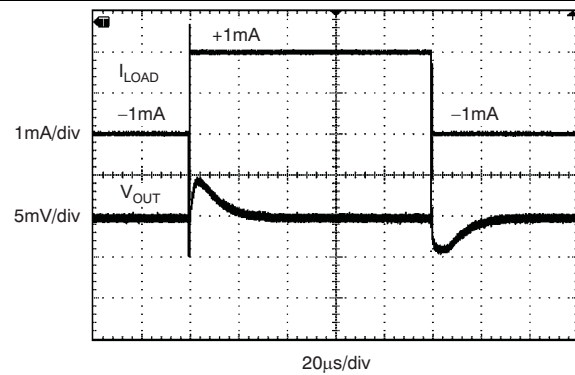


Figure 16. Load Transient

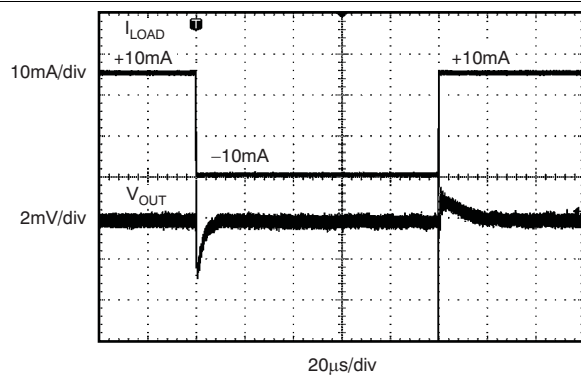


Figure 17. Load Transient

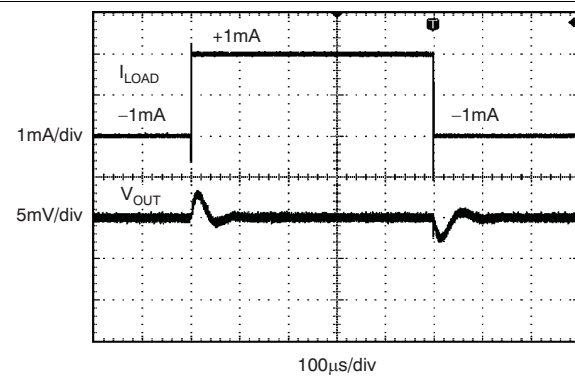
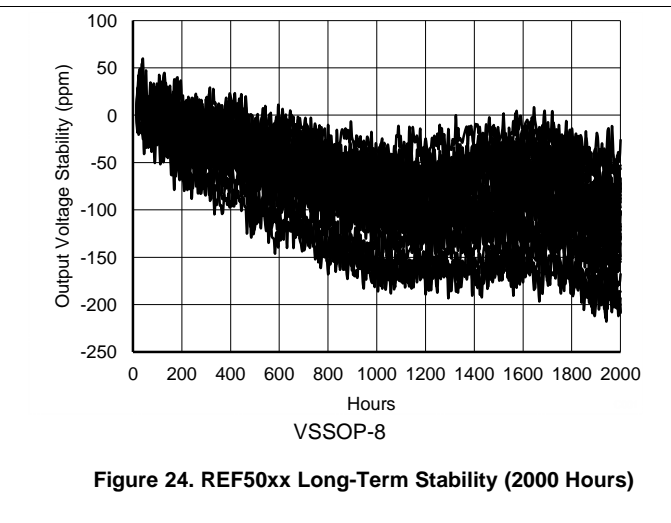
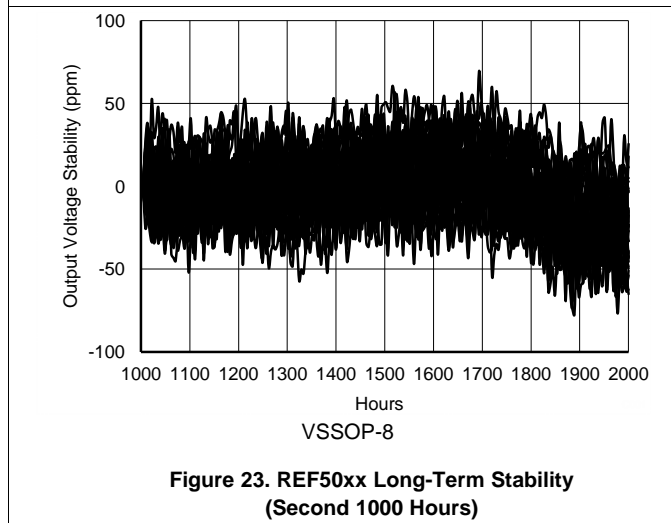
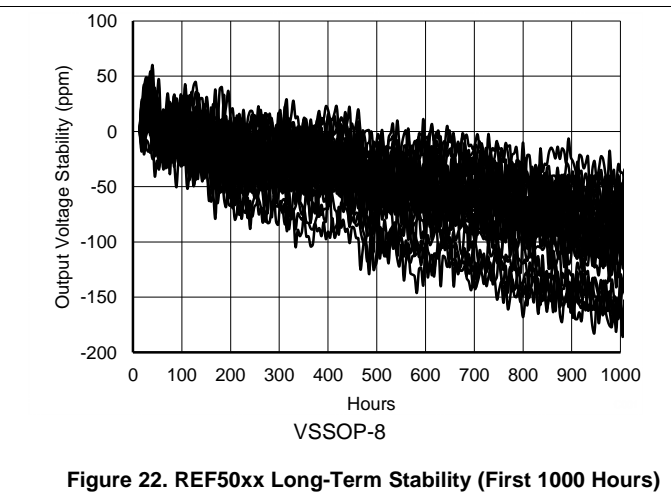
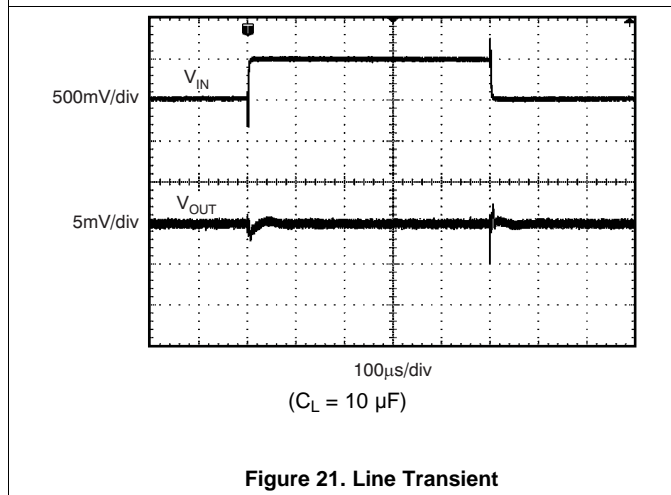
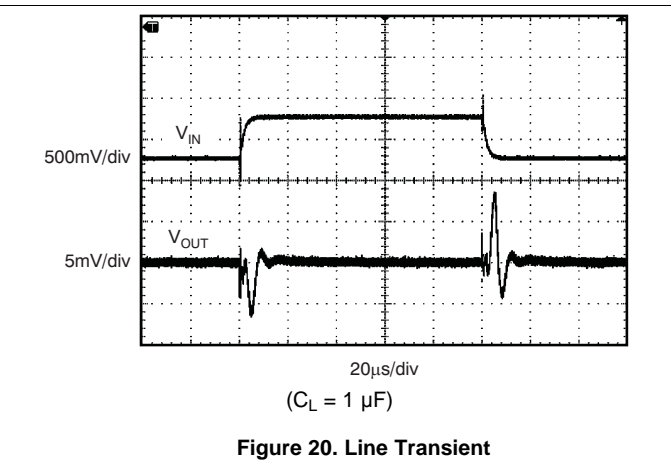
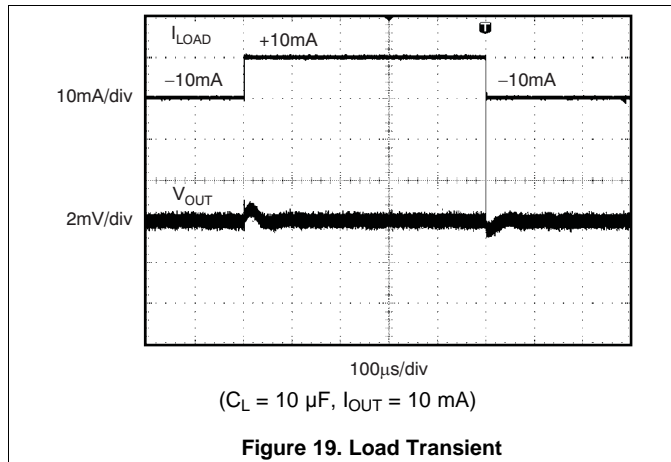


Figure 18. Load Transient

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{ V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{ V}$ , the minimum supply voltage is 2.7 V.



## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{ V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{ V}$ , the minimum supply voltage is 2.7 V.

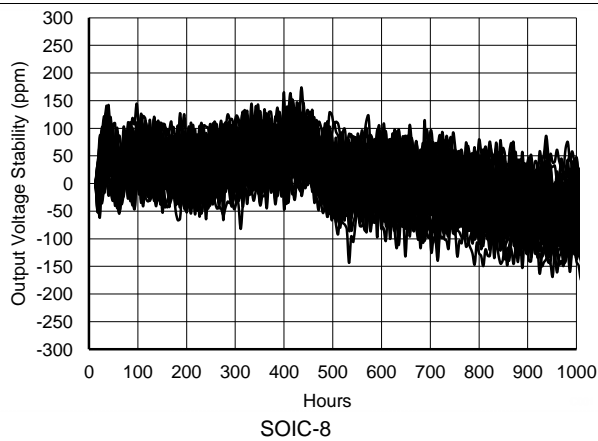


Figure 25. REF50xx Long-Term Stability (First 1000 Hours)

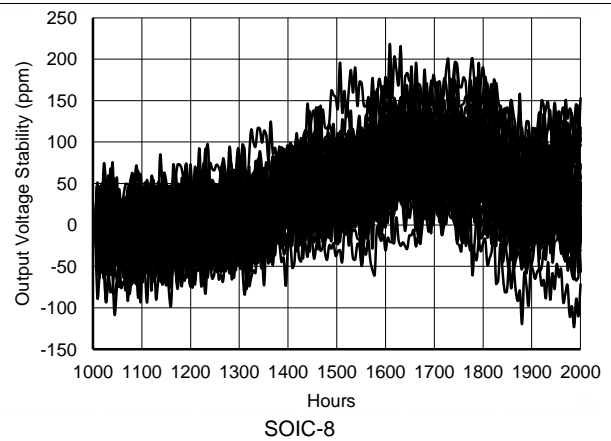


Figure 26. REF50xx Long-Term Stability (Second 1000 Hours)

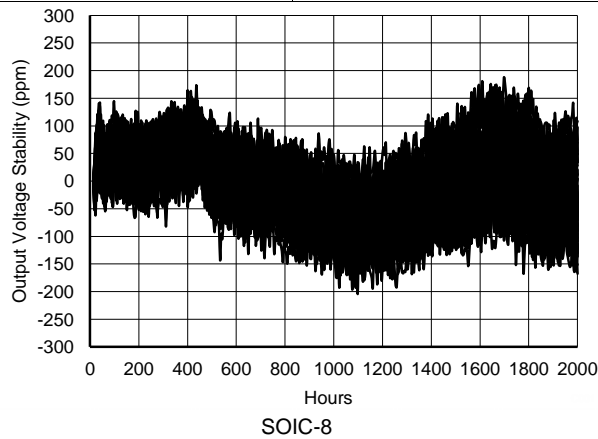


Figure 27. REF50xx Long-Term Stability (2000 Hours)

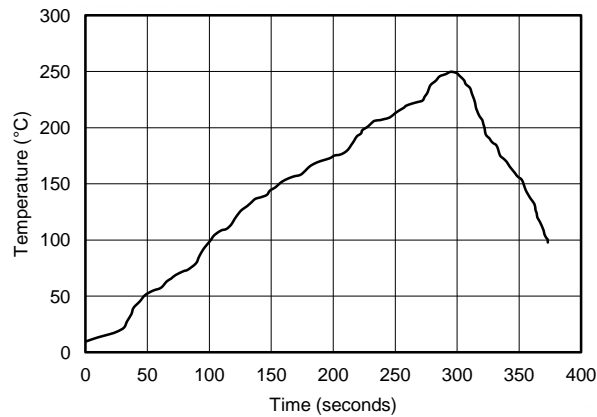
## 8 Parameter Measurement Information

### 8.1 Solder Heat Shift

The materials used in the manufacture of the REF50xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device can cause the output voltages to shift, degrading the initial accuracy and drift specifications of the product. Reflow soldering is a common cause of this error.

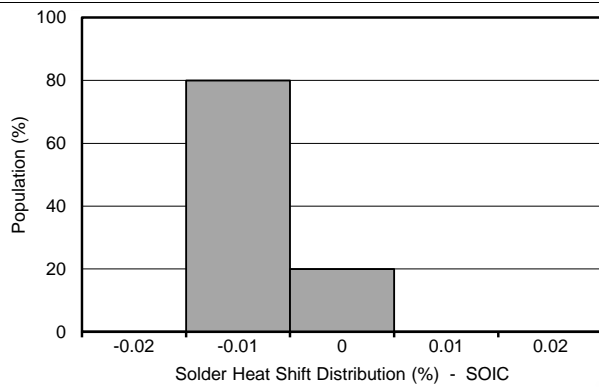
To illustrate this effect, a total of 36 devices were soldered on printed-circuit-boards using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in [Figure 28](#). The printed-circuit-board is comprised of FR4 material. The board thickness is 0.8 mm and the area is 13 mm × 13 mm.

The reference voltage is measured before and after the reflow process across temperature; the typical shift of accuracy and drift is displayed in [Figure 29](#) through [Figure 36](#). Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed-circuit-board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on printed circuit boards (PCBs) with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, then solder the device in the last pass to minimize device exposure to thermal stress.

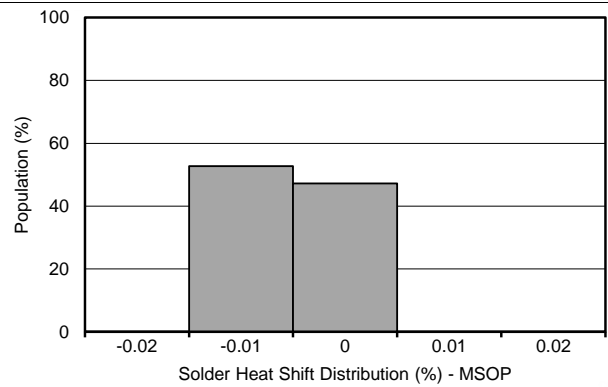


**Figure 28. Reflow Profile**

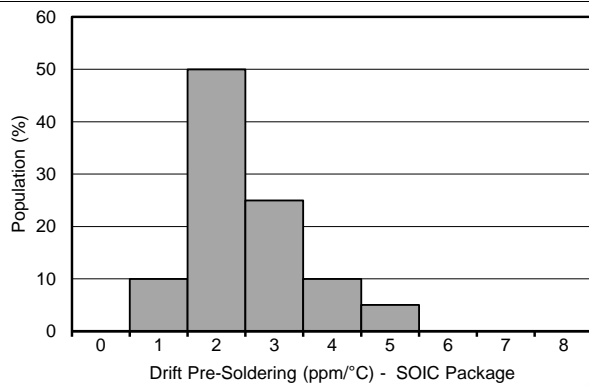
**Solder Heat Shift (continued)**



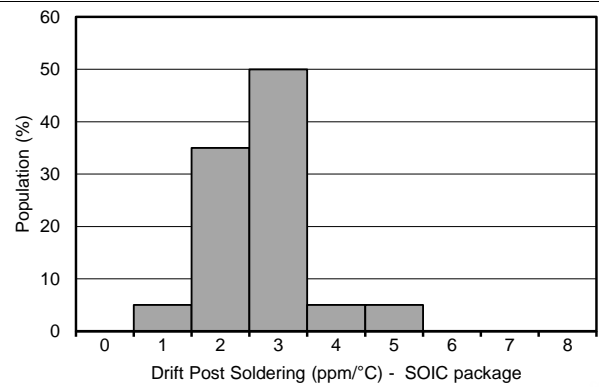
**Figure 29. Solder Heat Shift Distribution (%), SOIC Package**



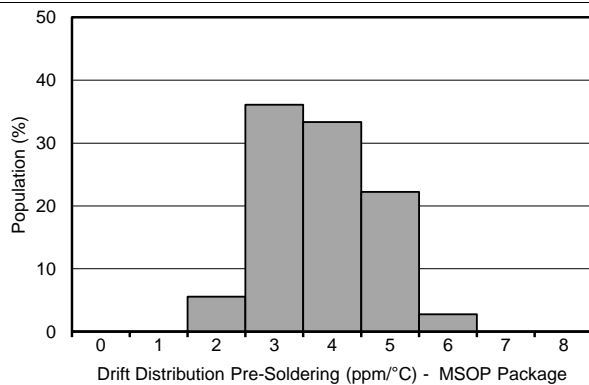
**Figure 30. Solder Heat Shift Distribution (%), VSSOP Package**



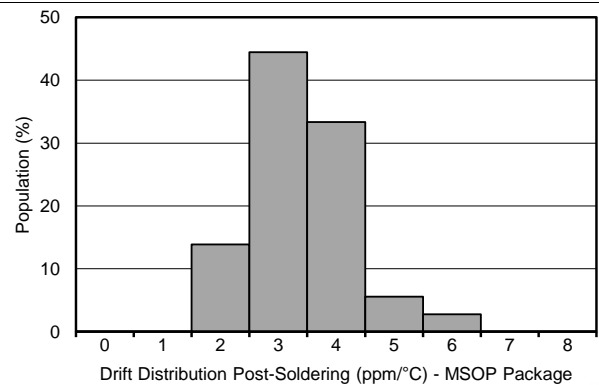
**Figure 31. Drift Pre-Soldering Distribution, SOIC Package**



**Figure 32. Drift Post Soldering Distribution, SOIC Package**

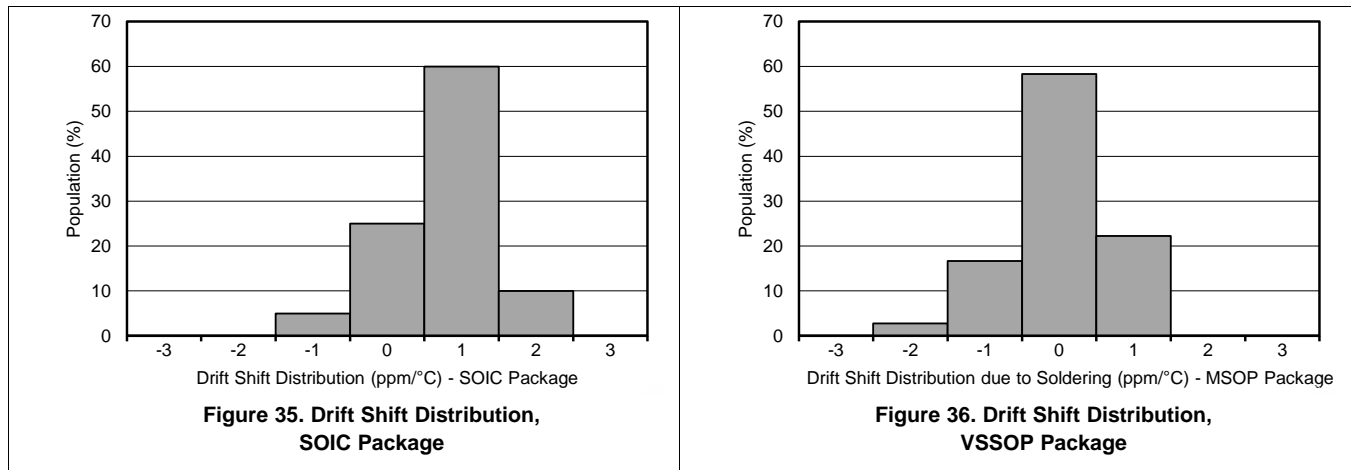


**Figure 33. Drift Distribution Pre-Soldering, VSSOP Package**



**Figure 34. Drift Distribution Post-Soldering, VSSOP Package**

## Solder Heat Shift (continued)

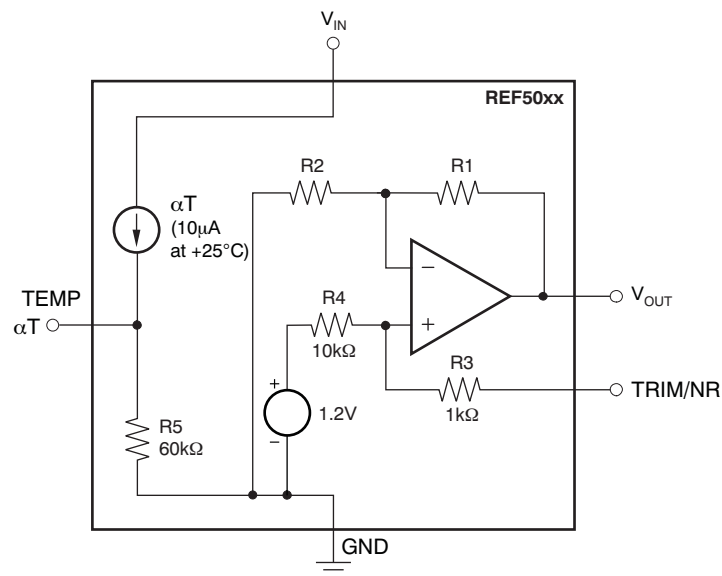


## 9 Detailed Description

### 9.1 Overview

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. See the [Functional Block Diagram](#) for a simplified block diagram of the REF50xx.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Temperature Monitoring

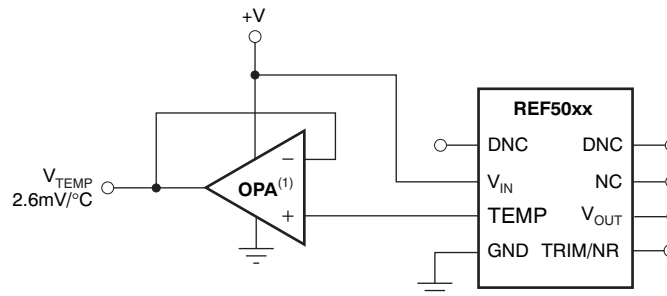
The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-k $\Omega$  source impedance. As illustrated in Figure 8, the output voltage follows the nominal relationship:

$$V_{\text{TEMP PIN}} = 509 \text{ mV} + 2.64 \times T(^{\circ}\text{C}) \quad (1)$$

This pin indicates general chip temperature, accurate to approximately  $\pm 15^{\circ}\text{C}$ . Although not generally suitable for accurate temperature measurements, this pin can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of  $30^{\circ}\text{C}$  corresponds to an approximate 79-mV change in voltage at the TEMP pin.

The TEMP pin has high-output impedance (see the *Functional Block Diagram*). Loading this pin with a low-impedance circuit induces a measurement error; however, this pin does not have any effect on  $V_{\text{OUT}}$  accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 37.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

**Figure 37. Buffering the TEMP Pin Output**

### 9.3.2 Temperature Drift

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described in Equation 2.

$$\text{Drift} = \left( \frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (2)$$

The REF50xx features a maximum drift coefficient of 3 ppm/ $^{\circ}\text{C}$  for the high-grade version, and 8 ppm/ $^{\circ}\text{C}$  for the standard-grade.

### 9.3.3 Thermal Hysteresis

Thermal hysteresis for the REF50xx is defined as the change in output voltage after operating the device at  $25^{\circ}\text{C}$ , cycling the device through the specified temperature range, and returning to  $25^{\circ}\text{C}$ . Thermal hysteresis can be expressed as Equation 3:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 (\text{ppm})$$

where

- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm).
  - $V_{\text{NOM}}$  = the specified output voltage.
  - $V_{\text{PRE}}$  = output voltage measured at  $25^{\circ}\text{C}$  pretemperature cycling.
  - $V_{\text{POST}}$  = output voltage measured after the device has been cycled from  $25^{\circ}\text{C}$  through the specified temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and returned to  $25^{\circ}\text{C}$ .
- (3)



## Feature Description (continued)

### 9.3.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for each member of the REF50xx family is specified in the [Electrical Characteristics](#) table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although take care to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. This three-part series is available for download from the TI website under three literature numbers: [SLYT331](#), [SLYT339](#), and [SLYT355](#) for [Part I](#), [Part II](#), and [Part III](#), respectively.

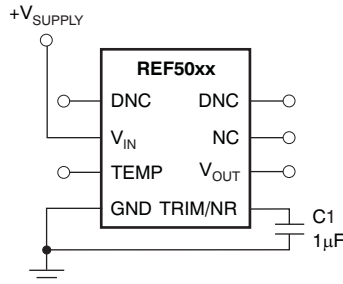


Figure 38. Noise Reduction Using the TRIM/NR Pin

### 9.3.5 Output Adjustment Using the TRIM/NR Pin

The REF50xx provides a very accurate, factory-trimmed voltage output. However,  $V_{OUT}$  can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). [Figure 39](#) shows a typical circuit that allows an output adjustment of  $\pm 15\text{mV}$

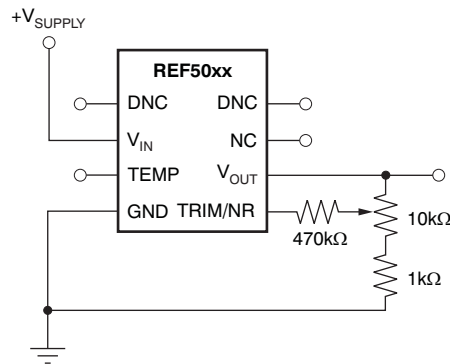


Figure 39.  $V_{OUT}$  Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND ([Figure 38](#)) in combination with the internal  $R_3$  and  $R_4$  resistors creates a low-pass filter. A capacitance of  $1\mu\text{F}$  creates a low-pass filter with the corner frequency from 10 Hz to 20 Hz. Such a filter decreases the overall noise measured on the  $V_{OUT}$  pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Using this capacitor increases start-up time.

## 9.4 Device Functional Modes

### 9.4.1 Basic Connections

Figure 40 shows the typical connections for the REF50xx. TI recommends a supply bypass capacitor ranging from 1  $\mu\text{F}$  to 10  $\mu\text{F}$ . A 1- $\mu\text{F}$  to 50- $\mu\text{F}$  output capacitor ( $C_L$ ) must be connected from  $V_{\text{OUT}}$  to GND. The equivalent series resistance (ESR) value of  $C_L$  must be less than or equal to 1.5  $\Omega$  to ensure output stability. To minimize noise, the recommended ESR of  $C_L$  is from 1  $\Omega$  and 1.5  $\Omega$ .

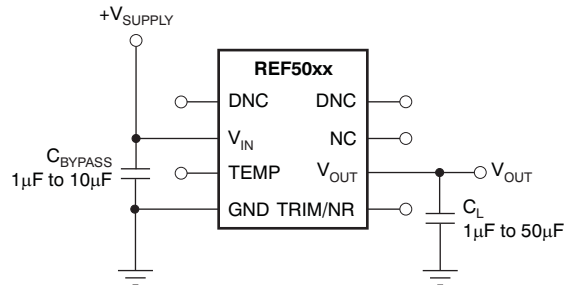


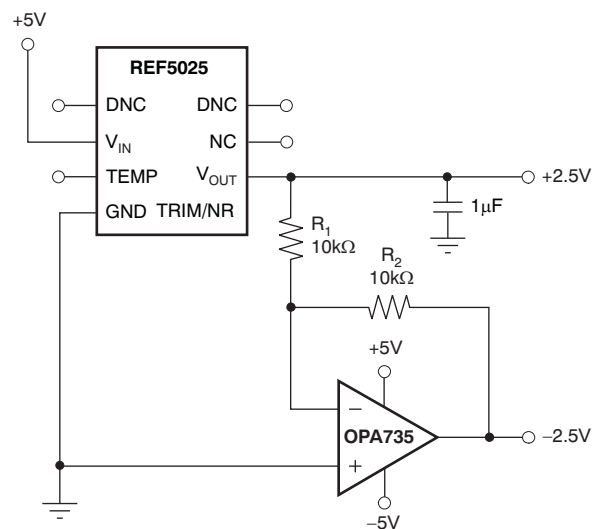
Figure 40. Basic Connections

### 9.4.2 Supply Voltage

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7 V, these references can be operated with a supply of 200 mV more than the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is provided in Figure 6 in the *Typical Characteristics*.

### 9.4.3 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 41 shows the REF5025 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of  $R_1$  and  $R_2$ .



NOTE: Bypass capacitors not shown.

Figure 41. The REF5025 and OPA735 Create Positive and Negative Reference Voltages

## 10 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 42 shows the REF5040 in a basic data acquisition system.

### 10.2 Typical Applications

#### 10.2.1 16-bit, 250-KSPS Data Acquisition System

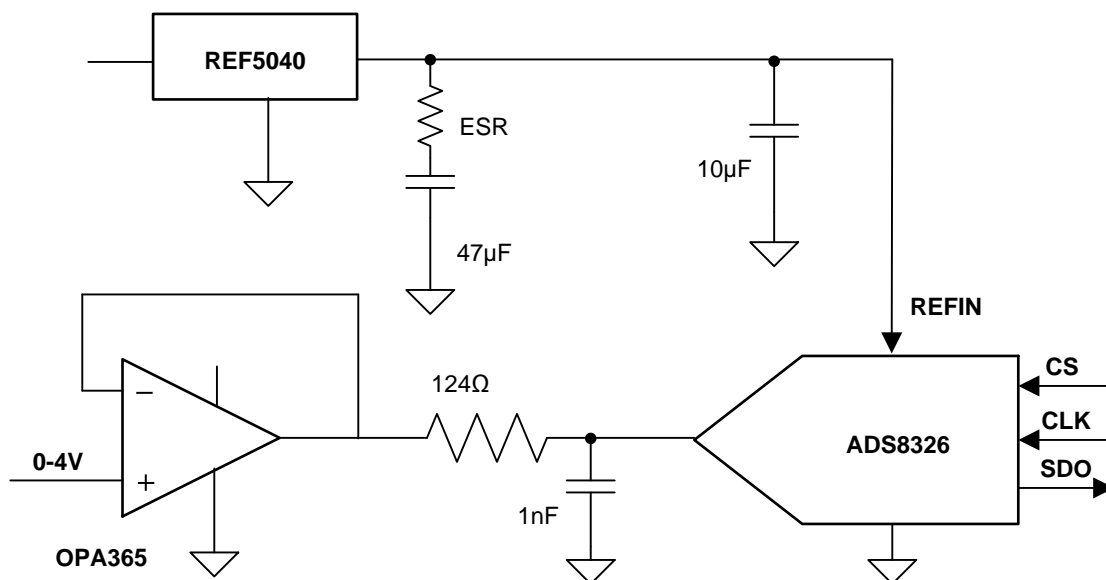


Figure 42. Complete Data Acquisition System Using REF50xx

##### 10.2.1.1 Design Requirements

When using the REF50xx in the design, select a proper output capacitor that does not create gain peaking, thereby increasing total system noise. At the same time, the capacitor must be selected to provide required filtering performance for the system. In addition, input bypass capacitor and noise reduction capacitors must be added for optimum performances. During the design of the data acquisition system, equal consideration must be given to the buffering analog input signal as well as the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement for good performance of the Data Acquisition System.

##### 10.2.1.2 Detailed Design Procedure

The OPA365 is used to drive the 16-bit Analog to Digital Converter (ADS8326). The RC filter at the output of the OPA365 is used to reduce the charge kick-back created by the opening and closing of the sampling switch inside the ADC. Design the RC filter such that the voltage at the sampling capacitor settles to 16-bit accuracy within the acquisition time of the ADC. The bandwidth of the driving amplifier must at least be 4 times the bandwidth of the RC filter.

## Typical Applications (continued)

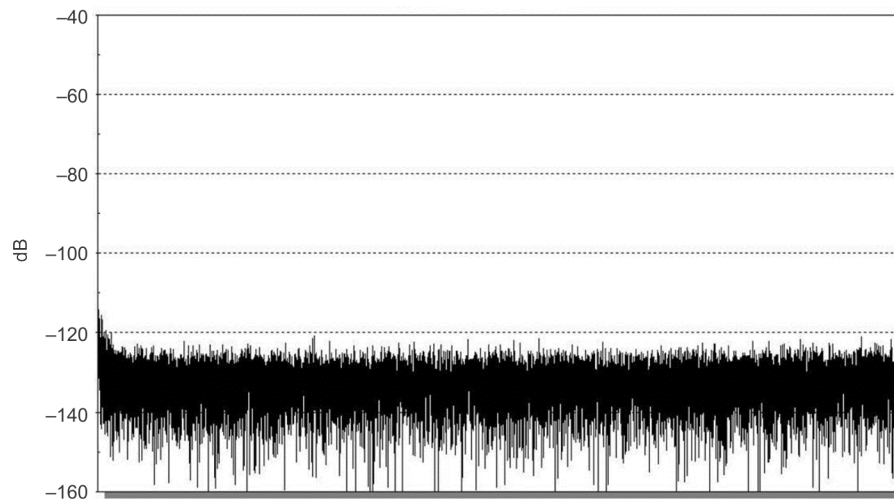
The REF5040 is used to drive the REF pin of the ADS8326. Proper selection of Voltage Reference output capacitor is very important for this design. Very Low equivalent series resistance (ESR) creates gain-peaking which degrades SNR of the total system. If the ESR of the capacitor is not enough, then an additional resistor must be added in series with the output capacitor. A capacitance of 1  $\mu\text{F}$  can be connected to the NR pin to reduce bandgap noise of the REF50xx.

SNR Measurements using different RC filters at the output of OPA365, different values of output capacitor for the REF50xx and different values of capacitors at the TRIM/NR pin are shown in [Table 1](#).

**Table 1. Data Acquisition Measurement Results for Different Conditions**

	TEST CONDITION 1	TEST CONDITION 2
OPA365 RC filter	124 $\Omega$ , 1 nF	124 $\Omega$ , 1 nF
REF5040 Output capacitor	10 $\mu\text{F}$	10 $\mu\text{F}$ + 47 $\mu\text{F}$
TRIM /NR pin capacitor	0 $\mu\text{F}$	1 $\mu\text{F}$
SNR	86.7 dB	92.8 dB

### 10.2.1.3 Application Curve



**Figure 43. FFT plot- Noise floor of Data Acquisition system**

## 11 Power Supply Recommendations

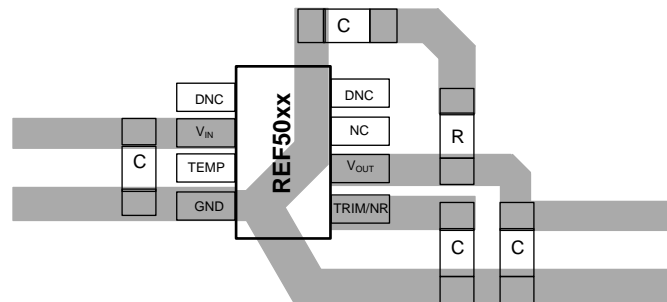
The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7 V, these references can be operated with a supply of 200 mV more than the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is provided in [Figure 6](#) in the *Typical Characteristics*. TI recommends a supply bypass capacitor ranging from 1  $\mu\text{F}$  to 50  $\mu\text{F}$ .

## 12 Layout

### 12.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 1  $\mu\text{F}$  to 10  $\mu\text{F}$ . If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Place a 1- $\mu\text{F}$  noise filtering capacitor between the NR pin and ground.
- The output must be decoupled with a 1- $\mu\text{F}$  to 50- $\mu\text{F}$  capacitor. A resistor in series with the output capacitor is optional. For better noise performance, the recommended ESR on the output capacitor is from 1  $\Omega$  to 1.5  $\Omega$ .
- A high-frequency, 1- $\mu\text{F}$  capacitor can be added in parallel between the output and ground to filter noise and help with switching loads as data converters.

### 12.2 Layout Example



**Figure 44. Layout Example**

### 12.3 Power Dissipation

The REF50xx family is specified to deliver current loads of  $\pm 10$  mA over the specified input voltage range. The temperature of the device increases according to [Equation 4](#):

$$T_J = T_A + P_D \times \theta_{JA}$$

where

- $T_J$  = Junction temperature ( $^{\circ}\text{C}$ )
  - $T_A$  = Ambient temperature ( $^{\circ}\text{C}$ )
  - $P_D$  = Power dissipated (W)
  - $\theta_{JA}$  = Junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )
- (4)

The REF50xx junction temperature must not exceed the absolute maximum rating of 150 $^{\circ}\text{C}$ .

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- *0.05uV/degC (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier*, [SBOS282](#).
- *REF5020 PSpice Model*, [SLIM160](#).
- *REF5020 TINA-TI Reference Design*, [SLIM159](#).
- *REF5020 TINA-TI Spice Model*, [SLIM158](#).
- *INA270 PSpice Model*, [SBOM485](#).
- *INA270 TINA-TI Reference Design*, [SBOC246](#).
- *INA270 TINA-TI Spice Model*, [SBOM306](#).

#### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REF5010	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5020	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5025	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5030	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5040	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5045	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
REF5050	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 13.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

#### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5010AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	<a href="#">Samples</a>
REF5010AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	<a href="#">Samples</a>
REF5010ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010	<a href="#">Samples</a>
REF5010IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5020AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5020IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5020IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5020IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5025AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5025IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5025IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5025IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5030AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5030IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5030IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5040AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>
REF5040AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>
REF5040AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5040AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>
REF5040ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5045AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	<a href="#">Samples</a>
REF5045IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5045IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	<a href="#">Samples</a>
REF5050AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF REF5020, REF5025, REF5040, REF5050 :**

- Enhanced Product: [REF5020-EP](#), [REF5025-EP](#), [REF5040-EP](#), [REF5050-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5030AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5010AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5010IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5020IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5030AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030AIDR	SOIC	D	8	2500	367.0	367.0	35.0



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5030IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

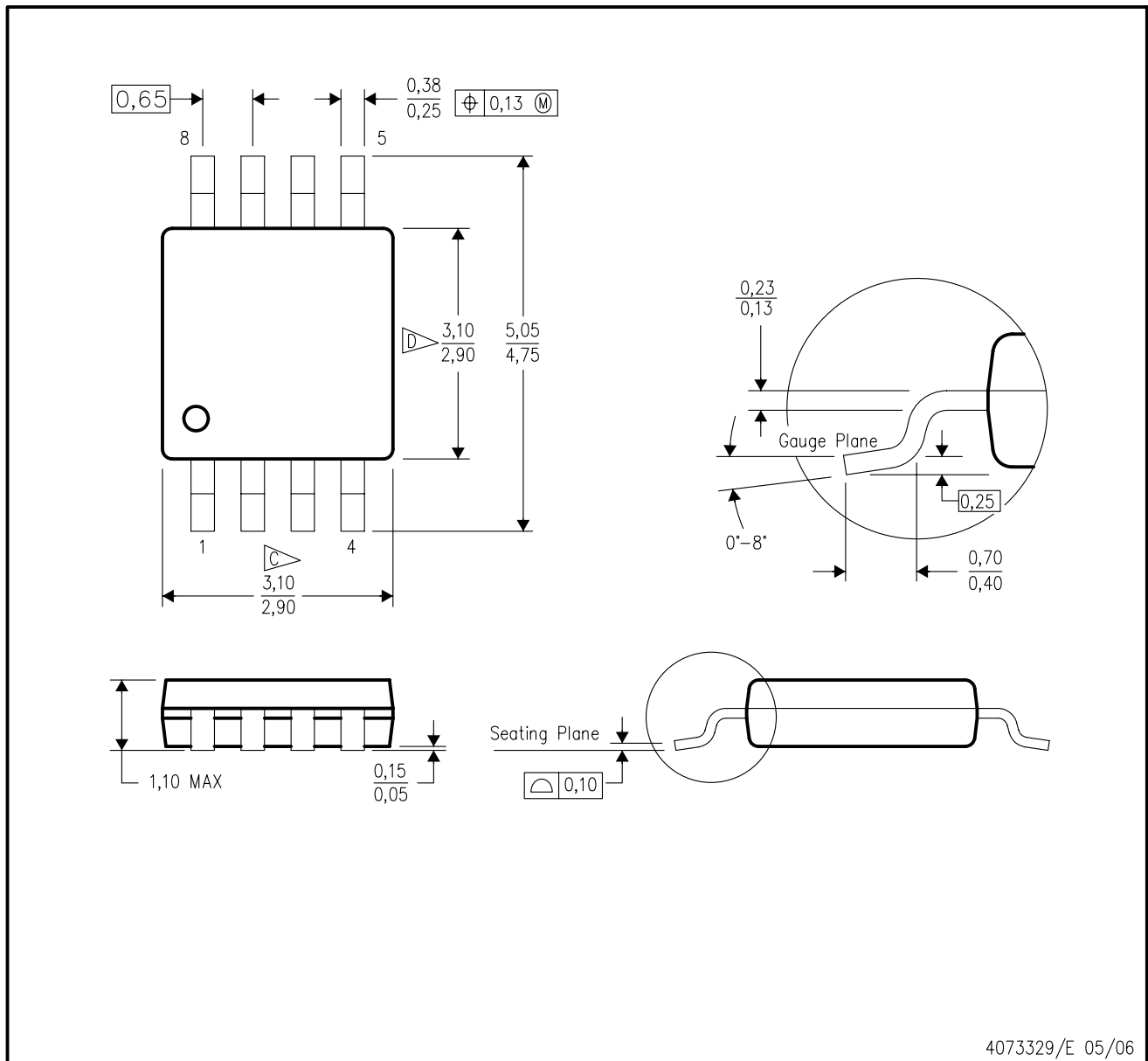
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)