

# SN54AC245, SN74AC245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS461F – FEBRUARY 1995 – REVISED OCTOBER 2003

- 2-V to 6-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 6 V
- Max  $t_{pd}$  of 7 ns at 5 V

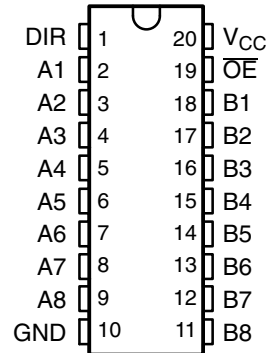
## description/ordering information

The 'AC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

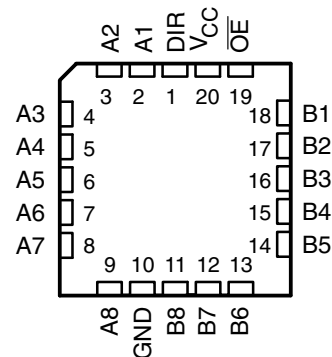
When the output-enable ( $\overline{OE}$ ) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction control (DIR) input. A high on  $\overline{OE}$  disables the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AC245 . . . J OR W PACKAGE  
SN74AC245 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AC245 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC245N	SN74AC245N
	SOIC – DW	Tube	SN74AC245DW	AC245
		Tape and reel	SN74AC245DWR	
	SOP – NS	Tape and reel	SN74AC245NSR	AC245
	SSOP – DB	Tape and reel	SN74AC245DBR	AC245
	TSSOP – PW	Tube	SN74AC245PW	AC245
		Tape and reel	SN74AC245PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54AC245J	SNJ54AC245J
	CFP – W	Tube	SNJ54AC245W	SNJ54AC245W
	LCCC – FK	Tube	SNJ54AC245FK	SNJ54AC245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

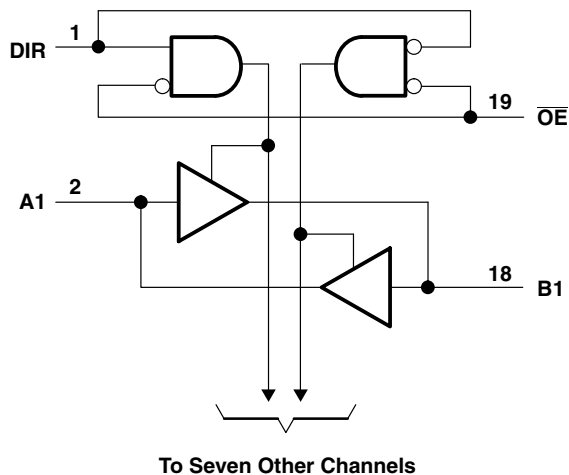
# SN54AC245, SN74AC245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

		SN54AC245		SN74AC245		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$		2.1		V
		$V_{CC} = 4.5\text{ V}$		3.15		
		$V_{CC} = 5.5\text{ V}$		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9		V
		$V_{CC} = 4.5\text{ V}$		1.35		
		$V_{CC} = 5.5\text{ V}$		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		-12		mA
		$V_{CC} = 4.5\text{ V}$		-24		
		$V_{CC} = 5.5\text{ V}$		-24		
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		12		mA
		$V_{CC} = 4.5\text{ V}$		24		
		$V_{CC} = 5.5\text{ V}$		24		
$\Delta t/\Delta v$	Input transition rise or fall rate	8		8		ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AC245, SN74AC245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC245		SN74AC245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
	I <sub>OH</sub> = -24 mA	5.5 V	4.86			4.7		4.76		
		I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V			3.85				
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V					3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		5.5 V		0.001	0.1		0.1	0.1		
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5	0.44		
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V				1.65			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V					1.65				
I <sub>I</sub>	A or B ports <sup>‡</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA
	$\overline{\text{OE}}$ or DIR					±0.1		±1	±1	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.5		±10	±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4.5				pF	
C <sub>io</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			15				pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54AC245		SN74AC245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1.5	5	8.5	1	11.5	1	9	ns
t <sub>PHL</sub>			1.5	5	8.5	1	10	1	9	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	2.5	7	11.5	1	13.5	2	12.5	ns
t <sub>PZL</sub>			2.5	7.5	12	1	14.5	2	13.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	2	6.5	12	1	13.5	1	12.5	ns
t <sub>PLZ</sub>			2	7	11.5	1	14	1.5	13	



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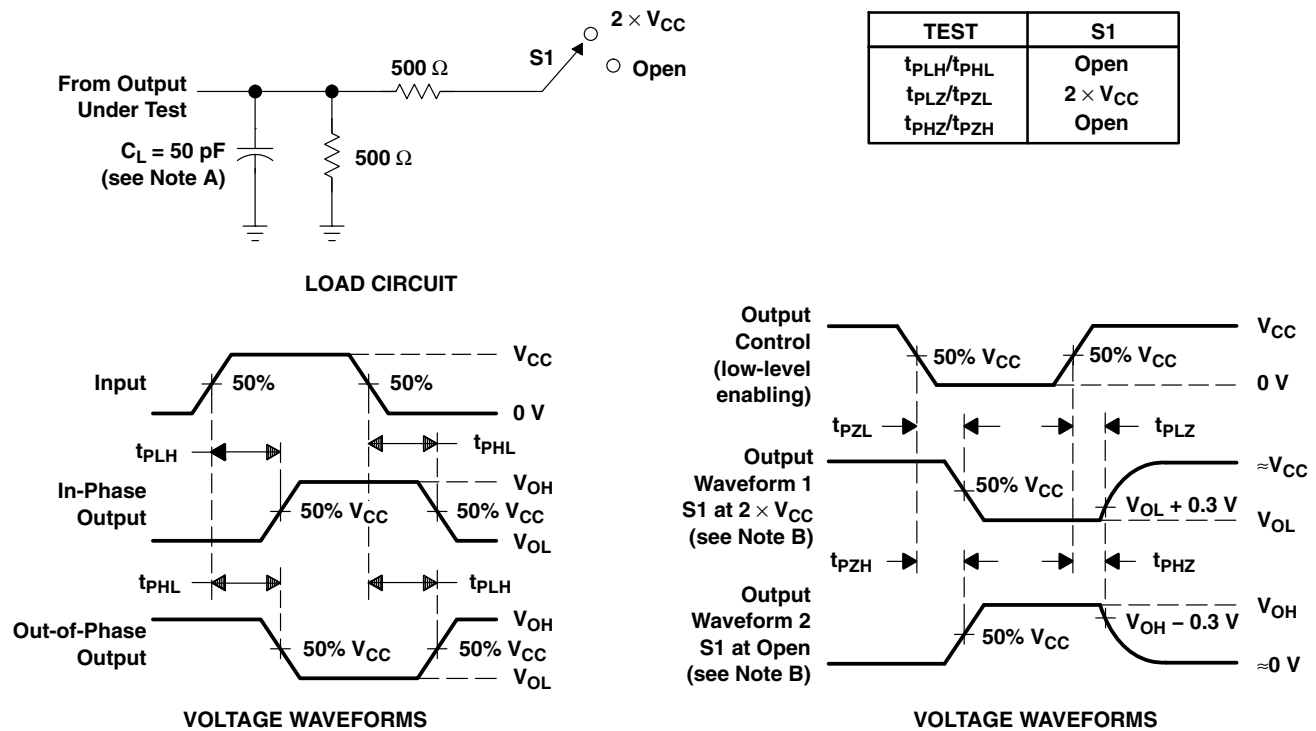
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC245		SN74AC245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.5	3.5	6.5	1	8.5	1	7	ns
$t_{PHL}$			1.5	3.5	6	1	7.5	1	7	
$t_{PZH}$	$\overline{\text{OE}}$	A or B	1.5	5	8.5	1	10	1	9	ns
$t_{PZL}$			1.5	5.5	9	1	10.5	1	9.5	
$t_{PHZ}$	$\overline{\text{OE}}$	A or B	1.5	5.5	9	1	10.5	1	10	ns
$t_{PLZ}$			1.5	5.5	9	1	10.5	1	10	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	45	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87758012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87758012A SNJ54AC 245FK	<a href="#">Samples</a>
5962-8775801RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775801RA SNJ54AC245J	<a href="#">Samples</a>
5962-8775801SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775801SA SNJ54AC245W	<a href="#">Samples</a>
5962-8775801VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775801VS A SNV54AC245W	<a href="#">Samples</a>
SN74AC245DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74AC245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC245N	<a href="#">Samples</a>
SN74AC245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC245N	<a href="#">Samples</a>
SN74AC245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC245PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74AC245PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SN74AC245PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC245	<a href="#">Samples</a>
SNJ54AC245FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87758012A SNJ54AC245FK	<a href="#">Samples</a>
SNJ54AC245J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775801RA SNJ54AC245J	<a href="#">Samples</a>
SNJ54AC245W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775801SA SNJ54AC245W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC245, SN54AC245-SP, SN74AC245 :**

- Catalog: [SN74AC245](#), [SN54AC245](#)
  
- Enhanced Product: [SN74AC245-EP](#), [SN74AC245-EP](#)
  
- Military: [SN54AC245](#)
  
- Space: [SN54AC245-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
  
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
  
- Military - QML certified for Military and Defense Applications
  
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC245NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74AC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC245DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AC245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC245PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

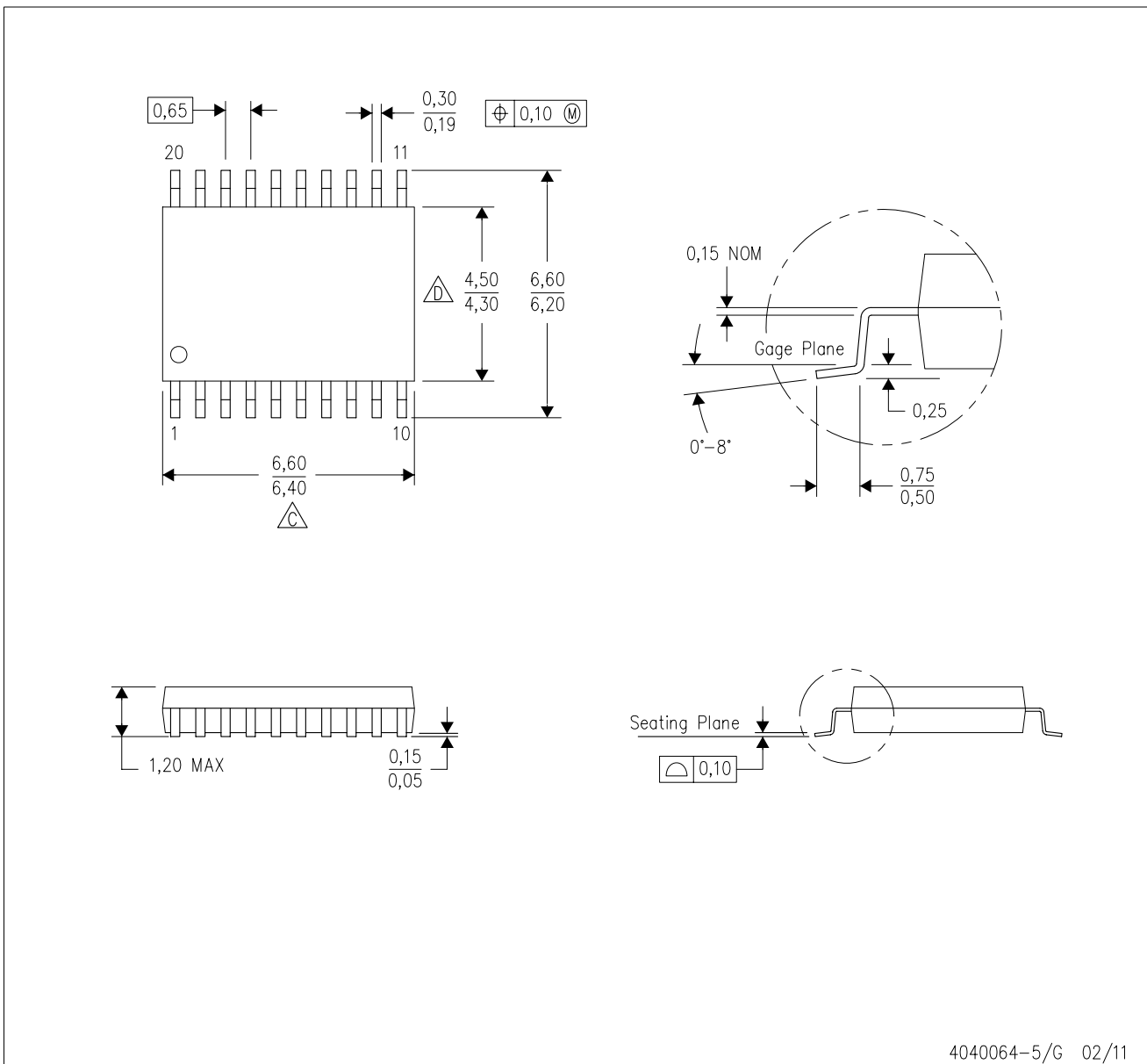


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\triangle$  C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - $\triangle$  D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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