Micropower, 150-mA Ultralow-Dropout CMOS Voltage Regulator With Power Good

Check for Samples: LP3988-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **SOT-23-5 Package**
- **Power-Good Flag Output**
- **Logic-Controlled Enable**
- **Stable With Ceramic and High Quality Tantalum Capacitors**
- **Fast Turnon**
- **Thermal Shutdown and Short-Circuit Current Limit**

APPLICATIONS

- **Automotive**
- **CDMA Cellular Handsets**
- **Wideband CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**
- **Tiny 3.3-V ± 5% to 2.85-V, 150-mA Converter**

DESCRIPTION

The LP3988-Q1 is a 150-mA low-dropout regulator designed specially to meet requirements of portable battery applications. The LP3988-Q1 works with a space-saving, 1-µF ceramic capacitor. The LP3988-Q1 features an error flag-output that indicates a faulty output condition.

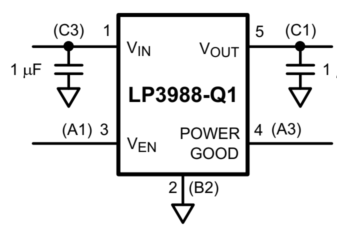
The LP3988-Q1 has performance optimized for battery-powered systems to deliver low noise, extremely low dropout voltage, and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power-supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. The device maintains high power-supply rejection down to lower input voltage levels common to battery-operated circuits.

The device is ideal for mobile phone and similar battery-powered wireless applications. It provides up to 150 mA, from a 2.5-V to 6-V input, consuming less than 1 µA in disable mode, and has fast turnon time less than 200 µs.

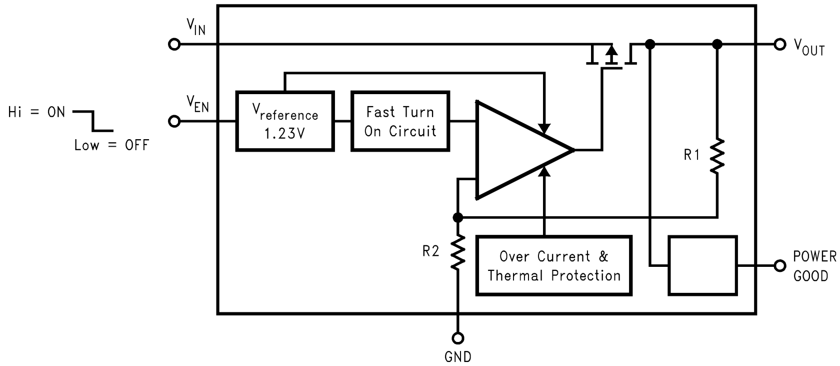
The LP3988-Q1 is available in a 5-pin SOT-23 package, has performance specified for the −40°C to 125°C temperature range, and is available in 2.85-V output voltages. **Note:** For other voltage options, please contact TI sales.

Typical Application Circuit

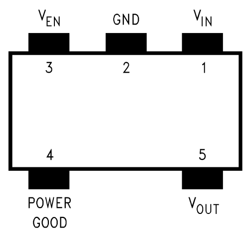


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Block Diagram



SOT-23-5 PACKAGE
TOP VIEW



Pin Descriptions

Name	SOT-23	Function
V_{EN}	3	Enable Input Logic, Enable High
GND	2	Common Ground
V_{OUT}	5	Output Voltage of the LDO
V_{IN}	1	Input Voltage of the LDO
Power Good	4	Power Good Flag (output): open-drain output, connected to an external pull-up resistor. Active low indicates an output voltage out of tolerance condition.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage		−0.3	6.5	V
Power good	V_{OUT}, V_{EN}	−0.3 V to (V_{IN} + 0.3 V)	6	V
Junction temperature			150	°C
Storage Temperature		−65	150	°C
Power dissipation (1)	SOT-23-5		364	mW
ESD rating (2)	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C4B		750	V

(1) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A) / \theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364-mW rating appearing under *Absolute Maximum Ratings* for the SOT-23-5 package results from substituting the absolute-maximum junction temperature, 150°C, for T_J, 70°C for T_A, and 175°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The absolute-maximum power dissipation can be increased by 4.5 mW for each degree below 70°C, and it must be derated by 4.5 mW for each degree above 70°C.

(2) The human-body model is 100 pF discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} (2)	2.5		6	V
V_{OUT}, V_{EN}	0		V_{IN}	V
Operating temperature	−40		125	°C

(1) All voltages are with respect to the potential at the GND pin.

(2) The minimum V_{IN} depends on the device output option. For $Vout_{(NOM)}$ < 2.5V, $V_{IN(MIN)}$ will equal 2.5V. For $Vout_{(NOM)} \geq$ 2.5V, $V_{IN(MIN)}$ will equal $Vout_{(NOM)}$ + 200mV.

Thermal Information

THERMAL METRIC(1)		SOT-23 Package	UNIT
		DBV-5	
θ_{JA}	Junction-to-ambient thermal resistance	175	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	78	°C/W
θ_{JB}	Junction-to-board thermal resistance	31.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface type** apply over the entire operating temperature range for operation, −40°C to 125°C. (1) (2)

Symbol	Parameter	Conditions	Limit Min	Limit Typ	Limit Max	Units
ΔV_{OUT}	Output voltage tolerance	−40°C ≤ T_A ≤ 125°C, SOT-23-5	−2 **−3.5**		2 **3.5**	% of $V_{OUT(nom)}$
	Line-regulation error	V_{IN} = $V_{OUT\ (NOM)}$ + 0.5 V to 6 V	−0.15 **−0.2**		0.15 **0.2**	%/V
	Load-regulation error (3)	I_{OUT} = 1 mA to 150 mA			0.005 **0.007**	%/mA
PSRR	Power-supply rejection ratio	V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 1 kHz, I_{OUT} = 50 mA (Figure 3)		65		dB
		V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 10 kHz, I_{OUT} = 50 mA (Figure 3)		45		
I_Q	Quiescent current	V_{EN} = 1.4 V, I_{OUT} = 0 mA		85	120	µA
		V_{EN} = 1.4 V, I_{OUT} = 0 to 150 mA		140	**200**	
		V_{EN} = 0.4V		0.003	**1.0**	
	Dropout Voltage (4)	I_{OUT} = 1 mA		1	**5**	mV
		I_{OUT} = 150 mA		80	115 **150**	
I_{SC}	Short Circuit Current Limit	See (5)		600		mA
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1 µF		220		µVrms
C_{OUT}	Output Capacitor	Capacitance (6)	**1**		**20**	µF
		ESR (6)	**5**		**500**	mΩ
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		°C
Enable Control Characteristics (7)						
I_{EN}	Maximum Input Current at EN	V_{EN} = 0 and V_{IN} = 6 V			**0.1**	µA
V_{IL}	Logic Low Input threshold	V_{IN} = 2.5 V to 6 V			**0.5**	V
V_{IH}	Logic High Input threshold	V_{IN} = 2.5 V to 6 V	**1.2**			V
Power Good						
V_{THL} V_{THH}	Power Good Low threshold High Threshold	% of V_{OUT} (PG ON) Figure 2 % of V_{OUT} (PG OFF) Figure 2 (8)	90 92	93 95	95 98	%
V_{OL}	PG Output Logic Low Voltage	$I_{PULL\text{-}UP}$ = 100 µA, fault condition		0.02	**0.1**	V
I_{PGL}	PG Output Leakage Current	PG off, V_{PG} = 6 V		0.02		µA
t_{ON}	Power Good Turn On time, (4)	V_{IN} = 4.2V		10		µs
t_{OFF}	Power Good Turn Off time, (4)	V_{IN} = 4.2V		10		µs

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_A = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.
(5) Short-circuit current is measured on input supply line after pulling down V_{OUT} to 95% $V_{OUT(nom)}$.
(6) Specified by design. The capacitor tolerance should be ±30% or better over the full temperature range. The full range of operating conditions such as temperature, dc bias and even capacitor case size for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range.
(7) Turnon time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.
(8) The low and high thresholds are generated together. Typically a 2.6% difference is seen between these thresholds.

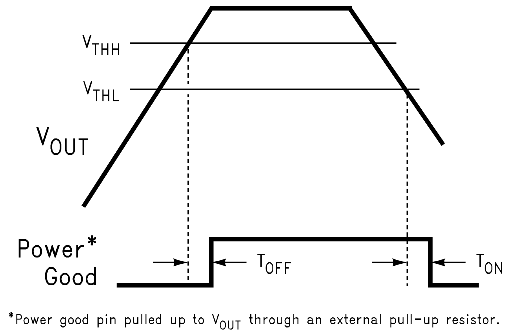


Figure 1. Power Good Flag Timing

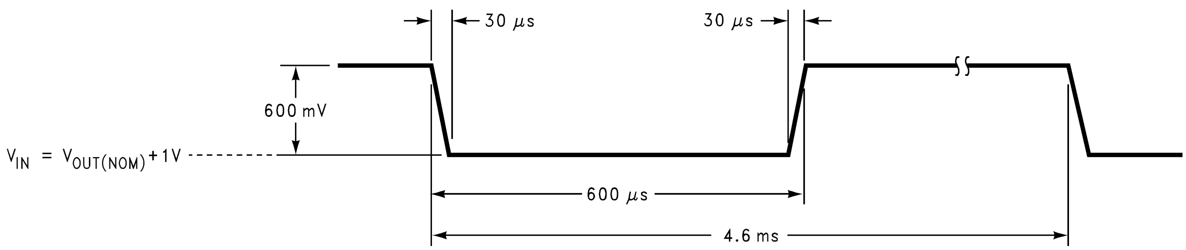


Figure 2. Line Transient Response Input Perturbation

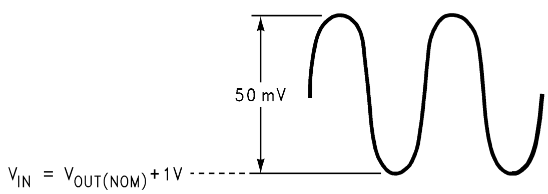


Figure 3. PSRR Input Perturbation

Typical Performance Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF ceramic, V_{IN} = V_{OUT} + 0.2 V, T_A = 25°C, enable pin is tied to V_{IN}.

RIPPLE REJECTION RATIO (LP3988-Q1-2.85)

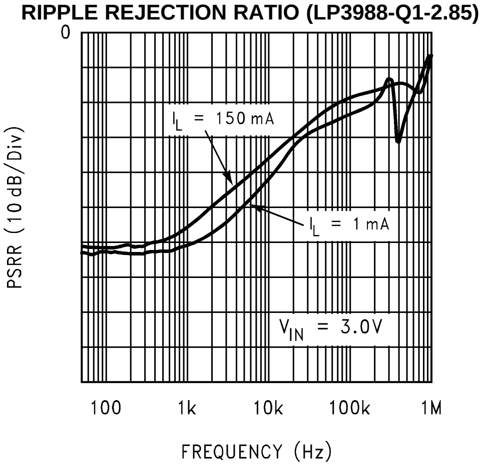


Figure 4.

RIPPLE REJECTION RATIO (LM3988-2.85)

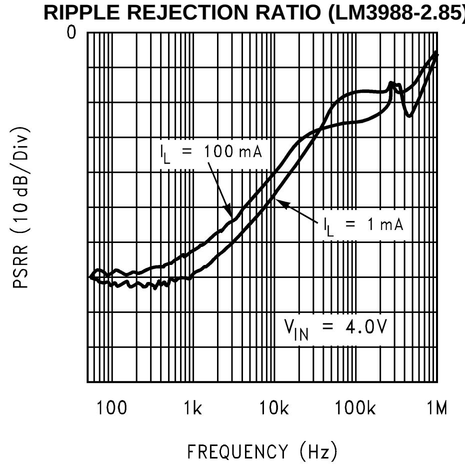


Figure 5.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{OUT} through a 100-kΩ resistor)

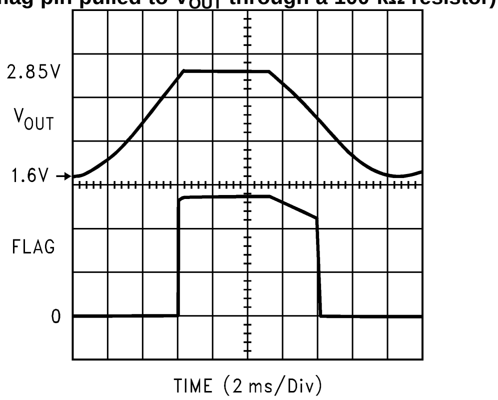


Figure 6.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{IN} through a 100-kΩ resistor)

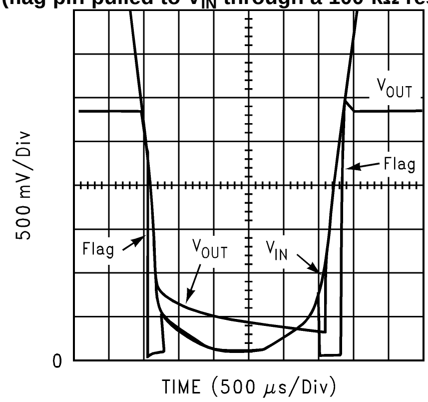


Figure 7.

POWER-GOOD RESPONSE TIME (LP3988-Q1-2.85) (flag pin pulled to V_{OUT} through a 100-kΩ resistor)

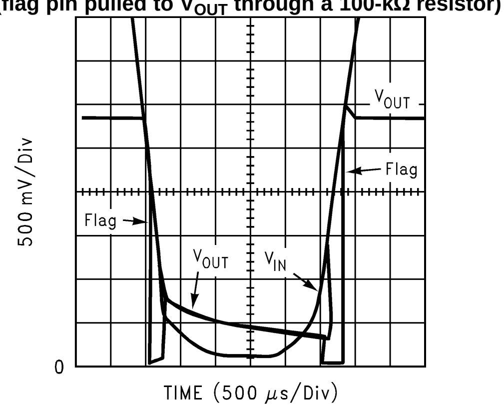


Figure 8.

LINE TRANSIENT RESPONSE (LP3988-Q1-2.85)

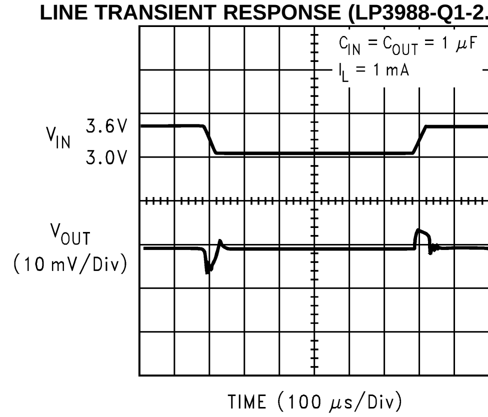


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF ceramic, V_{IN} = V_{OUT} + 0.2 V, T_A = 25°C, enable pin is tied to V_{IN}.

LINE TRANSIENT RESPONSE (LP3988-Q1-2.85)

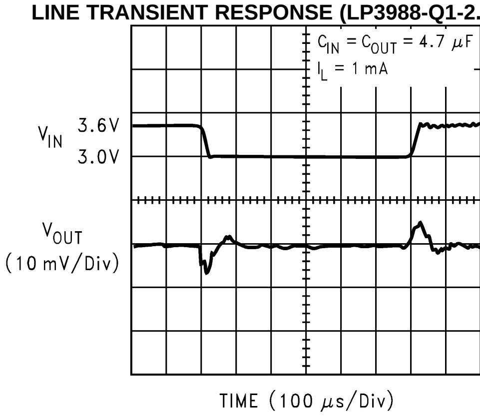


Figure 10.

POWER-UP RESPONSE

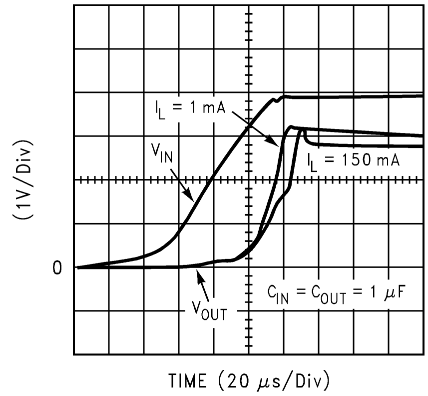


Figure 11.

ENABLE RESPONSE

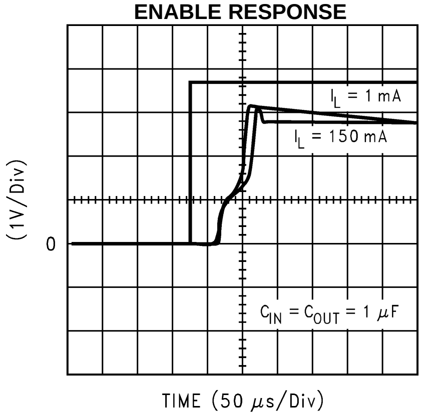


Figure 12.

ENABLE RESPONSE

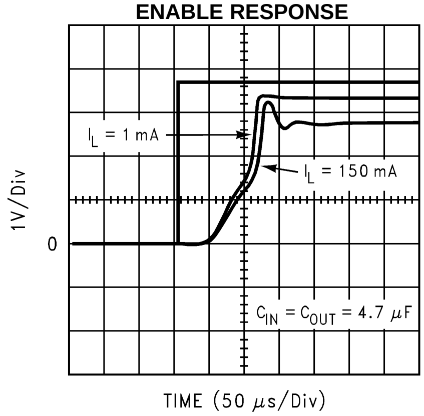


Figure 13.

LOAD-TRANSIENT RESPONSE

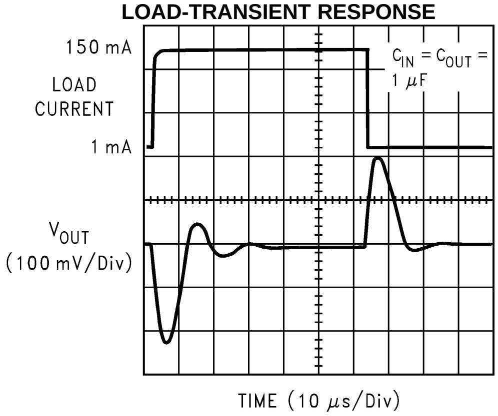


Figure 14.

LOAD-TRANSIENT RESPONSE

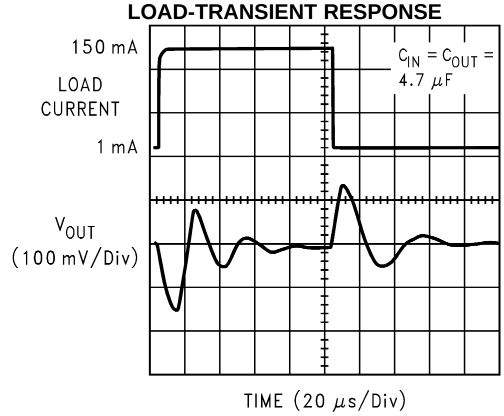


Figure 15.

APPLICATION INFORMATION

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3988-Q1 requires external capacitors for regulator stability. The LP3988-Q1 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3988-Q1 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge-current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is ≅ 1 µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3988-Q1 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 1-µF to 22-µF range with a 5-mΩ to 500-mΩ ESR range is suitable in the LP3988-Q1 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see the *CAPACITOR CHARACTERISTICS* section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an Equivalent Series Resistance (ESR) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3988-Q1 remains stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3988-Q1 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3988-Q1.

The ceramic capacitor's capacitance can vary with temperature. Most large-value ceramic capacitors (≅ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent-size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

ON/OFF INPUT OPERATION

The LP3988-Q1 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turnon/turnoff voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3988-Q1 utilizes a speed-up circuit to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turnon time.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3988QMFX-2P85	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	RABQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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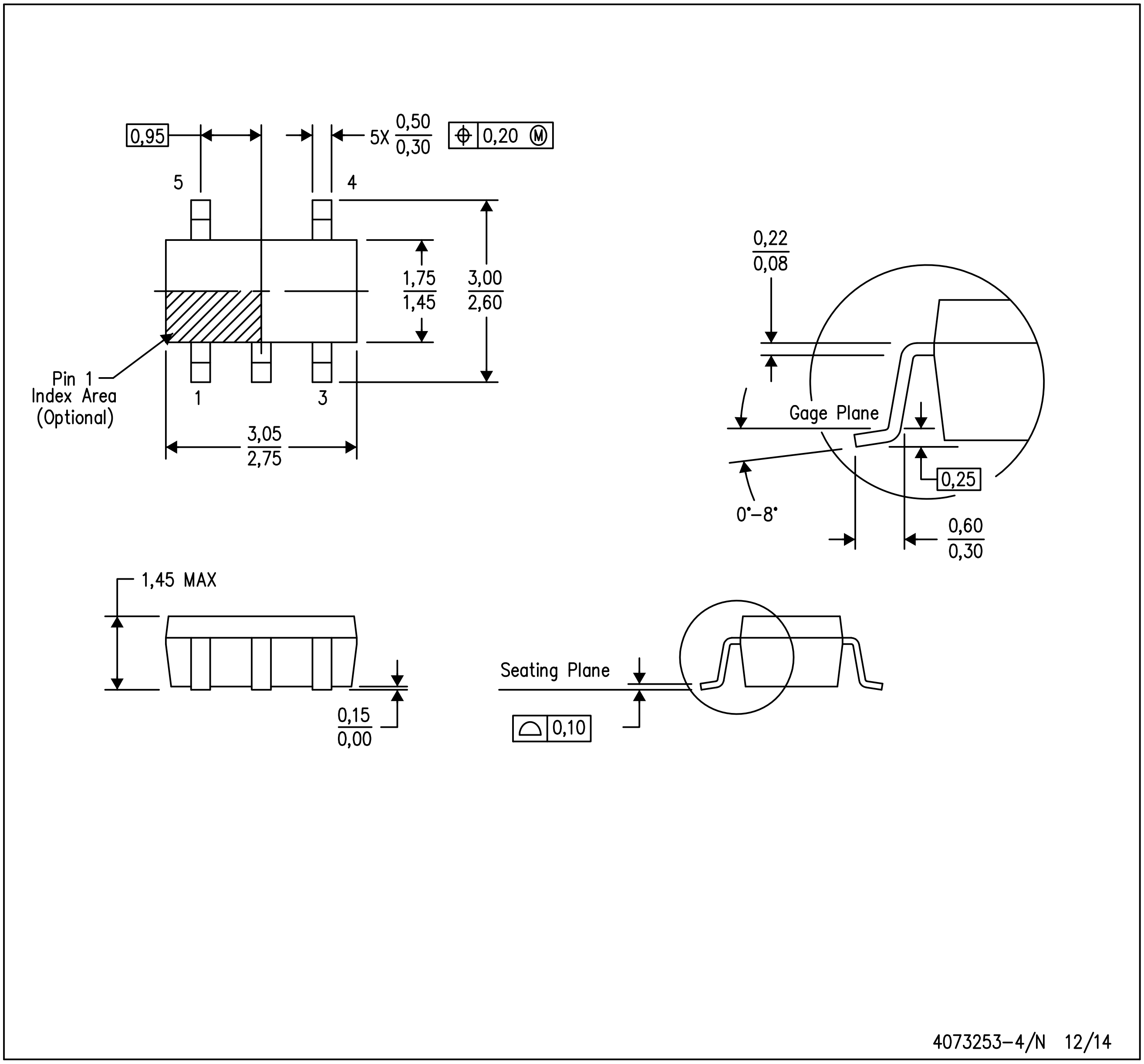
OTHER QUALIFIED VERSIONS OF LP3988-Q1 :

- Catalog: LP3988

NOTE: Qualified Version Definitions:

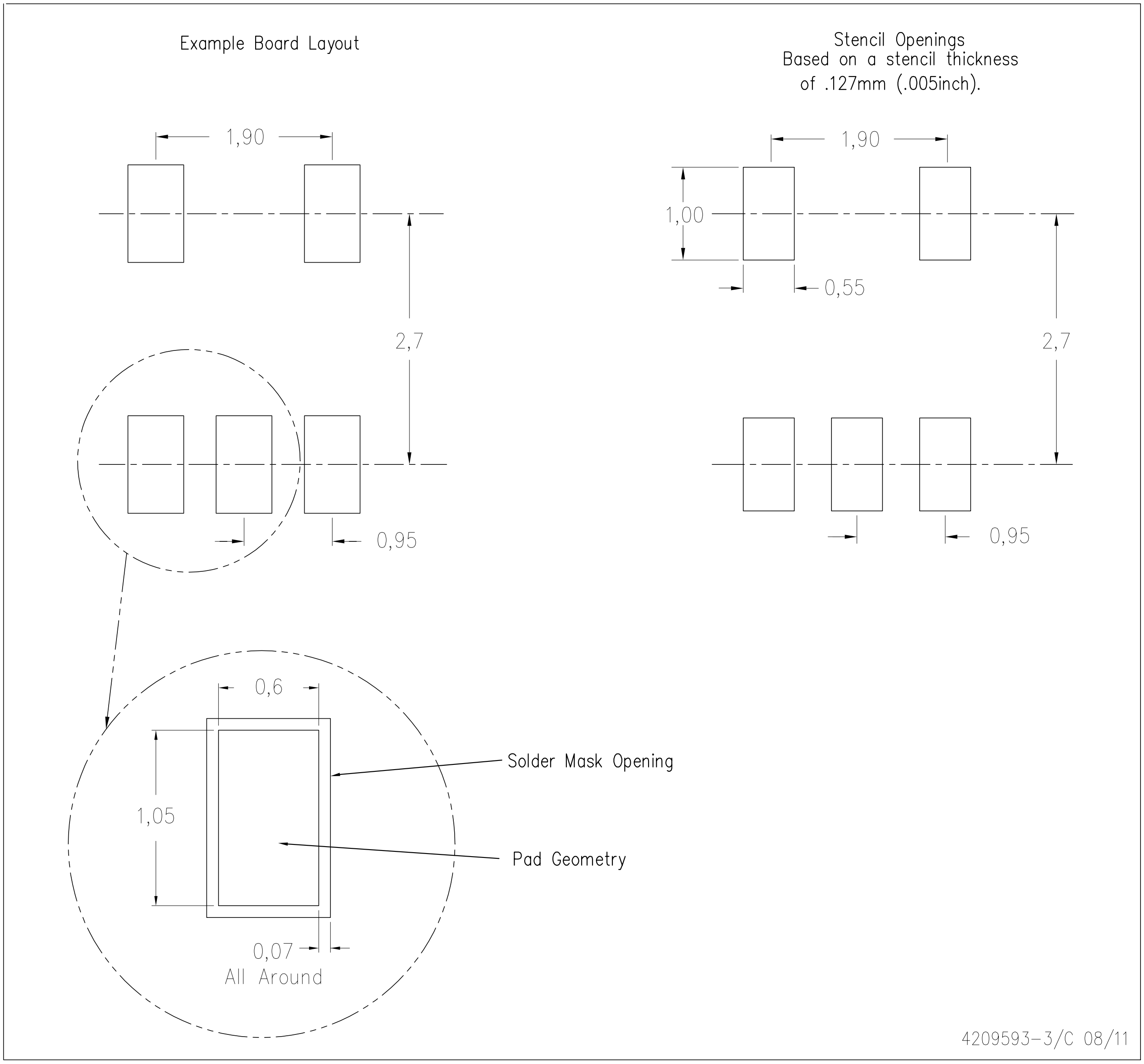
- Catalog - TI's standard catalog product

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.