SN74AUP1G125 Low-Power Single Bus Buffer Gate With 3-State Output

1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption (I_{CC} = 0.9 µA Maximum)
- Low Dynamic-Power Consumption (C_{pd} = 4 pF Typical at 3.3 V)
- Low Input Capacitance (C_I = 1.5 pF Typical)
- Low Noise – Overshoot and Undershoot < 10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.6 ns Maximum at 3.3 V

2 Applications

- Audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards, and Mice

3 Description

This bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. This device has the input-disable feature, which allows floating input signals.

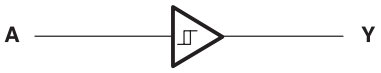
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G125	SOT-23 (5)	2.90 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.30 mm
	SOT (5)	1.65 mm x 1.20 mm
	SON (6)	1.45 mm x 1.00 mm
		1.00 mm x 1.00 mm
	DSBGA (5)	0.76 mm x 1.16 mm
		0.89 mm x 1.39 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (February 2013) to Revision M — **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision K (November 2012) to Revision L — **Page**

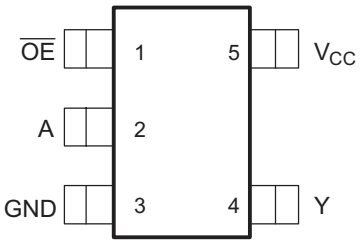
- Changed $\overline{Y}$ to Y for pin 4 in DSF Package pin out ... 3

5 Device Comparison Table

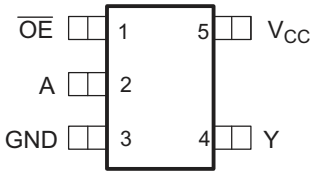
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G125DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74AUP1G125DCK	SC70 (5)	2.00 mm x 1.30 mm
SN74AUP1G125DRL	SOT (5)	1.65 mm x 1.20 mm
SN74AUP1G125DRY	SON (6)	1.45 mm x 1.00 mm
SN74AUP1G125DSF	SON (6)	1.00 mm x 1.00 mm
SN74AUP1G125YFP	DSBGA (5)	0.76 mm x 1.16 mm
SN74AUP1G125YZP	DSBGA (5)	0.89 mm x 1.39 mm

6 Pin Configuration and Functions

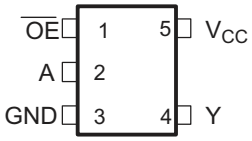
DBV Package
5-Pin SOT-23
Top View



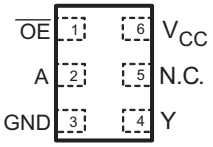
DCK Package
5-Pin SC70
Top View



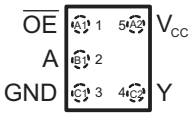
DRL Package
5-Pin SOT
Top View



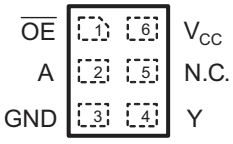
DSF Package
6-Pin SON
Top View



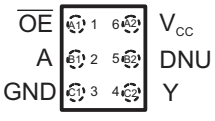
YZP or YZT Package
5-Pin DSBGA
Top View



DRY Package
6-Pin SON
Top View



YFP Package
5-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70, SOT, DSBGA	SON, DSBGA		
A	2	2	I	Input
GND	3	3	—	Ground
N.C.	—	5	—	No connection
$\overline{OE}$	1	1	I	Output Enable
V_{CC}	5	6	—	Power terminal
Y	4	4	O	Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)		–0.5	4.6	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}	3.6	V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}	3.6	
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	
		V_{CC} = 3 V to 3.6 V	2	3.6	
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V	0	0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V	0	0.7	
		V_{CC} = 3 V to 3.6 V	0	0.9	
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow of Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		SN74AUP1G125							UNIT
		DCK (SC70)	DBV (SOT-23)	DRL (SOT)	DRY (SON)	DSF (SON)	YFP (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225	206	142	234	300	132	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			
		I_{OH} = –1.7 mA	1.4 V	1.11			
		I_{OH} = –1.9 mA	1.65 V	1.32			
		I_{OH} = –2.3 mA	2.3 V	2.05			
		I_{OH} = –3.1 mA		1.9			
		I_{OH} = –2.7 mA	3 V	2.72			
		I_{OH} = –4 mA		2.6			
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31	
		I_{OL} = 1.9 mA	1.65 V			0.31	
		I_{OL} = 2.3 mA	2.3 V			0.31	
		I_{OL} = 3.1 mA				0.44	
		I_{OL} = 2.7 mA	3 V			0.31	
		I_{OL} = 4 mA				0.44	
I_I	A or $\overline{OE}$ input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			0.1	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), $\overline{OE}$ = GND, I_O = 0	0.8 V to 3.6 V			0.5	µA
ΔI_{CC}	A input	V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			40	µA
	$\overline{OE}$ input					110	
	All inputs	V_I = GND to 3.6 V, $\overline{OE}$ = V_{CC} (2)	0.8 V to 3.6 V			0	
C_I		V_I = V_{CC} or GND	0 V		1.5		pF
			3.6 V		1.5		
C_o		V_O = V_{CC} or GND	3.6 V		3		pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled

7.6 Electrical Characteristics, T_A = –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V
		I_{OH} = –1.1 mA	1.1 V	0.7 × V_{CC}			
		I_{OH} = –1.7 mA	1.4 V	1.03			
		I_{OH} = –1.9 mA	1.65 V	1.3			
		I_{OH} = –2.3 mA	2.3 V	1.97			
		I_{OH} = –3.1 mA		1.85			
		I_{OH} = –2.7 mA	3 V	2.67			
		I_{OH} = –4 mA		2.55			
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.37	
		I_{OL} = 1.9 mA	1.65 V			0.35	
		I_{OL} = 2.3 mA	2.3 V			0.33	
		I_{OL} = 3.1 mA				0.45	
		I_{OL} = 2.7 mA	3 V			0.33	
		I_{OL} = 4 mA				0.45	
I_I	A or $\overline{OE}$ input	V_I = GND to 3.6 V	0 V to 3.6 V			0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.6	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			0.5	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), $\overline{OE}$ = GND, I_O = 0	0.8 V to 3.6 V			0.9	µA
ΔI_{CC}	A input	V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			50	µA
	$\overline{OE}$ input					120	
	All inputs	V_I = GND to 3.6 V, $\overline{OE}$ = V_{CC} (2)	0.8 V to 3.6 V			0	

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled

7.7 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	0.8 V	T_A = 25°C		18.1		ns
			1.2 V ± 0.1 V	T_A = 25°C	4.3	7.4	12.6	
				T_A = –40°C to 85°C	2.7		15.3	
			1.5 V ± 0.1 V	T_A = 25°C	3.3	5.2	8.5	
				T_A = –40°C to 85°C	1		10.2	
			1.8 V ± 0.15 V	T_A = 25°C	2.6	4.1	6.8	
				T_A = –40°C to 85°C	1.3		8.3	
			2.5 V ± 0.2 V	T_A = 25°C	2	2.9	4.7	
				T_A = –40°C to 85°C	1.1		5.8	
			3.3 V ± 0.3 V	T_A = 25°C	1.7	2.4	3.8	
				T_A = –40°C to 85°C	1		4.6	
t_{en}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		19.1		ns
			1.2 V ± 0.1 V	T_A = 25°C	5.1	9.3	15.9	
				T_A = –40°C to 85°C	3.6		19.2	
			1.5 V ± 0.1 V	T_A = 25°C	4.1	6.6	10.5	
				T_A = –40°C to 85°C	2.5		12.7	
			1.8 V ± 0.15 V	T_A = 25°C	3.2	5.3	8.7	
				T_A = –40°C to 85°C	2.1		10.3	
			2.5 V ± 0.2 V	T_A = 25°C	2.5	3.8	6	
				T_A = –40°C to 85°C	1.6		7.2	
			3.3 V ± 0.3 V	T_A = 25°C	2.1	3.2	4.9	
				T_A = –40°C to 85°C	1.4		5.9	
t_{dis}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		12.1		ns
			1.2 V ± 0.1 V	T_A = 25°C	2.4	4.1	6.9	
				T_A = –40°C to 85°C	2.2		7.7	
			1.5 V ± 0.1 V	T_A = 25°C	1.8	2.9	4.5	
				T_A = –40°C to 85°C	1.7		5.1	
			1.8 V ± 0.15 V	T_A = 25°C	1	2.9	4.3	
				T_A = –40°C to 85°C	1.5		4.7	
			2.5 V ± 0.2 V	T_A = 25°C	1	1.8	2.7	
				T_A = –40°C to 85°C	1		3.3	
			3.3 V ± 0.3 V	T_A = 25°C	1.2	2.2	3.2	
				T_A = –40°C to 85°C	1.1		4	

7.8 Switching Characteristics, C_L = 10 pF

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	0.8 V	T_A = 25°C		20.5		ns
			1.2 V ± 0.1 V	T_A = 25°C	4.6	8.4	13.7	
				T_A = –40°C to 85°C	3.6		16.6	
			1.5 V ± 0.1 V	T_A = 25°C	3.5	5.9	9.3	
				T_A = –40°C to 85°C	2.4		11.1	
			1.8 V ± 0.15 V	T_A = 25°C	3.9	4.7	7.5	
				T_A = –40°C to 85°C	1.3		9.1	
			2.5 V ± 0.2 V	T_A = 25°C	2.3	3.4	5.3	
				T_A = –40°C to 85°C	1.6		6.4	
			3.3 V ± 0.3 V	T_A = 25°C	2.1	2.8	4.3	
				T_A = –40°C to 85°C	1.4		5.2	
t_{en}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		21.8		ns
			1.2 V ± 0.1 V	T_A = 25°C	4.9	10.2	16.8	
				T_A = –40°C to 85°C	4.4		20.2	
			1.5 V ± 0.1 V	T_A = 25°C	3.9	7.3	11.2	
				T_A = –40°C to 85°C	3.3		13.5	
			1.8 V ± 0.15 V	T_A = 25°C	3.4	5.8	9.2	
				T_A = –40°C to 85°C	2.7		11	
			2.5 V ± 0.2 V	T_A = 25°C	2.5	4.3	6.4	
				T_A = –40°C to 85°C	2.1		7.8	
			3.3 V ± 0.3 V	T_A = 25°C	2.1	3.7	5.4	
				T_A = –40°C to 85°C	1.9		6.4	
t_{dis}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		13		ns
			1.2 V ± 0.1 V	T_A = 25°C	3.8	6.6	11.7	
				T_A = –40°C to 85°C	1.2		14	
			1.5 V ± 0.1 V	T_A = 25°C	2.2	4.7	7.9	
				T_A = –40°C to 85°C	1.3		9.3	
			1.8 V ± 0.15 V	T_A = 25°C	2.4	4.4	6.4	
				T_A = –40°C to 85°C	2.2		7.5	
			2.5 V ± 0.2 V	T_A = 25°C	1.3	3.1	4.9	
				T_A = –40°C to 85°C	1.2		5.4	
			3.3 V ± 0.3 V	T_A = 25°C	1.9	3.4	5	
				T_A = –40°C to 85°C	1.9		5.6	

7.9 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	0.8 V	T_A = 25°C		22.5		ns
			1.2 V ± 0.1 V	T_A = 25°C	5.8	9.3	15.1	
				T_A = –40°C to 85°C	4.3		17.9	
			1.5 V ± 0.1 V	T_A = 25°C	4.4	6.6	10.2	
				T_A = –40°C to 85°C	3		12.1	
			1.8 V ± 0.15 V	T_A = 25°C	3.5	5.3	8.3	
				T_A = –40°C to 85°C	2.3		9.9	
			2.5 V ± 0.2 V	T_A = 25°C	2.7	3.9	5.8	
				T_A = –40°C to 85°C	1.9		7	
			3.3 V ± 0.3 V	T_A = 25°C	2.4	3.2	4.7	
				T_A = –40°C to 85°C	1.8		5.7	
t_{en}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		25.2		ns
			1.2 V ± 0.1 V	T_A = 25°C	7	11.3	18.1	
				T_A = –40°C to 85°C	5.4		21.4	
			1.5 V ± 0.1 V	T_A = 25°C	5.5	8.1	12.2	
				T_A = –40°C to 85°C	4.1		14.5	
			1.8 V ± 0.15 V	T_A = 25°C	4.3	6.5	10.1	
				T_A = –40°C to 85°C	3.3		12	
			2.5 V ± 0.2 V	T_A = 25°C	3.4	4.8	7.1	
				T_A = –40°C to 85°C	2.6		8.4	
			3.3 V ± 0.3 V	T_A = 25°C	2.9	4.1	5.9	
				T_A = –40°C to 85°C	2.3		6.9	
t_{dis}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		14		ns
			1.2 V ± 0.1 V	T_A = 25°C	3.7	5.8	8.2	
				T_A = –40°C to 85°C	3.3		11	
			1.5 V ± 0.1 V	T_A = 25°C	5.5	3.9	5.9	
				T_A = –40°C to 85°C	2.1		8	
			1.8 V ± 0.15 V	T_A = 25°C	3.3	4.5	6.6	
				T_A = –40°C to 85°C	2.9		7.4	
			2.5 V ± 0.2 V	T_A = 25°C	2.3	3.2	4.3	
				T_A = –40°C to 85°C	1.8		5.1	
			3.3 V ± 0.3 V	T_A = 25°C	2.4	4.8	6.2	
				T_A = –40°C to 85°C	3.1		6.7	

7.10 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	0.8 V	T_A = 25°C		29		ns
			1.2 V ± 0.1 V	T_A = 25°C	7.4	12	18.7	
				T_A = –40°C to 85°C	6.6		21.4	
			1.5 V ± 0.1 V	T_A = 25°C	5.7	8.6	12.5	
				T_A = –40°C to 85°C	4.9		14.7	
			1.8 V ± 0.15 V	T_A = 25°C	4.8	6.9	10.1	
				T_A = –40°C to 85°C	3.1		12	
			2.5 V ± 0.2 V	T_A = 25°C	3.9	5.1	7.2	
				T_A = –40°C to 85°C	3.3		8.7	
			3.3 V ± 0.3 V	T_A = 25°C	3.5	4.8	6	
				T_A = –40°C to 85°C	3		7	
t_{en}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		33.4		ns
			1.2 V ± 0.1 V	T_A = 25°C	8.8	14.1	21.8	
				T_A = –40°C to 85°C	7.4		25.5	
			1.5 V ± 0.1 V	T_A = 25°C	6.9	10.1	14.6	
				T_A = –40°C to 85°C	5.6		17.4	
			1.8 V ± 0.15 V	T_A = 25°C	5.6	8.1	12	
				T_A = –40°C to 85°C	4.7		14.1	
			2.5 V ± 0.2 V	T_A = 25°C	4.3	6.1	8.5	
				T_A = –40°C to 85°C	3.8		10	
			3.3 V ± 0.3 V	T_A = 25°C	3.7	5.2	7.1	
				T_A = –40°C to 85°C	3.4		8.3	
t_{dis}	$\overline{OE}$	Y	0.8 V	T_A = 25°C		17.7		ns
			1.2 V ± 0.1 V	T_A = 25°C	5.8	10	16	
				T_A = –40°C to 85°C	3.7		16	
			1.5 V ± 0.1 V	T_A = 25°C	5.7	7.7	10.9	
				T_A = –40°C to 85°C	1		10.7	
			1.8 V ± 0.15 V	T_A = 25°C	4.5	7.7	9.8	
				T_A = –40°C to 85°C	4.4		12.5	
			2.5 V ± 0.2 V	T_A = 25°C	3.9	5.6	7.4	
				T_A = –40°C to 85°C	3.2		9	
			3.3 V ± 0.3 V	T_A = 25°C	3.3	8.4	10.7	
				T_A = –40°C to 85°C	6.6		10.8	

7.11 Operating Characteristics

T_A = 25°c

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	3.8	pF
				1.2 V ± 0.1 V	3.8	
				1.5 V ± 0.1 V	3.7	
				1.8 V ± 0.15 V	3.8	
				2.5 V ± 0.2 V	3.9	
				3.3 V ± 0.3 V	4	
		Outputs disabled	f = 10 MHz	0.8 V	0	
				1.2 V ± 0.1 V	0	
				1.5 V ± 0.1 V	0	
				1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

7.12 Typical Characteristics

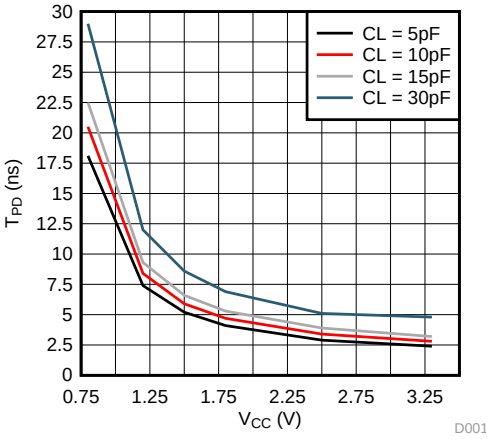
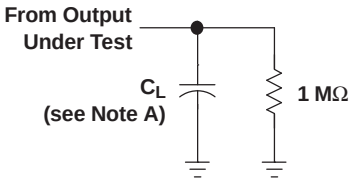


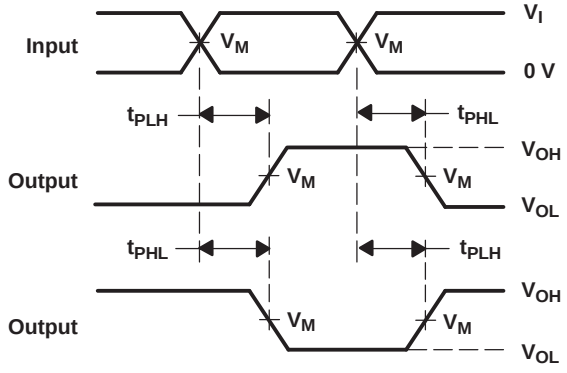
Figure 1. Propagation Delay vs. Supply Voltage and Load Capacitance

8 Parameter Measurement Information

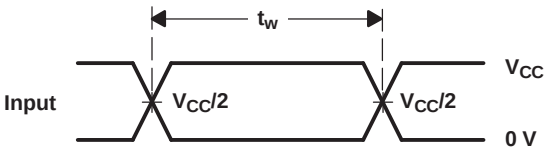


LOAD CIRCUIT

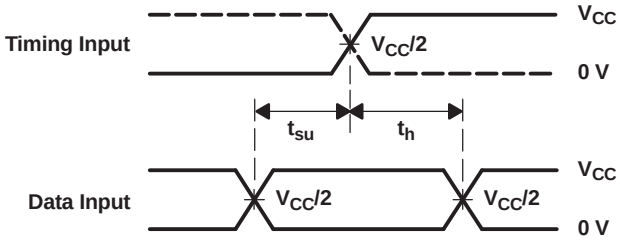
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

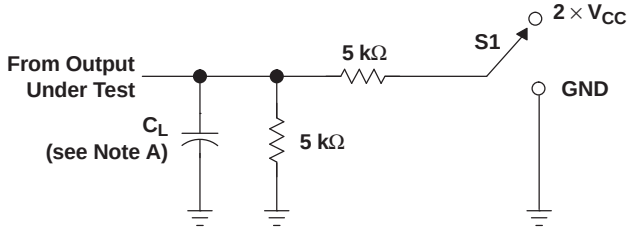


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

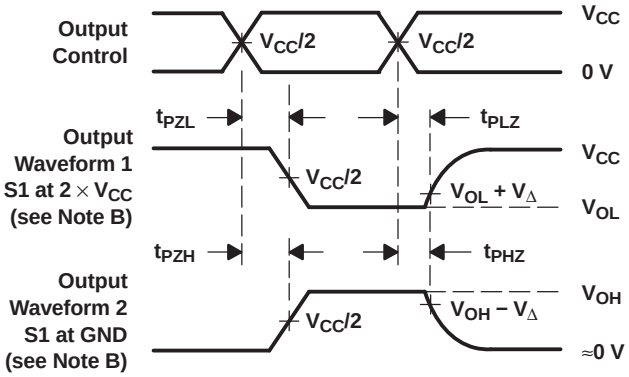
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms (Enable and Disable Times)

9 Detailed Description

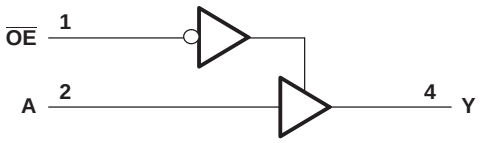
9.1 Overview

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 2 and Figure 3).

The SN74AUP1G125 device contains one buffer gate device with output enable control and performs the Boolean function Y = A. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram



9.3 Feature Description

The SN74AUP1G125 has an operating voltage range of 0.8 V to 3.6 V.

The SN74AUP1G125 allows down voltage translation and the inputs of the device accept voltages up tp 3.6 V.

The I_{off} feature also allows voltages on the inputs and outputs when the V_{CC} is 0 V.

9.4 Device Functional Modes

Table 1 lists the functional modes for SN74AUP1G125.

Table 1. Function Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AUP1G125 device is a high-drive CMOS device that can be used as a output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant, allowing it to translate down to V_{CC}.

10.2 Typical Application

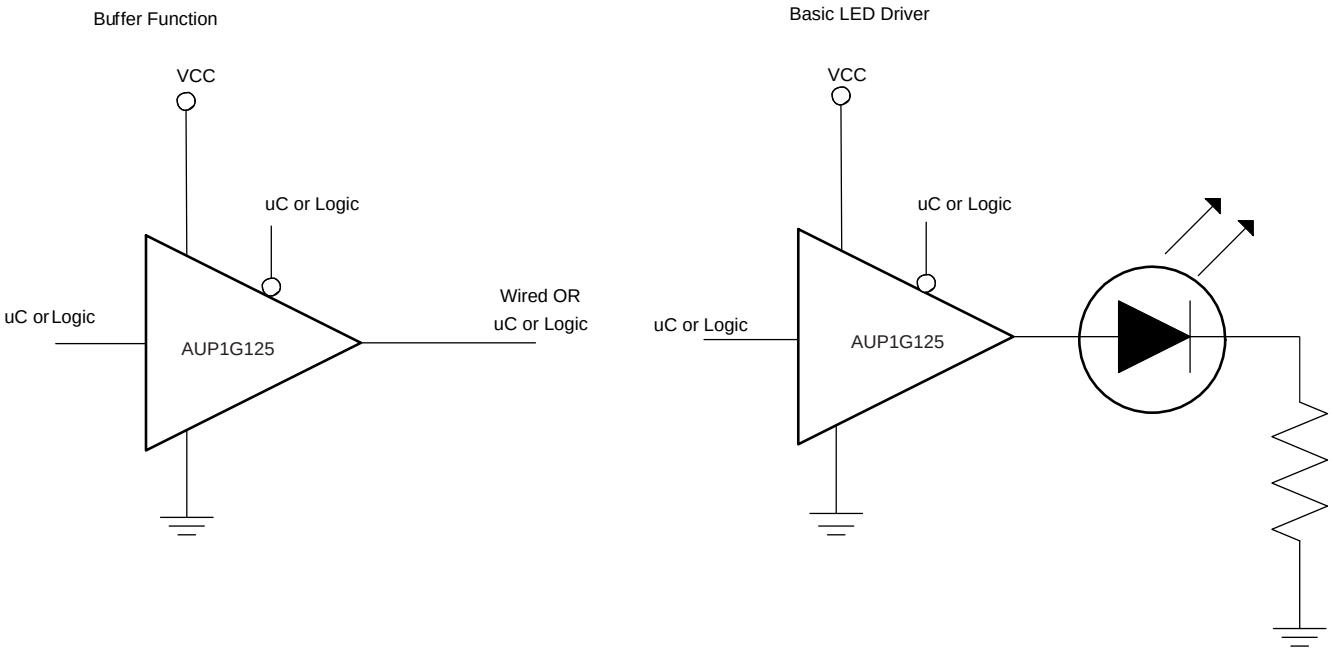


Figure 4. Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Typical Application (continued)

– Outputs should not be pulled above V_{CC}.

10.2.3 Application Curve

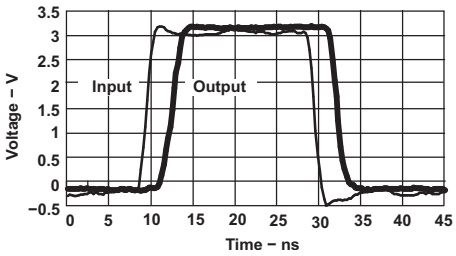


Figure 5. Switching Characteristics at 25 MHz

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

VCC pin should have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1-µF capacitor for this device. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

12.2 Layout Example

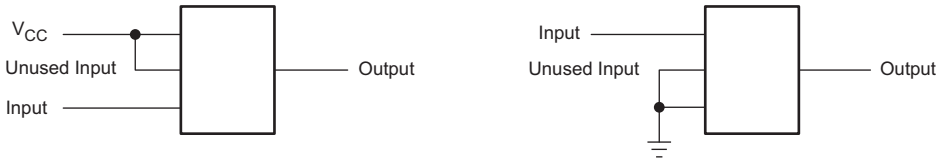


Figure 6. Package Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
BluRay is a trademark of Blu-ray Disc Association (BDA).
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AUP1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
74AUP1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMF ~ HMK ~ HMR)	Samples
74AUP1G125DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMR)	Samples
SN74AUP1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
SN74AUP1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
SN74AUP1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMF ~ HMK ~ HMR)	Samples
SN74AUP1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMR)	Samples
SN74AUP1G125DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMR)	Samples
SN74AUP1G125DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HM	Samples
SN74AUP1G125DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HM	Samples
SN74AUP1G125YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		(HM2 ~ HM7 ~ HMN)	Samples
SN74AUP1G125YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMN)	Samples
SN74AUP1G125YZTR	ACTIVE	DSBGA	YZT	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HM ~ HM2)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

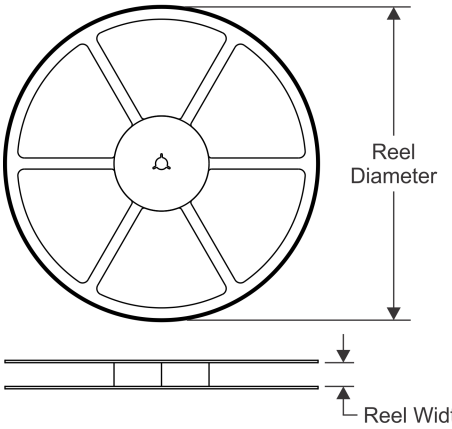
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

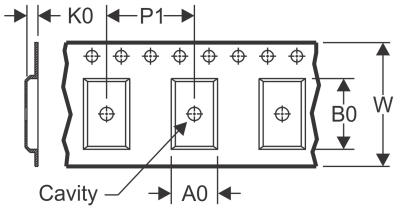
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

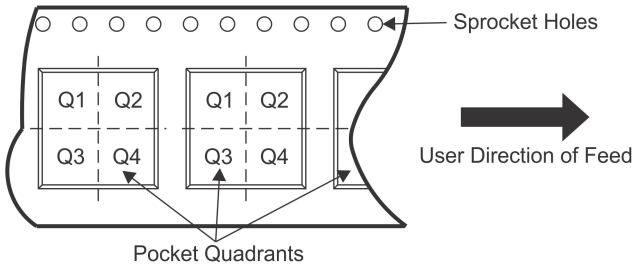


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

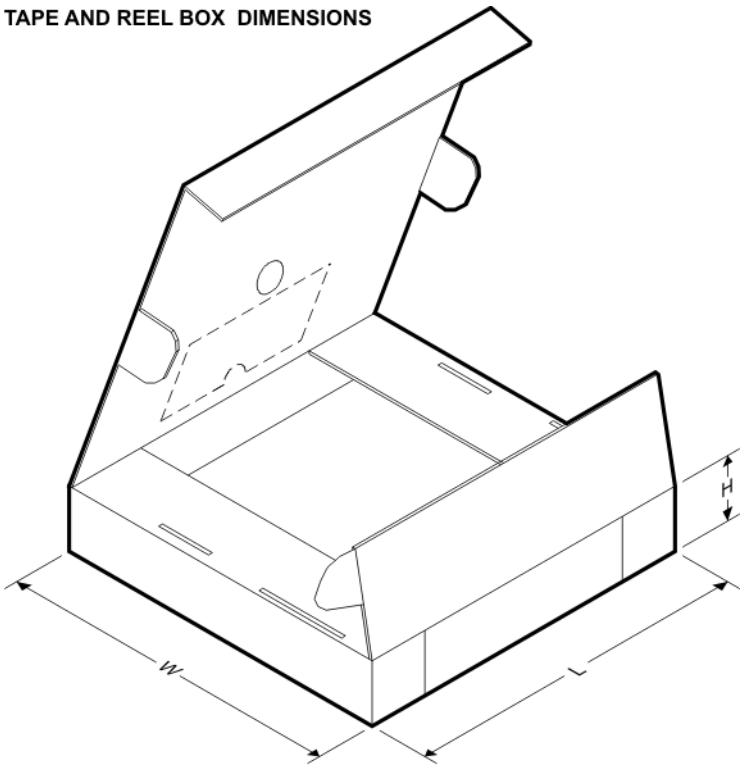
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G125DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G125DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G125DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G125DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G125YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

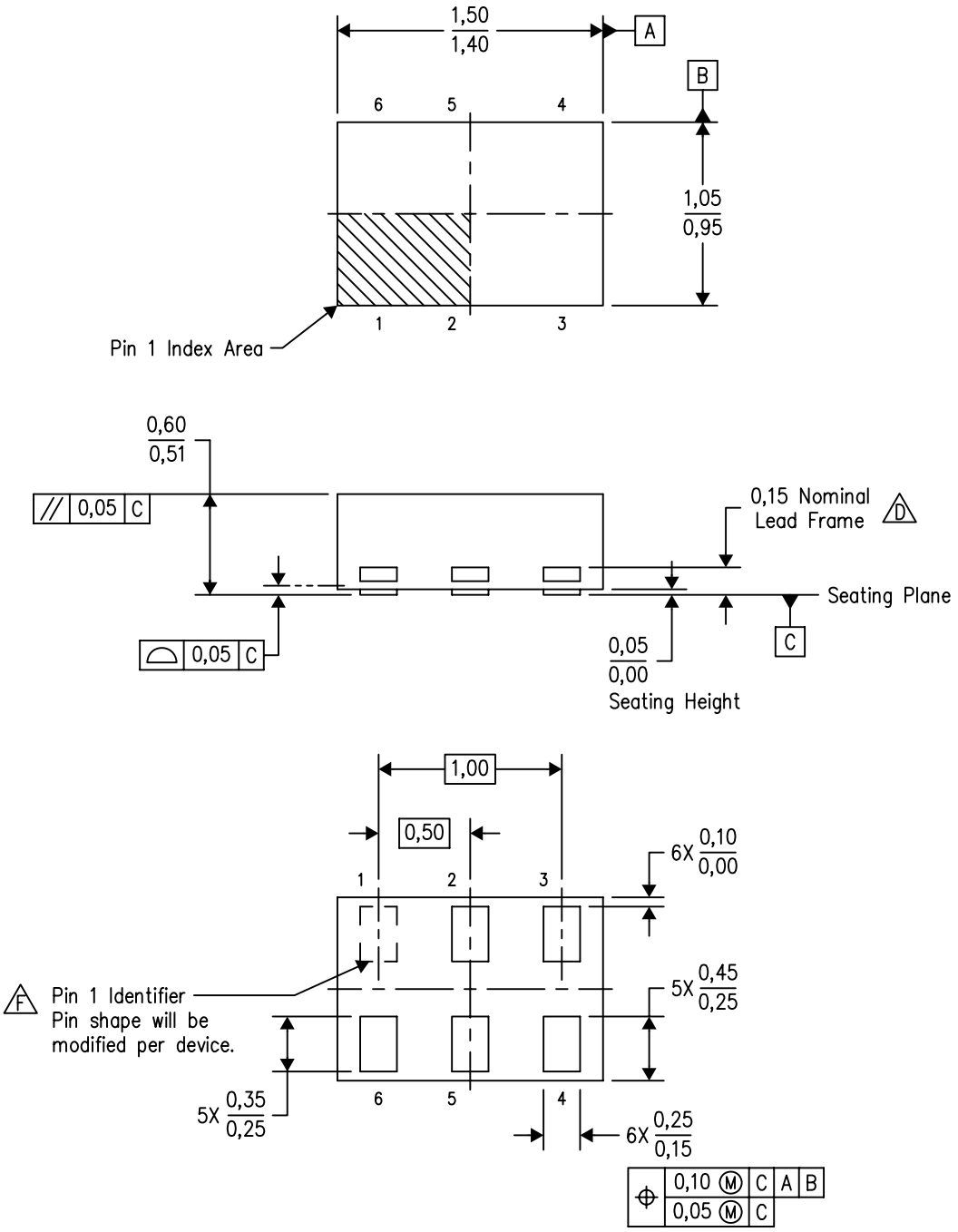
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G125DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G125DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G125DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G125DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G125DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G125YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

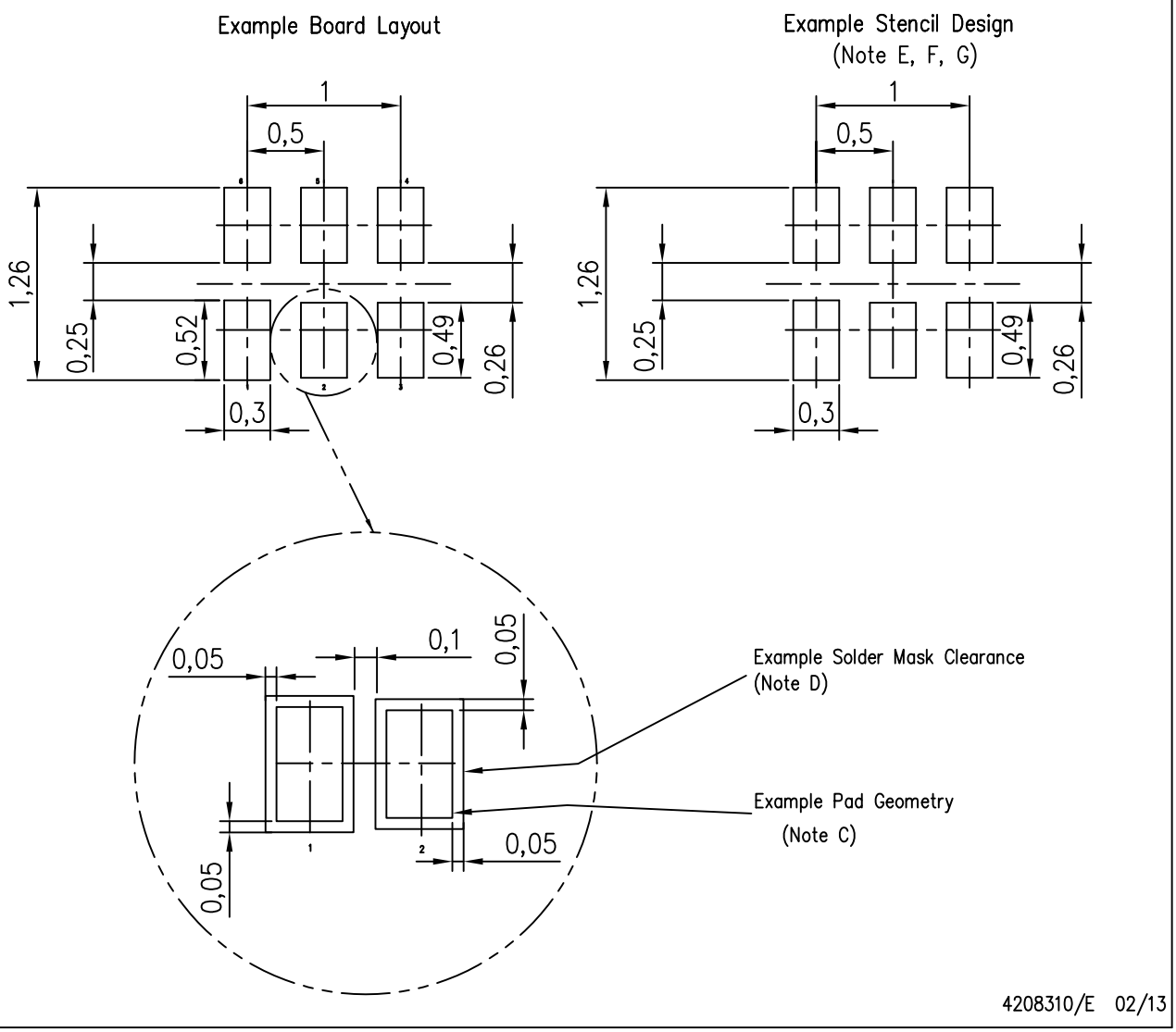
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



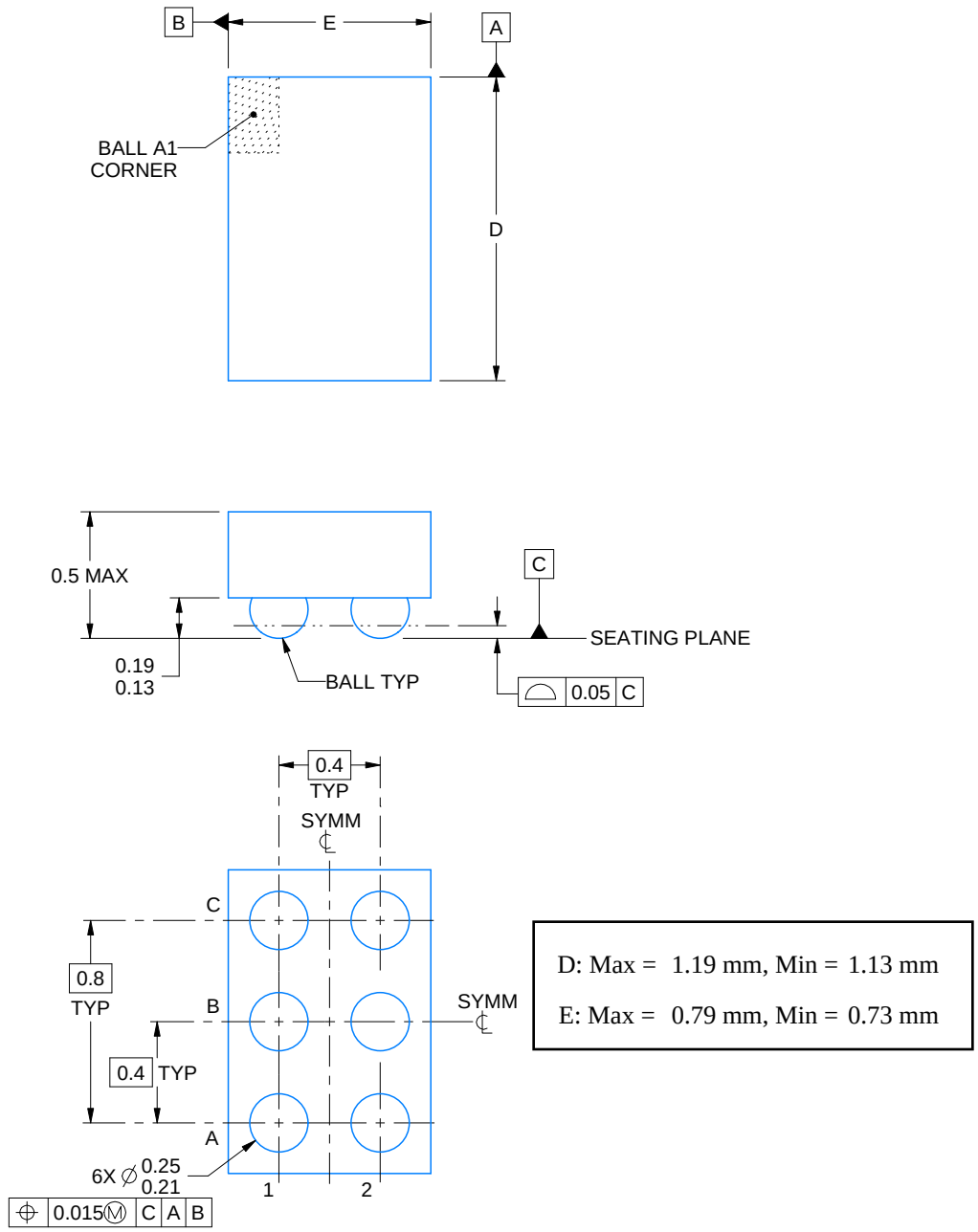
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

YFP0006

DSBGA - 0.5 mm max height

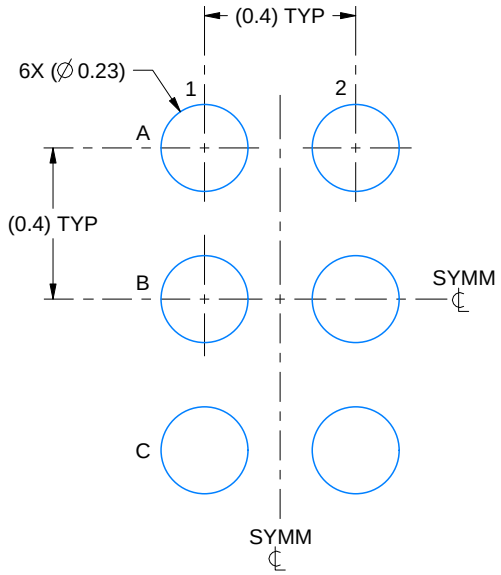
DIE SIZE BALL GRID ARRAY



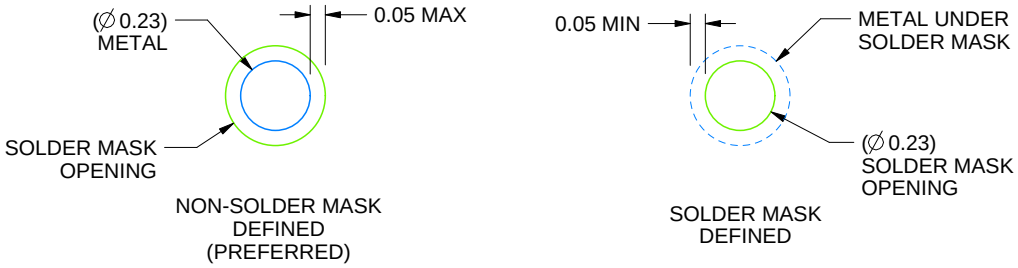
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

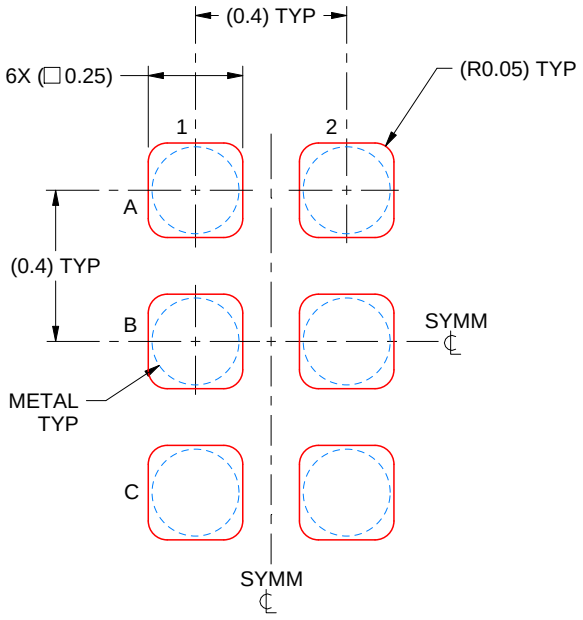


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

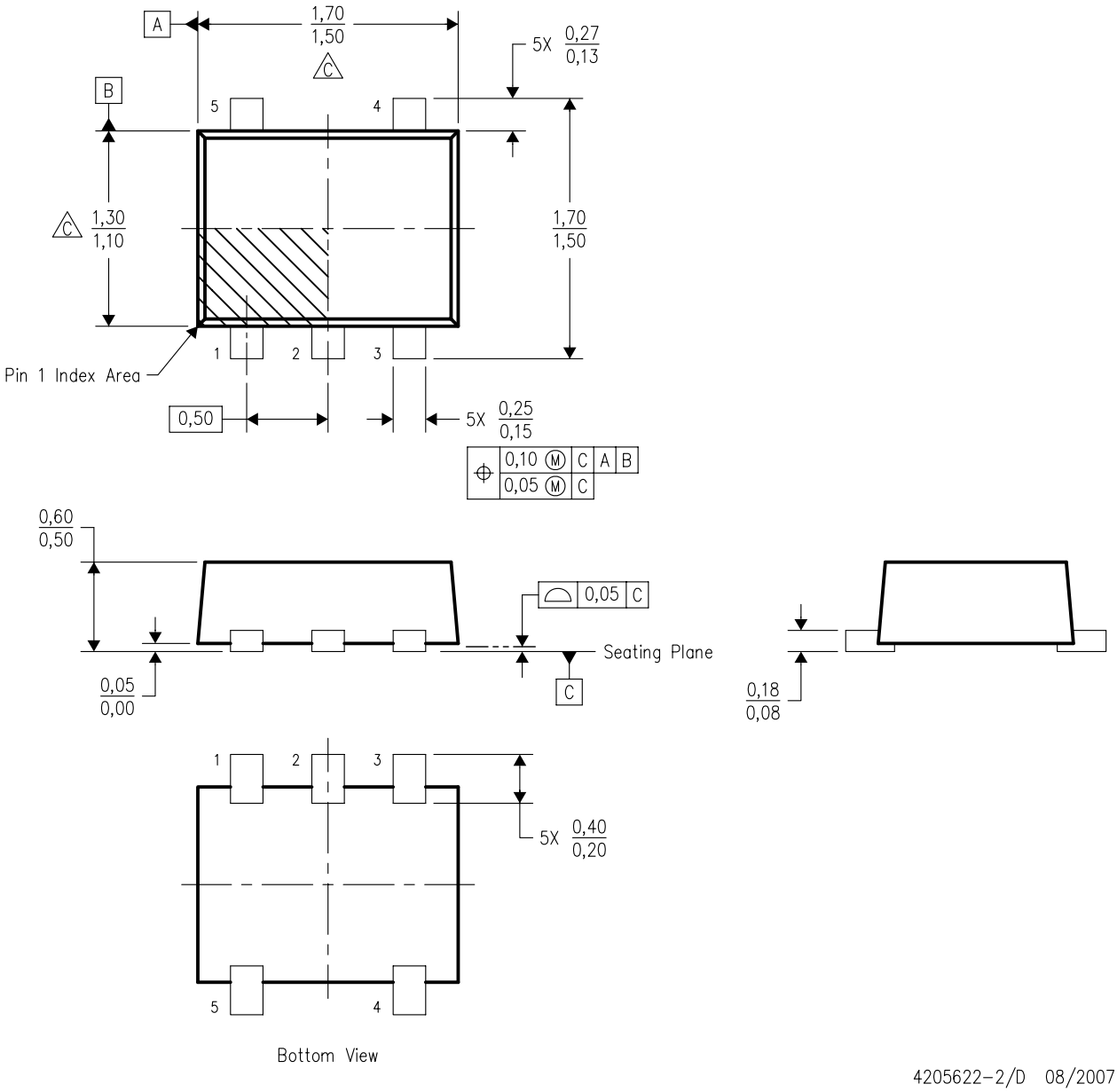


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

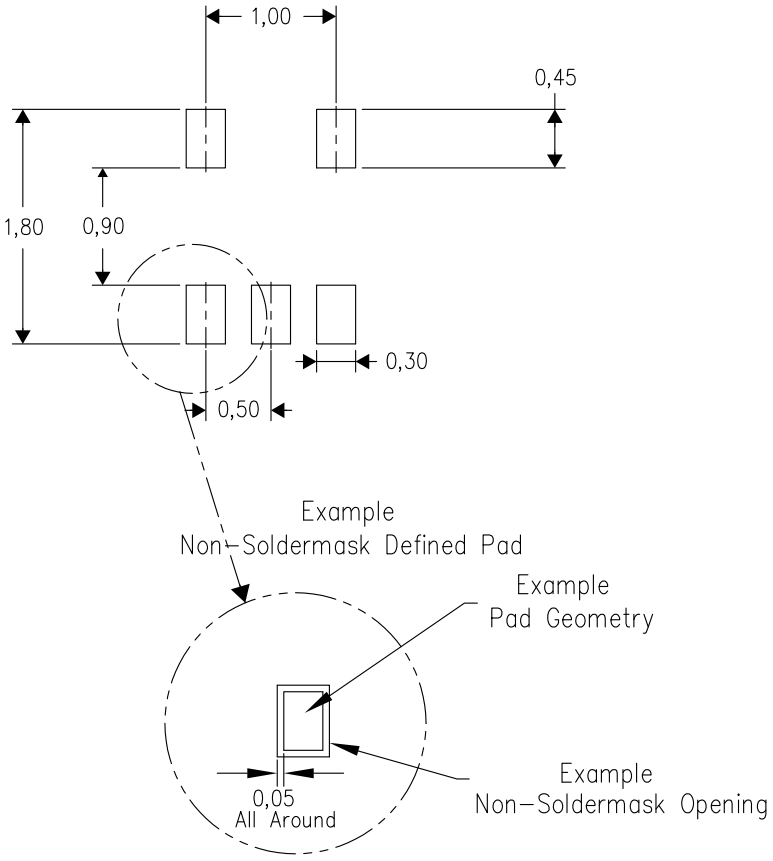
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



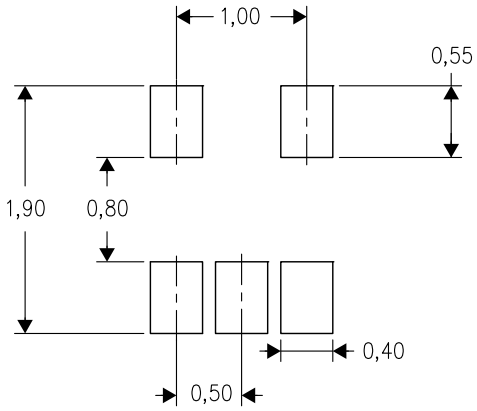
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



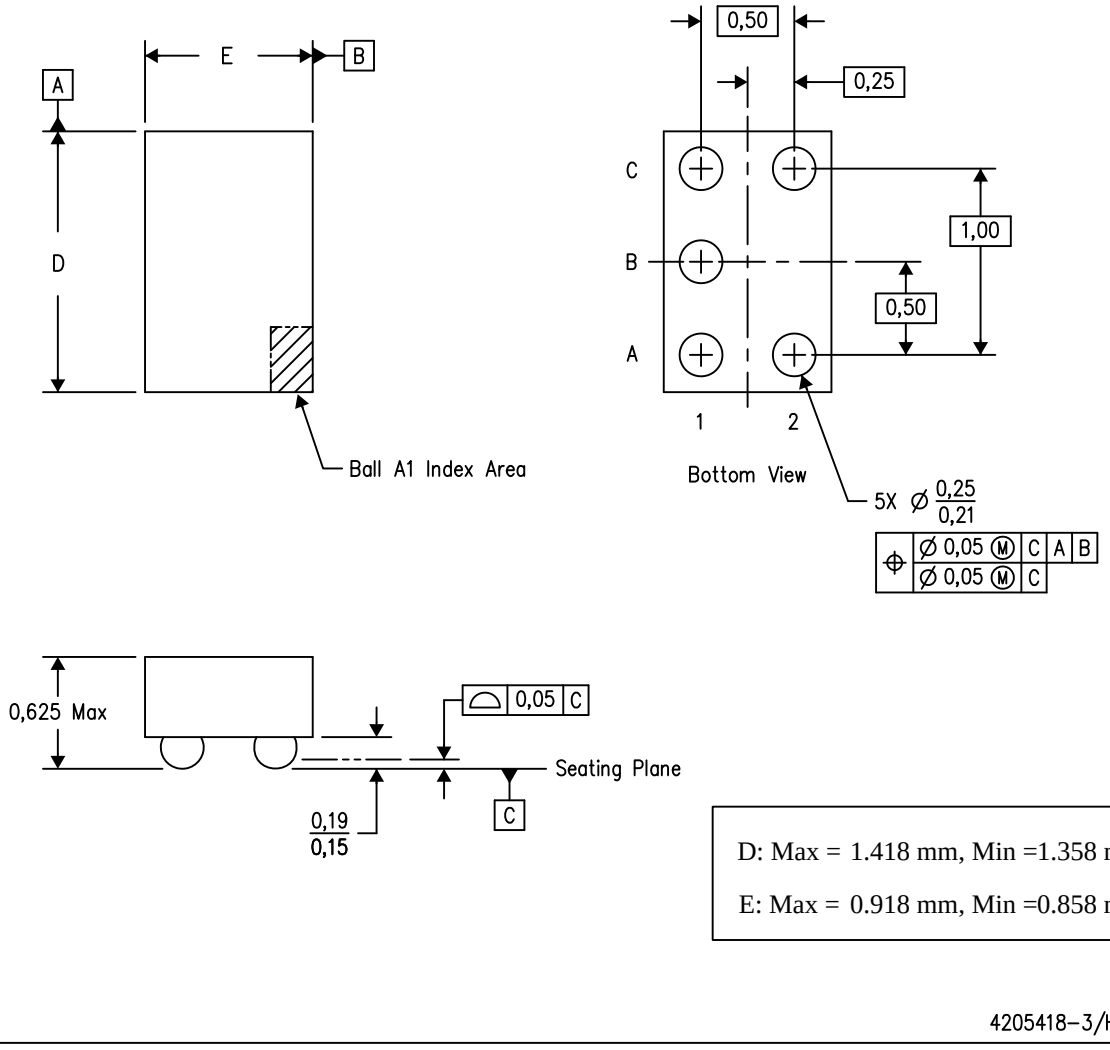
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

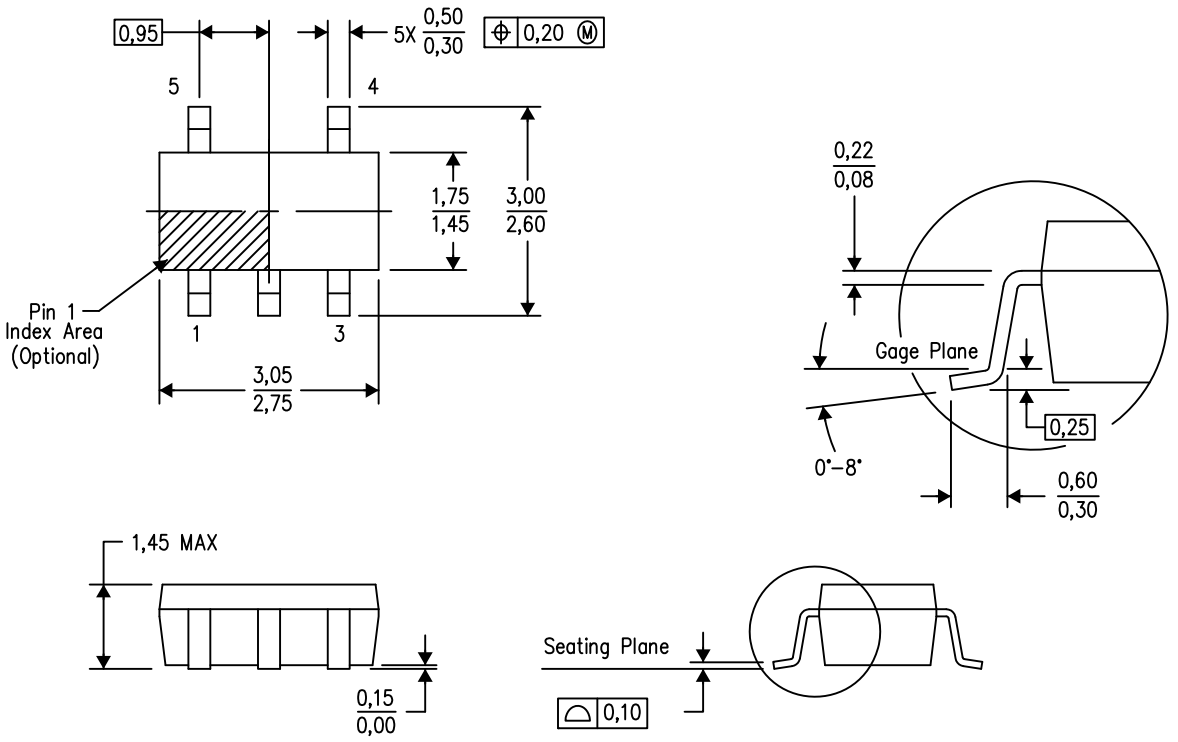
YZT (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

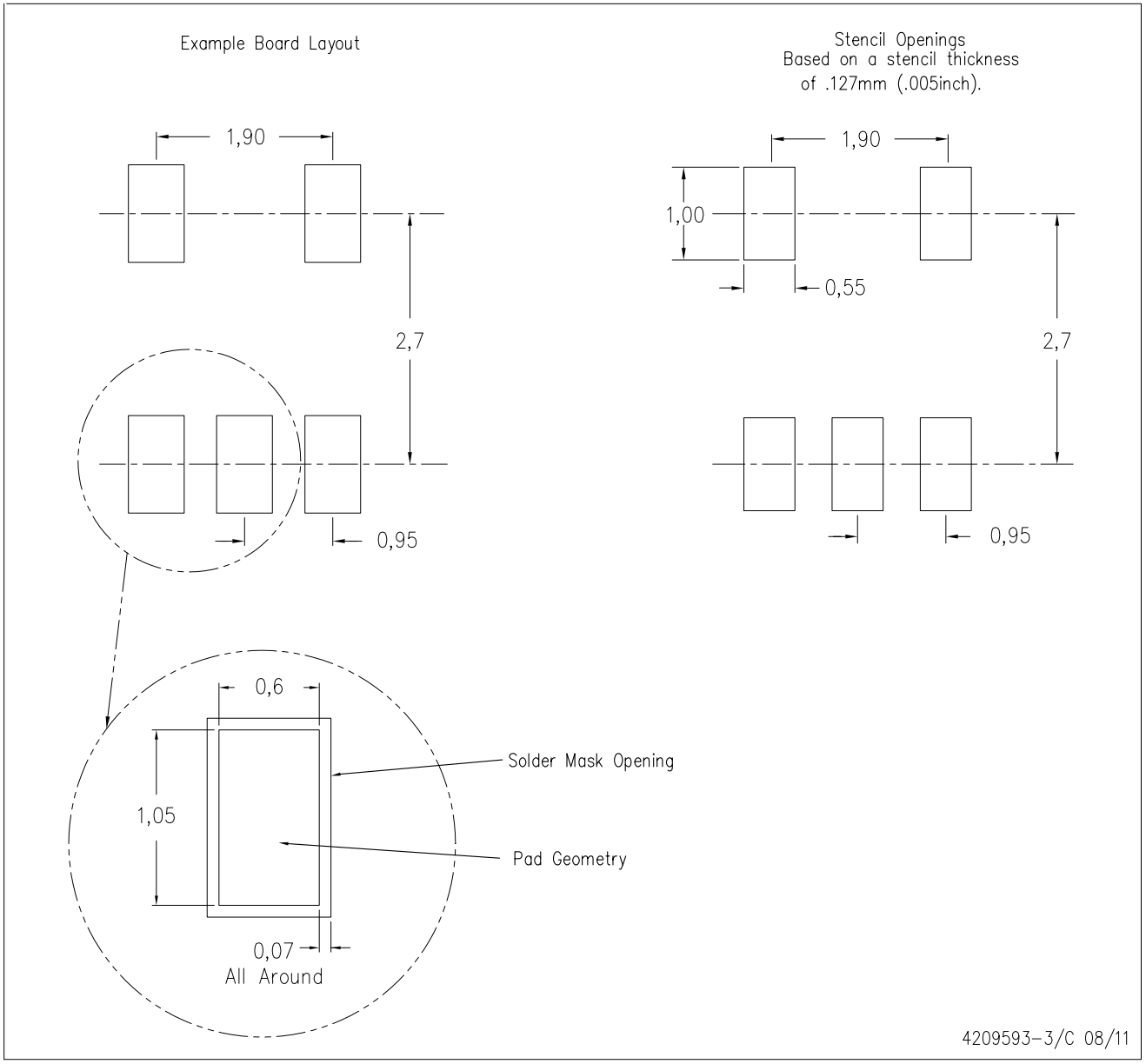
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

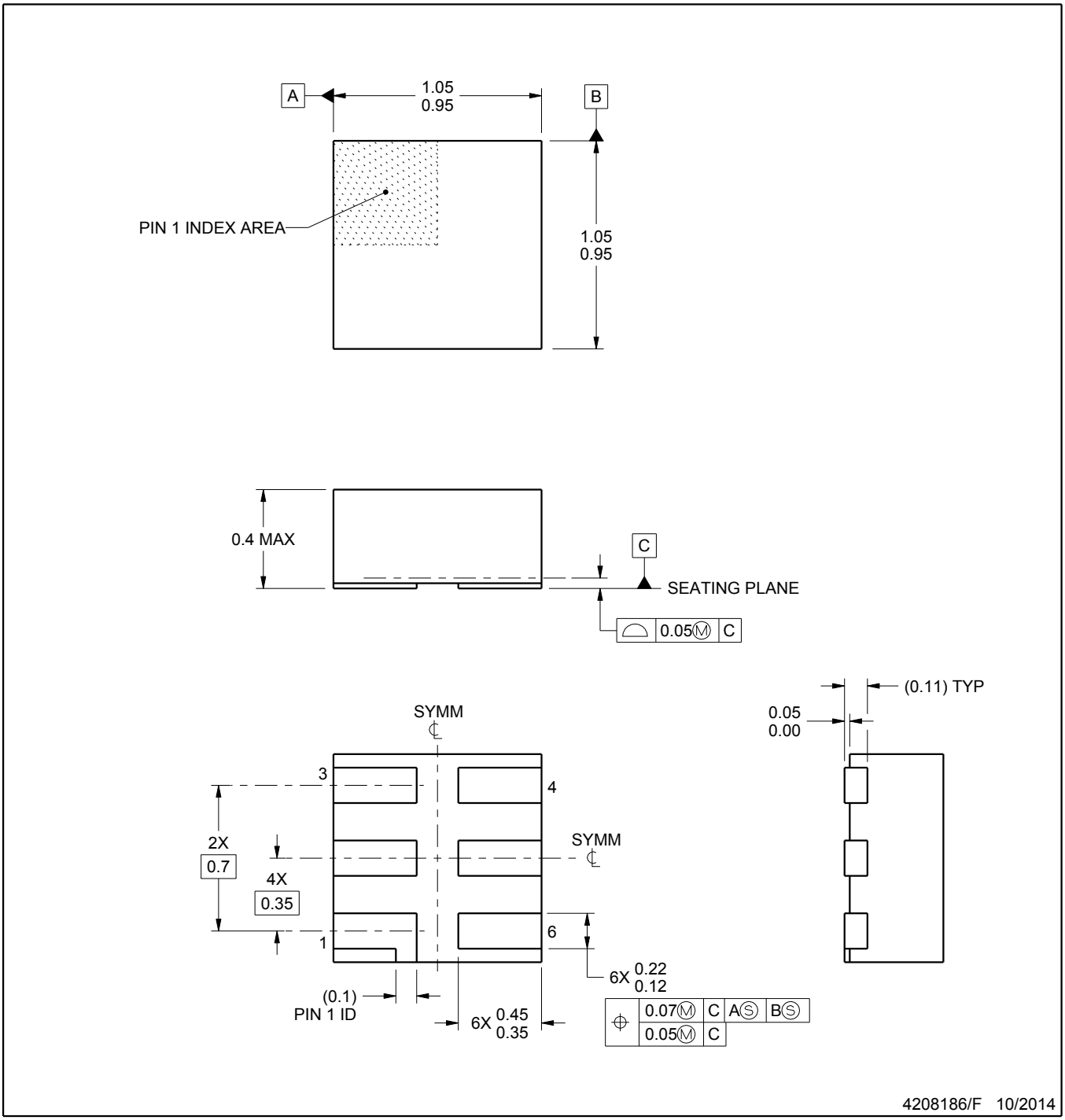
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

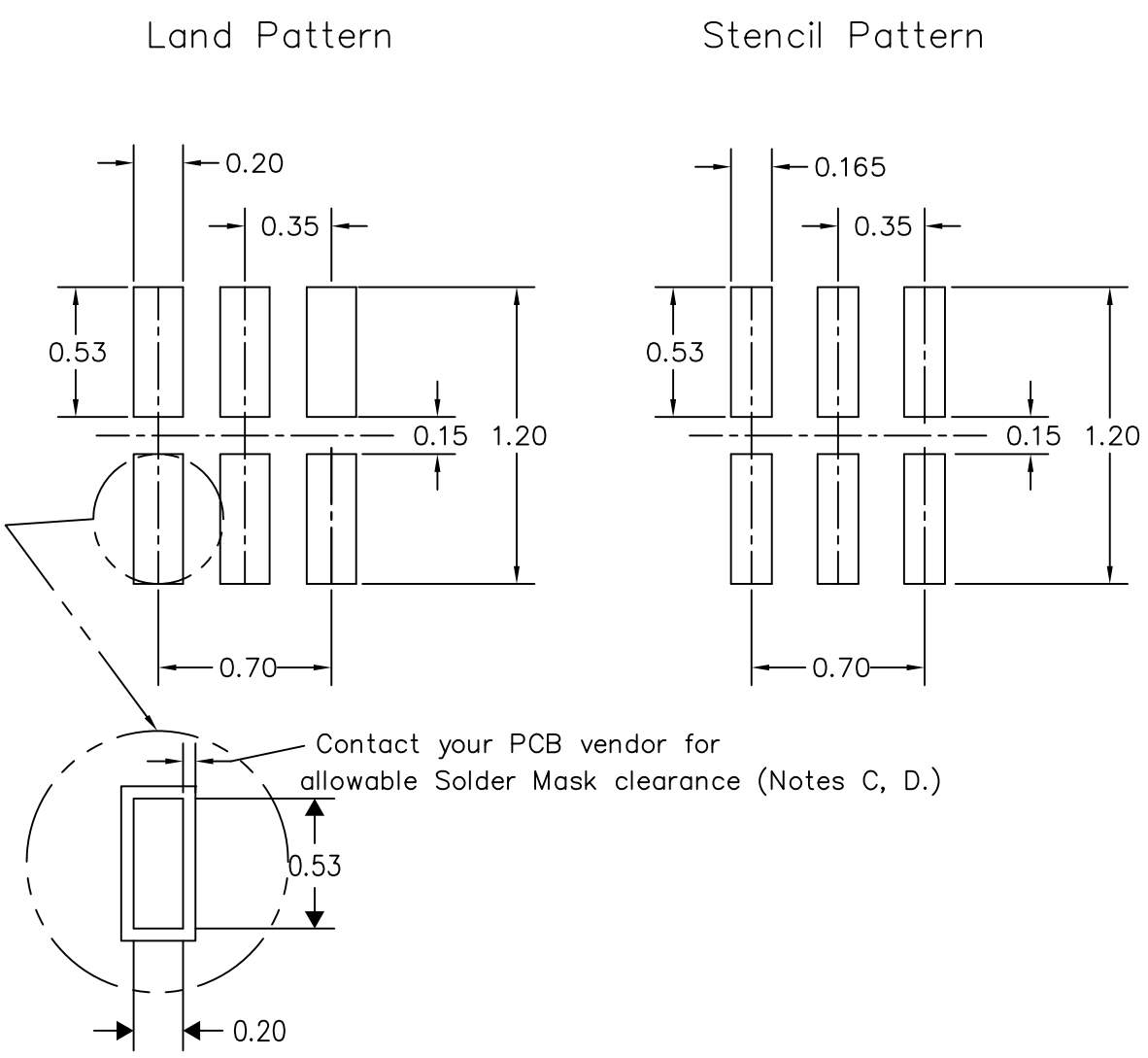
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

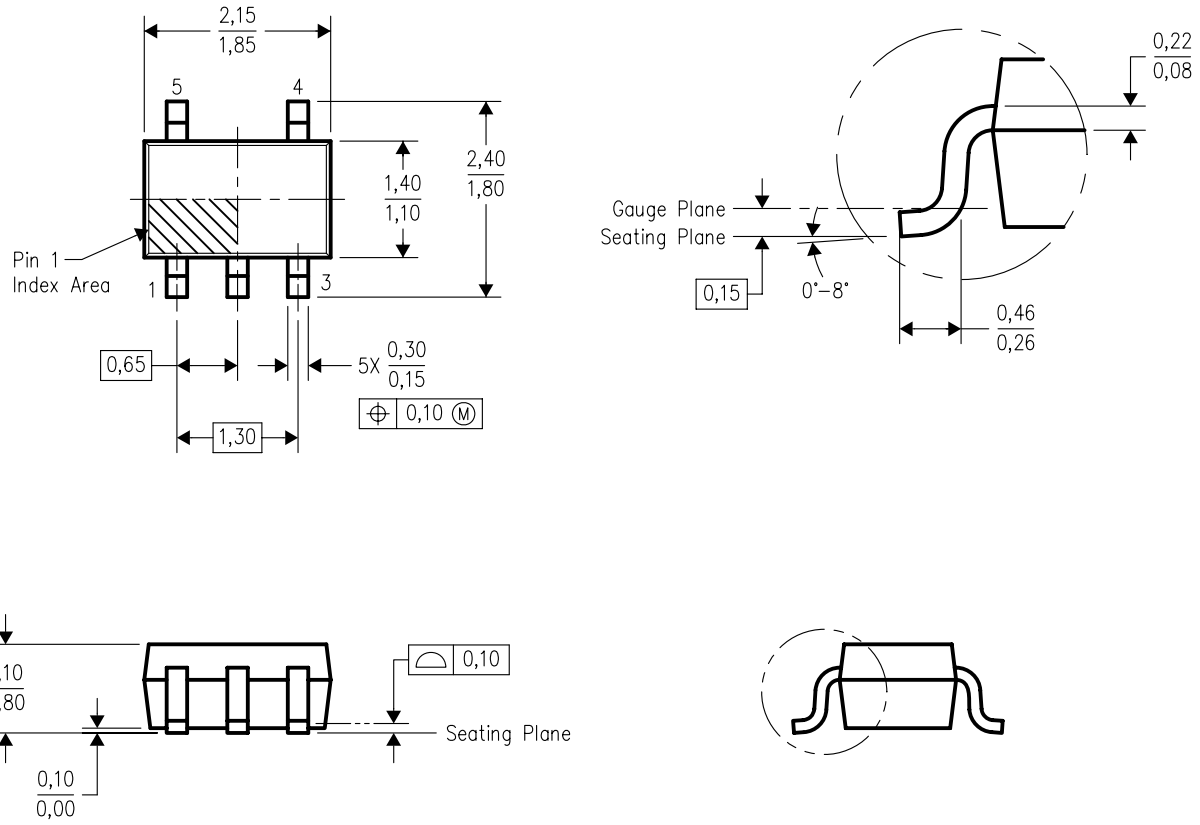
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210277/D 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

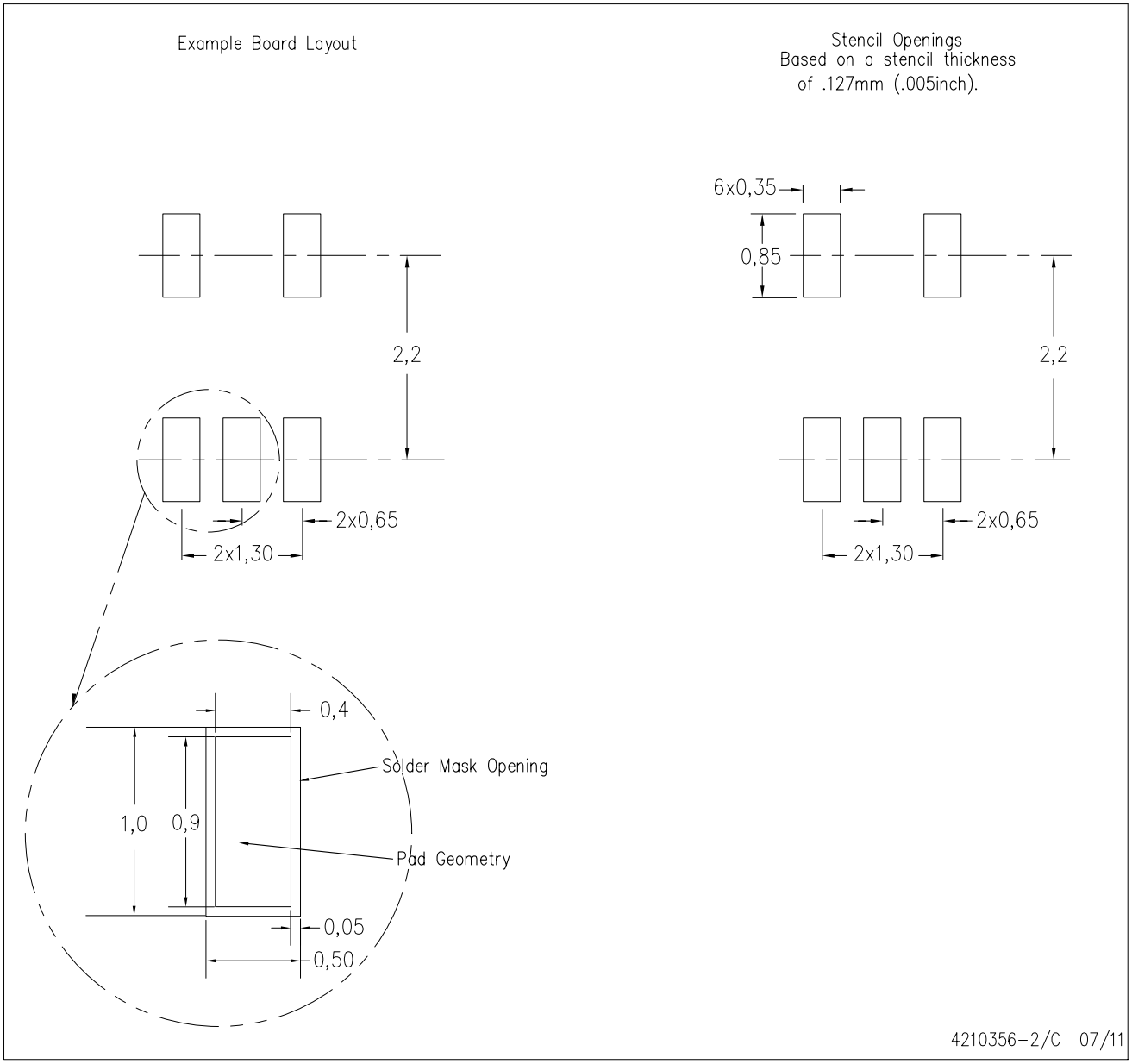
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

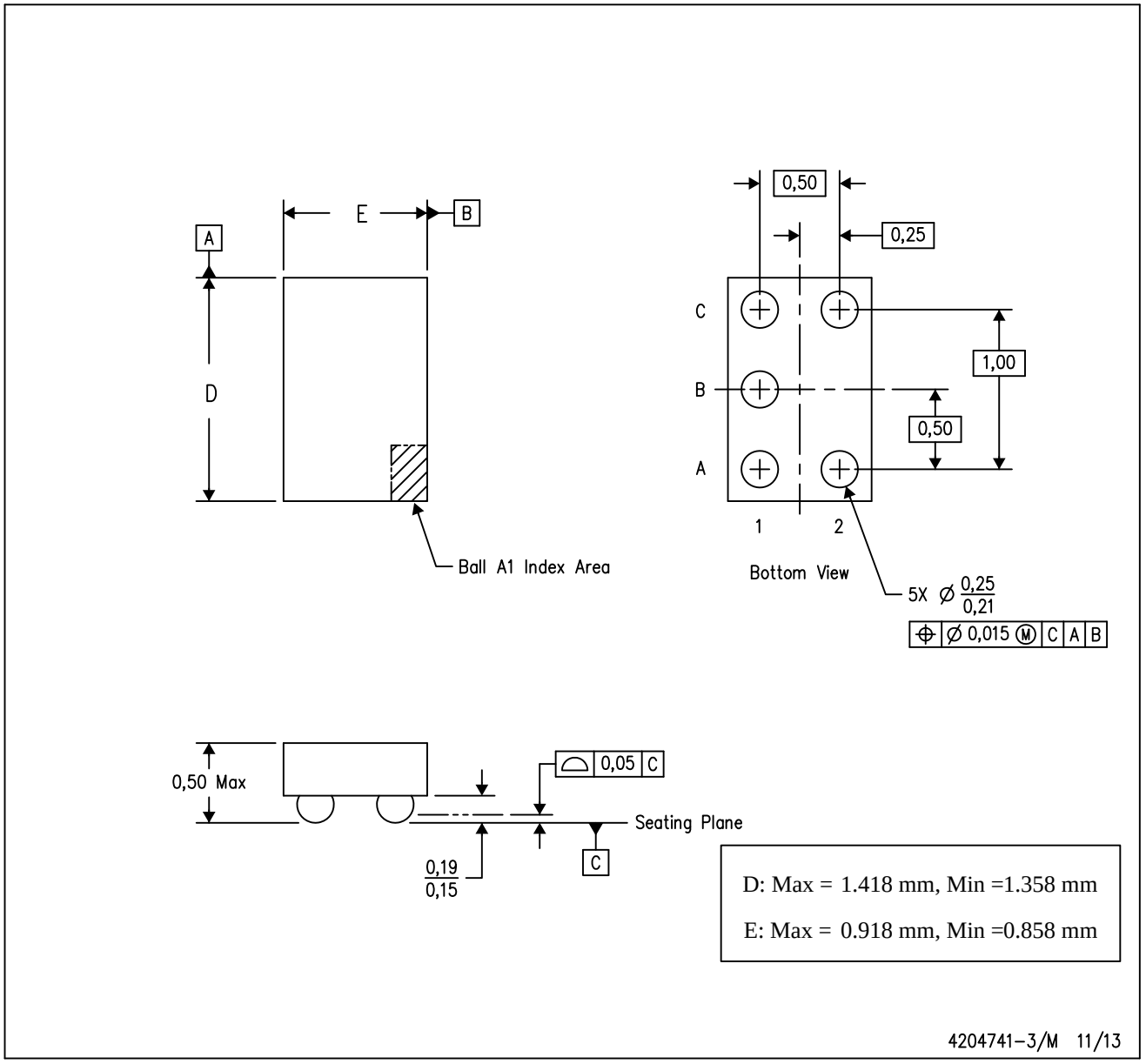
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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