

## MSP430FR263x, MSP430FR253x Mixed-Signal Microcontrollers

### 1 Device Overview

#### 1.1 Features

- Embedded Microcontroller
  - 16-Bit RISC Architecture
  - Clock Supports Frequencies up to 16 MHz
  - Wide Supply Voltage Range From 1.8 V to 3.6 V <sup>(1)</sup>
- Optimized Ultra-Low-Power Modes
  - Active Mode: 126  $\mu$ A/MHz (Typical)
  - Standby
    - 1.7  $\mu$ A/Button Average (Typical) (16 Self-Capacitance Buttons, 8-Hz Scanning)
    - 1.7  $\mu$ A/Button Average (Typical) (64 Mutual-Capacitance Buttons, 8-Hz Scanning)
  - LPM3.5 Real-Time Clock (RTC) Counter With 32768-Hz Crystal: 770 nA (Typical)
  - Shutdown (LPM4.5): 15 nA (Typical)
- Low-Power Ferroelectric RAM (FRAM)
  - Up to 15.5KB of Nonvolatile Memory
  - Built-In Error Correction Code (ECC)
  - Configurable Write Protection
  - Unified Memory of Program, Constants, and Storage
  - $10^{15}$  Write Cycle Endurance
  - Radiation Resistant and Nonmagnetic
  - High FRAM-to-SRAM Ratio, up to 4:1
- Intelligent Digital Peripherals
  - Four 16-Bit Timers
    - Two Timers With Three Capture/Compare Registers Each (Timer\_A3)
    - Two Timers With Two Capture/Compare Registers Each (Timer\_A2)
  - One 16-Bit Timer Associated With CapTIvate™ Technology
  - One 16-Bit Counter-Only RTC
  - 16-Bit Cyclic Redundancy Check (CRC)
- Enhanced Serial Communications
  - Two Enhanced Universal Serial Communication Interfaces (eUSCI\_A) Support UART, IrDA, and SPI
  - One eUSCI (eUSCI\_B) Supports SPI and I<sup>2</sup>C
- High-Performance Analog
  - 8-Channel 10-Bit Analog-to-Digital Converter (ADC)
    - Internal 1.5-V Reference
    - Sample-and-Hold 200 ksp/s
- [CapTIvate Technology](#) – Capacitive Touch
  - Performance
    - Fast Electrode Scanning With Four Simultaneous Scans
    - Support for High-Resolution Sliders With >1024 Points
    - 30-cm Proximity Sensing
  - Reliability
    - Increased Immunity to Power Line, RF, and Other Environmental Noise
    - Built-in Spread Spectrum, Automatic Tuning, Noise Filtering, and Debouncing Algorithms
    - Enables [Reliable Touch Solutions](#) With 10-V RMS Common-Mode Noise, 4-kV Electrical Fast Transients, and 15-kV Electrostatic Discharge, Allowing for IEC-61000-4-6, IEC-61000-4-4, and IEC-61000-4-2 Compliance
    - Reduced RF Emissions to Simplify Electrical Designs
    - Support for Metal Touch and Water Rejection Designs
  - Flexibility
    - Up to 16 Self-Capacitance and 64 Mutual-Capacitance Electrodes
    - Mix and Match [Self- and Mutual-Capacitive Electrodes in the Same Design](#)
    - Supports Multitouch Functionality
    - Wide Range of Capacitance Detection, Wide Electrode Range of 0 to 300 pF
  - Low Power
    - <0.9  $\mu$ A/Button in Wake-on-Touch Mode, Where Capacitive Measurement and Touch Detection is Done by Hardware State Machine While CPU is Asleep
    - Wake-on-Touch State Machine Allows Electrode Scanning While CPU is Asleep
    - Hardware Acceleration for Environmental Compensation, Filtering, and Threshold Detection
  - Ease of Use
    - [CapTIvate Design Center](#), PC GUI Lets Engineers Design and Tune Capacitive Buttons in Real Time Without Having to Write Code

(1) Minimum supply voltage is restricted by SVS levels (see  $V_{SVSH-}$  and  $V_{SVSH+}$  in [Table 5-2](#))



- CapTIvate Software Library in ROM Provides Ample FRAM for Customer Application
- Clock System (CS)
  - On-Chip 32-kHz RC Oscillator (REFO)
  - On-Chip 16-MHz Digitally Controlled Oscillator (DCO) With Frequency-Locked Loop (FLL)
    - $\pm 1\%$  Accuracy With On-Chip Reference at Room Temperature
  - On-Chip Very Low-Frequency 10-kHz Oscillator (VLO)
  - On-Chip High-Frequency Modulation Oscillator (MODOSC)
  - External 32-kHz Crystal Oscillator (LFXT)
  - Programmable MCLK Prescaler of 1 to 128
  - SMCLK Derived from MCLK With Programmable Prescaler of 1, 2, 4, or 8
- General Input/Output and Pin Functionality
  - Total of 19 I/Os on TSSOP-32 Package
  - 16 Interrupt Pins (P1 and P2) Can Wake MCU From Low-Power Modes
- Development Tools and Software
  - Ease-of-Use Ecosystem
    - CapTIvate Design Center – Code Generation, Customizable GUI, Real-Time Tuning
- Free Professional Development Environments
- 12-KB ROM Library Includes CapTIvate Touch Libraries and Driver Libraries
- Family Members (Also See [Section 3](#))
  - MSP430FR2633: 15KB of Program FRAM + 512B of Information FRAM + 4KB of RAM up to 16 Self-Capacitive and 64 Mutual-Capacitive Sensors
  - MSP430FR2533: 15KB of Program FRAM + 512B of Information FRAM + 2KB of RAM up to 16 Self-Capacitive or 16 Mutual-Capacitive Sensors
  - MSP430FR2632: 8KB of Program FRAM + 512B of Information FRAM + 2KB of RAM up to 8 Self-Capacitive or 16 Mutual-Capacitive Sensors
  - MSP430FR2532: 8KB of Program FRAM + 512B of Information FRAM + 1KB of RAM up to 8 Self-Capacitive or 8 Mutual-Capacitive Sensors
- Package Options
  - 32-Pin: VQFN (RHB)
  - 32-Pin: TSSOP (DA)
  - 24-Pin: VQFN (RGE)
- For Complete Module Descriptions, See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#))

## 1.2 Applications

- Thermostats
- Electronic Access Control
- Lighting Control
- Electronic Door Locks
- White Goods
- Small Appliances
- Personal Electronics

## 1.3 Description

The MSP430FR263x and MSP430FR253x are FRAM-based ultra-low-power MSP microcontrollers that feature CapTIvate touch technology for buttons, sliders, wheels (BSW), and proximity applications. CapTIvate technology provides the highest resolution capacitive-touch solution in the market with high reliability and noise immunity at the lowest power. CapTIvate technology supports concurrent self-capacitance and mutual-capacitance electrodes on the same design for maximum flexibility. Using the CapTIvate Design Center, engineers can quickly develop BSW applications with an easy-to-use GUI.

The TI MSP family of low-power microcontrollers consists of several devices that feature different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The MCU features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the MCU to wake up from low-power modes to active mode typically in less than 10  $\mu$ s.

**Device Information<sup>(1)</sup>**

| PART NUMBER      | PACKAGE    | BODY SIZE <sup>(2)</sup> |
|------------------|------------|--------------------------|
| MSP430FR2633IRHB | VQFN (32)  | 5 mm × 5 mm              |
| MSP430FR2533IRHB | VQFN (32)  | 5 mm × 5 mm              |
| MSP430FR2633IDA  | TSSOP (32) | 11 mm × 6.2 mm           |
| MSP430FR2533IDA  | TSSOP (32) | 11 mm × 6.2 mm           |
| MSP430FR2632IRGE | VQFN (24)  | 4 mm × 4 mm              |
| MSP430FR2532IRGE | VQFN (24)  | 4 mm × 4 mm              |

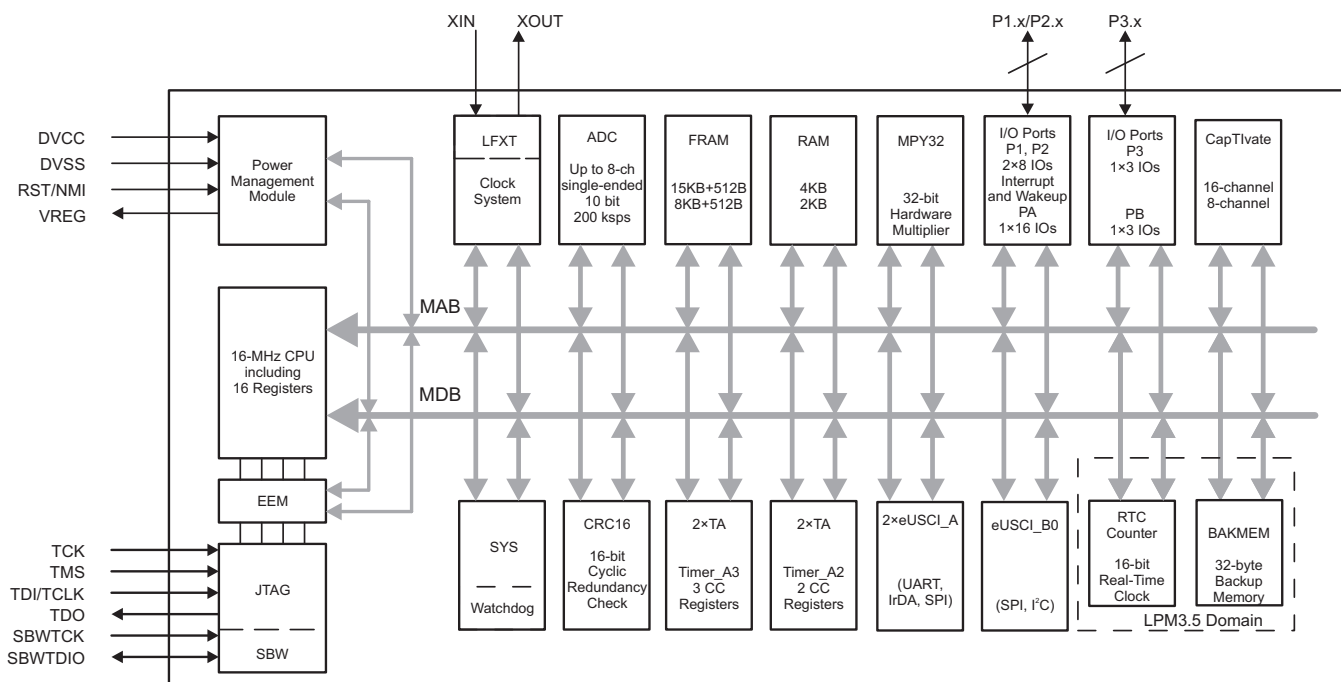
- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 9](#), or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

**CAUTION**

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See the application report *MSP430 System-Level ESD Considerations* ([SLAA530](#)) for more information.

## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



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**Figure 1-1. Functional Block Diagram**

- The MCU has one main power pair of DVCC and DVSS that supplies digital and analog modules. Recommended bypass and decoupling capacitors are 4.7  $\mu\text{F}$  to 10  $\mu\text{F}$  and 0.1  $\mu\text{F}$ , respectively, with  $\pm 5\%$  accuracy.
- VREG is the decoupling capacitor of the CapTIvate regulator. The recommended value for the required decoupling capacitor is 1  $\mu\text{F}$ , with a maximum ESR of  $\leq 200 \text{ m}\Omega$ .
- P1 and P2 feature the pin interrupt function and can wake the MCU from all LPMs, including LPM3.5 and LPM4.
- Each Timer\_A3 has three capture/compare registers. Only CCR1 and CCR2 are externally connected. CCR0 registers can be used only for internal period timing and interrupt generation.
- Each Timer\_A2 has two capture/compare registers. Both registers can be used only for internal period timing and interrupt generation.
- In LPM3 mode, the CapTIvate module can be functional while the rest of the peripherals are off.

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from November 10, 2015 to December 8, 2015   | Page               |
|--|--------------------|
| • Changed document status from Preview to Production Data  | <a href="#">1</a>  |
| • Added note to list item that starts "Wide Supply Voltage Range..."   | <a href="#">1</a>  |
| • Changed list item that starts "Enables Reliable Touch Solutions..."  | <a href="#">1</a>  |
| • In the note that starts "Low-power mode 3, VLO, excludes SVS test conditions...", changed "f <sub>XT1</sub> = 0 Hz" to "f <sub>XT1</sub> = 32768 Hz" | <a href="#">19</a> |
| • Added note that starts "The VLO clock frequency is reduced by 15%..."  | <a href="#">28</a> |
| • Added note to "Clock" in <a href="#">Table 6-1, Operating Modes</a>  | <a href="#">44</a> |
| • Added note that starts "XT1CLK and VLOCLK can be active during LPM4..."  | <a href="#">44</a> |
| • Corrected description in <a href="#">Section 6.10.10, Backup Memory (BKMEM)</a>  | <a href="#">55</a> |

### 3 Device Comparison

Table 3-1 summarizes the features of the available family members.

**Table 3-1. Device Comparison<sup>(1)(2)</sup>**

| DEVICE           | PROGRAM FRAM<br>+ INFORMATION<br>FRAM (bytes) | SRAM<br>(bytes) | TA0 TO TA3                              | eUSCI_A |         | eUSCI_B | 10-BIT ADC<br>CHANNELS | CapTIvate™<br>CHANNELS | GPIOs | PACKAGE<br>TYPE  |
|------------------|---|-----------------|---|---------|---------|---------|------------------------|------------------------|-------|------------------|
|                  |   |                 |   | UART    | SPI     |         |                        |                        |       |                  |
| MSP430FR2633IRHB | 15360 + 512                                   | 4096            | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | up to 2 | 1       | 8                      | 16 <sup>(4)</sup>      | 19    | 32 RHB<br>(VQFN) |
| MSP430FR2533IRHB | 15360 + 512                                   | 2048            | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | up to 2 | 1       | 8                      | 16 <sup>(4)</sup>      | 19    | 32 RHB<br>(VQFN) |
| MSP430FR2633IDA  | 15360 + 512                                   | 4096            | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | up to 2 | 1       | 8                      | 16 <sup>(4)</sup>      | 19    | 32 DA<br>(TSSOP) |
| MSP430FR2533IDA  | 15360 + 512                                   | 2048            | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | up to 2 | 1       | 8                      | 16 <sup>(4)</sup>      | 19    | 32 DA<br>(TSSOP) |
| MSP430FR2632IRGE | 8192 + 512                                    | 2048            | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | 1       | 1       | 8                      | 8 <sup>(5)</sup>       | 15    | 24 RGE<br>(VQFN) |
| MSP430FR2532IRGE | 8192 + 512                                    | 1,024           | 2, 3 × CCR <sup>(3)</sup><br>2, 2 × CCR | up to 2 | 1       | 1       | 8                      | 8 <sup>(5)</sup>       | 15    | 24 RGE<br>(VQFN) |

- (1) For the most current package and ordering information, see the *Package Option Addendum* in [Section 9](#), or see the TI website at [www.ti.com](http://www.ti.com)
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging)
- (3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.
- (4) Eight dedicated CapTIvate channels are included.
- (5) Four dedicated CapTIvate channels are included.

## 4 Terminal Configuration and Functions

### 4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 24-pin RHB package.

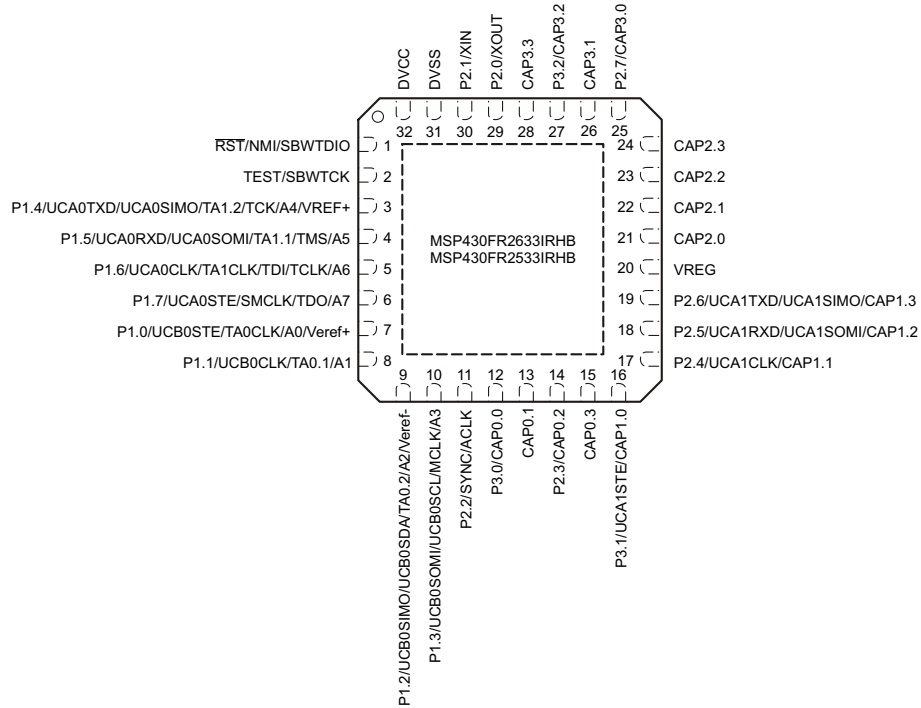


Figure 4-1. 32-Pin RHB Package (Top View)

Figure 4-2 shows the pinout for the 32-pin DA package.

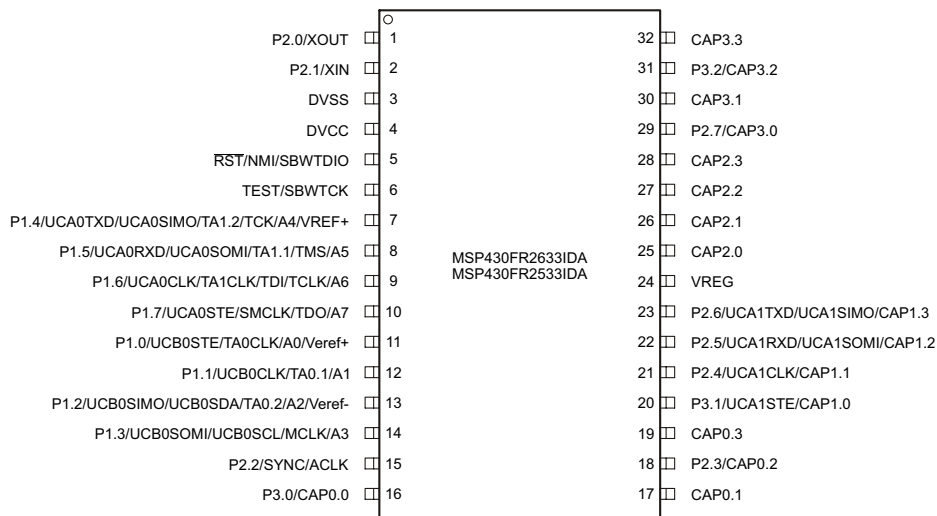
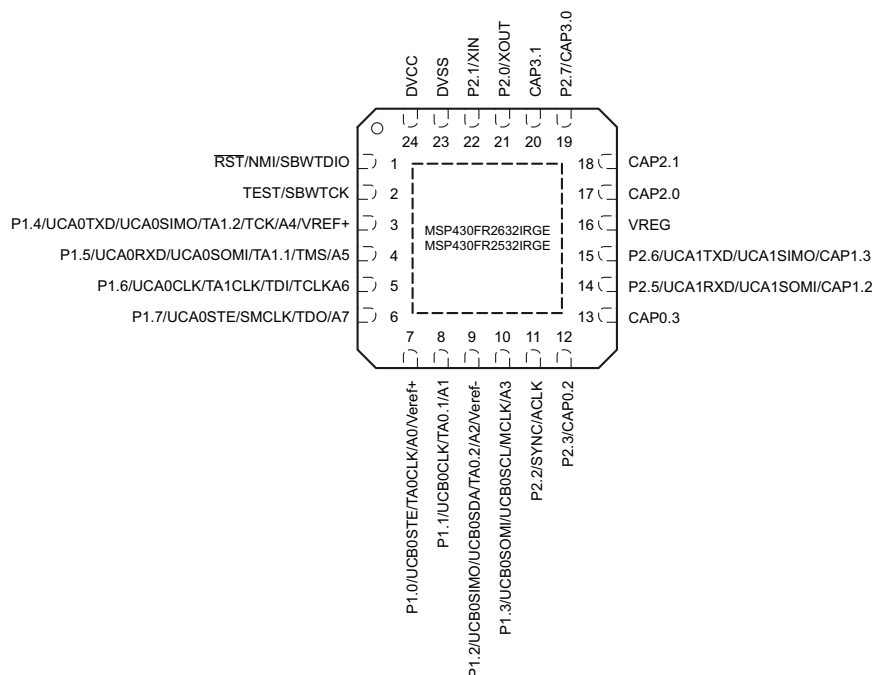


Figure 4-2. 32-Pin DA Package (Top View)



Figure 4-3 shows the pinout for the 24-pin RGE package.



**Figure 4-3. 24-Pin RGE Package (Top View)**

## 4.2 Pin Attributes

Table 4-1 lists the attributes of all pins.

**Table 4-1. Pin Attributes**

| PIN NUMBER |    |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6)</sup> |
|------------|----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| RHB        | DA | RGE |                                |                            |                            |                             |                                      |
| 1          | 5  | 1   | RST (RD)                       | I                          | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | NMI                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | SBWTDIO                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 2          | 6  | 2   | TEST (RD)                      | I                          | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | SBWTCK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
| 3          | 7  | 3   | P1.4 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA0TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCA0SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA1.2                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TCK                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A4                             | I                          | Analog                     | DVCC                        | –                                    |
|            |    |     | VREF+                          | O                          | Power                      | DVCC                        | –                                    |
| 4          | 8  | 4   | P1.5 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA0RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCA0SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA1.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TMS                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A5                             | I                          | Analog                     | DVCC                        | –                                    |
| 5          | 9  | 5   | P1.6 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA0CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA1CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TDI                            | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TCLK                           | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A6                             | I                          | Analog                     | DVCC                        | –                                    |
| 6          | 10 | 6   | P1.7 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA0STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | SMCLK                          | O                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TDO                            | O                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A7                             | I                          | Analog                     | DVCC                        | –                                    |
| 7          | 11 | 7   | P1.0 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCB0STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA0CLK                         | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A0                             | I                          | Analog                     | DVCC                        | –                                    |
|            |    |     | Veref+                         | I                          | Power                      | DVCC                        | –                                    |

(1) Signals names with (RD) denote the reset default pin name.

(2) To determine the pin mux encodings for each pin, see Section 6.11, *Input/Output Schematics*.

(3) Signal Types: I = Input, O = Output, I/O = Input or Output

(4) Buffer Types: LVC MOS, Analog, or Power (see Table 4-3)

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled

N/A = Not applicable

**Table 4-1. Pin Attributes (continued)**

| PIN NUMBER |    |     | SIGNAL NAME <sup>(1) (2)</sup> | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6)</sup> |
|------------|----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| RHB        | DA | RGE |                                |                            |                            |                             |                                      |
| 8          | 12 | 8   | P1.1 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCB0CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA0.1                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A1                             | I                          | Analog                     | DVCC                        | –                                    |
| 9          | 13 | 9   | P1.2 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCB0SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCB0SDA                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | TA0.2                          | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A2                             | I                          | Analog                     | DVCC                        | –                                    |
|            |    |     | Veref-                         | I                          | Power                      | DVCC                        | –                                    |
| 10         | 14 | 10  | P1.3 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCB0SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCB0SCL                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | MCLK                           | O                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | A3                             | I                          | Analog                     | DVCC                        | –                                    |
| 11         | 15 | 11  | P2.2 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | SYNC                           | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | ACLK                           | I/O                        | LVC MOS                    | DVCC                        | –                                    |
| 12         | 16 |     | P3.0 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | CAP0.0                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 13         | 17 |     | CAP0.1                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 14         | 18 | 12  | P2.3 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | CAP0.2                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 15         | 19 | 13  | CAP0.3                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 16         | 20 |     | P3.1 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA1STE                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | CAP1.0                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 17         | 21 |     | P2.4 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA1CLK                        | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | CAP1.1                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 18         | 22 | 14  | P2.5 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA1RXD                        | I                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCA1SOMI                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | CAP1.2                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 19         | 23 | 15  | P2.6 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | UCA1TXD                        | O                          | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | UCA1SIMO                       | I/O                        | LVC MOS                    | DVCC                        | –                                    |
|            |    |     | CAP1.3                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 20         | 24 | 16  | VREG                           | P                          | Power                      | V <sub>REG</sub>            | N/A                                  |
| 21         | 25 | 17  | CAP2.0                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 22         | 26 | 18  | CAP2.1                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 23         | 27 |     | CAP2.2                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 24         | 28 |     | CAP2.3                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 25         | 29 | 19  | P2.7 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | CAP3.0                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 26         | 30 | 20  | CAP3.1                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |

Table 4-1. Pin Attributes (continued)

| PIN NUMBER |    |     | SIGNAL NAME <sup>(1)</sup> (2) | SIGNAL TYPE <sup>(3)</sup> | BUFFER TYPE <sup>(4)</sup> | POWER SOURCE <sup>(5)</sup> | RESET STATE AFTER BOR <sup>(6)</sup> |
|------------|----|-----|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| RHB        | DA | RGE |                                |                            |                            |                             |                                      |
| 27         | 31 |     | P3.2 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | CAP3.2                         | I/O                        | Analog                     | V <sub>REG</sub>            | –                                    |
| 28         | 32 |     | CAP3.3                         | I/O                        | Analog                     | V <sub>REG</sub>            | OFF                                  |
| 29         | 1  | 21  | P2.0 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | XOUT                           | O                          | LVC MOS                    | DVCC                        | –                                    |
| 30         | 2  | 22  | P2.1 (RD)                      | I/O                        | LVC MOS                    | DVCC                        | OFF                                  |
|            |    |     | XIN                            | I                          | LVC MOS                    | DVCC                        | –                                    |
| 31         | 3  | 23  | DVSS                           | P                          | Power                      | DVCC                        | N/A                                  |
| 32         | 4  | 24  | DVCC                           | P                          | Power                      | DVCC                        | N/A                                  |

### 4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

**Table 4-2. Signal Descriptions**

| FUNCTION  | SIGNAL NAME | PIN NUMBER |    |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----------|-------------|------------|----|-----|-------------------------|---|
|           |             | RHB        | DA | RGE |                         |   |
| ADC       | A0          | 7          | 11 | 7   | I                       | Analog input A0   |
|           | A1          | 8          | 12 | 8   | I                       | Analog input A1   |
|           | A2          | 9          | 13 | 9   | I                       | Analog input A2   |
|           | A3          | 10         | 14 | 10  | I                       | Analog input A3   |
|           | A4          | 3          | 7  | 3   | I                       | Analog input A4   |
|           | A5          | 4          | 8  | 4   | I                       | Analog input A5   |
|           | A6          | 5          | 9  | 5   | I                       | Analog input A6   |
|           | A7          | 6          | 10 | 6   | I                       | Analog input A7   |
|           | Veref+      | 7          | 11 | 7   | I                       | ADC positive reference  |
|           | Veref-      | 9          | 13 | 9   | I                       | ADC negative reference  |
| CapTlvate | CAP0.0      | 12         | 16 |     | I/O                     | CapTlvate channel   |
|           | CAP0.1      | 13         | 17 |     | I/O                     | CapTlvate channel   |
|           | CAP0.2      | 14         | 18 | 12  | I/O                     | CapTlvate channel   |
|           | CAP0.3      | 15         | 19 | 13  | I/O                     | CapTlvate channel   |
|           | CAP1.0      | 16         | 20 |     | I/O                     | CapTlvate channel   |
|           | CAP1.1      | 17         | 21 |     | I/O                     | CapTlvate channel   |
|           | CAP1.2      | 18         | 22 | 14  | I/O                     | CapTlvate channel   |
|           | CAP1.3      | 19         | 23 | 15  | I/O                     | CapTlvate channel   |
|           | CAP2.0      | 21         | 25 | 17  | I/O                     | CapTlvate channel   |
|           | CAP2.1      | 22         | 26 | 18  | I/O                     | CapTlvate channel   |
|           | CAP2.2      | 23         | 27 |     | I/O                     | CapTlvate channel   |
|           | CAP2.3      | 24         | 28 |     | I/O                     | CapTlvate channel   |
|           | CAP3.0      | 25         | 29 | 19  | I/O                     | CapTlvate channel   |
|           | CAP3.1      | 26         | 30 | 20  | I/O                     | CapTlvate channel   |
|           | CAP3.2      | 27         | 31 |     | I/O                     | CapTlvate channel   |
|           | CAP3.3      | 28         | 32 |     | I/O                     | CapTlvate channel   |
|           | SYNC        | 11         | 15 | 11  | I                       | CapTlvate synchronous trigger input for processing and conversion |
| Clock     | ACLK        | 11         | 15 | 11  | I/O                     | ACLK output   |
|           | MCLK        | 10         | 14 | 10  | O                       | MCLK output   |
|           | SMCLK       | 6          | 10 | 6   | O                       | SMCLK output  |
|           | XIN         | 30         | 2  | 22  | I                       | Input terminal for crystal oscillator                             |
|           | XOUT        | 29         | 1  | 21  | O                       | Output terminal for crystal oscillator                            |
| Debug     | SBWTCK      | 2          | 6  | 2   | I                       | Spy-Bi-Wire input clock   |
|           | SBWTDIO     | 1          | 5  | 1   | I/O                     | Spy-Bi-Wire data input/output                                     |
|           | TCK         | 3          | 7  | 3   | I                       | Test clock  |
|           | TCLK        | 5          | 9  | 5   | I                       | Test clock input  |
|           | TDI         | 5          | 9  | 5   | I                       | Test data input   |
|           | TDO         | 6          | 10 | 6   | O                       | Test data output  |
|           | TEST        | 2          | 6  | 2   | I                       | Test Mode pin – selected digital I/O on JTAG pins                 |
|           | TMS         | 4          | 8  | 4   | I                       | Test mode select  |

(1) Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

Table 4-2. Signal Descriptions (continued)

| FUNCTION         | SIGNAL NAME | PIN NUMBER |    |     | PIN TYPE <sup>(1)</sup>        | DESCRIPTION   |
|------------------|-------------|------------|----|-----|--------------------------------|---|
|                  |             | RHB        | DA | RGE |                                |   |
| GPIO             | P1.0        | 7          | 11 | 7   | I/O                            | General-purpose I/O   |
|                  | P1.1        | 8          | 12 | 8   | I/O                            | General-purpose I/O   |
|                  | P1.2        | 9          | 13 | 9   | I/O                            | General-purpose I/O   |
|                  | P1.3        | 10         | 14 | 10  | I/O                            | General-purpose I/O   |
|                  | P1.4        | 3          | 7  | 3   | I/O                            | General-purpose I/O <sup>(2)</sup>                            |
|                  | P1.5        | 4          | 8  | 4   | I/O                            | General-purpose I/O <sup>(2)</sup>                            |
|                  | P1.6        | 5          | 9  | 5   | I/O                            | General-purpose I/O <sup>(2)</sup>                            |
|                  | P1.7        | 6          | 10 | 6   | I/O                            | General-purpose I/O <sup>(2)</sup>                            |
|                  | P2.0        | 29         | 1  | 21  | I/O                            | General-purpose I/O   |
|                  | P2.1        | 30         | 2  | 22  | I/O                            | General-purpose I/O   |
|                  | P2.2        | 11         | 15 | 11  | I/O                            | General-purpose I/O   |
|                  | P2.3        | 14         | 18 | 12  | I/O                            | General-purpose I/O   |
|                  | P2.4        | 17         | 21 |     | I/O                            | General-purpose I/O   |
|                  | P2.5        | 18         | 22 | 14  | I/O                            | General-purpose I/O   |
|                  | P2.6        | 19         | 23 | 15  | I/O                            | General-purpose I/O   |
|                  | P2.7        | 25         | 29 | 19  | I/O                            | General-purpose I/O   |
|                  | P3.0        | 12         | 16 |     | I/O                            | General-purpose I/O   |
|                  | P3.1        | 16         | 20 |     | I/O                            | General-purpose I/O   |
| P3.2             | 27          | 31         |    | I/O | General-purpose I/O            |   |
| I <sup>2</sup> C | UCB0SCL     | 10         | 14 | 10  | I/O                            | eUSCI_B0 I <sup>2</sup> C clock                               |
|                  | UCB0SDA     | 9          | 13 | 9   | I/O                            | eUSCI_B0 I <sup>2</sup> C data                                |
| Power            | DVCC        | 32         | 4  | 24  | P                              | Power supply  |
|                  | DVSS        | 31         | 3  | 23  | P                              | Power ground  |
|                  | VREF+       | 3          | 7  | 3   | P                              | Output of positive reference voltage with ground as reference |
|                  | VREG        | 20         | 24 | 16  | O                              | CapTIvate regulator external decoupling capacitor             |
| SPI              | UCA0CLK     | 5          | 9  | 5   | I/O                            | eUSCI_A0 SPI clock input/output                               |
|                  | UCA0SIMO    | 3          | 7  | 3   | I/O                            | eUSCI_A0 SPI slave in/master out                              |
|                  | UCA0SOMI    | 4          | 8  | 4   | I/O                            | eUSCI_A0 SPI slave out/master in                              |
|                  | UCA0STE     | 6          | 10 | 6   | I/O                            | eUSCI_A0 SPI slave transmit enable                            |
|                  | UCA1CLK     | 17         | 21 |     | I/O                            | eUSCI_A1 SPI clock input/output                               |
|                  | UCA1SIMO    | 19         | 23 | 15  | I/O                            | eUSCI_A1 SPI slave in/master out                              |
|                  | UCA1SOMI    | 18         | 22 | 14  | I/O                            | eUSCI_A1 SPI slave out/master in                              |
|                  | UCA1STE     | 16         | 20 |     | I/O                            | eUSCI_A1 SPI slave transmit enable                            |
|                  | UCB0CLK     | 8          | 12 | 8   | I/O                            | eUSCI_B0 clock input/output                                   |
|                  | UCB0SIMO    | 9          | 13 | 9   | I/O                            | eUSCI_B0 SPI slave in/master out                              |
|                  | UCB0SOMI    | 10         | 14 | 10  | I/O                            | eUSCI_B0 SPI slave out/master in                              |
| UCB0STE          | 7           | 11         | 7  | I/O | eUSCI_B0 slave transmit enable |   |
| System           | NMI         | 1          | 5  | 1   | I                              | Nonmaskable interrupt input                                   |
|                  | RST         | 1          | 5  | 1   | I                              | Active-low reset input  |

(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

**Table 4-2. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NUMBER |    |     | PIN TYPE <sup>(1)</sup> | DESCRIPTION  |
|----------|-------------|------------|----|-----|-------------------------|--|
|          |             | RHB        | DA | RGE |                         |  |
| Timer_A  | TA0.1       | 8          | 12 | 8   | I/O                     | Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs |
|          | TA0.2       | 9          | 13 | 9   | I/O                     | Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs |
|          | TA0CLK      | 7          | 11 | 7   | I                       | Timer clock input TACLK for TA0                            |
|          | TA1.1       | 4          | 8  | 4   | I/O                     | Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs |
|          | TA1.2       | 3          | 7  | 3   | I/O                     | Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs |
|          | TA1CLK      | 5          | 9  | 5   | I                       | Timer clock input TACLK for TA1                            |
| UART     | UCA0RXD     | 4          | 8  | 4   | I                       | eUSCI_A0 UART receive data                                 |
|          | UCA0TXD     | 3          | 7  | 3   | O                       | eUSCI_A0 UART transmit data                                |
|          | UCA1RXD     | 18         | 22 | 14  | I                       | eUSCI_A1 UART receive data                                 |
|          | UCA1TXD     | 19         | 23 | 15  | O                       | eUSCI_A1 UART transmit data                                |

## 4.4 Pin Multiplexing

Pin multiplexing for these MCUs is controlled by both register settings and operating modes (for example, if the MCU is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 6.11](#).

## 4.5 Buffer Types

[Table 4-3](#) defines the pin buffer types that are listed in [Table 4-1](#).

**Table 4-3. Buffer Types**

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS       | PU OR PD     | NOMINAL PU OR PD STRENGTH ( $\mu$ A) | OUTPUT DRIVE STRENGTH (mA)         | OTHER CHARACTERISTICS  |
|------------------------|-----------------|------------------|--------------|--------------------------------------|------------------------------------|--|
| LVC MOS                | 3.0 V           | Y <sup>(1)</sup> | Programmable | See <a href="#">Section 5.11.4</a>   | See <a href="#">Section 5.11.4</a> |  |
| Analog                 | 3.0 V           | N                | N/A          | N/A                                  | N/A                                | See analog modules in <a href="#">Section 5</a> for details. |
| Power (DVCC)           | 3.0 V           | N                | N/A          | N/A                                  | N/A                                | SVS enables hysteresis on DVCC.                              |
| Power (AVCC)           | 3.0 V           | N                | N/A          | N/A                                  | N/A                                |  |

(1) Only for input pins.

## 4.6 Connection of Unused Pins

[Table 4-4](#) lists the correct termination of unused pins.

**Table 4-4. Connection of Unused Pins<sup>(1)</sup>**

| PIN                                | POTENTIAL        | COMMENT  |
|------------------------------------|------------------|--|
| Px.0 to Px.7                       | Open             | Switched to port function, output direction (PxDIR.n = 1)  |
| $\overline{\text{RST}}/\text{NMI}$ | DV <sub>CC</sub> | 47-k $\Omega$ pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown <sup>(2)</sup>      |
| TEST                               | Open             | This pin always has an internal pulldown enabled.  |
| CAP2.x, CAPx.1, CAPx.3             | Open             | These pins have internal pullup and pulldown resistors, and high impedance is their default setting. |

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.

(2) The pulldown capacitor should not exceed 1.1 nF when using MCUs with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.



## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|  | MIN  | MAX                                  | UNIT |
|--|------|--------------------------------------|------|
| Voltage applied at DVCC pin to V <sub>SS</sub>   | -0.3 | 4.1                                  | V    |
| Voltage applied to any dedicated CapTIvate pin or pin in CapTIvate mode <sup>(2)</sup> | -0.3 | V <sub>REG</sub>                     | V    |
| Voltage applied to any other pin <sup>(3)</sup>  | -0.3 | V <sub>CC</sub> + 0.3<br>(4.1 V Max) | V    |
| Diode current at any device pin  |      | ±2                                   | mA   |
| Maximum junction temperature, T <sub>J</sub>   |      | 85                                   | °C   |
| Storage temperature, T <sub>stg</sub> <sup>(4)(5)</sup>                                | -40  | 125                                  | °C   |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- This applies to dedicated CapTIvate I/Os only or I/Os worked in CapTIvate mode.
- All voltages referenced to V<sub>SS</sub>.
- Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
- Data retention on FRAM cannot be ensured when exceeding the specified maximum storage temperature, T<sub>stg</sub>. Therefore, programming of devices with user application code should only be performed after soldering.

### 5.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

### 5.3 Recommended Operating Conditions

|                        |  | MIN  | NOM | MAX               | UNIT |
|------------------------|--|--|-----|-------------------|------|
| V <sub>CC</sub>        | Supply voltage applied at DVCC pin <sup>(1)(2)(3)</sup>                | 1.8  |     | 3.6               | V    |
| V <sub>SS</sub>        | Supply voltage applied at DVSS pin                                     |  | 0   |                   | V    |
| T <sub>A</sub>         | Operating free-air temperature   | -40  |     | 85                | °C   |
| T <sub>J</sub>         | Operating junction temperature   | -40  |     | 85                | °C   |
| C <sub>DVCC</sub>      | Recommended capacitor at DVCC <sup>(4)</sup>                           | 4.7  | 10  |                   | µF   |
| C <sub>REG</sub>       | External buffer capacitor, ESR ≤ 200 mΩ                                | 0.8  | 1   | 1.2               | µF   |
| C <sub>ELECTRODE</sub> | Maximum capacitance of all external electrodes on all CapTIvate blocks |  |     | 300               | pF   |
| f <sub>SYSTEM</sub>    | Processor frequency (maximum MCLK frequency) <sup>(3)(5)</sup>         | No FRAM wait states (NWAITS <sub>x</sub> = 0)                  |     | 8                 | MHz  |
|                        |  | With FRAM wait states (NWAITS <sub>x</sub> = 1) <sup>(6)</sup> |     | 16 <sup>(7)</sup> |      |
| f <sub>ACLK</sub>      | Maximum ACLK frequency   |  |     | 40                | kHz  |
| f <sub>SMCLK</sub>     | Maximum SMCLK frequency  |  |     | 16 <sup>(7)</sup> | MHz  |

- Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range.
- Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- The minimum supply voltage is defined by the SVS levels. Refer to the SVS threshold parameters in [Table 5-2](#).
- A capacitor tolerance of ±20% or better is required.
- Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
- If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

See <sup>(1)</sup>

| PARAMETER             | EXECUTION MEMORY             | TEST CONDITION | FREQUENCY ( $f_{MCLK} = f_{SMCLK}$ )                |     |   |     |   |      | UNIT    |
|-----------------------|------------------------------|----------------|---|-----|---|-----|---|------|---------|
|                       |                              |                | 1 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 8 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 16 MHz<br>1 WAIT STATE<br>(NWAITS <sub>x</sub> = 1) |      |         |
|                       |                              |                | TYP   | MAX | TYP   | MAX | TYP   | MAX  |         |
| $I_{AM, FRAM(0\%)}$   | FRAM<br>0% cache hit ratio   | 3 V, 25°C      | 504   |     | 2772  |     | 3047  | 3480 | $\mu A$ |
|                       |                              | 3 V, 85°C      | 516   |     | 2491  |     | 2871  |      |         |
| $I_{AM, FRAM(100\%)}$ | FRAM<br>100% cache hit ratio | 3 V, 25°C      | 203   |     | 625   |     | 1000  | 1215 | $\mu A$ |
|                       |                              | 3 V, 85°C      | 212   |     | 639   |     | 1016  |      |         |
| $I_{AM, RAM}^{(2)}$   | RAM                          | 3 V, 25°C      | 229   |     | 818   |     | 1377  |      | $\mu A$ |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current. Characterized with program executing typical data processing.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = f_{SMCLK} = f_{DCO}$  at specified frequency

Program and data entirely reside in FRAM. All execution is from FRAM.

(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

## 5.5 Active Mode Supply Current Per MHz

 $V_{CC} = 3$  V,  $T_A = 25^\circ C$  (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS  | TYP  | UNIT               |
|-------------------|--|--|--------------------|
| $dI_{AM,FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states | $I_{AM}$ (75% cache hit rate) at 8 MHz –<br>$I_{AM}$ (75% cache hit rate) at 1 MHz / 7 MHz | 126<br>$\mu A/MHz$ |

## 5.6 Low-Power Mode LPM0 Supply Currents Into $V_{CC}$ Excluding External Current

 $V_{CC} = 3$  V,  $T_A = 25^\circ C$  (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER  | $V_{CC}$ | FREQUENCY ( $f_{SMCLK}$ ) |     |       |     |        |     | UNIT    |
|------------|----------|---------------------------|-----|-------|-----|--------|-----|---------|
|            |          | 1 MHz                     |     | 8 MHz |     | 16 MHz |     |         |
|            |          | TYP                       | MAX | TYP   | MAX | TYP    | MAX |         |
| $I_{LPM0}$ | 2 V      | 156                       |     | 328   |     | 420    |     | $\mu A$ |
|            | 3 V      | 166                       |     | 342   |     | 433    |     |         |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$  Hz,  $f_{MCLK} = 0$  MHz,  $f_{SMCLK}$  at specified frequency.

## 5.7 Low-Power Mode LPM3 Supply Currents (Into $V_{CC}$ ) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER  | $V_{CC}$ | -40°C |     | 25°C  |      | 85°C |     | UNIT    |
|--|----------|-------|-----|-------|------|------|-----|---------|
|  |          | TYP   | MAX | TYP   | MAX  | TYP  | MAX |         |
| $I_{LPM3,XT1}$ Low-power mode 3, 12.5-pF crystal, includes SVS <sup>(2)(3)(4)</sup>                        | 3 V      | 0.98  |     | 1.18  | 1.65 | 3.24 |     | $\mu$ A |
|  | 2 V      | 0.96  |     | 1.16  |      | 3.21 |     |         |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS <sup>(5)</sup>  | 3 V      | 0.78  |     | 0.98  | 1.40 | 3.04 |     | $\mu$ A |
|  | 2 V      | 0.76  |     | 0.96  |      | 3.01 |     |         |
| $I_{LPM3,RTC}$ Low-power mode 3, RTC, excludes SVS <sup>(6)</sup>  | 3 V      | 0.93  |     | 1.13  |      | 3.19 |     | $\mu$ A |
| $I_{LPM3, CapTlvate, 1 proximity, wake on touch}$ Low-power mode 3, CapTlvate, excludes SVS <sup>(7)</sup> | 3.3 V    |       |     | 5     |      |      |     | $\mu$ A |
| $I_{LPM3, CapTlvate, 1 button, wake on touch}$ Low-power mode 3, CapTlvate, excludes SVS <sup>(8)</sup>    | 3.3 V    |       |     | 3.4   |      |      |     | $\mu$ A |
| $I_{LPM3, CapTlvate, 4 button, wake on touch}$ Low-power mode 3, CapTlvate, excludes SVS <sup>(9)</sup>    | 3.3 V    |       |     | 3.6   |      |      |     | $\mu$ A |
| $I_{LPM3, CapTlvate, 16 button}$ Low-power mode 3, CapTlvate, excludes SVS <sup>(10)</sup>                 | 3.3 V    |       |     | 27.2  |      |      |     | $\mu$ A |
| $I_{LPM3, CapTlvate, 64 button}$ Low-power mode 3, CapTlvate, excludes SVS <sup>(11)</sup>                 | 3.3 V    |       |     | 109.2 |      |      |     | $\mu$ A |
| $I_{LPM4,SVS}$ Low-power mode 4, includes SVS  | 3 V      | 0.51  |     | 0.65  |      | 2.65 |     | $\mu$ A |
|  | 2 V      | 0.49  |     | 0.64  |      | 2.63 |     |         |
| $I_{LPM4}$ Low-power mode 4, excludes SVS  | 3 V      | 0.35  |     | 0.49  |      | 2.49 |     | $\mu$ A |
|  | 2 V      | 0.34  |     | 0.48  |      | 2.46 |     |         |

(1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current.

(2) Not applicable for MCUs with HF crystal oscillator only.

(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.

(4) Low-power mode 3, 12.5-pF crystal, includes SVS test conditions:

Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz

(5) Low-power mode 3, VLO, excludes SVS test conditions:

Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3)

$f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz

(6) RTC periodically wakes up every second with external 32768-Hz input as source.

(7) CapTlvate technology works in LPM3 with one proximity sensor for wake on touch. CapTlvate BSWP demo panel with 1.5-mm overlay.

Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 800

(8) CapTlvate technology works in LPM3 with one button, wake on touch. CapTlvate BSWP demo panel with 1.5-mm overlay, Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250

(9) CapTlvate technology works in LPM3 with four self-capacitance buttons, wake on touch. CapTlvate BSWP demo panel with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250

(10) CapTlvate technology works in LPM3 with 16 self-capacitance buttons, process only, CapTlvate BSWP demo panel with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250.

(11) CapTlvate technology works in LPM3 with 64 mutual-capacitance buttons, process only. CapTlvate BSWP demo panel with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250.

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250.

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250.

(11) CapTlvate technology works in LPM3 with 64 mutual-capacitance buttons, process only. CapTlvate BSWP demo panel with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$  Hz,  $f_{CONVER} = 2$  MHz, COUNTS = 250.

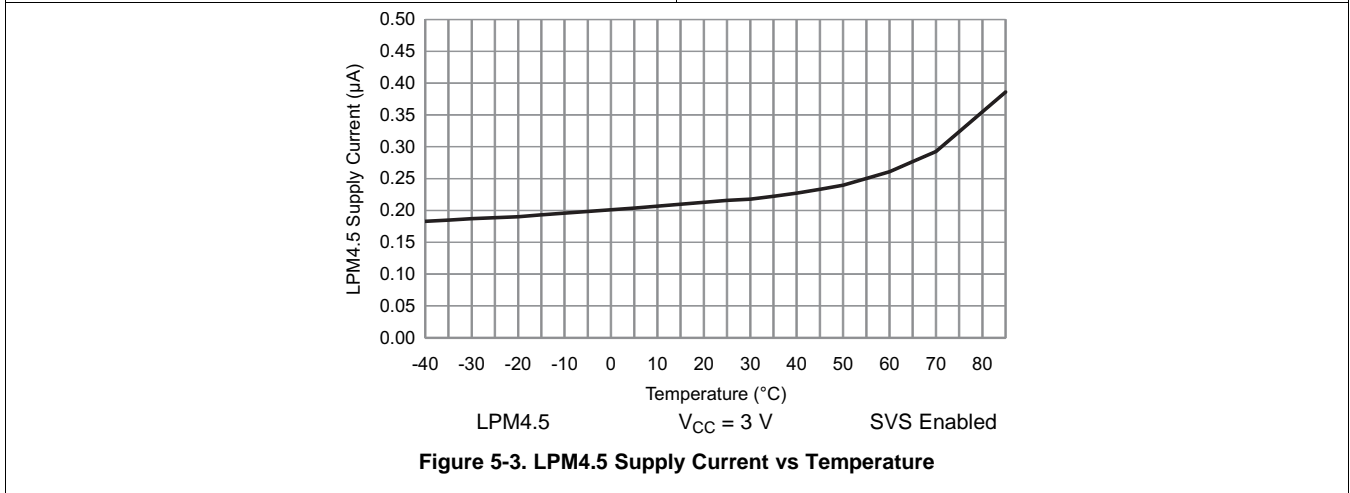
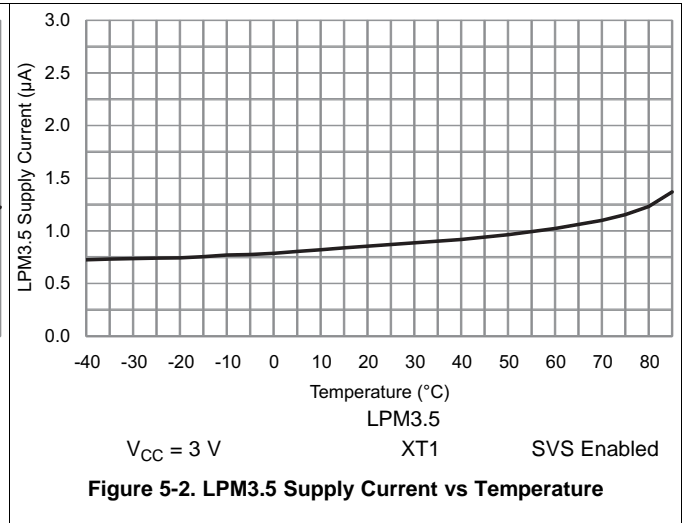
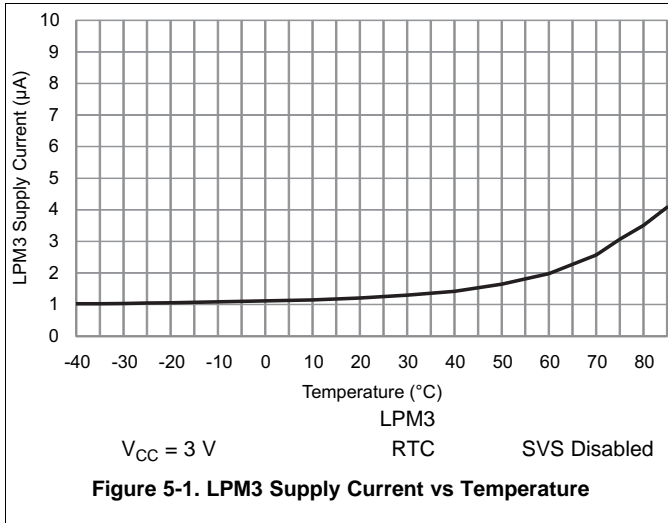
## 5.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER         |  | $V_{CC}$ | -40°C |     | 25°C  |       | 85°C  |       | UNIT          |
|-------------------|--|----------|-------|-----|-------|-------|-------|-------|---------------|
|                   |  |          | TYP   | MAX | TYP   | MAX   | TYP   | MAX   |               |
| $I_{LPM3.5, XT1}$ | Low-power mode 3.5, 12.5-pF crystal, includes SVS <sup>(1)(2)(3)</sup><br>(also see <a href="#">Figure 5-2</a> ) | 3 V      | 0.65  |     | 0.73  | 0.95  | 0.99  | 1.42  | $\mu\text{A}$ |
|                   |  | 2 V      | 0.63  |     | 0.71  |       | 0.87  |       |               |
| $I_{LPM4.5, SVS}$ | Low-power mode 4.5, includes SVS <sup>(4)</sup>  | 3 V      | 0.22  |     | 0.24  | 0.31  | 0.30  | 0.38  | $\mu\text{A}$ |
|                   |  | 2 V      | 0.21  |     | 0.23  |       | 0.28  |       |               |
| $I_{LPM4.5}$      | Low-power mode 4.5, excludes SVS <sup>(5)</sup>  | 3 V      | 0.012 |     | 0.016 | 0.055 | 0.061 | 0.120 | $\mu\text{A}$ |
|                   |  | 2 V      | 0.002 |     | 0.007 |       | 0.044 |       |               |

- (1) Not applicable for MCUs with HF crystal oscillator only.
- (2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5-pF load.
- (3) Low-power mode 3.5, 12.5-pF crystal, includes SVS test conditions:  
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),  
 $f_{XT1} = 32768 \text{ Hz}$ ,  $f_{ACLK} = 0$ ,  $f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$
- (4) Low-power mode 4.5, includes SVS test conditions:  
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)  
 $f_{XT1} = 0 \text{ Hz}$ ,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$
- (5) Low-power mode 4.5, excludes SVS test conditions:  
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.  
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)  
 $f_{XT1} = 0 \text{ Hz}$ ,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}$

### 5.9 Typical Characteristics - Low-Power Mode Supply Currents



**Table 5-1. Typical Characteristics – Current Consumption Per Module**

| MODULE  | TEST CONDITIONS                  | REFERENCE CLOCK    | MIN | TYP | MAX | UNIT   |
|---------|----------------------------------|--------------------|-----|-----|-----|--------|
| Timer_A |                                  | Module input clock |     | 5   |     | μA/MHz |
| eUSCI_A | UART mode                        | Module input clock |     | 7   |     | μA/MHz |
| eUSCI_A | SPI mode                         | Module input clock |     | 5   |     | μA/MHz |
| eUSCI_B | SPI mode                         | Module input clock |     | 5   |     | μA/MHz |
| eUSCI_B | I <sup>2</sup> C mode, 100 kbaud | Module input clock |     | 5   |     | μA/MHz |
| RTC     |                                  | 32 kHz             |     | 85  |     | nA     |
| CRC     | From start to end of operation   | MCLK               |     | 8.5 |     | μA/MHz |

## 5.10 Thermal Resistance Characteristics

|                 |  | VALUE             | UNIT |
|-----------------|--|-------------------|------|
| R $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air <sup>(1)</sup> | VQFN 32 pin (RHB) | 33.5 |
|                 |  | TSSOP 32 pin (DA) | 69.4 |
|                 |  | VQFN 24 pin (RGE) | 32.6 |
| R $\theta_{JC}$ | Junction-to-case (top) thermal resistance <sup>(2)</sup>         | VQFN 32 pin (RHB) | 25.7 |
|                 |  | TSSOP 32 pin (DA) | 18.1 |
|                 |  | VQFN 24 pin (RGE) | 32.4 |
| R $\theta_{JB}$ | Junction-to-board thermal resistance                             | VQFN 32 pin (RHB) | 7.6  |
|                 |  | TSSOP 32 pin (DA) | 33.1 |
|                 |  | VQFN 24 pin (RGE) | 10.1 |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold place test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## 5.11 Timing and Switching Characteristics

### 5.11.1 Power Supply Sequencing

**Table 5-2. PMM, SVS and BOR**

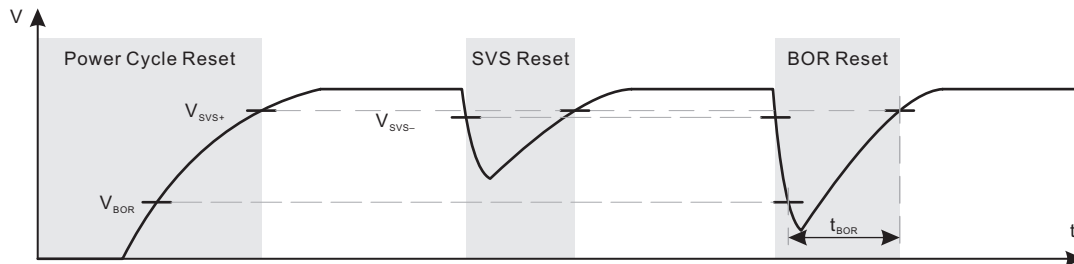
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS         | MIN   | TYP  | MAX   | UNIT          |
|---------------------|---|-------------------------|-------|------|-------|---------------|
| $V_{BOR, safe}$     | Safe BOR power-down level <sup>(1)</sup>              |                         | 0.1   |      |       | V             |
| $t_{BOR, safe}$     | Safe BOR reset delay <sup>(2)</sup>                   |                         | 10    |      |       | ms            |
| $I_{SVSH, AM}$      | SVS <sub>H</sub> current consumption, active mode     | $V_{CC} = 3.6\text{ V}$ |       |      | 1.5   | $\mu\text{A}$ |
| $I_{SVSH, LPM}$     | SVS <sub>H</sub> current consumption, low-power modes | $V_{CC} = 3.6\text{ V}$ |       | 240  |       | nA            |
| $V_{SVSH-}$         | SVS <sub>H</sub> power-down level                     |                         | 1.71  | 1.80 | 1.86  | V             |
| $V_{SVSH+}$         | SVS <sub>H</sub> power-up level                       |                         | 1.74  | 1.89 | 1.99  | V             |
| $V_{SVSH, hys}$     | SVS <sub>H</sub> hysteresis                           |                         |       | 80   |       | mV            |
| $t_{PD, SVSH, AM}$  | SVS <sub>H</sub> propagation delay, active mode       |                         |       |      | 10    | $\mu\text{s}$ |
| $t_{PD, SVSH, LPM}$ | SVS <sub>H</sub> propagation delay, low-power modes   |                         |       |      | 100   | $\mu\text{s}$ |
| $V_{REF, 1.2V}$     | 1.2-V REF voltage <sup>(3)</sup>                      |                         | 1.158 | 1.20 | 1.242 | V             |

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.

(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches  $V_{SVSH+}$ .

(3) This is a characterized result with external 1-mA load to ground from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



**Figure 5-4. Power Cycle, SVS, and BOR Reset Conditions**



### 5.11.2 Reset Timing

**Table 5-3. Wake-Up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |  | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX                             | UNIT |
|-----------------------------|--|-----------------|-----------------|-----|-----|---------------------------------|------|
| t <sub>WAKE-UP FRAM</sub>   | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup <sup>(1)</sup> |                 | 3 V             |     | 10  |                                 | μs   |
| t <sub>WAKE-UP LPM0</sub>   | Wake-up time from LPM0 to active mode <sup>(1)</sup>   |                 | 3 V             |     |     | 200 +<br>2.5 / f <sub>DCO</sub> | ns   |
| t <sub>WAKE-UP LPM3</sub>   | Wake-up time from LPM3 to active mode <sup>(2)</sup>   |                 | 3 V             |     | 10  |                                 | μs   |
| t <sub>WAKE-UP LPM4</sub>   | Wake-up time from LPM4 to active mode  |                 | 3 V             |     | 10  |                                 | μs   |
| t <sub>WAKE-UP LPM3.5</sub> | Wake-up time from LPM3.5 to active mode <sup>(2)</sup>   |                 | 3 V             |     | 350 |                                 | μs   |
| t <sub>WAKE-UP LPM4.5</sub> | Wake-up time from LPM4.5 to active mode <sup>(2)</sup>   | SVSHE = 1       | 3 V             |     | 350 |                                 | μs   |
|                             |  | SVSHE = 0       |                 |     | 1   |                                 | ms   |
| t <sub>WAKE-UP-RESET</sub>  | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode <sup>(2)</sup>   |                 | 3 V             |     | 1   |                                 | ms   |
| t <sub>RESET</sub>          | Pulse duration required at $\overline{\text{RST}}$ /NMI pin to accept a reset  |                 | 3 V             | 2   |     |                                 | μs   |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

### 5.11.3 Clock Specifications

**Table 5-4. XT1 Crystal Oscillator (Low Frequency)**

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                |  | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP    | MAX  | UNIT |
|--------------------------|--|---|-----------------|-----|--------|------|------|
| f <sub>XT1, LF</sub>     | XT1 oscillator crystal, low frequency                    | LFXTBYPASS = 0  |                 |     | 32768  |      | Hz   |
| DC <sub>XT1, LF</sub>    | XT1 oscillator LF duty cycle                             | Measured at MCLK,<br>f <sub>LFXT</sub> = 32768 Hz   |                 | 30% |        | 70%  |      |
| f <sub>XT1, SW</sub>     | XT1 oscillator logic-level square-wave input frequency   | LFXTBYPASS = 1 <sup>(2)(3)</sup>  |                 |     | 32.768 |      | kHz  |
| DC <sub>XT1, SW</sub>    | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1  |                 | 40% |        | 60%  |      |
| OA <sub>LFXT</sub>       | Oscillation allowance for LF crystals <sup>(4)</sup>     | LFXTBYPASS = 0, LFXTDRIVE = {3},<br>f <sub>LFXT</sub> = 32768 Hz, C <sub>L,eff</sub> = 12.5 pF                          |                 |     | 200    |      | kΩ   |
| C <sub>L,eff</sub>       | Integrated effective load capacitance <sup>(5)</sup>     | See <sup>(6)</sup>  |                 |     | 1      |      | pF   |
| t <sub>START, LFXT</sub> | Start-up time <sup>(7)</sup>                             | f <sub>OSC</sub> = 32768 Hz,<br>LFXTBYPASS = 0, LFXTDRIVE = {3},<br>T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12.5 pF |                 |     | 1000   |      | ms   |
| f <sub>FAULT, LFXT</sub> | Oscillator fault frequency <sup>(8)</sup>                | XTS = 0 <sup>(9)</sup>  |                 | 0   |        | 3500 | Hz   |

- (1) To improve EMI on the LFXT oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DC<sub>LFXT, SW</sub>.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, C<sub>L,eff</sub> = 3.7 pF
  - For LFXTDRIVE = {1}, 6 pF ≤ C<sub>L,eff</sub> ≤ 9 pF
  - For LFXTDRIVE = {2}, 6 pF ≤ C<sub>L,eff</sub> ≤ 10 pF
  - For LFXTDRIVE = {3}, 6 pF ≤ C<sub>L,eff</sub> ≤ 12 pF
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Includes start-up counter of 1024 clock cycles.
- (8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.
- (9) Measured with logic-level input frequency but also applies to operation with crystals.

**Table 5-5. DCO FLL, Frequency**

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER              |   | TEST CONDITIONS                                      | V <sub>CC</sub> | MIN   | TYP    | MAX  | UNIT |
|------------------------|---|--|-----------------|-------|--------|------|------|
| f <sub>DCO, FLL</sub>  | FLL lock frequency, 16 MHz, 25°C          | Measured at MCLK, Internal trimmed REFO as reference | 3 V             | -1.0% |        | 1.0% |      |
|                        | FLL lock frequency, 16 MHz, -40°C to 85°C | Measured at MCLK, Internal trimmed REFO as reference | 3 V             | -2.0% |        | 2.0% |      |
|                        | FLL lock frequency, 16 MHz, -40°C to 85°C | Measured at MCLK, XT1 crystal as reference           | 3 V             | -0.5% |        | 0.5% |      |
| f <sub>DUTY</sub>      | Duty cycle                                |  | 3 V             | 40%   | 50%    | 60%  |      |
| Jitter <sub>CC</sub>   | Cycle-to-cycle jitter, 16 MHz             | Measured at MCLK, XT1 crystal as reference           | 3 V             |       | 0.25%  |      |      |
| Jitter <sub>long</sub> | Long term jitter, 16 MHz                  |  | 3 V             |       | 0.022% |      |      |
| t <sub>FLL, lock</sub> | FLL lock time                             |  | 3 V             |       | 280    |      | ms   |
| t <sub>start-up</sub>  | DCO start-up time, 2 MHz                  | Measured at MCLK                                     | 3 V             |       | 16     |      | μs   |

**Table 5-6. DCO Frequency**

 over recommended operating free-air temperature (unless otherwise noted) (see [Figure 5-5](#))

| PARAMETER                                     | TEST CONDITIONS   | V <sub>CC</sub> | TYP    | UNIT |
|---|---|-----------------|--------|------|
| f <sub>DCO, 16MHz</sub> DCO frequency, 16 MHz | DCORSEL = 101b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 7.46   | MHz  |
|   | DCORSEL = 101b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 12.26  |      |
|   | DCORSEL = 101b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 17.93  |      |
|   | DCORSEL = 101b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 29.1   |      |
| f <sub>DCO, 12MHz</sub> DCO frequency, 12 MHz | DCORSEL = 100b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 5.75   | MHz  |
|   | DCORSEL = 100b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 9.5    |      |
|   | DCORSEL = 100b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 13.85  |      |
|   | DCORSEL = 100b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 22.5   |      |
| f <sub>DCO, 8MHz</sub> DCO frequency, 8 MHz   | DCORSEL = 011b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 3.91   | MHz  |
|   | DCORSEL = 011b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 6.49   |      |
|   | DCORSEL = 011b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 9.5    |      |
|   | DCORSEL = 011b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 15.6   |      |
| f <sub>DCO, 4MHz</sub> DCO frequency, 4 MHz   | DCORSEL = 010b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 2.026  | MHz  |
|   | DCORSEL = 010b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 3.407  |      |
|   | DCORSEL = 010b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 4.95   |      |
|   | DCORSEL = 010b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 8.26   |      |
| f <sub>DCO, 2MHz</sub> DCO frequency, 2 MHz   | DCORSEL = 001b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 1.0225 | MHz  |
|   | DCORSEL = 001b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 1.729  |      |
|   | DCORSEL = 001b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 2.525  |      |
|   | DCORSEL = 001b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 4.25   |      |
| f <sub>DCO, 1MHz</sub> DCO frequency, 1 MHz   | DCORSEL = 000b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 0   | 3 V             | 0.5319 | MHz  |
|   | DCORSEL = 000b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 |                 | 0.9029 |      |
|   | DCORSEL = 000b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 0   |                 | 1.307  |      |
|   | DCORSEL = 000b, DISMOD = 1b, DCOFRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 |                 | 2.21   |      |

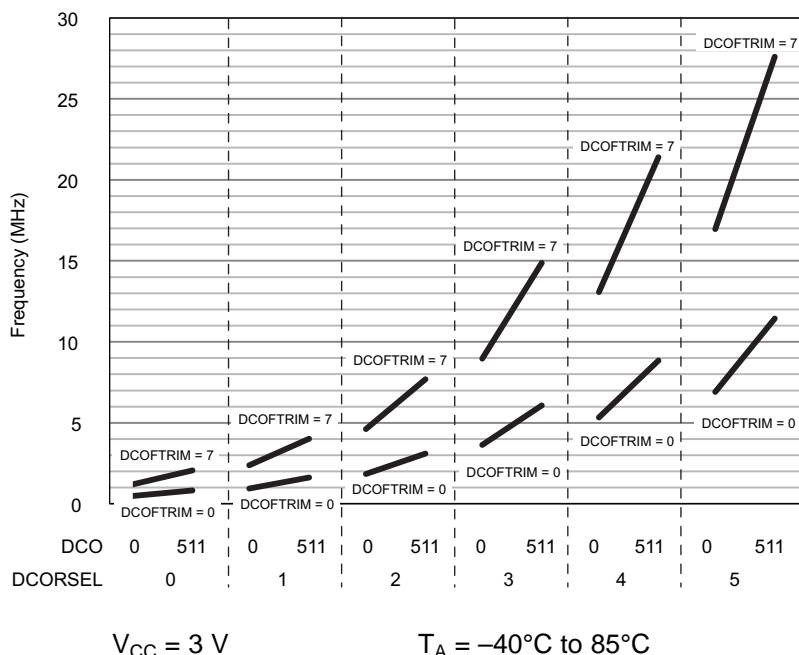


Figure 5-5. Typical DCO Frequency

Table 5-7. REFO

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER                            |                                     | TEST CONDITIONS                         | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|--------------------------------------|-------------------------------------|---|-----------------|-------|-------|-------|------|
| I <sub>REFO</sub>                    | REFO oscillator current consumption | T <sub>A</sub> = 25°C                   | 3 V             |       | 15    |       | μA   |
| f <sub>REFO</sub>                    | REFO calibrated frequency           | Measured at MCLK                        | 3 V             |       | 32768 |       | Hz   |
|                                      | REFO absolute calibrated tolerance  | -40°C to 85°C                           | 1.8 V to 3.6 V  | -3.5% |       | +3.5% |      |
| df <sub>REFO</sub> /dT               | REFO frequency temperature drift    | Measured at MCLK <sup>(1)</sup>         | 3 V             |       | 0.01  |       | %/°C |
| df <sub>REFO</sub> /dV <sub>CC</sub> | REFO frequency supply voltage drift | Measured at MCLK at 25°C <sup>(2)</sup> | 1.8 V to 3.6 V  |       | 1     |       | %/V  |
| f <sub>DC</sub>                      | REFO duty cycle                     | Measured at MCLK                        | 1.8 V to 3.6 V  | 40%   | 50%   | 60%   |      |
| t <sub>START</sub>                   | REFO start-up time                  | 40% to 60% duty cycle                   |                 |       | 50    |       | μs   |

(1) Calculated using the box method: (MAX(-40°C to 85°C) – MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | TYP | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                      | Measured at MCLK                | 3 V             | 10  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at MCLK <sup>(1)</sup> | 3 V             | 0.5 | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at MCLK <sup>(2)</sup> | 1.8 V to 3.6 V  | 4   | %/V  |
| f <sub>VLO,DC</sub>                 | Duty cycle                         | Measured at MCLK                | 3 V             | 50% |      |

(1) Calculated using the box method: (MAX(-40°C to 85°C) – MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

**NOTE**

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-8).

**Table 5-9. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                             |                                       | TEST CONDITIONS | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|---------------------------------------|---------------------------------------|-----------------|-----------------|-------|-----|-----|------|
| f <sub>MODOSC</sub>                   | MODOSC frequency                      |                 | 3 V             | 3.8   | 4.8 | 5.8 | MHz  |
| f <sub>MODOSC</sub> /dT               | MODOSC frequency temperature drift    |                 | 3 V             | 0.102 |     |     | %/°C |
| f <sub>MODOSC</sub> /dV <sub>CC</sub> | MODOSC frequency supply voltage drift |                 | 1.8 V to 3.6 V  | 1.02  |     |     | %/V  |
| f <sub>MODOSC,DC</sub>                | Duty cycle                            |                 | 3 V             | 40%   | 50% | 60% |      |

### 5.11.4 Digital I/Os

**Table 5-10. Digital Inputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|------------------------|---|--|-----------------|------|-----|------|------|
| V <sub>IT+</sub>       | Positive-going input threshold voltage                          |  | 2 V             | 0.90 |     | 1.50 | V    |
|                        |   |  | 3 V             | 1.35 |     | 2.25 |      |
| V <sub>IT-</sub>       | Negative-going input threshold voltage                          |  | 2 V             | 0.50 |     | 1.10 | V    |
|                        |   |  | 3 V             | 0.75 |     | 1.65 |      |
| V <sub>hys</sub>       | Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) |  | 2 V             | 0.3  |     | 0.8  | V    |
|                        |   |  | 3 V             | 0.4  |     | 1.2  |      |
| R <sub>Pull</sub>      | Pullup or pulldown resistor                                     | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I,dig</sub>     | Input capacitance, digital only port pins                       | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |      | 3   |      | pF   |
| C <sub>I,ana</sub>     | Input capacitance, port pins with shared analog functions       | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |      | 5   |      | pF   |
| I <sub>lkg(Px.y)</sub> | High-impedance leakage current                                  | See <sup>(1)</sup> <sup>(2)</sup>  | 2 V, 3 V        | -20  |     | 20   | nA   |

(1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

**Table 5-11. Digital Outputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS                             | V <sub>CC</sub> | MIN | TYP | MAX  | UNIT |
|-----------------------|---|---|-----------------|-----|-----|------|------|
| V <sub>OH</sub>       | High-level output voltage                     | I <sub>(OHmax)</sub> = -3 mA <sup>(1)</sup> | 2 V             | 1.4 |     | 2.0  | V    |
|                       |   | I <sub>(OHmax)</sub> = -5 mA <sup>(1)</sup> | 3 V             | 2.4 |     | 3.0  |      |
| V <sub>OL</sub>       | Low-level output voltage                      | I <sub>(OLmax)</sub> = 3 mA <sup>(1)</sup>  | 2 V             | 0.0 |     | 0.60 | V    |
|                       |   | I <sub>(OHmax)</sub> = 5 mA <sup>(1)</sup>  | 3 V             | 0.0 |     | 0.60 |      |
| f <sub>Port_CLK</sub> | Clock output frequency                        | C <sub>L</sub> = 20 pF <sup>(2)</sup>       | 2 V             | 16  |     |      | MHz  |
|                       |   |   | 3 V             | 16  |     |      |      |
| t <sub>rise,dig</sub> | Port output rise time, digital only port pins | C <sub>L</sub> = 20 pF                      | 2 V             | 10  |     |      | ns   |
|                       |   |   | 3 V             | 7   |     |      |      |
| t <sub>fall,dig</sub> | Port output fall time, digital only port pins | C <sub>L</sub> = 20 pF                      | 2 V             | 10  |     |      | ns   |
|                       |   |   | 3 V             | 5   |     |      |      |

(1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.11.4.1 Typical Characteristics – Outputs at 3 V and 2 V

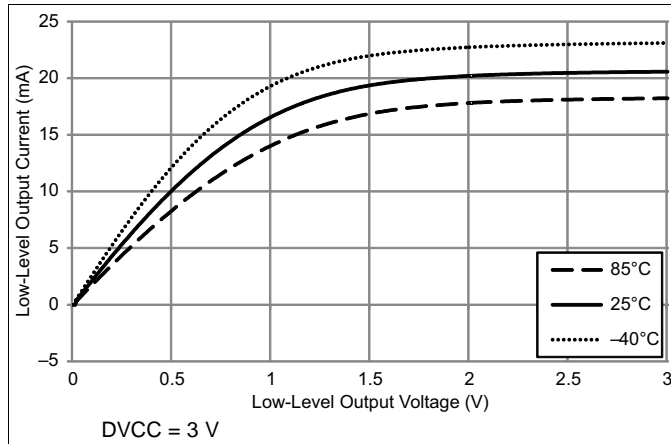


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

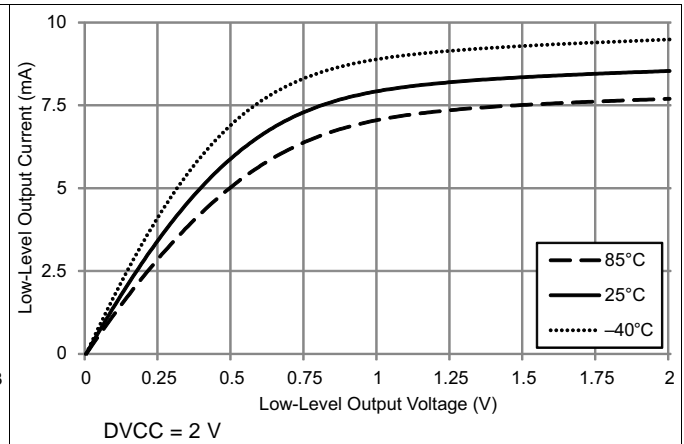


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

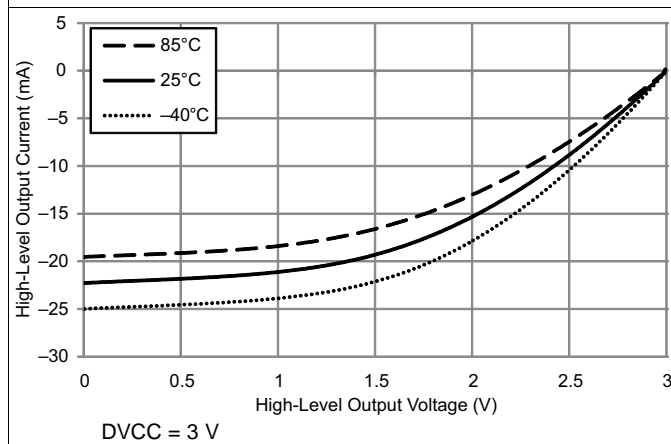


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

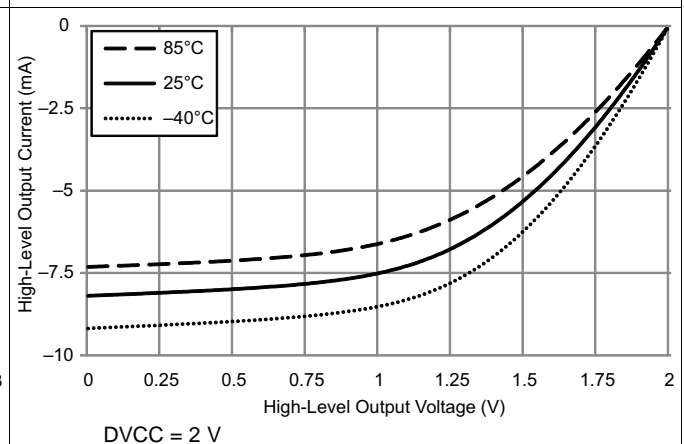


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

### 5.11.5 VREF+ Built-in Reference

**Table 5-12. VREF+**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

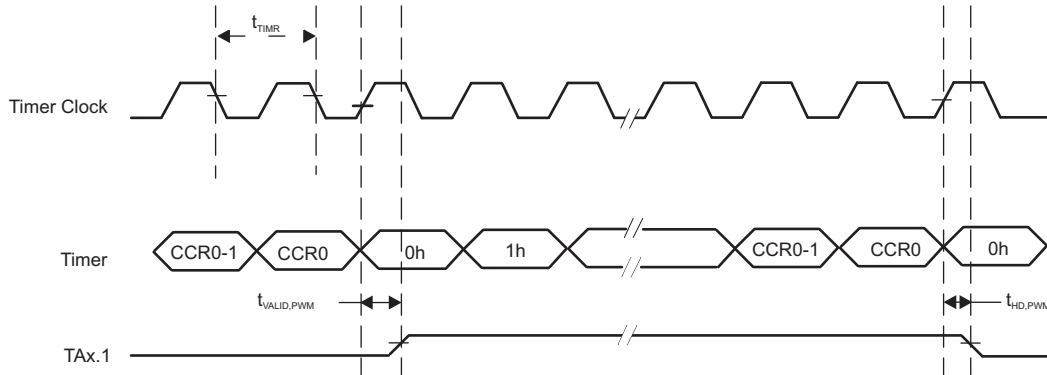
| PARAMETER          | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT  |
|--------------------|--|-----------------|------|------|------|-------|
| V <sub>REF+</sub>  | Positive built-in reference voltage<br>EXTREFEN = 1 with 1-mA load current | 2 V, 3 V        | 1.15 | 1.19 | 1.23 | V     |
| TC <sub>REF+</sub> | Temperature coefficient of built-in reference voltage                      |                 |      | 30   |      | μV/°C |

### 5.11.6 Timer\_A

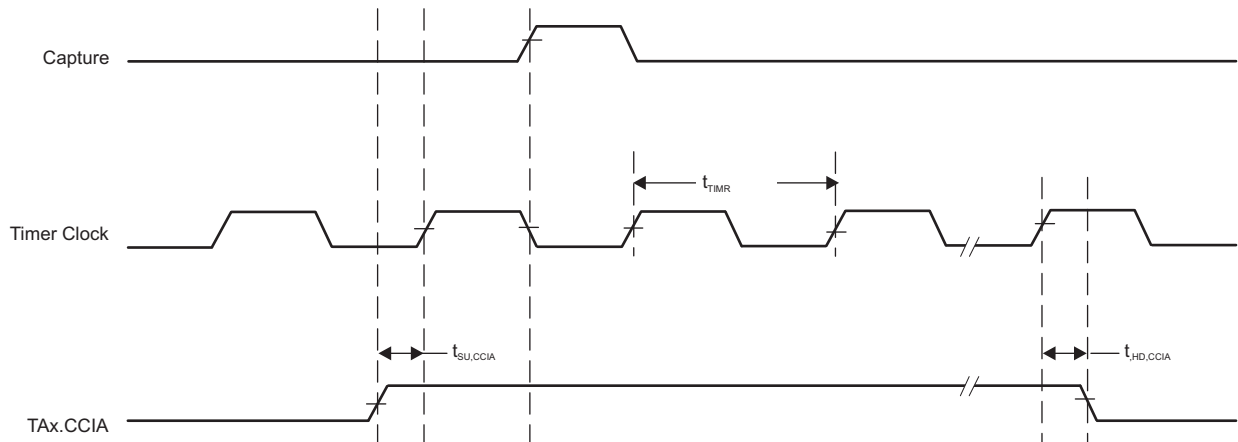
**Table 5-13. Timer\_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS  | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------|--|-----------------|-----|-----|-----|------|
| f <sub>TA</sub> | Timer_A input clock frequency<br>Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ±10% | 2 V, 3 V        |     |     | 16  | MHz  |



**Figure 5-10. Timer PWM Mode**



**Figure 5-11. Timer Capture Mode**

### 5.11.7 eUSCI

**Table 5-14. eUSCI (UART Mode) Clock Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|---|--|-----------------|-----|-----|------|
| f <sub>eUSCI</sub>  | eUSCI input clock frequency                           | Internal: SMCLK, MODCLK<br>External: UCLK<br>Duty cycle = 50% ±10% | 2 V, 3 V        |     | 16  | MHz  |
| f <sub>BITCLK</sub> | BITCLK clock frequency<br>(equals baud rate in Mbaud) |  | 2 V, 3 V        |     | 5   | MHz  |

**Table 5-15. eUSCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |   | TEST CONDITIONS | V <sub>CC</sub> | TYP | UNIT |
|----------------|---|-----------------|-----------------|-----|------|
| t <sub>t</sub> | UART receive deglitch time <sup>(1)</sup> | UCGLITx = 0     | 2 V, 3 V        | 12  | ns   |
|                |   | UCGLITx = 1     |                 | 40  |      |
|                |   | UCGLITx = 2     |                 | 68  |      |
|                |   | UCGLITx = 3     |                 | 110 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

**Table 5-16. eUSCI (SPI Master Mode) Clock Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER          |                             | TEST CONDITIONS                                  | MIN | MAX | UNIT |
|--------------------|-----------------------------|--|-----|-----|------|
| f <sub>eUSCI</sub> | eUSCI input clock frequency | Internal: SMCLK, MODCLK<br>Duty cycle = 50% ±10% |     | 8   | MHz  |

**Table 5-17. eUSCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER             |  | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | MAX | UNIT          |
|-----------------------|--|--|-----------------|-----|-----|---------------|
| t <sub>STE,LEAD</sub> | STE lead time, STE active to clock         | UCSTEM = 0, UCMODEx = 01 or 10                     |                 | 1   |     | UCxCLK cycles |
|                       |  | UCSTEM = 1, UCMODEx = 01 or 10                     |                 |     |     |               |
| t <sub>STE,LAG</sub>  | STE lag time, last clock to STE inactive   | UCSTEM = 0, UCMODEx = 01 or 10                     |                 | 1   |     | UCxCLK cycles |
|                       |  | UCSTEM = 1, UCMODEx = 01 or 10                     |                 |     |     |               |
| t <sub>SU,MI</sub>    | SOMI input data setup time                 |  | 2 V             | 45  |     | ns            |
|                       |  |  | 3 V             | 35  |     |               |
| t <sub>HD,MI</sub>    | SOMI input data hold time                  |  | 2 V             | 0   |     | ns            |
|                       |  |  | 3 V             | 0   |     |               |
| t <sub>VALID,MO</sub> | SIMO output data valid time <sup>(2)</sup> | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | 2 V             |     | 20  | ns            |
|                       |  |  | 3 V             |     | 20  |               |
| t <sub>HD,MO</sub>    | SIMO output data hold time <sup>(3)</sup>  | C <sub>L</sub> = 20 pF                             | 2 V             | 0   |     | ns            |
|                       |  |  | 3 V             | 0   |     |               |

- (1)  $f_{UCxCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$ . For the slave parameters  $t_{SU,SI}(Slave)$  and  $t_{VALID,SO}(Slave)$ , see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-12](#) and [Figure 5-13](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in [Figure 5-12](#) and [Figure 5-13](#).



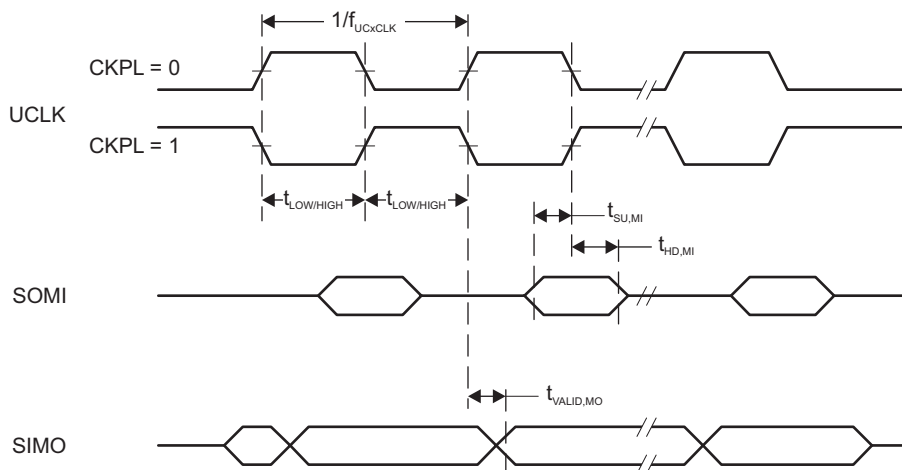


Figure 5-12. SPI Master Mode, CKPH = 0

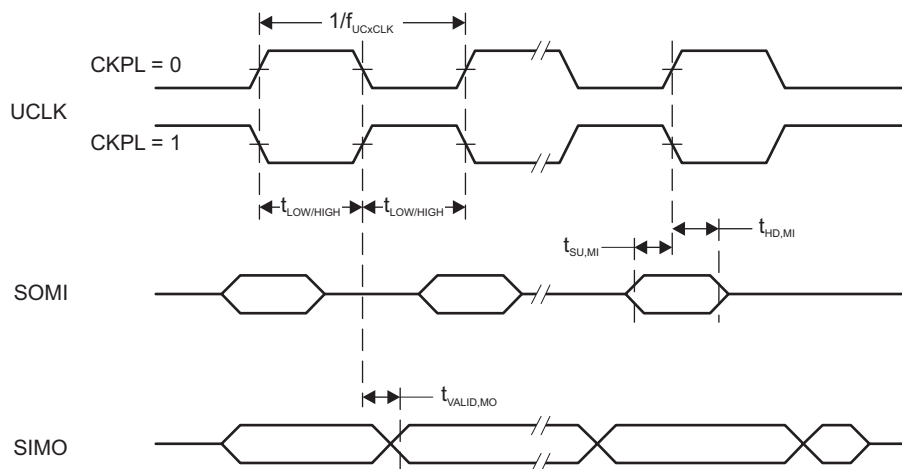


Figure 5-13. SPI Master Mode, CKPH = 1

**Table 5-18. eUSCI (SPI Slave Mode)**over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER             |   | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time, STE active to clock                    |  | 2 V             | 55  |     | ns   |
|                       |   |  | 3 V             | 45  |     |      |
| t <sub>STE,LAG</sub>  | STE lag time, Last clock to STE inactive              |  | 2 V             | 20  |     | ns   |
|                       |   |  | 3 V             | 20  |     |      |
| t <sub>STE,ACC</sub>  | STE access time, STE active to SOMI data out          |  | 2 V             |     | 65  | ns   |
|                       |   |  | 3 V             |     | 40  |      |
| t <sub>STE,DIS</sub>  | STE disable time, STE inactive to SOMI high impedance |  | 2 V             |     | 40  | ns   |
|                       |   |  | 3 V             |     | 35  |      |
| t <sub>SU,SI</sub>    | SIMO input data setup time                            |  | 2 V             | 6   |     | ns   |
|                       |   |  | 3 V             | 4   |     |      |
| t <sub>HD,SI</sub>    | SIMO input data hold time                             |  | 2 V             | 12  |     | ns   |
|                       |   |  | 3 V             | 12  |     |      |
| t <sub>VALID,SO</sub> | SOMI output data valid time <sup>(2)</sup>            | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2 V             |     | 65  | ns   |
|                       |   |  | 3 V             |     | 40  |      |
| t <sub>HD,SO</sub>    | SOMI output data hold time <sup>(3)</sup>             | C <sub>L</sub> = 20 pF                             | 2 V             | 5   |     | ns   |
|                       |   |  | 3 V             | 5   |     |      |

- (1)  $f_{UCxCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$ .  
For the master parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$ , see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-14](#) and [Figure 5-15](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-14](#) and [Figure 5-15](#).

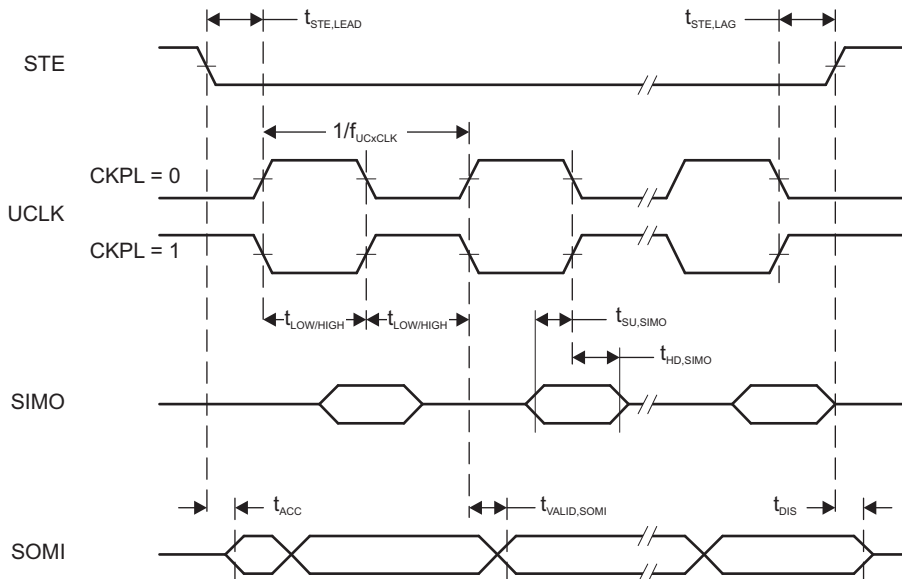


Figure 5-14. SPI Slave Mode, CKPH = 0

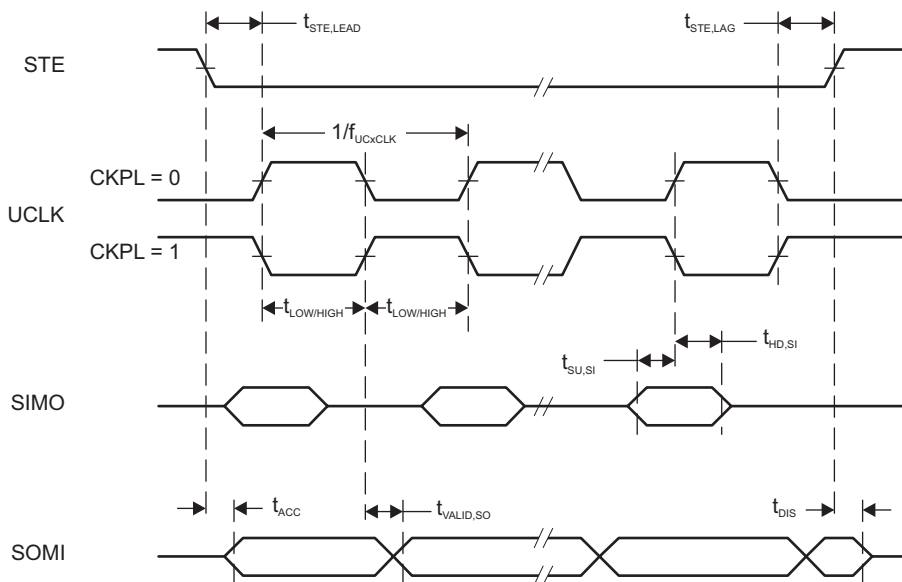
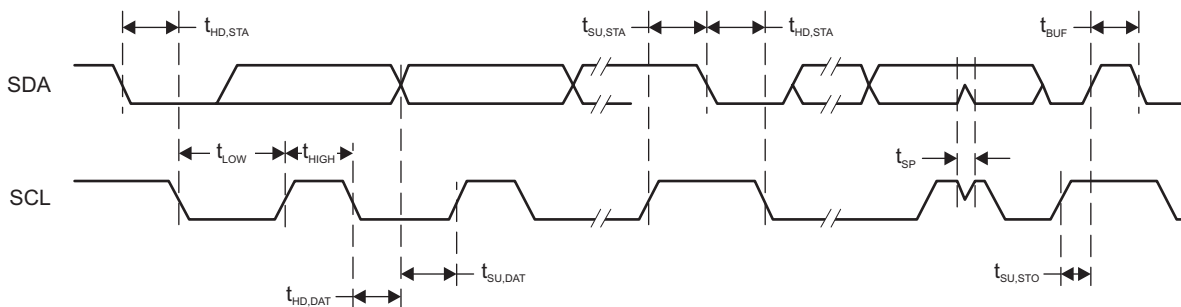


Figure 5-15. SPI Slave Mode, CKPH = 1

**Table 5-19. eUSCI (I<sup>2</sup>C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-16](#))

| PARAMETER   | TEST CONDITIONS  | V <sub>CC</sub> | MIN        | TYP | MAX | UNIT |
|---|--|-----------------|------------|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency                      | Internal: SMCLK, MODCLK<br>External: UCLK<br>Duty cycle = 50% ±10% |                 |            |     | 16  | MHz  |
| f <sub>SCL</sub> SCL clock frequency                                |  | 2 V, 3 V        | 0          |     | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START                      | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz           | 2 V, 3 V        | 4.0<br>0.6 |     |     | μs   |
| t <sub>SU,STA</sub> Setup time for a repeated START                 | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz           | 2 V, 3 V        | 4.7<br>0.6 |     |     | μs   |
| t <sub>HD,DAT</sub> Data hold time                                  |  | 2 V, 3 V        | 0          |     |     | ns   |
| t <sub>SU,DAT</sub> Data setup time                                 |  | 2 V, 3 V        | 250        |     |     | ns   |
| t <sub>SU,STO</sub> Setup time for STOP                             | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz           | 2 V, 3 V        | 4.0<br>0.6 |     |     | μs   |
| t <sub>SP</sub> Pulse duration of spikes suppressed by input filter | UCGLITx = 0  | 2 V, 3 V        | 50         |     | 600 | ns   |
|   | UCGLITx = 1  |                 | 25         | 300 |     |      |
|   | UCGLITx = 2  |                 | 12.5       | 150 |     |      |
|   | UCGLITx = 3  |                 | 6.3        | 75  |     |      |
| t <sub>TIMEOUT</sub> Clock low time-out                             | UCCLTOx = 1  | 2 V, 3 V        |            | 27  |     | ms   |
|   | UCCLTOx = 2  |                 |            | 30  |     |      |
|   | UCCLTOx = 3  |                 |            | 33  |     |      |



**Figure 5-16. I<sup>2</sup>C Mode Timing**

### 5.11.8 ADC

**Table 5-20. ADC, Power Supply and Input Range Conditions**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER         |   | TEST CONDITIONS   | V <sub>CC</sub> | MIN | TYP | MAX              | UNIT |
|-------------------|---|---|-----------------|-----|-----|------------------|------|
| DV <sub>CC</sub>  | ADC supply voltage  |   |                 | 2.0 |     | 3.6              | V    |
| V <sub>(Ax)</sub> | Analog input voltage range  | All ADC pins  |                 | 0   |     | DV <sub>CC</sub> | V    |
| I <sub>ADC</sub>  | Operating supply current into DV <sub>CC</sub> terminal, reference current not included, repeat-single-channel mode | f <sub>ADCCLK</sub> = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b                 | 2 V             | 185 |     |                  | μA   |
|                   |   |   | 3 V             | 207 |     |                  |      |
| C <sub>I</sub>    | Input capacitance   | Only one terminal Ax can be selected at one time, from the pad to the ADC capacitor array, including wiring and pad | 2.2 V           |     | 1.6 | 2.0              | pF   |
| R <sub>I</sub>    | Input MUX ON resistance   | DV <sub>CC</sub> = 2 V, 0 V = V <sub>Ax</sub> = DV <sub>CC</sub>  |                 |     |     | 2                | kΩ   |

**Table 5-21. ADC, 10-Bit Timing Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                  | TEST CONDITIONS   | V <sub>CC</sub> | MIN                | TYP | MAX  | UNIT |
|----------------------|----------------------------------|---|-----------------|--------------------|-----|------|------|
| f <sub>ADCCLK</sub>  |                                  | For specified performance of ADC linearity parameters   | 2 V to 3.6 V    | 0.45               | 5   | 5.5  | MHz  |
| f <sub>ADCOSC</sub>  | Internal ADC oscillator (MODOSC) | ADCDIV = 0, f <sub>ADCCLK</sub> = f <sub>ADCOSC</sub>   | 2 V to 3.6 V    | 4.5                | 5.0 | 5.5  | MHz  |
| t <sub>CONVERT</sub> | Conversion time                  | REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f <sub>ADCOSC</sub> = 4.5 MHz to 5.5 MHz   | 2 V to 3.6 V    | 2.18               |     | 2.67 | μs   |
|                      |                                  | External f <sub>ADCCLK</sub> from ACLK or SMCLK, ADCSSEL ≠ 0  | 2 V to 3.6 V    | See <sup>(1)</sup> |     |      |      |
| t <sub>ADCON</sub>   | Turnon settling time of the ADC  | The error in a conversion started after t <sub>ADCON</sub> is less than ±0.5 LSB, Reference and input signal already settled                        |                 |                    |     | 100  | ns   |
| t <sub>Sample</sub>  | Sampling time                    | R <sub>S</sub> = 1000 Ω, R <sub>I</sub> = 36000 Ω, C <sub>I</sub> = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB | 2 V             | 1.5                |     |      | μs   |
|                      |                                  |   | 3 V             | 2.0                |     |      |      |

(1)  $12 \times \text{ADCDIV} \times 1 / f_{\text{ADCCLK}}$

**Table 5-22. ADC, 10-Bit Linearity Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                    |   | TEST CONDITIONS   | V <sub>CC</sub> | MIN   | TYP  | MAX  | UNIT  |
|------------------------------|---|---|-----------------|-------|------|------|-------|
| E <sub>I</sub>               | Integral linearity error (10-bit mode)                        | V <sub>eref+</sub> as reference   | 2.4 V to 3.6 V  | -2    |      | 2    | LSB   |
|                              | Integral linearity error (8-bit mode)                         |   | 2 V to 3.6 V    | -2    |      | 2    |       |
| E <sub>D</sub>               | Differential linearity error (10-bit mode)                    | V <sub>eref+</sub> as reference   | 2.4 V to 3.6 V  | -1    |      | 1    | LSB   |
|                              | Differential linearity error (8-bit mode)                     |   | 2 V to 3.6 V    | -1    |      | 1    |       |
| E <sub>O</sub>               | Offset error (10-bit mode)                                    | V <sub>eref+</sub> as reference   | 2.4 V to 3.6 V  | -6.5  |      | 6.5  | mV    |
|                              | Offset error (8-bit mode)                                     |   | 2 V to 3.6 V    | -6.5  |      | 6.5  |       |
| E <sub>G</sub>               | Gain error (10-bit mode)                                      | V <sub>eref+</sub> as reference   | 2.4 V to 3.6 V  | -2.0  |      | 2.0  | LSB   |
|                              |   | Internal 1.5-V reference  |                 | -3.0% |      | 3.0% |       |
|                              | Gain error (8-bit mode)                                       | V <sub>eref+</sub> as reference   | 2 V to 3.6 V    | -2.0  |      | 2.0  | LSB   |
|                              |   | Internal 1.5-V reference  |                 | -3.0% |      | 3.0% |       |
| E <sub>T</sub>               | Total unadjusted error (10-bit mode)                          | V <sub>eref+</sub> as reference   | 2.4 V to 3.6 V  | -2.0  |      | 2.0  | LSB   |
|                              |   | Internal 1.5-V reference  |                 | -3.0% |      | 3.0% |       |
|                              | Total unadjusted error (8-bit mode)                           | V <sub>eref+</sub> as reference   | 2 V to 3.6 V    | -2.0  |      | 2.0  | LSB   |
|                              |   | Internal 1.5-V reference  |                 | -3.0% |      | 3.0% |       |
| V <sub>SENSOR</sub>          | See <sup>(1)</sup>  | ADCON = 1, INCH = 0Ch, T <sub>A</sub> = 0°C   | 3 V             |       | 913  |      | mV    |
| TC <sub>SENSOR</sub>         | See <sup>(2)</sup>  | ADCON = 1, INCH = 0Ch   | 3 V             |       | 3.35 |      | mV/°C |
| t <sub>SENSOR (sample)</sub> | Sample time required if channel 12 is selected <sup>(3)</sup> | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, AM and all LPMs above LPM3 | 3 V             |       | 30   |      | μs    |
|                              |   | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, LPM3                       | 3 V             |       | 100  |      |       |

- (1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, } ^\circ\text{C}) + V_{SENSOR}$ , where TC<sub>SENSOR</sub> and V<sub>SENSOR</sub> can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor on time, t<sub>SENSOR(on)</sub>.

### 5.11.9 CapTivate

**Table 5-23. CapTivate Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER         |  | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT |
|-------------------|--|---|-----|------|-----|------|
| $V_{REG}$         | Reference voltage output   |   | 1.5 | 1.55 | 1.6 | V    |
| $t_{WAKEUP,COLD}$ | Voltage regulator wake-up time: LDO completely off then turned on    |   |     |      | 1   | ms   |
| $t_{WAKEUP,WARM}$ | Voltage regulator wake-up time: LDO in low-power mode then turned on |   |     |      | 300 | us   |
| $f_{CAPCLK}$      | Captivate oscillator frequency, nominal                              | $T_A = 25^\circ\text{C}$ , CAPCLK0, FREQSHFT = 00b                  | -3% | 16   | +3% | MHz  |
| $f_{CAPCLK,DC}$   | Duty cycle   | Duty cycle (excluding first clock cycle, $DC = t_{high} \times f$ ) | 40% | 50%  | 60% |      |

### 5.11.10 FRAM

**Table 5-24. FRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                      | TEST CONDITIONS       | MIN              | TYP                                    | MAX | UNIT   |
|--|-----------------------|------------------|--|-----|--------|
| Read and write endurance                       |                       | 10 <sup>15</sup> |  |     | cycles |
| t <sub>Retention</sub> Data retention duration | T <sub>J</sub> = 25°C | 100              |  |     | years  |
|  | T <sub>J</sub> = 70°C | 40               |  |     |        |
|  | T <sub>J</sub> = 85°C | 10               |  |     |        |
| I <sub>WRITE</sub> Current to write into FRAM  |                       |                  | I <sub>READ</sub> <sup>(1)</sup>       |     | nA     |
| I <sub>ERASE</sub> Erase current               |                       |                  | N/A <sup>(2)</sup>                     |     | nA     |
| t <sub>WRITE</sub> Write time                  |                       |                  | t <sub>READ</sub> <sup>(3)</sup>       |     | ns     |
| t <sub>READ</sub> Read time                    | NWAITSx = 0           |                  | 1 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     | ns     |
|  | NWAITSx = 1           |                  | 2 / f <sub>SYSTEM</sub> <sup>(4)</sup> |     |        |

- (1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I<sub>READ</sub> is included in the active mode current consumption parameter I<sub>AM,FRAM</sub>.
- (2) FRAM does not require a special erase sequence.
- (3) Writing into FRAM is as fast as reading.
- (4) The maximum read (and write) speed is specified by f<sub>SYSTEM</sub> using the appropriate wait state settings (NWAITSx).



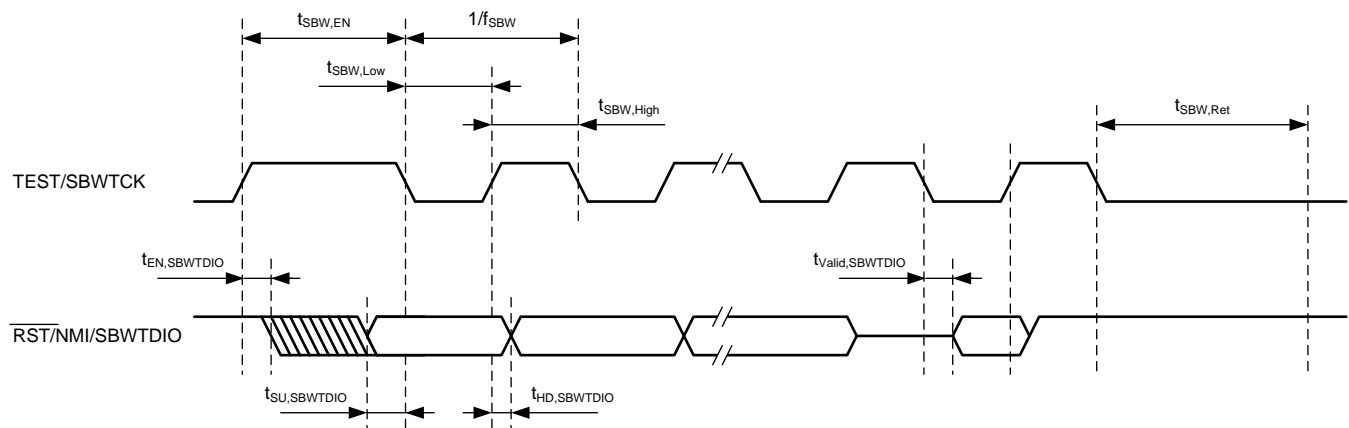
### 5.11.11 Debug and Emulation

**Table 5-25. JTAG, Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-17](#))

| PARAMETER                   |  | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|-----------------------------|--|-----------------|-------|-----|-----|------|
| f <sub>SBW</sub>            | Spy-Bi-Wire input frequency  | 2 V, 3 V        | 0     |     | 10  | MHz  |
| t <sub>SBW,Low</sub>        | Spy-Bi-Wire low clock pulse duration   | 2 V, 3 V        | 0.028 |     | 15  | μs   |
| t <sub>SU, SBWTDIO</sub>    | SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire)  | 2 V, 3 V        | 4     |     |     | ns   |
| t <sub>HD, SBWTDIO</sub>    | SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire)     | 2 V, 3 V        | 19    |     |     | ns   |
| t <sub>valid, SBWTDIO</sub> | SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot, Spy-Bi-Wire)      | 2 V, 3 V        |       |     | 31  | ns   |
| t <sub>SBW, En</sub>        | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup> | 2 V, 3 V        |       |     | 110 | μs   |
| t <sub>SBW, Ret</sub>       | Spy-Bi-Wire return to normal operation time <sup>(2)</sup>                           | 2 V, 3 V        | 15    |     | 100 | μs   |
| R <sub>internal</sub>       | Internal pulldown resistance on TEST   | 2 V, 3 V        | 20    | 35  | 50  | kΩ   |

- (1) Tools that access the Spy-Bi-Wire interface must wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) Maximum t<sub>SBW,Ret</sub> time after pulling or releasing the TEST/SBWTCK pin low until the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode is selected.



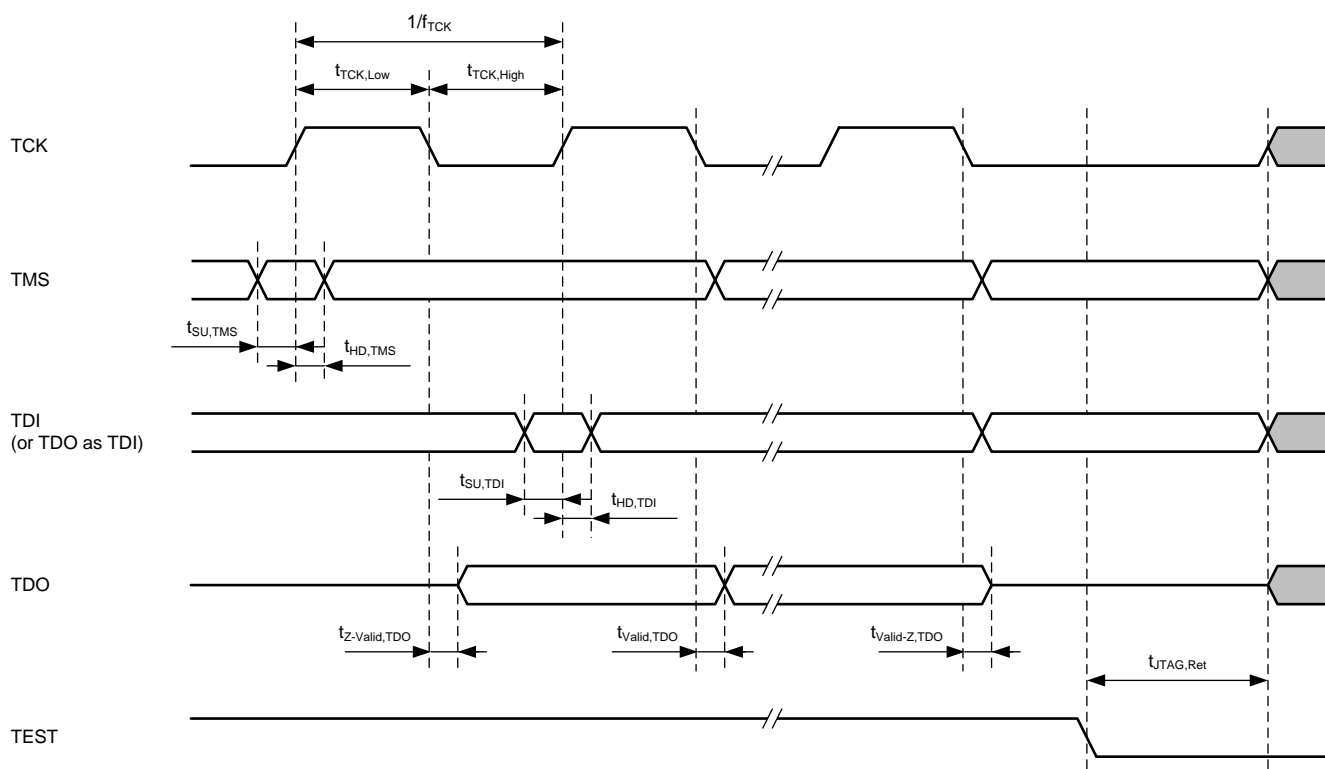
**Figure 5-17. JTAG Spy-Bi-Wire Timing**

**Table 5-26. JTAG, 4-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-18](#))

| PARAMETER                |   | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------|---|-----------------|-----|-----|-----|------|
| f <sub>TCK</sub>         | TCK input frequency <sup>(1)</sup>                                  | 2 V, 3 V        | 0   |     | 10  | MHz  |
| t <sub>TCK,Low</sub>     | TCK low clock pulse duration  | 2 V, 3 V        | 15  |     |     | ns   |
| t <sub>TCK,High</sub>    | TCK high clock pulse duration                                       | 2 V, 3 V        | 15  |     |     | ns   |
| t <sub>SU,TMS</sub>      | TMS setup time (before rising edge of TCK)                          | 2 V, 3 V        | 11  |     |     | ns   |
| t <sub>HD,TMS</sub>      | TMS hold time (after rising edge of TCK)                            | 2 V, 3 V        | 3   |     |     | ns   |
| t <sub>SU,TDI</sub>      | TDI setup time (before rising edge of TCK)                          | 2 V, 3 V        | 13  |     |     | ns   |
| t <sub>HD,TDI</sub>      | TDI hold time (after rising edge of TCK)                            | 2 V, 3 V        | 5   |     |     | ns   |
| t <sub>Z-Valid,TDO</sub> | TDO high impedance to valid output time (after falling edge of TCK) | 2 V, 3 V        |     |     | 26  | ns   |
| t <sub>Valid,TDO</sub>   | TDO to new valid output time (after falling edge of TCK)            | 2 V, 3 V        |     |     | 26  | ns   |
| t <sub>Valid-Z,TDO</sub> | TDO valid to high-impedance output time (after falling edge of TCK) | 2 V, 3 V        |     |     | 26  | ns   |
| t <sub>JTAG,Ret</sub>    | Spy-Bi-Wire return to normal operation time                         |                 | 15  |     | 100 | μs   |
| R <sub>internal</sub>    | Internal pulldown resistance on TEST                                | 2 V, 3 V        | 20  | 35  | 50  | kΩ   |

(1) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.



**Figure 5-18. JTAG 4-Wire Timing**

## 6 Detailed Description

### 6.1 Overview

The MSP430FR263x and MSP430FR253x ultra-low-power MCUs are the first FRAM-based MCUs with integrated high-performance charge-transfer CapTIvate technology in ultra-low-power high-reliability high-flexibility MCUs. The MSP430FR263x and MSP430FR253x MCU features up to 16 self-capacitance or 64 mutual-capacitance electrodes, 30-cm proximity sensing, and high accuracy up to 1-fF detection. The MCUs also include four 16-bit timers, eUSCs that support UART, SPI, and I<sup>2</sup>C, a hardware multiplier, an RTC module with alarm capabilities, and a high-performance 10-bit ADC.

### 6.2 CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

### 6.3 Operating Modes

The MSP430 has one active mode and several software-selectable low-power modes of operation (see [Table 6-1](#)). An interrupt event can wake the MCU from low-power mode LPM0 or LPM3, service the request, and restore the MCU back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

**Table 6-1. Operating Modes**

| MODE                           |           | AM                    | LPM0            | LPM3                                 | LPM4                | LPM3.5                                | LPM4.5            |
|--------------------------------|-----------|-----------------------|-----------------|--------------------------------------|---------------------|---------------------------------------|-------------------|
|                                |           | ACTIVE MODE (FRAM ON) | CPU OFF         | STANDBY                              | OFF                 | ONLY RTC                              | SHUTDOWN          |
| Maximum system clock           |           | 16 MHz                | 16 MHz          | 40 kHz                               | 0                   | 40 kHz                                | 0                 |
| Power consumption at 25°C, 3 V |           | 126 µA/MHz            | 40 µA/MHz       | 1.7 µA/button average with 8-Hz scan | 0.49 µA without SVS | 0.73 µA with RTC counter only in LFXT | 16 nA without SVS |
| Wake-up time                   |           | N/A                   | Instant         | 10 µs                                | 10 µs               | 350 µs                                | 350 µs            |
| Wake-up events                 |           | N/A                   | All             | All                                  | I/O                 | RTC<br>CapTIvate<br>I/O               | I/O               |
| Power                          | Regulator | Full Regulation       | Full Regulation | Partial Power Down                   | Partial Power Down  | Partial Power Down                    | Power Down        |
|                                | SVS       | On                    | On              | Optional                             | Optional            | Optional                              | Optional          |
|                                | Brownout  | On                    | On              | On                                   | On                  | On                                    | On                |

**Table 6-1. Operating Modes (continued)**

| MODE                 |                                      | AM                    | LPM0     | LPM3       | LPM4       | LPM3.5     | LPM4.5     |
|----------------------|--------------------------------------|-----------------------|----------|------------|------------|------------|------------|
|                      |                                      | ACTIVE MODE (FRAM ON) | CPU OFF  | STANDBY    | OFF        | ONLY RTC   | SHUTDOWN   |
| Clock <sup>(1)</sup> | MCLK                                 | Active                | Off      | Off        | Off        | Off        | Off        |
|                      | SMCLK                                | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | FLL                                  | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | DCO                                  | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | MODCLK                               | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | REFO                                 | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | ACLK                                 | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | XT1CLK                               | Optional              | Optional | Optional   | Off        | Optional   | Off        |
|                      | VLOCLK                               | Optional              | Optional | Optional   | Off        | Optional   | Off        |
| CapTivate MODCLK     | Optional                             | Optional              | Optional | Off        | Off        | Off        |            |
| Core                 | CPU                                  | On                    | Off      | Off        | Off        | Off        | Off        |
|                      | FRAM                                 | On                    | On       | Off        | Off        | Off        | Off        |
|                      | RAM                                  | On                    | On       | On         | On         | Off        | Off        |
|                      | Backup memory <sup>(2)</sup>         | On                    | On       | On         | On         | On         | Off        |
| Peripherals          | Timer0_A3                            | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | Timer1_A3                            | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | Timer2_A2                            | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | Timer3_A2                            | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | WDT                                  | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | eUSCI_A0                             | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | eUSCI_A1                             | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | eUSCI_B0                             | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | CRC                                  | Optional              | Optional | Off        | Off        | Off        | Off        |
|                      | ADC                                  | Optional              | Optional | Optional   | Off        | Off        | Off        |
|                      | RTC                                  | Optional              | Optional | Optional   | Off        | Optional   | Off        |
| CapTivate            | Optional                             | Optional              | Optional | Off        | Off        | Off        |            |
| I/O                  | General-purpose digital input/output | On                    | Optional | State Held | State Held | State Held | State Held |

(1) The status shown for LPM4 applies to internal clocks only.

(2) Backup memory contains 32 bytes of register space in peripheral memory. See [Table 6-24](#) and [Table 6-43](#) for its memory allocation.

**NOTE**

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals.

## 6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-2. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE  | INTERRUPT FLAG   | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|---|--|------------------|--------------|-------------|
| <b>System Reset</b><br>Power up, Brownout, Supply supervisor<br>External reset RST<br>Watchdog time-out, Key violation<br>FRAM uncorrectable bit error detection<br>Software POR, BOR<br>FLL unlock error | SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>PMMPORIFG, PMMBORIFG<br>SYSRSTIV<br>FLLUNLOCKIFG   | Reset            | FFFEh        | 63, Highest |
| <b>System NMI</b><br>Vacant memory access<br>JTAG mailbox<br>FRAM access time error<br>FRAM bit error detection   | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>CBDIFG, UBDIFG  | Nonmaskable      | FFFCh        | 62          |
| <b>User NMI</b><br>External NMI<br>Oscillator fault   | NMIFG<br>OFIFG   | Nonmaskable      | FFFAh        | 61          |
| Timer0_A3   | TA0CCR0 CCIFG0   | Maskable         | FFF8h        | 60          |
| Timer0_A3   | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2,<br>TA0IFG (TA0IV)  | Maskable         | FFF6h        | 59          |
| Timer1_A3   | TA1CCR0 CCIFG0   | Maskable         | FFF4h        | 58          |
| Timer1_A3   | TA1CCR1 CCIFG1, TA1CCR2 CCIFG2,<br>TA1IFG (TA1IV)  | Maskable         | FFF2h        | 57          |
| Timer2_A2   | TA2CCR0 CCIFG0   | Maskable         | FFF0h        | 56          |
| Timer2_A2   | TA2CCR1 CCIFG1, TA2IFG (TA2IV)   |                  | FFEEh        | 55          |
| Timer3_A2   | TA3CCR0 CCIFG0   | Maskable         | FFECh        | 54          |
| Timer3_A2   | TA3CCR1 CCIFG1, TA3IFG (TA3IV)   |                  | FFEAh        | 53          |
| RTC   | RTCIFG   | Maskable         | FFE8h        | 52          |
| Watchdog timer interval mode  | WDTIFG   | Maskable         | FFE6h        | 51          |
| eUSCI_A0 receive or transmit  | UCTXCPTIFG, UCSTTIFG, UCRXIFG,<br>UCTXIFG (UART mode)<br>UCRXIFG, UCTXIFG (SPI mode)<br>(UCA0IV)   | Maskable         | FFE4h        | 50          |
| eUSCI_A1 receive or transmit  | UCTXCPTIFG, UCSTTIFG, UCRXIFG,<br>UCTXIFG (UART mode)<br>UCRXIFG, UCTXIFG (SPI mode)<br>(UCA1IV)   | Maskable         | FFE2h        | 49          |
| eUSCI_B0 receive or transmit  | UCB0RXIFG, UCB0TXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG,<br>UCSTPIFG, UCRXIFG0, UCTXIFG0,<br>UCRXIFG1, UCTXIFG1, UCRXIFG2,<br>UCTXIFG2, UCRXIFG3, UCTXIFG3,<br>UCCNTIFG, UCBIT9IFG (I <sup>2</sup> C mode)<br>(UCB0IV) | Maskable         | FFE0h        | 48          |
| ADC   | ADCIFG0, ADCINIFG, ADCLOIFG,<br>ADCHIIFG, ADCTOVIFG, ADCOVIFG<br>(ADCIV)   | Maskable         | FFDEh        | 47          |
| P1  | P1IFG.0 to P1IFG.7 (P1IV)  | Maskable         | FFDCh        | 46          |
| P2  | P2IFG.0 to P2IFG.7 (P2IV)  | Maskable         | FFDAh        | 45          |
| CapTivate   | (See <a href="#">CapTivate Design Center</a> for details )   | Maskable         | FFD8h        | 44, Lowest  |
| Reserved  | Reserved   | Maskable         | FFD6h–FF88h  |             |

**Table 6-2. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG   | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|------------------|------------------|--------------|----------|
| Signatures       | BSL Signature 2  |                  | 0FF86h       |          |
|                  | BSL Signature 1  |                  | 0FF84h       |          |
|                  | JTAG Signature 2 |                  | 0FF82h       |          |
|                  | JTAG Signature 1 |                  | 0FF80h       |          |

## 6.5 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using either the UART serial interface or the I<sup>2</sup>C interface. Access to the MCU memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins (see [Table 6-3](#) and [Table 6-4](#)). The BSL entry requires a specific entry sequence on the  $\overline{\text{RST}}$ /NMI/SBWDIO and TEST/SBWTCK pins. For the complete description of the feature of the BSL, see the *MSP430FR4xx and MSP430FR2xx Bootloader (BSL) User's Guide (SLAU610)*.

**Table 6-3. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL                       | BSL FUNCTION          |
|-------------------------------------|-----------------------|
| $\overline{\text{RST}}$ /NMI/SBWDIO | Entry sequence signal |
| TEST/SBWTCK                         | Entry sequence signal |
| P1.4                                | Data transmit         |
| P1.5                                | Data receive          |
| VCC                                 | Power supply          |
| VSS                                 | Ground supply         |

**Table 6-4. I<sup>2</sup>C BSL Pin Requirements and Functions**

| DEVICE SIGNAL                       | BSL FUNCTION              |
|-------------------------------------|---------------------------|
| $\overline{\text{RST}}$ /NMI/SBWDIO | Entry sequence signal     |
| TEST/SBWTCK                         | Entry sequence signal     |
| P1.2                                | Data transmit and receive |
| P1.3                                | Clock                     |
| VCC                                 | Power supply              |
| VSS                                 | Ground supply             |

## 6.6 JTAG Standard Interface

The MSP low-power microcontrollers support the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin enables the JTAG signals. In addition to these signals, the  $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$  is required to interface with MSP430 development tools and device programmers. [Table 6-5](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide (SLAU278)*. For details on using the JTAG interface, see the *MSP430 Programming Via the JTAG Interface User's Guide (SLAU320)*.

**Table 6-5. JTAG Pin Requirements and Function**

| DEVICE SIGNAL                                     | DIRECTION | JTAG FUNCTION               |
|---|-----------|-----------------------------|
| P1.4/UCA0TXD/UCA0SIMO/TA1.2/TCK/A4/VREF+          | IN        | JTAG clock input            |
| P1.5/UCA0RXD/UCA0SOMI/TA1.1/TMS/A5                | IN        | JTAG state control          |
| P1.6/UCA0CLK/TA1CLK/TDI/TCLK/A6                   | IN        | JTAG data input, TCLK input |
| P1.7/UCA0STE/SMCLK/TDO/A7                         | OUT       | JTAG data output            |
| TEST/SBWTCK                                       | IN        | Enable JTAG pins            |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN        | External reset              |
| DVCC  |           | Power supply                |
| DVSS  |           | Ground supply               |

## 6.7 Spy-Bi-Wire Interface (SBW)

The MSP low-power microcontrollers support the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. [Table 6-6](#) lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide (SLAU278)*. For details on using the SBW interface, see the *MSP430 Programming Via the JTAG Interface User's Guide (SLAU320)*.

**Table 6-6. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL                                     | DIRECTION | SBW FUNCTION                      |
|---|-----------|-----------------------------------|
| TEST/SBWTCK                                       | IN        | Spy-Bi-Wire clock input           |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN, OUT   | Spy-Bi-Wire data input and output |
| DVCC  |           | Power supply                      |
| DVSS  |           | Ground supply                     |

## 6.8 FRAM

The FRAM can be programmed using the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

## 6.9 Memory Protection

The device features memory protection for user access authority and write protection, including options to:

- Secure the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Enable write protection to prevent unwanted write operation to FRAM contents by setting the control bits in the System Configuration 0 register. For detailed information, see the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide (SLAU445)*.

## 6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MP430FR4xx and MP430FR2xx Family User's Guide (SLAU445)*.

### 6.10.1 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as [Equation 1](#) by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5 \text{ V}) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when EXTREFEN = 1 in the PMMCTL1 register. ADC channel 4 can also be selected to monitor this voltage. For more detailed information, see the *MP430FR4xx and MP430FR2xx Family User's Guide (SLAU445)*.

### 6.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- **Main Clock (MCLK):** The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- **Sub-Main Clock (SMCLK):** The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- **Auxiliary Clock (ACLK):** This clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.



All peripherals may have one or several clock sources depending on specific functionality. [Table 6-7](#) lists the clock distribution used in this device.

**Table 6-7. Clock Distribution**

|                 | CLOCK SOURCE SELECT BITS | MCLK         | SMCLK        | ACLK         | MODCLK     | XT1CLK       | VLOCLK      | EXTERNAL PIN      |
|-----------------|--------------------------|--------------|--------------|--------------|------------|--------------|-------------|-------------------|
| Frequency Range |                          | DC to 16 MHz | DC to 16 MHz | DC to 40 kHz | 5 MHz ±10% | DC to 40 kHz | 10 kHz ±50% |                   |
| CPU             | N/A                      | Default      |              |              |            |              |             |                   |
| FRAM            | N/A                      | Default      |              |              |            |              |             |                   |
| RAM             | N/A                      | Default      |              |              |            |              |             |                   |
| CRC             | N/A                      | Default      |              |              |            |              |             |                   |
| I/O             | N/A                      | Default      |              |              |            |              |             |                   |
| TA0             | TASSEL                   |              | 10b          | 01b          |            |              |             | 00b (TA0CLK pin)  |
| TA1             | TASSEL                   |              | 10b          | 01b          |            |              |             | 00b (TA1CLK pin)  |
| TA2             | TASSEL                   |              | 10b          | 01b          |            |              |             |                   |
| TA3             | TASSEL                   |              | 10b          | 01b          |            |              |             |                   |
| eUSCI_A0        | UCSSEL                   |              | 10b or 11b   |              | 01b        |              |             | 00b (UCA0CLK pin) |
| eUSCI_A1        | UCSSEL                   |              | 10b or 11b   |              | 01b        |              |             | 00b (UCA1CLK pin) |
| eUSCI_B0        | UCSSEL                   |              | 10b or 11b   |              | 01b        |              |             | 00b (UCB0CLK pin) |
| WDT             | WDTSSEL                  |              | 00b          | 01b          |            |              | 10b or 11b  |                   |
| ADC             | ADCSSEL                  |              | 11b          | 01b          | 00b        |              |             |                   |
| CapTlvate       | CAPTSSEL                 |              |              | 00b          |            |              | 01b         |                   |
|                 | CAPCLKSEL                |              | 1b           |              |            |              |             |                   |
| RTC             | RTCSS                    |              | 01b          |              |            | 10b          | 11b         |                   |

### 6.10.3 General-Purpose Input/Output Port (I/O)

Up to 19 I/O ports are implemented.

- P1 and P2 are full 8-bit ports; P3 has 3 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- CapTlvate functionality is supported on all CAPx.y pins.

#### NOTE

##### Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the *MP430FR4xx and MP430FR2xx Family User's Guide (SLAU445)*

#### 6.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals. [Table 6-8](#) lists the system clocks that can be used to source the WDT.

**Table 6-8. WDT Clocks**

| WDTSEL | NORMAL OPERATION<br>(WATCHDOG AND INTERVAL TIMER MODE) |
|--------|--|
| 00     | SMCLK  |
| 01     | ACLK   |
| 10     | VLOCLK   |
| 11     | Reserved   |

### 6.10.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These features include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application. [Table 6-9](#) summarizes the interrupts that are managed by the SYS module.

**Table 6-9. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS         | INTERRUPT EVENT                          | VALUE      | PRIORITY |
|---------------------------|-----------------|--|------------|----------|
| SYSRSTIV, System Reset    | 015Eh           | No interrupt pending                     | 00h        |          |
|                           |                 | Brownout (BOR)                           | 02h        | Highest  |
|                           |                 | RSTIFG RST/NMI (BOR)                     | 04h        |          |
|                           |                 | PMMSWBOR software BOR (BOR)              | 06h        |          |
|                           |                 | LPMx.5 wake up (BOR)                     | 08h        |          |
|                           |                 | Security violation (BOR)                 | 0Ah        |          |
|                           |                 | Reserved                                 | 0Ch        |          |
|                           |                 | SVSHIFG SVSH event (BOR)                 | 0Eh        |          |
|                           |                 | Reserved                                 | 10h        |          |
|                           |                 | Reserved                                 | 12h        |          |
|                           |                 | PMMSWPOR software POR (POR)              | 14h        |          |
|                           |                 | WDTIFG watchdog time-out (PUC)           | 16h        |          |
|                           |                 | WDTPW password violation (PUC)           | 18h        |          |
|                           |                 | FRCTLPW password violation (PUC)         | 1Ah        |          |
|                           |                 | Uncorrectable FRAM bit error detection   | 1Ch        |          |
|                           |                 | Peripheral area fetch (PUC)              | 1Eh        |          |
|                           |                 | PMMPW PMM password violation (PUC)       | 20h        |          |
|                           |                 | FLL unlock (PUC)                         | 24h        |          |
| Reserved                  | 22h, 26h to 3Eh | Lowest                                   |            |          |
| SYSSNIV, System NMI       | 015Ch           | No interrupt pending                     | 00h        |          |
|                           |                 | SVS low-power reset entry                | 02h        | Highest  |
|                           |                 | Uncorrectable FRAM bit error detection   | 04h        |          |
|                           |                 | Reserved                                 | 06h        |          |
|                           |                 | Reserved                                 | 08h        |          |
|                           |                 | Reserved                                 | 0Ah        |          |
|                           |                 | Reserved                                 | 0Ch        |          |
|                           |                 | Reserved                                 | 0Eh        |          |
|                           |                 | Reserved                                 | 10h        |          |
|                           |                 | VMAIFG Vacant memory access              | 12h        |          |
|                           |                 | JMBINIFG JTAG mailbox input              | 14h        |          |
|                           |                 | JMBOUTIFG JTAG mailbox output            | 16h        |          |
|                           |                 | Correctable FRAM bit error detection     | 18h        |          |
|                           |                 | Reserved                                 | 1Ah to 1Eh | Lowest   |
| SYSUNIV, User NMI         | 015Ah           | No interrupt pending                     | 00h        |          |
|                           |                 | NMIIFG NMI pin or SVS <sub>H</sub> event | 02h        | Highest  |
|                           |                 | OFIFG oscillator fault                   | 04h        |          |
|                           |                 | Reserved                                 | 06h to 1Eh | Lowest   |

### 6.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of  $x^{16} + x^{12} + x^5 + 1$ .

### 6.10.7 Enhanced Universal Serial Communication Interface (eUSCI\_A0, eUSCI\_B0)

The eUSCI modules are used for serial data communications. The eUSCI\_A module supports either UART or SPI communications. The eUSCI\_B module supports either SPI or I<sup>2</sup>C communications. Additionally, eUSCI\_A supports automatic baud-rate detection and IrDA. [Table 6-10](#) lists the pin configurations that are required for each eUSCI mode.

**Table 6-10. eUSCI Pin Configurations**

|          | PIN  | UART             | SPI  |
|----------|------|------------------|------|
| eUSCI_A0 | P1.4 | TXD              | SIMO |
|          | P1.5 | RXD              | SOMI |
|          | P1.6 | –                | SCLK |
|          | P1.7 | –                | STE  |
| eUSCI_A1 | P2.6 | TXD              | SIMO |
|          | P2.5 | RXD              | SOMI |
|          | P2.4 | –                | SCLK |
|          | P3.1 | –                | STE  |
| eUSCI_B0 | PIN  | I <sup>2</sup> C | SPI  |
|          | P1.0 | –                | STE  |
|          | P1.1 | –                | SCLK |
|          | P1.2 | SDA              | SIMO |
|          | P1.3 | SCL              | SOMI |

### 6.10.8 Timers (Timer0\_A3, Timer1\_A3, Timer2\_A2 and Timer3\_A2)

The Timer0\_A3 and Timer1\_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each timer supports multiple captures or compares, PWM outputs, and interval timing (see [Table 6-11](#) and [Table 6-12](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both Timer0\_A3 and Timer1\_A3 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter.

**Table 6-11. Timer0\_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME   | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL            |      |     |                       |
|----------|---------------------|---------------------|--------------|----------------------|---------------------------------|------|-----|-----------------------|
| P1.0     | TA0CLK              | TACLK               | Timer        | N/A                  |                                 |      |     |                       |
|          | ACLK (internal)     | ACLK                |              |                      |                                 |      |     |                       |
|          | SMCLK (internal)    | SMCLK               |              |                      |                                 |      |     |                       |
|          |                     | CCI0A               | CCR0         | TA0                  |                                 |      |     |                       |
|          |                     | CCI0B               |              |                      | Timer1_A3 CCI0B input           |      |     |                       |
|          | DVSS                | GND                 |              |                      |                                 |      |     |                       |
|          | DVCC                | VCC                 |              |                      |                                 |      |     |                       |
|          | P1.1                | TA0.1               |              |                      | CCI1A                           | CCR1 | TA1 | TA0.1                 |
|          |                     | from RTC (internal) |              |                      | CCI1B                           |      |     | Timer1_A3 CCI1B input |
| DVSS     |                     | GND                 |              |                      |                                 |      |     |                       |
|          | DVCC                | VCC                 |              |                      |                                 |      |     |                       |
| P1.2     | TA0.2               | CCI2A               | CCR2         | TA2                  | TA0.2                           |      |     |                       |
|          |                     | CCI2B               |              |                      | Timer1_A3 CCI2B input, IR Input |      |     |                       |
|          | DVSS                | GND                 |              |                      |                                 |      |     |                       |
|          | DVCC                | VCC                 |              |                      |                                 |      |     |                       |

**Table 6-12. Timer1\_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL               | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|----------|-----------------------------------|-------------------|--------------|----------------------|----------------------|
| P1.6     | TA1CLK                            | TACLK             | Timer        | N/A                  |                      |
|          | ACLK (internal)                   | ACLK              |              |                      |                      |
|          | SMCLK (internal)                  | SMCLK             |              |                      |                      |
|          |                                   | CCI0A             | CCR0         | TA0                  |                      |
|          | Timer0_A3 CCR0B output (internal) | CCI0B             |              |                      |                      |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |
|          |                                   |                   |              |                      |                      |
| P1.5     | TA1.1                             | CCI1A             | CCR1         | TA1                  | TA1.1                |
|          | Timer0_A3 CCR1B output (internal) | CCI1B             |              |                      | to ADC trigger       |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |
| P1.4     | TA1.2                             | CCI2A             | CCR2         | TA2                  | TA1.2                |
|          | Timer0_A3 CCR2B output (internal) | CCI2B             |              |                      | IR Input             |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |

The interconnection of Timer0\_A3 and Timer1\_A3 can be used to modulate the eUSCI\_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the *MP430FR4xx and MP430FR2xx Family User's Guide (SLAU445)*.

The Timer2\_A2 and Timer3\_A2 modules are 16-bit timers and counters with two capture/compare registers each. Each timer supports multiple captures or compares and interval timing (see [Table 6-13](#) and [Table 6-14](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture registers. The CCR0 registers on both Timer2\_TA2 and Timer3\_TA2 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter. The Timer2\_A2 and Timer3\_A2 are only internal connected and do not support PWM output.

**Table 6-13. Timer2\_A2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |                       |
|---------------------|-------------------|--------------|----------------------|----------------------|-----------------------|
| ACLK (internal)     | ACLK              | Timer        | N/A                  |                      |                       |
| SMCLK (internal)    | SMCLK             |              |                      |                      |                       |
|                     |                   | CCR0         | TA0                  |                      |                       |
|                     |                   |              |                      | CCI0A                | Timer3_A3 CCI0B input |
|                     | DVSS              |              |                      | GND                  |                       |
|                     | DVCC              |              |                      | VCC                  |                       |
|                     |                   | CCR1         | CCR1                 |                      |                       |
|                     |                   |              |                      | CCI1A                | Timer3_A3 CCI1B input |
|                     | DVSS              |              |                      | GND                  |                       |
|                     | DVCC              |              |                      | VCC                  |                       |

**Table 6-14. Timer3\_A2 Signal Connections**

| DEVICE INPUT SIGNAL   | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|-----------------------|-------------------|--------------|----------------------|----------------------|
| ACLK (internal)       | ACLK              | Timer        | N/A                  |                      |
| SMCLK (internal)      | SMCLK             |              |                      |                      |
|                       | CCI0A             | CCR0         | TA0                  |                      |
| Timer3_A3 CCI0B input | CCI0B             |              |                      |                      |
| DVSS                  | GND               |              |                      |                      |
| DVCC                  | VCC               |              |                      |                      |
|                       | CCI1A             | CCR1         | CCR1                 |                      |
| Timer3_A3 CCI1B input | CCI1B             |              |                      |                      |
| DVSS                  | GND               |              |                      |                      |
| DVCC                  | VCC               |              |                      |                      |

### 6.10.9 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The MPY module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

### 6.10.10 Backup Memory (BKMEM)

The BKMEM supports data retention during LPM3.5. This device provides up to 32 bytes that are retained during LPM3.5.

### 6.10.11 Real-Time Clock (RTC)

The RTC is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3 and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0\_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

### 6.10.12 10-Bit Analog-to-Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and 4 internal inputs (see [Table 6-15](#)).

**Table 6-15. ADC Channel Connections**

| ADC <sub>SHSx</sub> | ADC CHANNELS               | EXTERNAL PINOUT |
|---------------------|----------------------------|-----------------|
| 0                   | A0/V <sub>ref</sub> +      | P1.0            |
| 1                   | A1                         | P1.1            |
| 2                   | A2/V <sub>ref</sub> -      | P1.2            |
| 3                   | A3                         | P1.3            |
| 4                   | A4 <sup>(1)</sup>          | P1.4            |
| 5                   | A5                         | P1.5            |
| 6                   | A6                         | P1.6            |
| 7                   | A7                         | P1.7            |
| 8                   | A8                         | NA              |
| 9                   | A9                         | NA              |
| 10                  | Not used                   | N/A             |
| 11                  | Not used                   | N/A             |
| 12                  | On-chip temperature sensor | N/A             |
| 13                  | Reference voltage (1.5 V)  | N/A             |
| 14                  | DVSS                       | N/A             |
| 15                  | DVCC                       | N/A             |

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.

The analog-to-digital conversion can be started by software or a hardware trigger. [Table 6-16](#) lists the trigger sources that are available.

**Table 6-16. ADC Trigger Signal Connections**

| ADCINCH <sub>x</sub> |         | TRIGGER SOURCE               |
|----------------------|---------|------------------------------|
| BINARY               | DECIMAL |                              |
| 00                   | 0       | ADCSC bit (software trigger) |
| 01                   | 1       | RTC event                    |
| 10                   | 2       | TA1.1B                       |
| 11                   | 3       | TA1.2B                       |



### 6.10.13 CapTivate

The CapTivate module detects the capacitance changed with a charge-transfer method and is functional in AM, LPM0, and LPM3. The CapTivate module can periodically wake the CPU from LPM0 or LPM3 based on a timer source such as the ACLK and VLO clocks. The CapTivate module supports the following touch-sensing capability:

- Up to 64 CapTivate sense channels composed of 4 CapTivate blocks. Each block consists of 4 I/Os, and these blocks scan in parallel of 4 electrodes.
- Each block can be individually configured in self or mutual mode. Each CapTivate I/O can be used for either self or mutual electrodes.
- Supports a wake-on-touch state machine.
- Supports synchronized conversion on a zero-crossing event trigger.
- Processing logic to perform filter calculation and threshold detection.

### 6.10.14 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level
- EEM version: S

## 6.11 Input/Output Schematics

### 6.11.1 Port P1 Input/Output With Schmitt Trigger

Figure 6-1 shows the port schematic. Table 6-17 summarizes the selection of pin function.

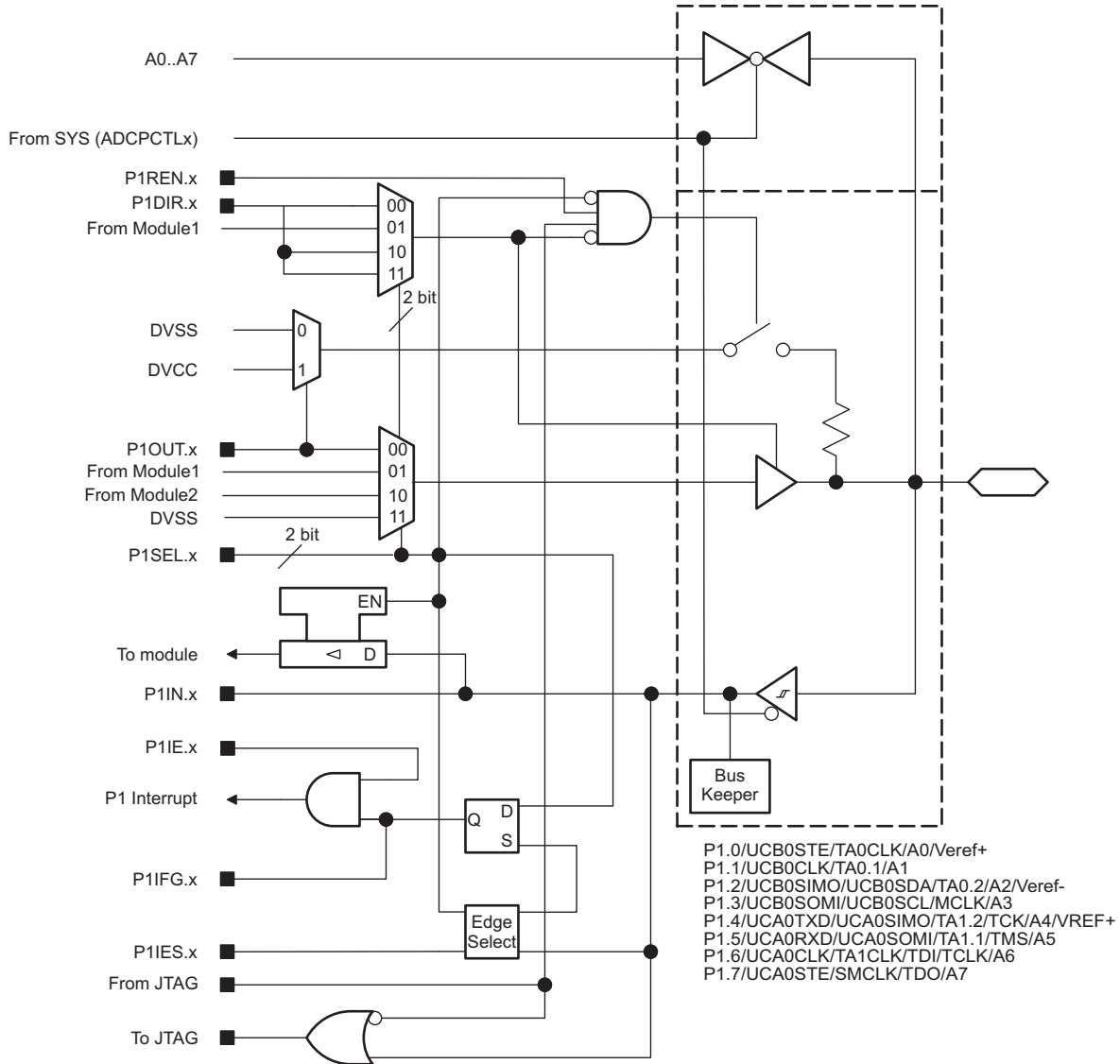


Figure 6-1. Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

**Table 6-17. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x)                                   | x | FUNCTION         | CONTROL BITS AND SIGNALS <sup>(1)</sup> |        |                         |          |
|---|---|------------------|---|--------|-------------------------|----------|
|   |   |                  | P1DIR.x                                 | P1SELx | ADCPCTLx <sup>(2)</sup> | JTAG     |
| P1.0/UCB0STE/<br>TA0CLK/A0                        | 0 | P1.0 (I/O)       | I: 0; O: 1                              | 00     | 0                       | N/A      |
|   |   | UCB0STE          | X                                       | 01     | 0                       | N/A      |
|   |   | TA0CLK           | 0                                       | 10     | 0                       | N/A      |
|   |   | A0/Veref+        | X                                       | X      | 1 (x = 0)               | N/A      |
| P1.1/UCB0CLK/TA0.1/<br>A1                         | 1 | P1.1 (I/O)       | I: 0; O: 1                              | 00     | 0                       | N/A      |
|   |   | UCB0CLK          | X                                       | 01     | 0                       | N/A      |
|   |   | TA0.CCI1A        | 0                                       | 10     | 0                       | N/A      |
|   |   | TA0.1            | 1                                       |        |                         |          |
|   |   | A1               | X                                       | X      | 1 (x = 1)               | N/A      |
| P1.2/UCB0SIMO/<br>UCB0SDA/TA0.2/A2                | 2 | P1.2 (I/O)       | I: 0; O: 1                              | 00     | 0                       | N/A      |
|   |   | UCB0SIMO/UCB0SDA | X                                       | 01     | 0                       | N/A      |
|   |   | TA0.CCI2A        | 0                                       | 10     | 0                       | N/A      |
|   |   | TA0.2            | 1                                       |        |                         |          |
|   |   | A2/Veref-        | X                                       | X      | 1 (x = 2)               | N/A      |
| P1.3/UCB0SOMI/<br>UCB0SCL/MCLK/A3                 | 3 | P1.3 (I/O)       | I: 0; O: 1                              | 00     | 0                       | N/A      |
|   |   | UCB0SOMI/UCB0SCL | X                                       | 01     | 0                       | N/A      |
|   |   | MCLK             | 1                                       | 10     | 0                       | N/A      |
|   |   | A3               | X                                       | X      | 1 (x = 3)               | N/A      |
| P1.4/UCA0TXD/<br>UCA0SIMO/TA1.2/TCK/<br>A4 /VREF+ | 4 | P1.4 (I/O)       | I: 0; O: 1                              | 00     | 0                       | Disabled |
|   |   | UCA0TXD/UCA0SIMO | X                                       | 01     | 0                       | Disabled |
|   |   | TA1.CCI2A        | 0                                       | 10     | 0                       | Disabled |
|   |   | TA1.2            | 1                                       |        |                         |          |
|   |   | A4, VREF+        | X                                       | X      | 1 (x = 4)               | Disabled |
|   |   | JTAG TCK         | X                                       | X      | X                       | TCK      |
| P1.5/UCA0RXD/<br>UCA0SOMI/TA1.1/TMS/<br>A5        | 5 | P1.5 (I/O)       | I: 0; O: 1                              | 00     | 0                       | Disabled |
|   |   | UCA0RXD/UCA0SOMI | X                                       | 01     | 0                       | Disabled |
|   |   | TA1.CCI1A        | 0                                       | 10     | 0                       | Disabled |
|   |   | TA1.1            | 1                                       |        |                         |          |
|   |   | A5               | X                                       | X      | 1 (x = 5)               | Disabled |
|   |   | JTAG TMS         | X                                       | X      | X                       | TMS      |
| P1.6/UCA0CLK/<br>TA1CLK/TDI/TCLK/A6               | 6 | P1.6 (I/O)       | I: 0; O: 1                              | 00     | 0                       | Disabled |
|   |   | UCA0CLK          | X                                       | 01     |                         | Disabled |
|   |   | TA1CLK           | 0                                       | 10     | 0                       | Disabled |
|   |   | A6               | X                                       | X      | 1 (x = 6)               | Disabled |
|   |   | JTAG TDI/TCLK    | X                                       | X      | X                       | TDI/TCLK |
| P1.7/UCA0STE/SMCLK/<br>TDO/A7                     | 7 | P1.7 (I/O)       | I: 0; O: 1                              | 00     | 0                       | Disabled |
|   |   | UCA0STE          | X                                       | 01     | 0                       | Disabled |
|   |   | SMCLK            | 1                                       | 10     | 0                       | Disabled |
|   |   | A7               | X                                       | X      | 1 (x = 7)               | Disabled |
|   |   | JTAG TDO         | X                                       | X      | X                       | TDO      |

(1) X = don't care

(2) Setting the ADCPCTLx bit in SYSCFG2 register disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

### 6.11.2 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

Figure 6-2 shows the port schematic. Table 6-18 summarizes the selection of pin function.

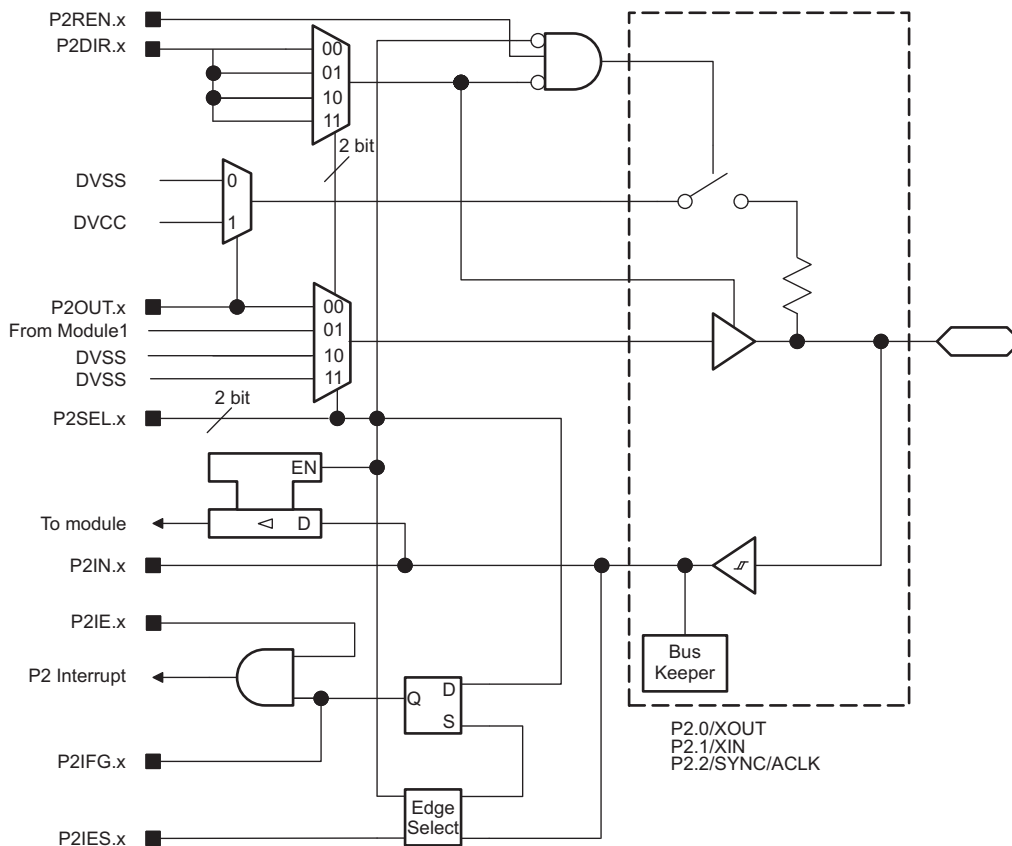


Figure 6-2. Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

Table 6-18. Port P2 (P2.0 to P2.2) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |        |
|-----------------|---|------------|---|--------|
|                 |   |            | P2DIR.x                                 | P2SELx |
| P2.0/XOUT       | 0 | P2.0 (I/O) | I: 0; O: 1                              | 00     |
|                 |   | XOUT       | 1                                       | 01     |
| P2.1/XIN        | 1 | P2.1 (I/O) | I: 0; O: 1                              | 00     |
|                 |   | XIN        | 0                                       | 01     |
| P2.2/SYNC/ACLK  | 2 | P2.2 (I/O) | I: 0; O: 1                              | 00     |
|                 |   | SYNC       | 0                                       | 01     |
|                 |   | ACLK       | 1                                       | 10     |

(1) X = don't care

### 6.11.3 Port P2 (P2.3 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port schematic. Table 6-19 summarizes the selection of pin function.

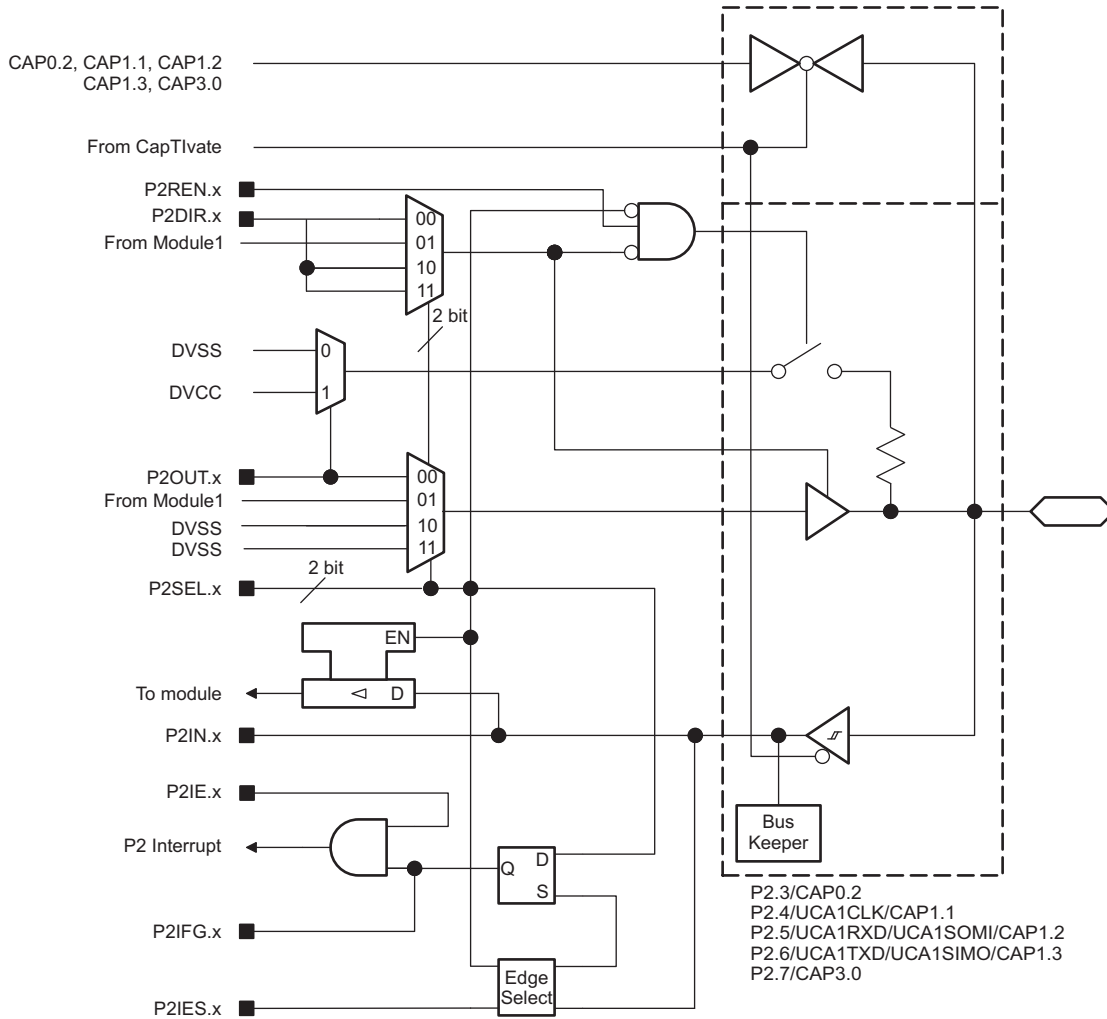


Figure 6-3. Port P2 (P2.3 to P2.7) Input/Output With Schmitt Trigger

**Table 6-19. Port P2 (P2.3 to P2.7) Pin Functions**

| PIN NAME (P2.x)                  | x | FUNCTION         | CONTROL BITS AND SIGNALS <sup>(1)</sup> |        |                 |
|----------------------------------|---|------------------|---|--------|-----------------|
|                                  |   |                  | P2DIR.x                                 | P2SELx | ANALOG FUNCTION |
| P2.3/CAP0.2                      | 3 | P2.3 (I/O)       | I: 0; O: 1                              | 00     | 0               |
|                                  |   | CAP0.2           | X                                       | X      | 1               |
| P2.4/UCA1CLK/<br>CAP1.1          | 4 | P2.4 (I/O)       | I: 0; O: 1                              | 00     | 0               |
|                                  |   | UCA1CLK          | X                                       | 01     | 0               |
|                                  |   | CAP1.1           | X                                       | X      | 1               |
| P2.5/UCA1RXD/<br>UCA1SOMI/CAP1.2 | 5 | P2.5 (I/O)       | I: 0; O: 1                              | 00     | 0               |
|                                  |   | UCA1RXD/UCA1SOMI | X                                       | 01     | 0               |
|                                  |   | CAP1.2           | X                                       | X      | 1               |
| P2.6/UCA1TXD/<br>UCA1SIMO/CAP1.3 | 6 | P2.6 (I/O)       | I: 0; O: 1                              | 00     | 0               |
|                                  |   | UCA1TXD/UCA1SIMO | X                                       | 01     | 0               |
|                                  |   | CAP1.3           | X                                       | X      | 1               |
| P2.7/CAP3.0                      | 7 | P2.7 (I/O)       | I: 0; O: 1                              | 0      | 0               |
|                                  |   | CAP3.0           | X                                       | X      | 1               |

(1) X = don't care

### 6.11.4 Port P3 (P3.0 to P3.2) Input/Output With Schmitt Trigger

Figure 6-4 shows the port schematic. Table 6-20 summarizes the selection of pin function.

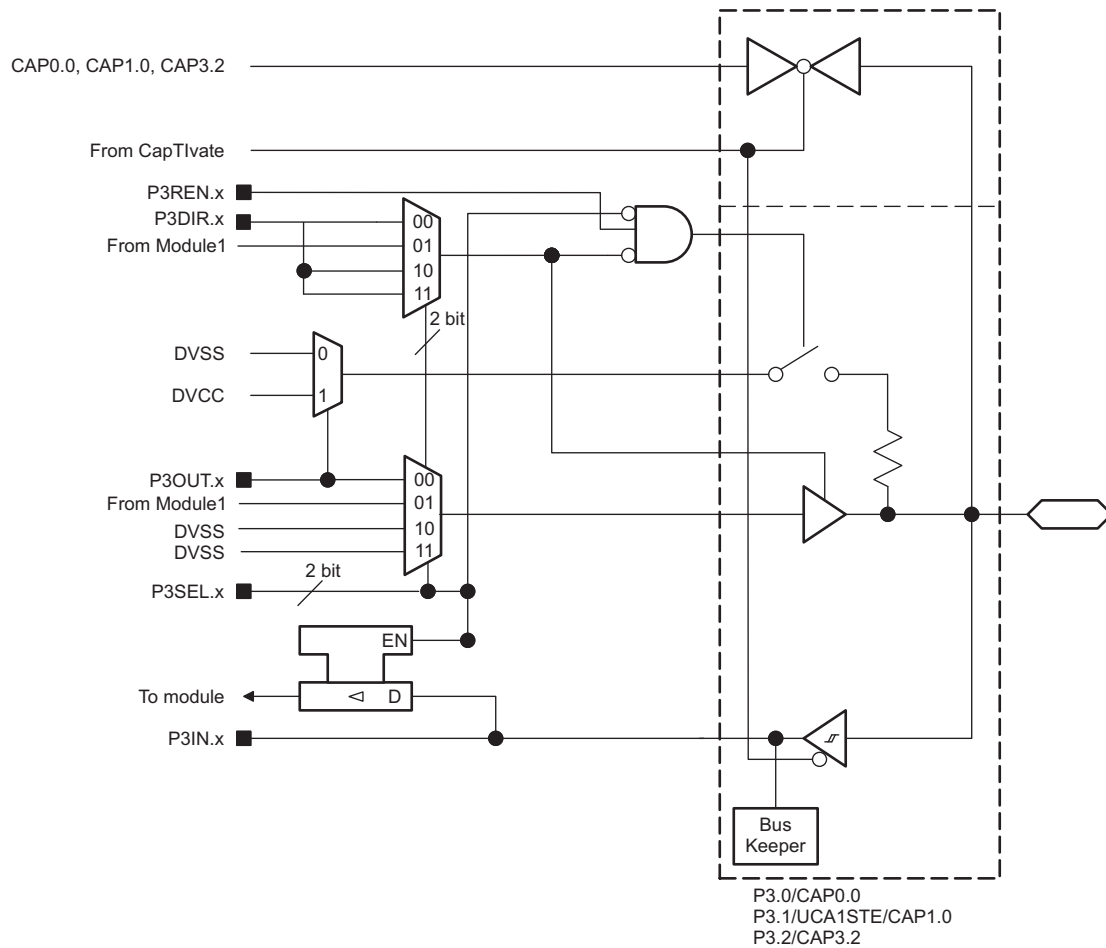


Figure 6-4. Port P3 (P3.0 to P3.2) Input/Output With Schmitt Trigger

#### NOTE

##### CapTlvate shared with I/Os configuration

The CapTlvate function and GPIOs are powered by different power supplies (1.5 V and 3.3 V, respectively).

To prevent pad damage when changing the function, TI recommends checking the external application circuit of each pad before enabling the alternate function.

**Table 6-20. Port P3 (P3.0 to P3.2) Pin Functions**

| PIN NAME (P3.x)         | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |                 |
|-------------------------|---|------------|---|---------|-----------------|
|                         |   |            | P3DIR.x                                 | P3SEL.x | ANALOG FUNCTION |
| P3.0/CAP0.0             | 0 | P3.0 (I/O) | I: 0; O: 1                              | 00      | 0               |
|                         |   | CAP0.0     | X                                       | X       | 1               |
| P3.1/UCA1STE/<br>CAP1.0 | 1 | P3.1 (I/O) | I: 0; O: 1                              | 00      | 0               |
|                         |   | UCA1STE    | X                                       | 01      | 0               |
|                         |   | CAP1.0     | X                                       | X       | 1               |
| P3.2/CAP3.2             | 2 | P3.2 (I/O) | I: 0; O: 1                              | 00      | 0               |
|                         |   | CAP3.2     | X                                       | X       | 1               |

(1) X = don't care



## 6.12 Device Descriptors

Table 6-21 lists the Device IDs of the devices. Table 6-22 lists the contents of the device descriptor tag-length-value (TLV) structure for the devices.

**Table 6-21. Device IDs**

| DEVICE       | DEVICE ID |       |
|--------------|-----------|-------|
|              | 1A05h     | 1A04h |
| MSP430FR2633 | 82h       | 3Ch   |
| MSP430FR2533 | 82h       | 3Dh   |
| MSP430FR2632 | 82h       | 3Eh   |
| MSP430FR2532 | 82h       | 3Fh   |

**Table 6-22. Device Descriptors**

| DESCRIPTION                          |                                      | MSP430FR2633, MSP430FR2632,<br>MSP430FR2533, MSP430FR2532 |                |
|--------------------------------------|--------------------------------------|---|----------------|
|                                      |                                      | ADDRESS   | VALUE          |
| Information Block                    | Info length                          | 1A00h   | 06h            |
|                                      | CRC length                           | 1A01h   | 06h            |
|                                      | CRC value <sup>(1)</sup>             | 1A02h   | per unit       |
|                                      |                                      | 1A03h   | per unit       |
|                                      | Device ID                            | 1A04h   | See Table 6-21 |
|                                      |                                      | 1A05h   |                |
|                                      | Hardware revision                    | 1A06h   | per unit       |
| Firmware revision                    | 1A07h                                | per unit  |                |
| Die Record                           | Die record tag                       | 1A08h   | 08h            |
|                                      | Die record length                    | 1A09h   | 0Ah            |
|                                      | Lot wafer ID                         | 1A0Ah   | per unit       |
|                                      |                                      | 1A0Bh   | per unit       |
|                                      |                                      | 1A0Ch   | per unit       |
|                                      |                                      | 1A0Dh   | per unit       |
|                                      | Die X position                       | 1A0Eh   | per unit       |
|                                      |                                      | 1A0Fh   | per unit       |
|                                      | Die Y position                       | 1A10h   | per unit       |
|                                      |                                      | 1A11h   | per unit       |
| Test result                          | 1A12h                                | per unit  |                |
|                                      | 1A13h                                | per unit  |                |
| ADC Calibration                      | ADC calibration tag                  | 1A14h   | per unit       |
|                                      | ADC calibration length               | 1A15h   | per unit       |
|                                      | ADC gain factor                      | 1A16h   | per unit       |
|                                      |                                      | 1A17h   | per unit       |
|                                      | ADC offset                           | 1A18h   | per unit       |
|                                      |                                      | 1A19h   | per unit       |
|                                      | ADC 1.5-V reference temperature 30°C | 1A1Ah   | per unit       |
|                                      |                                      | 1A1Bh   | per unit       |
| ADC 1.5-V reference temperature 85°C | 1A1Ch                                | per unit  |                |
|                                      | 1A1Dh                                | per unit  |                |

(1) The CRC value covers the check sum from 0x1A04h to 0x1AEFh by applying the CRC-CCITT-16 polynomial of  $x^{16} + x^{12} + x^5 + 1$ .

**Table 6-22. Device Descriptors (continued)**

| DESCRIPTION                   |   | MSP430FR2633, MSP430FR2632,<br>MSP430FR2533, MSP430FR2532 |          |
|-------------------------------|---|---|----------|
|                               |   | ADDRESS   | VALUE    |
| Reference and DCO Calibration | Calibration tag   | 1A1Eh   | 12h      |
|                               | Calibration length  | 1A1Fh   | 04h      |
|                               | 1.5-V reference factor                                      | 1A20h   | per unit |
|                               |   | 1A21h   | per unit |
|                               | DCO tap setting for 16 MHz, temperature 30°C <sup>(2)</sup> | 1A22h   | per unit |
| 1A23h                         |   | per unit  |          |

- (2) This value can be directly loaded into DCO bits in CSCTL0 registers to get accurate 16-MHz frequency at room temperature, especially when the MCU exits from LPM3 and below. TI suggests using the predivider to decrease the frequency if the temperature drift might result an overshoot beyond 16 MHz.

## 6.13 Memory

### 6.13.1 Memory Organization

Table 6-23 summarizes the memory organization of the devices.

**Table 6-23. Memory Organization**

|  | ACCESS  | MSP430FR2633                       | MSP430FR2632                      | MSP430FR2533                       | MSP430FR2532                      |
|--|---|------------------------------------|-----------------------------------|------------------------------------|-----------------------------------|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Read/Write<br>(Optional Write Protect) <sup>(1)</sup> | 15KB<br>FFFFh–FF80h<br>FFFFh–C400h | 8KB<br>FFFFh–FF80h<br>FFFFh–E000h | 15KB<br>FFFFh–FF80h<br>FFFFh–C400h | 8KB<br>FFFFh–FF80h<br>FFFFh–E000h |
| RAM  | Read/Write  | 4KB<br>2FFFh–2000h                 | 2KB<br>27FFh–2000h                | 2KB<br>27FFh–2000h                 | 1KB<br>23FFh–2000h                |
| Information Memory (FRAM)  | Read/Write<br>(Optional Write Protect) <sup>(2)</sup> | 512B<br>19FFh–1800h                | 512B<br>19FFh–1800h               | 512B<br>19FFh–1800h                | 512B<br>19FFh–1800h               |
| Bootstrap loader (BSL1)<br>Memory (ROM)                                      | Read only   | 2KB<br>17FFh–1000h                 | 2KB<br>17FFh–1000h                | 2KB<br>17FFh–1000h                 | 2KB<br>17FFh–1000h                |
| Bootstrap loader (BSL2)<br>Memory (ROM)                                      | Read only   | 1KB<br>FFFFh–FFC00h                | 1KB<br>FFFFh–FFC00h               | 1KB<br>FFFFh–FFC00h                | 1KB<br>FFFFh–FFC00h               |
| CapTIvate Libraries and<br>Driver Libraries (ROM)                            | Read only   | 12KB<br>6FFFh–4000h                | 12KB<br>6FFFh–4000h               | 12KB<br>6FFFh–4000h                | 12KB<br>6FFFh–4000h               |
| Peripherals  | Read/Write  | 4KB<br>0FFFh–0000h                 | 4KB<br>0FFFh–0000h                | 4KB<br>0FFFh–0000h                 | 4KB<br>0FFFh–0000h                |

- (1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in *MSP430FR2633 Family User's Guide (SLAU445)* for more details
- (2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in *MSP430FR2633 Family User's Guide (SLAU445)* for more details

### 6.13.2 Peripheral File Map

Table 6-24 lists the available peripherals and the register base address for each. Table 6-25 through list the registers and address offsets for each peripheral.

**Table 6-24. Peripherals Summary**

| MODULE NAME  | BASE ADDRESS | SIZE  |
|--|--------------|-------|
| Special Functions (See Table 6-25)                                   | 0100h        | 0010h |
| PMM (See Table 6-26)   | 0120h        | 0020h |
| SYS (See Table 6-27)   | 0140h        | 0040h |
| CS (See Table 6-28)  | 0180h        | 0020h |
| FRAM (See Table 6-29)  | 01A0h        | 0010h |
| CRC (See Table 6-30)   | 01C0h        | 0008h |
| WDT (See Table 6-31)   | 01CCh        | 0002h |
| Port P1, P2 (See Table 6-32)   | 0200h        | 0020h |
| Port P3 (See Table 6-33)   | 0220h        | 0020h |
| RTC (See Table 6-34)   | 0300h        | 0010h |
| Timer0_A3 (See Table 6-35)   | 0380h        | 0030h |
| Timer1_A3 (See Table 6-36)   | 03C0h        | 0030h |
| Timer2_A2 (See Table 6-37)   | 0400h        | 0030h |
| Timer3_A2 (See Table 6-38)   | 0440h        | 0030h |
| MPY32 (See Table 6-39)   | 04C0h        | 0030h |
| eUSCI_A0 (See Table 6-40)  | 0500h        | 0020h |
| eUSCI_A1 (See Table 6-41)  | 0520h        | 0020h |
| eUSCI_B0 (See Table 6-42)  | 0540h        | 0030h |
| Backup Memory (See Table 6-43)                                       | 0660h        | 0020h |
| ADC (See Table 6-44)   | 0700h        | 0040h |
| CapTivate (See <a href="#">CapTivate Design Center</a> for details ) | 0A00h        | 0200h |

**Table 6-25. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | ACRONYM | OFFSET |
|-----------------------|---------|--------|
| SFR interrupt enable  | SFRIE1  | 00h    |
| SFR interrupt flag    | SFRIFG1 | 02h    |
| SFR reset pin control | SFRRPCR | 04h    |

**Table 6-26. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| PMM control 0        | PMMCTL0 | 00h    |
| PMM control 1        | PMMCTL1 | 02h    |
| PMM control 2        | PMMCTL2 | 04h    |
| PMM interrupt flags  | PMMIFG  | 0Ah    |
| PM5 control 0        | PM5CTL0 | 10h    |

**Table 6-27. SYS Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION          | ACRONYM   | OFFSET |
|-------------------------------|-----------|--------|
| System control                | SYSCTL    | 00h    |
| Bootloader configuration area | SYSBSLC   | 02h    |
| JTAG mailbox control          | SYSJMBC   | 06h    |
| JTAG mailbox input 0          | SYSJMBI0  | 08h    |
| JTAG mailbox input 1          | SYSJMBI1  | 0Ah    |
| JTAG mailbox output 0         | SYSJMBO0  | 0Ch    |
| JTAG mailbox output 1         | SYSJMBO1  | 0Eh    |
| Bus error vector generator    | SYSBERRIV | 18h    |
| User NMI vector generator     | SYSUNIV   | 1Ah    |
| System NMI vector generator   | SYSSNIV   | 1Ch    |
| Reset vector generator        | SYSRSTIV  | 1Eh    |
| System configuration 0        | SYSCFG0   | 20h    |
| System configuration 1        | SYSCFG1   | 22h    |
| System configuration 2        | SYSCFG2   | 24h    |

**Table 6-28. CS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| CS control 0         | CSCTL0  | 00h    |
| CS control 1         | CSCTL1  | 02h    |
| CS control 2         | CSCTL2  | 04h    |
| CS control 3         | CSCTL3  | 06h    |
| CS control 4         | CSCTL4  | 08h    |
| CS control 5         | CSCTL5  | 0Ah    |
| CS control 6         | CSCTL6  | 0Ch    |
| CS control 7         | CSCTL7  | 0Eh    |
| CS control 8         | CSCTL8  | 10h    |

**Table 6-29. FRAM Registers (Base Address: 01A0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| FRAM control 0       | FRCTL0  | 00h    |
| General control 0    | GCCTL0  | 04h    |
| General control 1    | GCCTL1  | 06h    |

**Table 6-30. CRC Registers (Base Address: 01C0h)**

| REGISTER DESCRIPTION          | ACRONYM   | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRC16DI   | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**Table 6-31. WDT Registers (Base Address: 01CCh)**

| REGISTER DESCRIPTION   | ACRONYM | OFFSET |
|------------------------|---------|--------|
| Watchdog timer control | WDTCTL  | 00h    |

**Table 6-32. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION          | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P1 input                 | P1IN    | 00h    |
| Port P1 output                | P1OUT   | 02h    |
| Port P1 direction             | P1DIR   | 04h    |
| Port P1 pulling enable        | P1REN   | 06h    |
| Port P1 selection 0           | P1SEL0  | 0Ah    |
| Port P1 selection 1           | P1SEL1  | 0Ch    |
| Port P1 interrupt vector word | P1IV    | 0Eh    |
| Port P1 interrupt edge select | P1IES   | 18h    |
| Port P1 interrupt enable      | P1IE    | 1Ah    |
| Port P1 interrupt flag        | P1IFG   | 1Ch    |
| Port P2 input                 | P2IN    | 01h    |
| Port P2 output                | P2OUT   | 03h    |
| Port P2 direction             | P2DIR   | 05h    |
| Port P2 pulling enable        | P2REN   | 07h    |
| Port P2 selection 0           | P2SEL0  | 0Bh    |
| Port P2 selection 1           | P2SEL1  | 0Ch    |
| Port P2 interrupt vector word | P2IV    | 1Eh    |
| Port P2 interrupt edge select | P2IES   | 19h    |
| Port P2 interrupt enable      | P2IE    | 1Bh    |
| Port P2 interrupt flag        | P2IFG   | 1Dh    |

**Table 6-33. Port P3 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION   | ACRONYM | OFFSET |
|------------------------|---------|--------|
| Port P3 input          | P3IN    | 00h    |
| Port P3 output         | P3OUT   | 02h    |
| Port P3 direction      | P3DIR   | 04h    |
| Port P3 pulling enable | P3REN   | 06h    |
| Port P3 selection 0    | P3SEL0  | 0Ah    |
| Port P3 selection 1    | P3SEL1  | 0      |

**Table 6-34. RTC Registers (Base Address: 0300h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| RTC control          | RTCCTL  | 00h    |
| RTC interrupt vector | RTCIV   | 04h    |
| RTC modulo           | RTCMOD  | 08h    |
| RTC counter          | RTCCNT  | 0Ch    |

**Table 6-35. Timer0\_A3 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA0 control               | TA0CTL   | 00h    |
| Capture/compare control 0 | TA0CCTL0 | 02h    |
| Capture/compare control 1 | TA0CCTL1 | 04h    |
| Capture/compare control 2 | TA0CCTL2 | 06h    |
| TA0 counter               | TA0R     | 10h    |
| Capture/compare 0         | TA0CCR0  | 12h    |
| Capture/compare 1         | TA0CCR1  | 14h    |
| Capture/compare 2         | TA0CCR2  | 16h    |
| TA0 expansion 0           | TA0EX0   | 20h    |
| TA0 interrupt vector      | TA0IV    | 2Eh    |

**Table 6-36. Timer1\_A3 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |
| TA1 counter               | TA1R     | 10h    |
| Capture/compare 0         | TA1CCR0  | 12h    |
| Capture/compare 1         | TA1CCR1  | 14h    |
| Capture/compare 2         | TA1CCR2  | 16h    |
| TA1 expansion 0           | TA1EX0   | 20h    |
| TA1 interrupt vector      | TA1IV    | 2Eh    |

**Table 6-37. Timer2\_A2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA2 control               | TA2CTL   | 00h    |
| Capture/compare control 0 | TA2CCTL0 | 02h    |
| Capture/compare control 1 | TA2CCTL1 | 04h    |
| TA2 counter               | TA2R     | 10h    |
| Capture/compare 0         | TA2CCR0  | 12h    |
| Capture/compare 1         | TA2CCR1  | 14h    |
| TA2 expansion 0           | TA2EX0   | 20h    |
| TA2 interrupt vector      | TA2IV    | 2Eh    |

**Table 6-38. Timer3\_A2 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION      | ACRONYM  | OFFSET |
|---------------------------|----------|--------|
| TA3 control               | TA3CTL   | 00h    |
| Capture/compare control 0 | TA3CCTL0 | 02h    |
| Capture/compare control 1 | TA3CCTL1 | 04h    |
| TA3 counter               | TA3R     | 10h    |
| Capture/compare 0         | TA3CCR0  | 12h    |
| Capture/compare 1         | TA3CCR1  | 14h    |
| TA3 expansion 0           | TA3EX0   | 20h    |
| TA3 interrupt vector      | TA3IV    | 2Eh    |

**Table 6-39. MPY32 Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | ACRONYM   | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2  | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension                                   | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1  | RES1      | 26h    |
| 32 × 32 result 2  | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control 0   | MPY32CTL0 | 2Ch    |

**Table 6-40. eUSCI\_A0 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION          | ACRONYM     | OFFSET |
|-------------------------------|-------------|--------|
| eUSCI_A control word 0        | UCA0CTLW0   | 00h    |
| eUSCI_A control word 1        | UCA0CTLW1   | 02h    |
| eUSCI_A control rate 0        | UCA0BR0     | 06h    |
| eUSCI_A control rate 1        | UCA0BR1     | 07h    |
| eUSCI_A modulation control    | UCA0MCTLW   | 08h    |
| eUSCI_A status                | UCA0STAT    | 0Ah    |
| eUSCI_A receive buffer        | UCA0RXBUF   | 0Ch    |
| eUSCI_A transmit buffer       | UCA0TXBUF   | 0Eh    |
| eUSCI_A LIN control           | UCA0ABCTL   | 10h    |
| eUSCI_A IrDA transmit control | IUCA0IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | IUCA0IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA0IE      | 1Ah    |
| eUSCI_A interrupt flags       | UCA0IFG     | 1Ch    |
| eUSCI_A interrupt vector word | UCA0IV      | 1Eh    |

**Table 6-41. eUSCI\_A1 Registers (Base Address: 0520h)**

| REGISTER DESCRIPTION          | ACRONYM     | OFFSET |
|-------------------------------|-------------|--------|
| eUSCI_A control word 0        | UCA1CTLW0   | 00h    |
| eUSCI_A control word 1        | UCA1CTLW1   | 02h    |
| eUSCI_A control rate 0        | UCA1BR0     | 06h    |
| eUSCI_A control rate 1        | UCA1BR1     | 07h    |
| eUSCI_A modulation control    | UCA1MCTLW   | 08h    |
| eUSCI_A status                | UCA1STAT    | 0Ah    |
| eUSCI_A receive buffer        | UCA1RXBUF   | 0Ch    |
| eUSCI_A transmit buffer       | UCA1TXBUF   | 0Eh    |
| eUSCI_A LIN control           | UCA1ABCTL   | 10h    |
| eUSCI_A IrDA transmit control | IUCA1IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | IUCA1IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA1IE      | 1Ah    |
| eUSCI_A interrupt flags       | UCA1IFG     | 1Ch    |
| eUSCI_A interrupt vector word | UCA1IV      | 1Eh    |

**Table 6-42. eUSCI\_B0 Registers (Base Address: 0540h)**

| REGISTER DESCRIPTION           | ACRONYM     | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB0CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB0CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB0BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB0BR1     | 07h    |
| eUSCI_B status word            | UCB0STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB0TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB0RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB0TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB0I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB0I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB0I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB0I2COA3  | 1Ah    |
| eUSCI_B receive address        | UCB0ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB0ADDMASK | 1Eh    |
| eUSCI_B I2C slave address      | UCB0I2CSA   | 20h    |
| eUSCI_B interrupt enable       | UCB0IE      | 2Ah    |
| eUSCI_B interrupt flags        | UCB0IFG     | 2Ch    |
| eUSCI_B interrupt vector word  | UCB0IV      | 2Eh    |



**Table 6-43. Backup Memory Registers (Base Address: 0660h)**

| REGISTER DESCRIPTION | ACRONYM  | OFFSET |
|----------------------|----------|--------|
| Backup memory 0      | BAKMEM0  | 00h    |
| Backup memory 1      | BAKMEM1  | 02h    |
| Backup memory 2      | BAKMEM2  | 04h    |
| Backup memory 3      | BAKMEM3  | 06h    |
| Backup memory 4      | BAKMEM4  | 08h    |
| Backup memory 5      | BAKMEM5  | 0Ah    |
| Backup memory 6      | BAKMEM6  | 0Ch    |
| Backup memory 7      | BAKMEM7  | 0Eh    |
| Backup memory 8      | BAKMEM8  | 10h    |
| Backup memory 9      | BAKMEM9  | 12h    |
| Backup memory 10     | BAKMEM10 | 14h    |
| Backup memory 11     | BAKMEM11 | 16h    |
| Backup memory 12     | BAKMEM12 | 18h    |
| Backup memory 13     | BAKMEM13 | 1Ah    |
| Backup memory 14     | BAKMEM14 | 1Ch    |
| Backup memory 15     | BAKMEM15 | 1Eh    |

**Table 6-44. ADC Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION                 | ACRONYM  | OFFSET |
|--------------------------------------|----------|--------|
| ADC control 0                        | ADCCTL0  | 00h    |
| ADC control 1                        | ADCCTL1  | 02h    |
| ADC control 2                        | ADCCTL2  | 04h    |
| ADC window comparator low threshold  | ADCLO    | 06h    |
| ADC window comparator high threshold | ADCHI    | 08h    |
| ADC memory control 0                 | ADCMCTL0 | 0Ah    |
| ADC conversion memory                | ADCMEM0  | 12h    |
| ADC interrupt enable                 | ADCIE    | 1Ah    |
| ADC interrupt flags                  | ADCIFG   | 1Ch    |
| ADC interrupt vector word            | ADCIV    | 1Eh    |

## 6.14 Identification

### 6.14.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see [Section 8.2](#)).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entries in [Section 6.12](#).

### 6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings (see [Section 8.2](#)).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entries in [Section 6.12](#).

### 6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming Via the JTAG Interface User's Guide* ([SLAU320](#)).

## 7 Applications, Implementation, and Layout

### NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

#### 7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10- $\mu$ F plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and to achieve high analog accuracy.

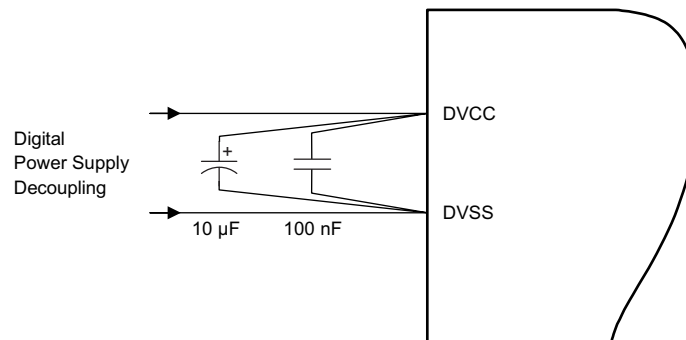


Figure 7-1. Power Supply Decoupling

#### 7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If the XIN and XOUT pins are not used, they must be terminated according to [Section 4.6](#).

Figure 7-2 shows a typical connection diagram.

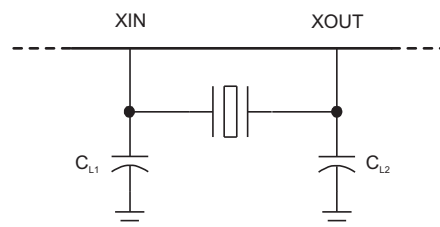


Figure 7-2. Typical Crystal Connection

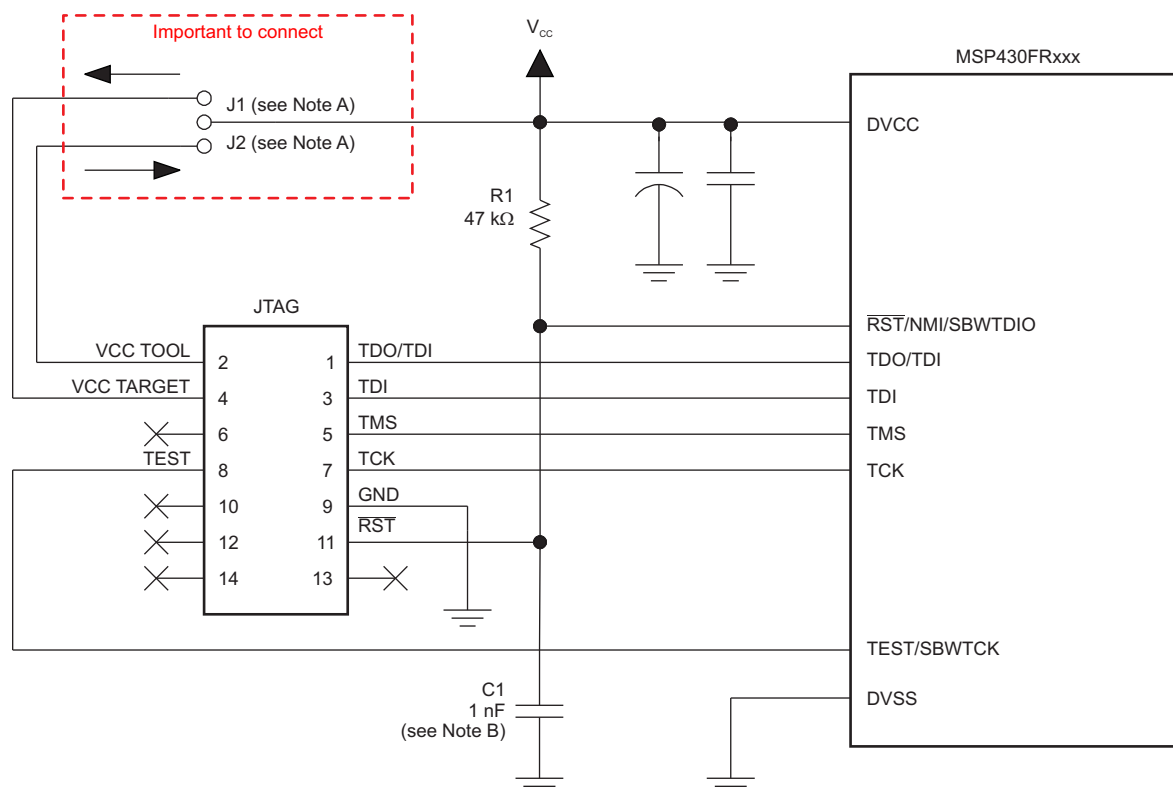
See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply  $V_{CC}$  to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a  $V_{CC}$  sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The  $V_{CC}$  sense feature detects the local  $V_{CC}$  present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying  $V_{CC}$  to the target board. If this flexibility is not required, the desired  $V_{CC}$  connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

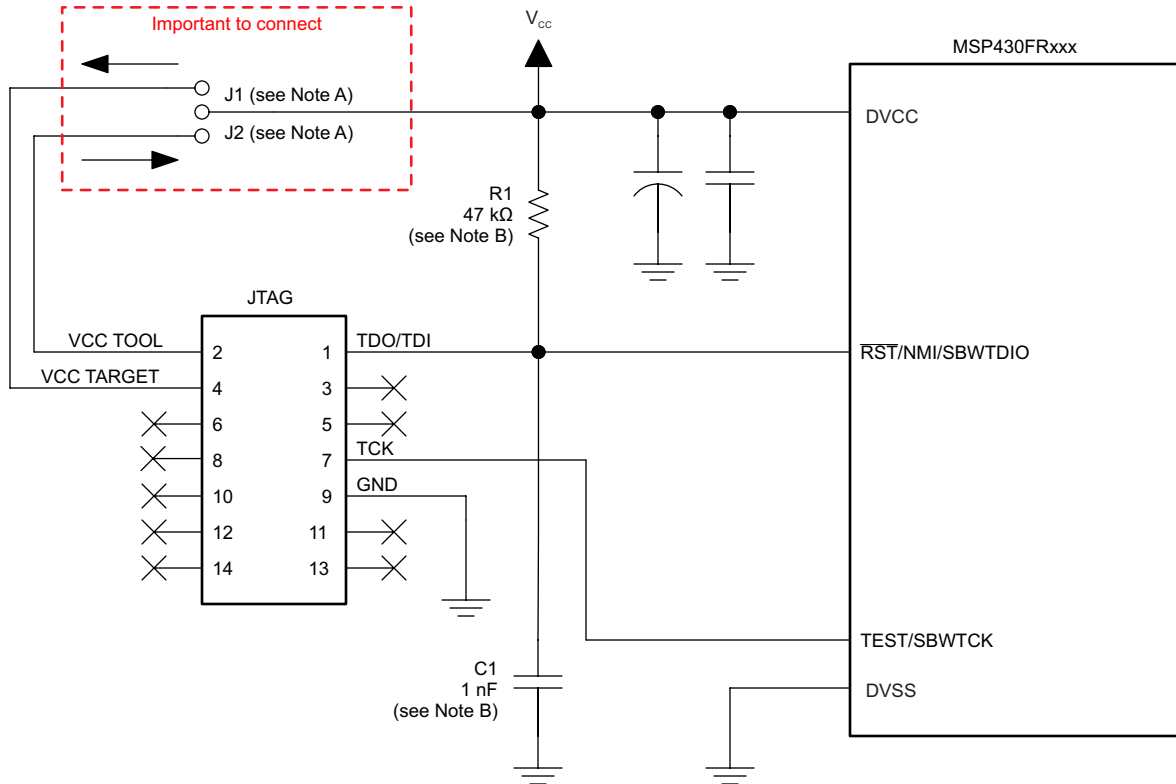
For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide* (SLAU278).



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- If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 7-3. Signal Connections for 4-Wire JTAG Communication**



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- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device  $\overline{\text{RST/NMI/SBWTIO}}$  pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the  $\overline{\text{RST/NMI}}$  pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the  $\overline{\text{RST/NMI}}$  pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The  $\overline{\text{RST/NMI}}$  pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the  $\overline{\text{RST/NMI}}$  pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k $\Omega$  pullup resistor to the  $\overline{\text{RST/NMI}}$  pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide (SLAU445)* for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.6](#).

### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322) for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Refer to the *Circuit Board Layout Techniques* design guide (SLOA089) for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* (SLAA530) for guidelines.

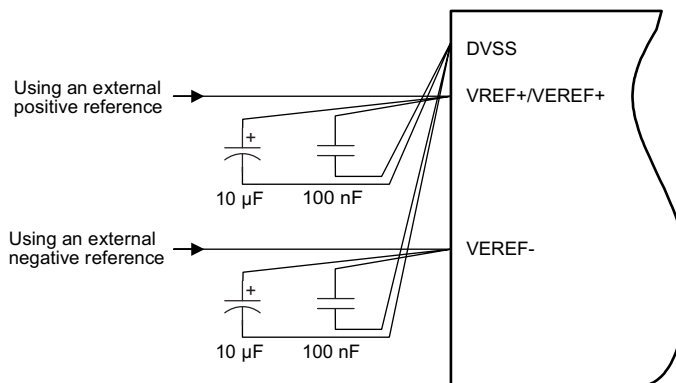
### 7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in [Section 5.1, Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC Peripheral

#### 7.2.1.1 Partial Schematic



**Figure 7-5. ADC Grounding and Noise Considerations**

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.1](#) combined with the connections shown in [Figure 7-5](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide (SLAU445)*.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- $\mu$ F capacitor buffers the reference pin and filters any low-frequency ripple. A bypass capacitor of 100 nF filters out any high-frequency noise.

### 7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see Figure 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

## 7.2.2 CapTivate Peripheral

This section provides a brief introduction to the CapTivate technology with examples of PCB layout and performance from the design kit. A more detailed description of the CapTivate technology and the tools needed to be successful, application development tools, hardware design guides, and software library, can be found in the [CapTivate Technology Design Center](#).

### 7.2.2.1 Device Connection and Layout Fundamentals

#### 7.2.2.1.1 VREG

The VREG pin requires a 1- $\mu$ F capacitor to regulate the 1.5-V LDO internal to the device (Vreg). This capacitor must be placed as close as possible to the microcontroller. Figure 7-6 shows the layout of the CAPTIVATE-FR2633, zooming in on the capacitor connected to the VREG pin.

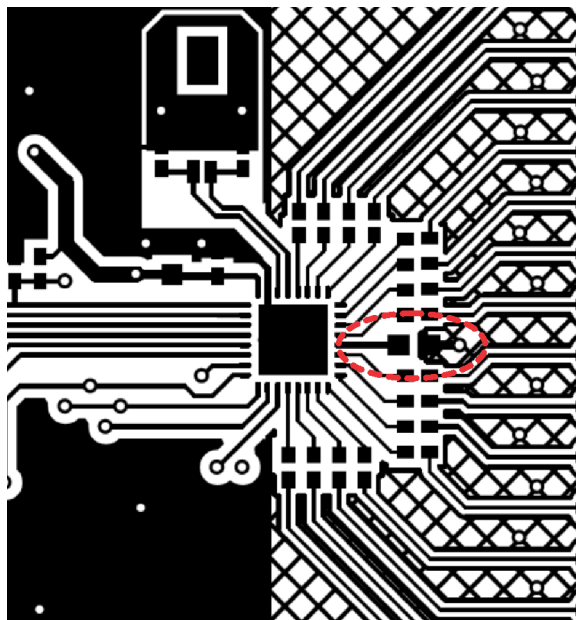


Figure 7-6. VREG Capacitor and Channel Series Resistors

### 7.2.2.1.2 ESD Protection

Typically, the laminate overlay provides several kilovolts of breakdown isolation to protect the circuit from ESD strikes. More ESD protection can be added with a series resistor placed on each channel used. A value of  $470\ \Omega$  is recommended and is found on the development tool.

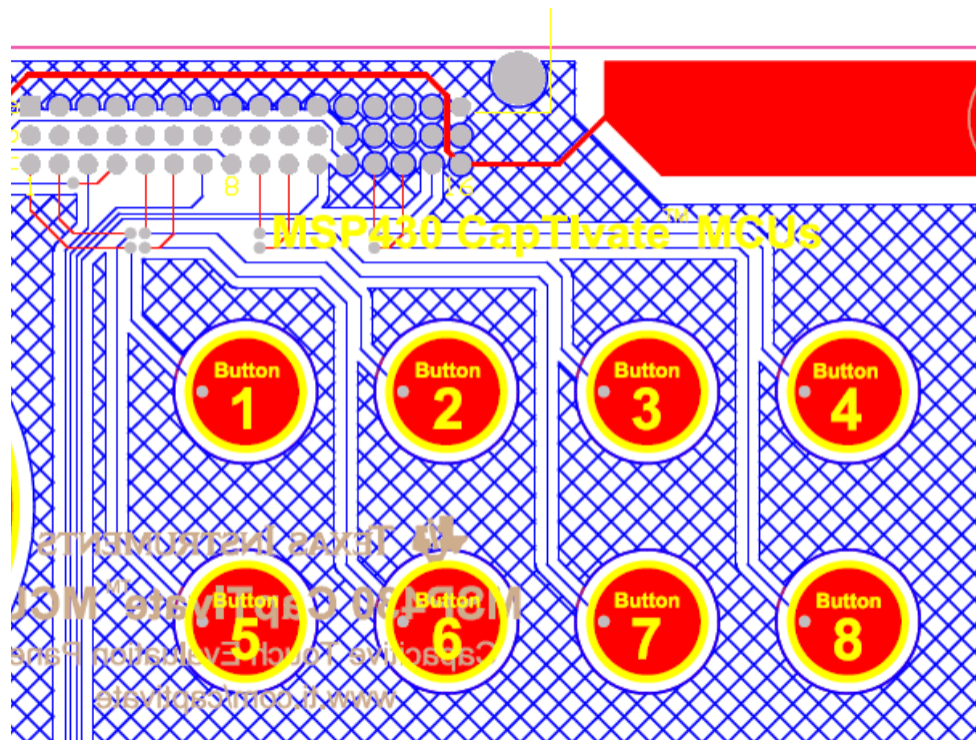
### 7.2.2.1.3 Mutual- and Self-Capacitance

CapTIvate technology enables both self-mode and mutual-mode capacitance measurements. [Section 7.2.2.1.4](#) and [Section 7.2.2.1.5](#) provide a brief description and examples, taken from the CAPTIVATE-PHONE and CAPTIVATE-BSWP panels found in the design kit, for self- and mutual-mode capacitance measurements, respectively.

### 7.2.2.1.4 Self-Capacitance

Self-capacitance electrodes are characterized by having only one channel from the IC that both excites and measures the capacitance. The capacitance being measured is between the electrode and earth ground, so any capacitance local to the PCB or outside of the PCB (a touch event) influences the measurement.

PCB layout design guidelines to minimize local parasitic capacitances and maximize the affect of external capacitances (a touch) can be found in the [CapTIvate Technology Design Center](#). [Figure 7-7](#), taken from the CAPTIVATE-BSWP panel, shows that the area of the button should be consistent with the touch area, in this case a 400-mil (10.16-mm) diameter circle. To minimize parasitics on the PCB, the ground pour on the bottom layer is hatched and there is no pour directly below the electrode: 50-mil (1.27-mm) spacing between the electrode and ground fill.



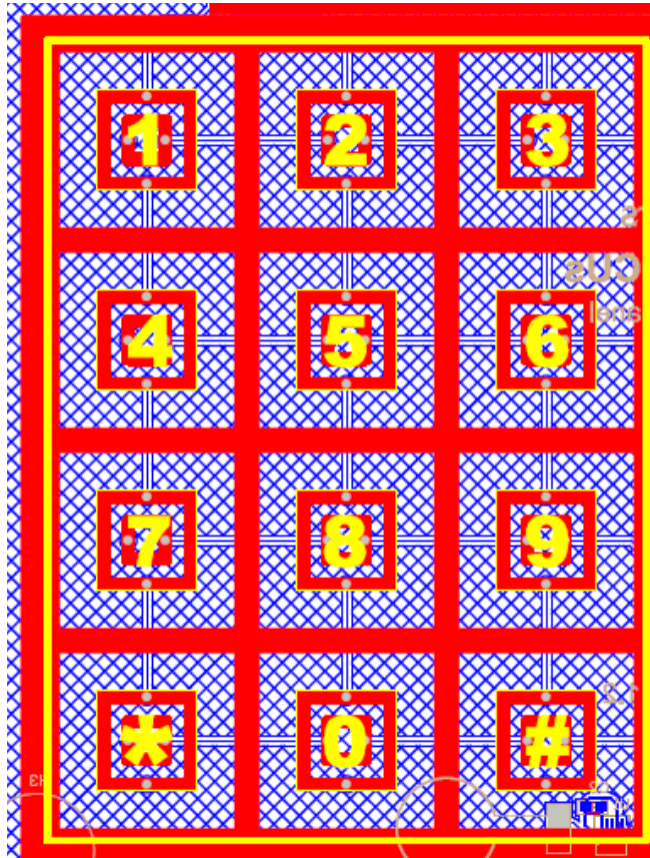
**Figure 7-7. Self-Capacitance Electrodes**



**7.2.2.1.5 Mutual Capacitance**

Mutual capacitance is characterized by having two channels, receive (Rx) and transmit (Tx), from the IC with the focus being the capacitance between the two. Coupling to earth ground still has an affect, but this is secondary to the mutual capacitance between the Rx and Tx electrodes.

PCB layout design guidelines for mutual capacitance structures can also be found in the [CapTivate Technology Design Center](#). Figure 7-8, taken from CAPTIVATE-PHONE, shows that the Tx electrode is a copy of the Rx electrode expanded to surround the Rx electrode. Both the Rx and Tx electrodes are in the shape of hollow squares: the Tx electrode is 300 x 300 mils (7.62 x 7.62 mm) and the Rx electrode is 150 x 150 mils (3.81 x 3.81 mm). Both electrodes are 50 mils (1.27 mm) wide.



**Figure 7-8. Mutual-Capacitance Electrodes**

### 7.2.2.2 Measurements

The following measurements are taken from the [CapTivate Technology Design Center](#), using the CAPTIVATE-PHONE and CAPTIVATE-BSWP panels. Unless otherwise stated, the settings used are the out-of-box settings, which can be found in the example projects. The intent of these measurements is to show performance in a configuration that is readily available and reproducible.



Figure 7-9. CAPTIVATE-PHONE and CAPTIVATE-BSWP Panels

#### 7.2.2.2.1 SNR

The [CapTivate technology Design Center](#) provides a specific view for analyzing the signal-to-noise ratio of each element. [Figure 7-10](#) shows that the SNR tab can be used to establish a confidence level in the settings that are chosen.

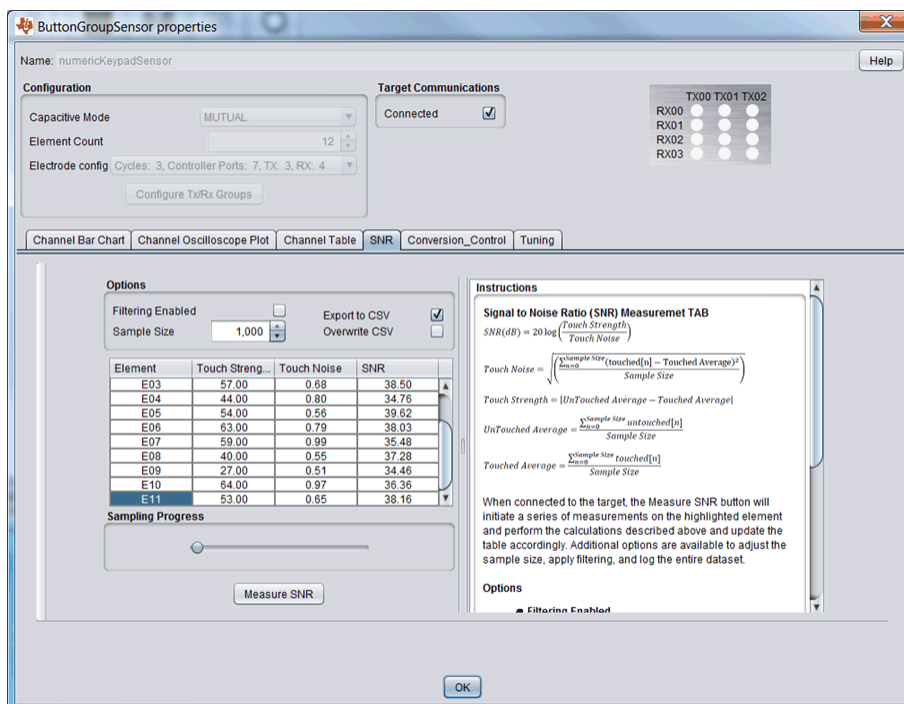


Figure 7-10. SNR Tab

[Table 7-1](#) summarizes the SNR results from the CAPTIVATE-PHONE panel keypad, numericKeypadSensor.

**Table 7-1. CAPTIVATE-PHONE SNR Results**

| ELEMENT | SNR (dB) | ELEMENT | SNR (dB) |
|---------|----------|---------|----------|
| E00     | 31.49    | E06     | 38.03    |
| E01     | 37.20    | E07     | 35.48    |
| E02     | 36.34    | E08     | 37.28    |
| E03     | 38.50    | E09     | –        |
| E04     | 34.76    | E10     | –        |
| E05     | 39.62    | E11     | –        |

Table 7-2 summarizes the SNR results from the CAPTIVATE-BSWP panel keypad, keypadSensor.

**Table 7-2. CAPTIVATE-BSWP SNR Results**

| ELEMENT | SNR (dB) | ELEMENT | SNR (dB) |
|---------|----------|---------|----------|
| E00     | 37.90    | E04     | 39.28    |
| E01     | 47.26    | E05     | 29.67    |
| E02     | 36.79    | E06     | 36.63    |
| E03     | 33.73    | E07     | 34.07    |

#### 7.2.2.2 Sensitivity

To show sensitivity, in terms of farads, the internal reference capacitor is used as the change in capacitance. In the mutual-capacitance case, the 0.1-pF capacitor is used. In the self-capacitance case, the 1-pF reference capacitor is used. For simplicity, the results for only button 1 on both the CAPTIVATE-PHONE and CAPTIVATE-BSWP panels are reported in Table 7-3.

**Table 7-3. Button Sensitivity**

| CONVERSION COUNT | CONVERSION GAIN | CAPTIVATE-PHONE BUTTON 1 |                          | CAPTIVATE-BSWP BUTTON 1 |                        |
|------------------|-----------------|--------------------------|--------------------------|-------------------------|------------------------|
|                  |                 | CONVERSION TIME (μs)     | COUNTS FOR 0.1-pF CHANGE | CONVERSION TIME (μs)    | COUNTS FOR 1-pF CHANGE |
| 100              | 100             | 25                       | 6                        | 50                      | 8                      |
| 200              | 200             | 50                       | 10                       | 100                     | 16                     |
| 200              | 100             | 50                       | 21                       | 100                     | 31                     |
| 800              | 400             | 200                      | 70                       | 400                     | 112                    |
| 800              | 200             | 200                      | 140                      | 400                     | 202                    |
| 800              | 100             | 200                      | 257                      | 400                     | 333                    |

An alternative measure in sensitivity is the ability to resolve capacitance change over a wide range of base capacitance. Table 7-4 shows example conversion times (for a self-mode measurement of discrete capacitors) that can be used to achieve the desired resolution for a given parasitic load capacitance.

**Table 7-4. Button Sensitivity**

| CAPACITANCE $C_p$<br>(pF) <sup>(1)</sup> | CONVERSION<br>COUNT/GAIN | CONVERSION TIME<br>( $\mu$ s) | COUNTS FOR<br>0.130-pF CHANGE | COUNTS FOR<br>0.260-pF CHANGE | COUNTS FOR<br>0.520-pF CHANGE |
|--|--------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| 23                                       | 400/100                  | 200                           | 10                            | 23                            | 35                            |
| 50                                       | 550/100                  | 275                           | 11                            | 24                            | 37                            |
| 78                                       | 650/100                  | 325                           | 11                            | 23                            | 36                            |
| 150                                      | 850/100                  | 425                           | 11                            | 22                            | 35                            |
| 150 <sup>(2)</sup>                       | 1200/200                 | 600                           | 11                            | 23                            | 37                            |
| 200 <sup>(2)</sup>                       | 1200/150                 | 600                           | 13                            | 26                            | 41                            |

(1) These measurements were taken with the CapTIvate MCU processor board with the 470- $\Omega$  series resistors replaced with 0- $\Omega$  resistors.

(2) 0-V discharge voltage is used.

### 7.2.2.2.3 Power

The low-power mode LPM3 specifications in [Section 5.7](#) are derived from the CapTIvate technology design kit as indicated in the notes.

## 7.3 Typical Applications

[Table 7-5](#) lists tools that demonstrate the use of the MSP430FR263x devices in various real-world application scenarios. Consult these designs for additional guidance regarding schematics, layout, and software implementation. For the most up-to-date list of available TI Designs, see the device-specific product folders listed in [Section 8.3](#).

**Table 7-5. TI Designs**

| DESIGN NAME   | LINK  |
|---|---|
| MSP CapTIvate™ MCU Development Kit Evaluation Model         | <a href="http://www.ti.com/tool/msp-capt-fr2633">http://www.ti.com/tool/msp-capt-fr2633</a>                           |
| Capacitive Touch Thermostat User Interface Reference Design | <a href="http://www.ti.com/tool/tidm-captivate-thermostat-ui">http://www.ti.com/tool/tidm-captivate-thermostat-ui</a> |

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Development Support

##### 8.1.1.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with your development, visit the [Getting Started](#) page.

##### 8.1.1.2 Development Tools Support

###### 8.1.1.2.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* ([SLAU157](#)) for details on the available features.

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT | EEM VERSION |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|-------------|
| MSP430Xv2           | Yes         | Yes         | 3                | Yes                | Yes           | No              | No           | No                       | S           |

###### 8.1.1.2.2 Recommended Hardware Options

All MSP430 MCUs are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [MSP430 Tools](#).

###### 8.1.1.2.2.1 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See [MSP430 Tools](#) for details.

###### 8.1.1.2.2.2 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third-party suppliers. See the full list of available tools at [MSP430 Tools](#).

| PART NUMBER                   | PC PORT | FEATURES  | PROVIDER          |
|-------------------------------|---------|---|-------------------|
| <a href="#">MSP-FET430UIF</a> | USB     | MSP430 USB debugging interface. Compatible with 4-wire JTAG and 2-wire Spy-Bi-Wire (SBW) JTAG modes | Texas Instruments |
| <a href="#">MSP-FET</a>       | USB     | MSP MCU programmer and debugger. The MSP-FET is compatible with Code Composer Studio v6 and later.  | Texas Instruments |

###### 8.1.1.2.2.3 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| PART NUMBER              | PC PORT        | FEATURES  | PROVIDER          |
|--------------------------|----------------|---|-------------------|
| <a href="#">MSP-GANG</a> | Serial and USB | Program up to eight devices at a time. Works with a PC or as a stand-alone package. | Texas Instruments |

###### 8.1.1.2.3 Recommended Software Options

###### 8.1.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open-source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

### 8.1.1.2.3.2 MSPWare

**MSPWare** is a collection of code examples, data sheets, and other design resources for all MSP devices delivered in a convenient package. In addition to providing a complete collection of existing MSP design resources, MSPWare also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP hardware. MSPWare is available as a component of CCS or as a stand-alone package.

### 8.1.1.2.3.3 Command-Line Programmer

**MSP Flasher** is an open-source shell-based interface for programming MSP MCUs through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can be used to download binary files (.txt or .hex) files directly to the MSP MCU without the need for an IDE.

## 8.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCUs and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430FR2633). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

**XMS** – Experimental device that is not necessarily representative of the electrical specifications of the final device

**MSP** – Fully qualified production device

Support tool development evolutionary flow:

**MSPX** – Development-support product that has not yet completed TI internal qualification testing.

**MSP** – Fully-qualified development-support product

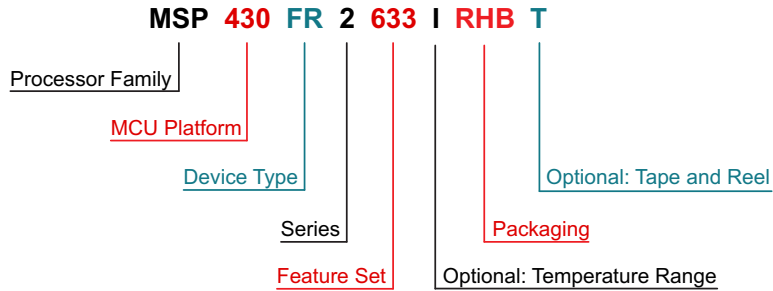
XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RHB) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.



|                                      |   |
|--------------------------------------|---|
| <b>Processor Family</b>              | MSP = Mixed-signal processor<br>XMS = Experimental silicon  |
| <b>MCU Platform</b>                  | 430 = MSP430 16-bit low-power platform  |
| <b>Device Type</b>                   | <b>Memory Type</b><br>FR = FRAM   |
| <b>Series</b>                        | 4 = Up to 16 MHz with LCD<br>2 = Up to 16 MHz without LCD   |
| <b>Feature Set</b>                   | <b>CapTIvate Performance</b><br>633 = 4 CapTIvate blocks support up to 16 self- or 64 mutual-capacitance buttons<br>533 = 4 CapTIvate blocks support up to 16 self- or 16 mutual-capacitance buttons<br>632 = 4 CapTIvate blocks support up to 8 self- or 16 mutual-capacitance buttons<br>532 = 4 CapTIvate blocks support up to 8 self- or 8 mutual-capacitance buttons |
| <b>Optional: Temperature Range</b>   | S = 0°C to 50°C<br>I = -40°C to 85°C<br>T = -40°C to 105°C  |
| <b>Packaging</b>                     | www.ti.com/packaging  |
| <b>Optional: Distribution Format</b> | T = Small Reel<br>R = Large Reel<br>No Marking = Tube or Tray   |

**Figure 8-1. Device Nomenclature**

## 8.2 Documentation Support

The following documents describe the MSP430FR263x and MSP430FR253x MCUs. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

- SLAU445** *MSP430FR4xx and MSP430FR2xx Family User's Guide.* Detailed description of all modules and peripherals available in this device family.
- SLAZ660** *MSP430FR2633 Device Erratasheet.* Describes the known exceptions to the functional specifications for all silicon revisions of this MCU.
- SLAZ661** *MSP430FR2533 Device Erratasheet.* Describes the known exceptions to the functional specifications for all silicon revisions of this MCU.
- SLAZ662** *MSP430FR2632 Device Erratasheet.* Describes the known exceptions to the functional specifications for all silicon revisions of this MCU.
- SLAZ663** *MSP430FR2532 Device Erratasheet.* Describes the known exceptions to the functional specifications for all silicon revisions of this MCU.
- SLAU278** *MSP430 Hardware Tools User's Guide.* This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.
- SLAU610** *MSP430FR4xx and MSP430FR2xx Bootloader (BSL) User's Guide.* The bootloader (BSL) provides a method to program memory during MSP430 MCU project development and updates. It can be activated by a utility that sends commands using a serial protocol. The BSL enables the user to control the activity of the MSP430 MCU and to exchange data using a personal computer or other device.
- SLAU320** *MSP430 Programming Via the JTAG Interface.* This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 MCUs. This document describes access to the MCU using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).
- SLAA322** *MSP430 32-kHz Crystal Oscillators.* Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.
- SLOA089** *Circuit Board Layout Techniques.* Op amp circuitry is analog circuitry and is very different from digital circuitry. It must be partitioned in its own section of the board using special layout techniques. Printed circuit board effects become most apparent in high-speed analog circuits, but common mistakes described in this chapter can even affect the performance of audio circuits. The purpose of this chapter is to discuss some of the more common mistakes made by designers and how they degrade performance, and to provide simple fixes to avoid the problems.
- SLAA530** *MSP430 System-Level ESD Considerations.* System-Level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.



### 8.3 Related Links

[Table 8-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS        | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FR2633 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR2533 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR2632 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| MSP430FR2532 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### [TI E2E™ Community](#)

*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

#### [TI Embedded Processors Wiki](#)

*Texas Instruments Embedded Processors Wiki.* Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

### 8.5 Trademarks

CapTIvate, MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments.

### 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

### 8.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FR2532IRGER | ACTIVE        | VQFN         | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2532                  | <a href="#">Samples</a> |
| MSP430FR2532IRGET | ACTIVE        | VQFN         | RGE             | 24   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2532                  | <a href="#">Samples</a> |
| MSP430FR2533IDA   | ACTIVE        | TSSOP        | DA              | 32   | 46          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2533                  | <a href="#">Samples</a> |
| MSP430FR2533IDAR  | ACTIVE        | TSSOP        | DA              | 32   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2533                  | <a href="#">Samples</a> |
| MSP430FR2533IRHBR | ACTIVE        | VQFN         | RHB             | 32   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | FR2533                  | <a href="#">Samples</a> |
| MSP430FR2533IRHBT | ACTIVE        | VQFN         | RHB             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | FR2533                  | <a href="#">Samples</a> |
| MSP430FR2632IRGER | ACTIVE        | VQFN         | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2632                  | <a href="#">Samples</a> |
| MSP430FR2632IRGET | ACTIVE        | VQFN         | RGE             | 24   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2632                  | <a href="#">Samples</a> |
| MSP430FR2633IDA   | ACTIVE        | TSSOP        | DA              | 32   | 46          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2633                  | <a href="#">Samples</a> |
| MSP430FR2633IDAR  | ACTIVE        | TSSOP        | DA              | 32   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | FR2633                  | <a href="#">Samples</a> |
| MSP430FR2633IRHBR | ACTIVE        | VQFN         | RHB             | 32   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | FR2633                  | <a href="#">Samples</a> |
| MSP430FR2633IRHBT | ACTIVE        | VQFN         | RHB             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | FR2633                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR2532IRGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| MSP430FR2533IDAR  | TSSOP        | DA              | 32   | 2000 | 330.0              | 24.4               | 8.6     | 11.5    | 1.6     | 12.0    | 24.0   | Q1            |
| MSP430FR2533IRHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| MSP430FR2632IRGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| MSP430FR2633IDAR  | TSSOP        | DA              | 32   | 2000 | 330.0              | 24.4               | 8.6     | 11.5    | 1.6     | 12.0    | 24.0   | Q1            |
| MSP430FR2633IRHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR2532IRGER | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |
| MSP430FR2533IDAR  | TSSOP        | DA              | 32   | 2000 | 367.0       | 367.0      | 45.0        |
| MSP430FR2533IRHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| MSP430FR2632IRGER | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |
| MSP430FR2633IDAR  | TSSOP        | DA              | 32   | 2000 | 367.0       | 367.0      | 45.0        |
| MSP430FR2633IRHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |

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### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

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