SM320F2808-EP, SM320F2806-EP
SM320F2801-EP
Digital Signal Processors

Data Manual

Literature Number: SGLS316A
March 2006 – Revised February 2007

TEXAS INSTRUMENTS

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(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Peripheral Interrupt Expansion (PIE) Block That Supports All 43 Peripheral Interrupts**
- **128-Bit Security Key/Lock**
  - **Protects Flash/OTP/L0/L1 Blocks**
  - **Prevents Firmware Reverse Engineering**
- **Enhanced Control Peripherals**
  - **Up to 16 PWM Outputs**
  - **Up to Four HRPWM Outputs With 150 ps MEP Resolution**
  - **Up to Four Capture Inputs**
  - **Up to Two Quadrature Encoder Interfaces**
  - **Up to Six 32-bit Timers**
  - **Up to Six 16-bit Timers**
- **Three 32-Bit CPU Timers**
- **Serial Port Peripherals**
  - **Up to Four Serial Peripheral Interface (SPI) Modules**
  - **Up to Two Serial Communications Interface (SCI), Standard UART Modules**
  - **Up to Two Enhanced Controller Area Network (eCAN) Modules**
  - **One Inter-Integrated-Circuit (I^2C) Bus**
- **12-Bit ADC, 16 Channels**
  - **2 x 8 Channel Input Multiplexer**
  - **Two Sample-and-Hold**
  - **Single/Simultaneous Conversions**
  - **Fast Conversion Rate: 160 ns/6.25 MSPS**
  - **Internal or External Reference**
- **Up to 35 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering**
- **Advanced Emulation Features**
  - **Analysis and Breakpoint Functions**
  - **Real-Time Debug via Hardware**
- **Low-Power Modes and Power Savings**
  - **IDLE, STANDBY, HALT Modes Supported**
  - **Disable Individual Peripheral Clocks**
- **Package Options**
  - **Thin Quad Flatpack (PZ)**
  - **MicroStar BGA™ (GGM, ZGM)**
- **Temperature Options:**
  - **M: -55°C to 125°C (PZ)**

2 Introduction

The SM320F2808, F2806, and F2801/UCD9501 devices, members of the TMS320C28x™ DSP generation, are highly integrated, high-performance solutions for demanding control applications. The UCD9501 is a 32-bit digital signal controller for power management.

Throughout this document, SM320F2808, F2806, and F2801/UCD9501 are abbreviated as F2808, F2806, and F2801/9501, respectively. TMS320x280x device reference guides, flash tools, and other collateral are applicable to the UCD9501 device as well. Table 2-1 provides a summary of each device's features.

Table 2-1. Hardware Features

FEATURE		F2808	F2806(1)	F2801/9501(1)
Instruction cycle (at 100 MHz)		10 ns	10 ns	10 ns
Single-access RAM (SARAM) (16-bit word)		18K (L0, L1, M0, M1, H0)	10K (L0, L1, M0, M1)	6K (L0, M0, M1)
3.3-V on-chip flash (16-bit word)		64K	32K	16K
Code security for on-chip flash/SARAM/OTP blocks		Yes	Yes	Yes
Boot ROM (4K X16)		Yes	Yes	Yes
One-time programmable (OTP) ROM		Yes	Yes	Yes
External memory interface		No	No	No
Enhanced PWM outputs (16-bit timer-based modules with 2 PWM outputs/module)		ePWM1, ePWM2 ePWM3, ePWM4, ePWM5, ePWM6	ePWM1, ePWM2 ePWM3, ePWM4, ePWM5, ePWM6	ePWM1, ePWM2, ePWM3
HRPWM channels		ePWM1A, ePWM2A ePWM3A, ePWM4A	ePWM1A, ePWM2A ePWM3A, ePWM4A	ePWM1A, ePWM2A ePWM3A
Enhanced 32-bit CAPTURE inputs or auxiliary PWM outputs		eCAP1, eCAP2 eCAP3, eCAP4	eCAP1, eCAP2 eCAP3, eCAP4	eCAP1, eCAP2
Enhanced 32-bit QEP channels (four inputs/channel)		eQEP1, eQEP2	eQEP1, eQEP2	eQEP1
Watchdog timer		Yes	Yes	Yes
12-Bit ADC channels		16	16	16
32-Bit CPU timers		3	3	3
Serial Peripheral Interface (SPI)		SPI-A, SPI-B, SPI-C, SPI-D	SPI-A, SPI-B, SPI-C, SPI-D	SPI-A, SPI-B
Serial Communications Interface (SCI)		SCI-A, SCI-B	SCI-A, SCI-B	SCI-A
Enhanced Controller Area Network (eCAN)		eCAN-A, eCAN-B	eCAN-A	eCAN-A
Inter-Integrated Circuit (I^2C)		I2C-A	I2C-A	I2C-A
Digital I/O pins (shared)		35	35	35
External interrupts		3	3	3
Supply voltage		1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O
Packaging		100-Pin PZ 100-Ball GGM, ZGM	100-Pin PZ 100-Ball GGM, ZGM	100-Pin PZ 100-Ball GGM, ZGM
Temperature options	M: -55°C to 125°C	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)
		(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)
		(PZ)	(PZ)	(PZ)

(1) Product Preview

ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER
-55°C to 125°C	LQFP-PZ	SM320F2801PZMEP
-55°C to 125°C	LQFP-PZ	SM320F2808PZMEP

2.1 Pin Assignments

The SM320F2808, F2806, and F2801/UCD9501 100-pin PZ low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2-1, Figure 2-2 and Figure 2-3. Table 2-2 describes the function(s) of each pin.

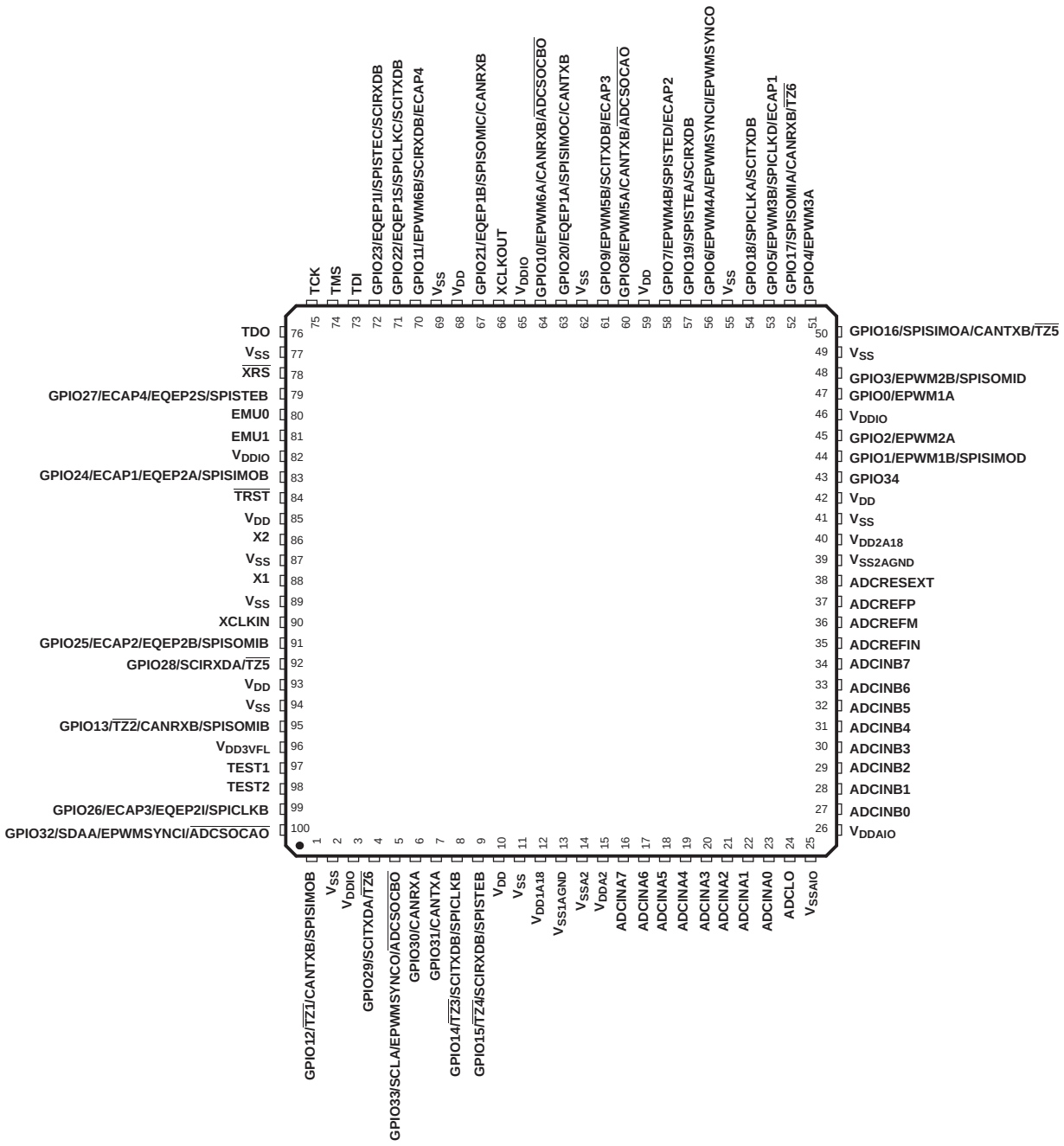


Figure 2-1. SM320F2808 100-Pin PZ LQFP (Top View)

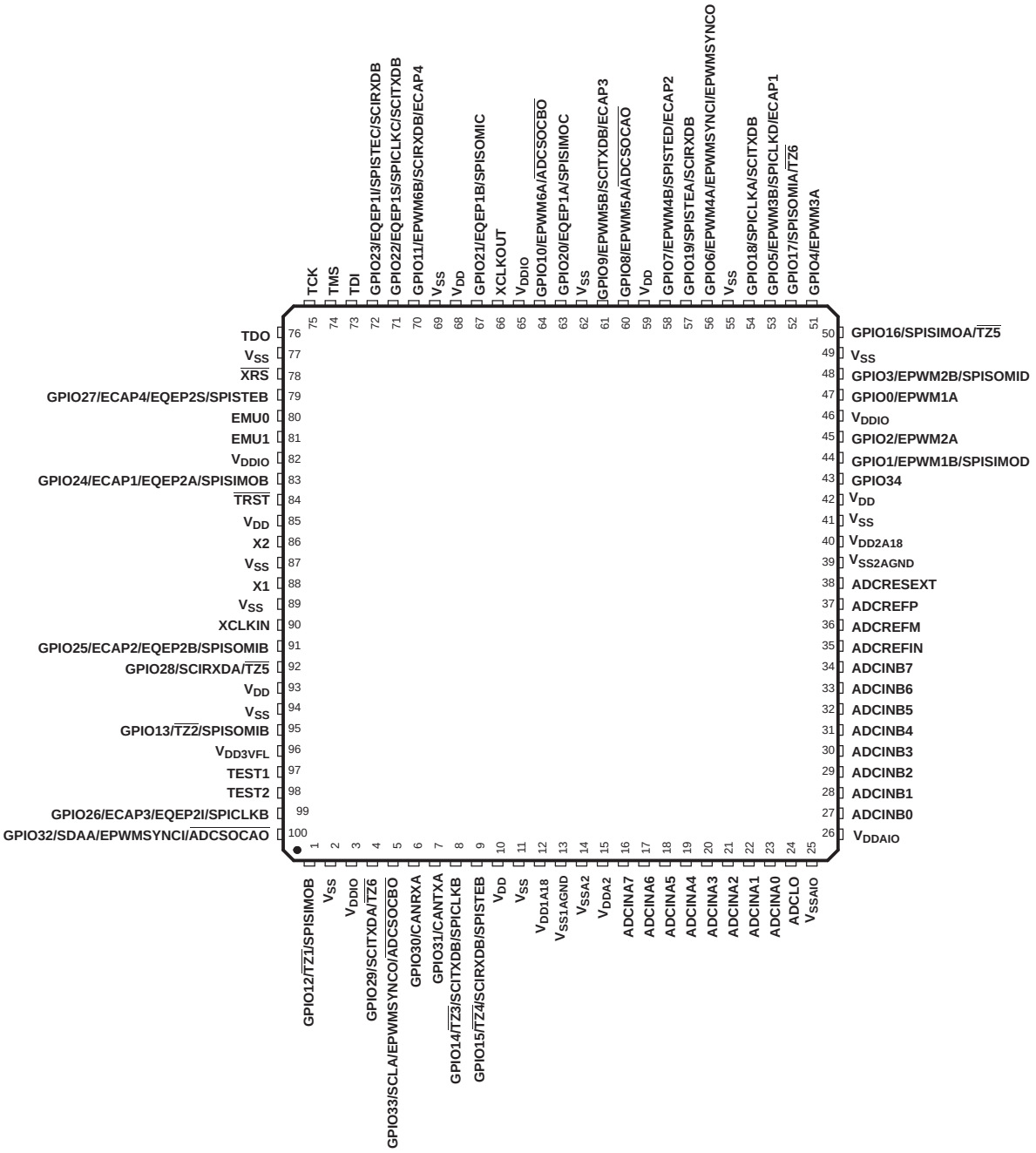


Figure 2-2. F2806 100-Pin PZ LQFP (Top View)

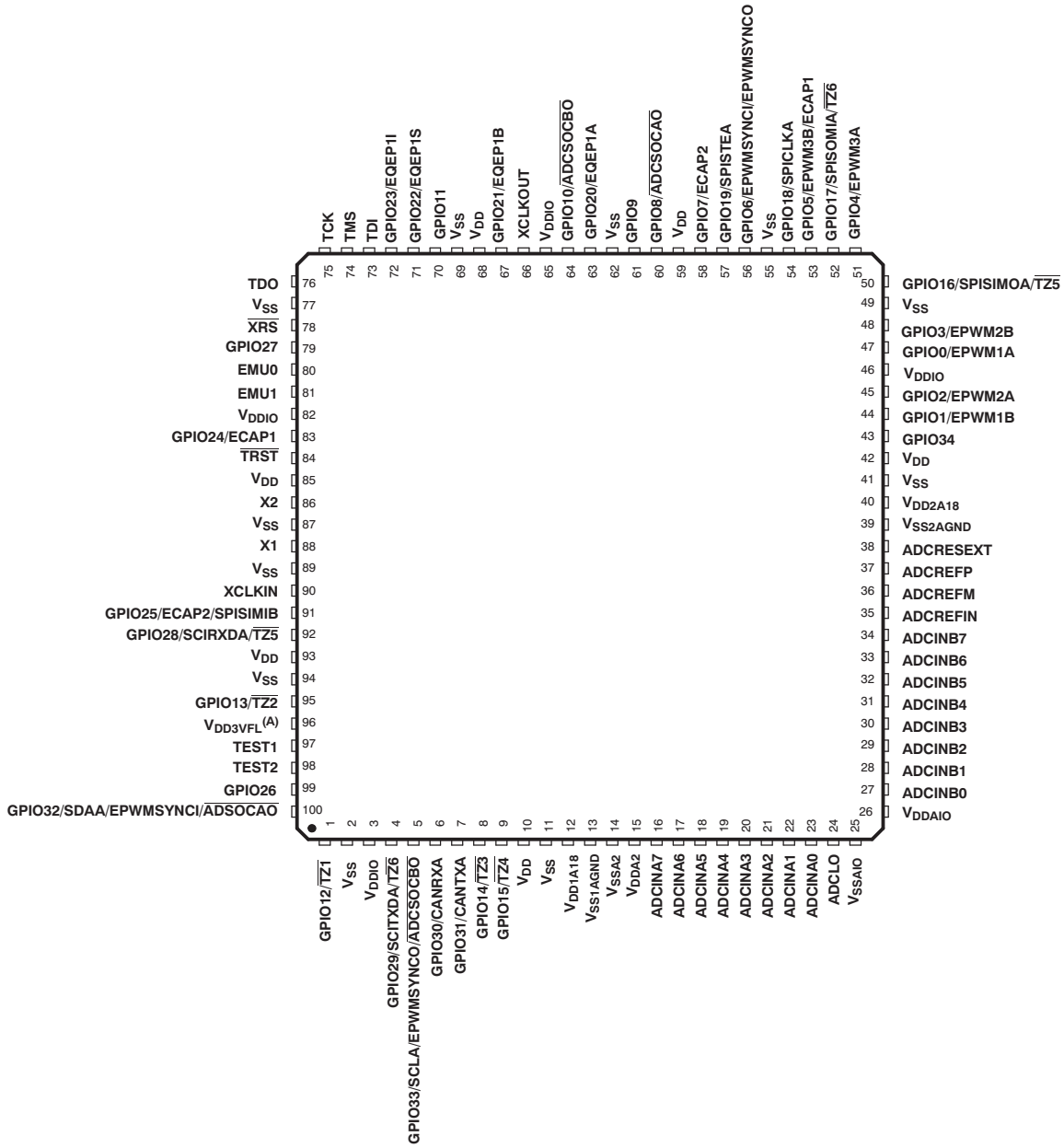


Figure 2-3. F2801/UCD9501 100-Pin PZ LQFP (Top View)

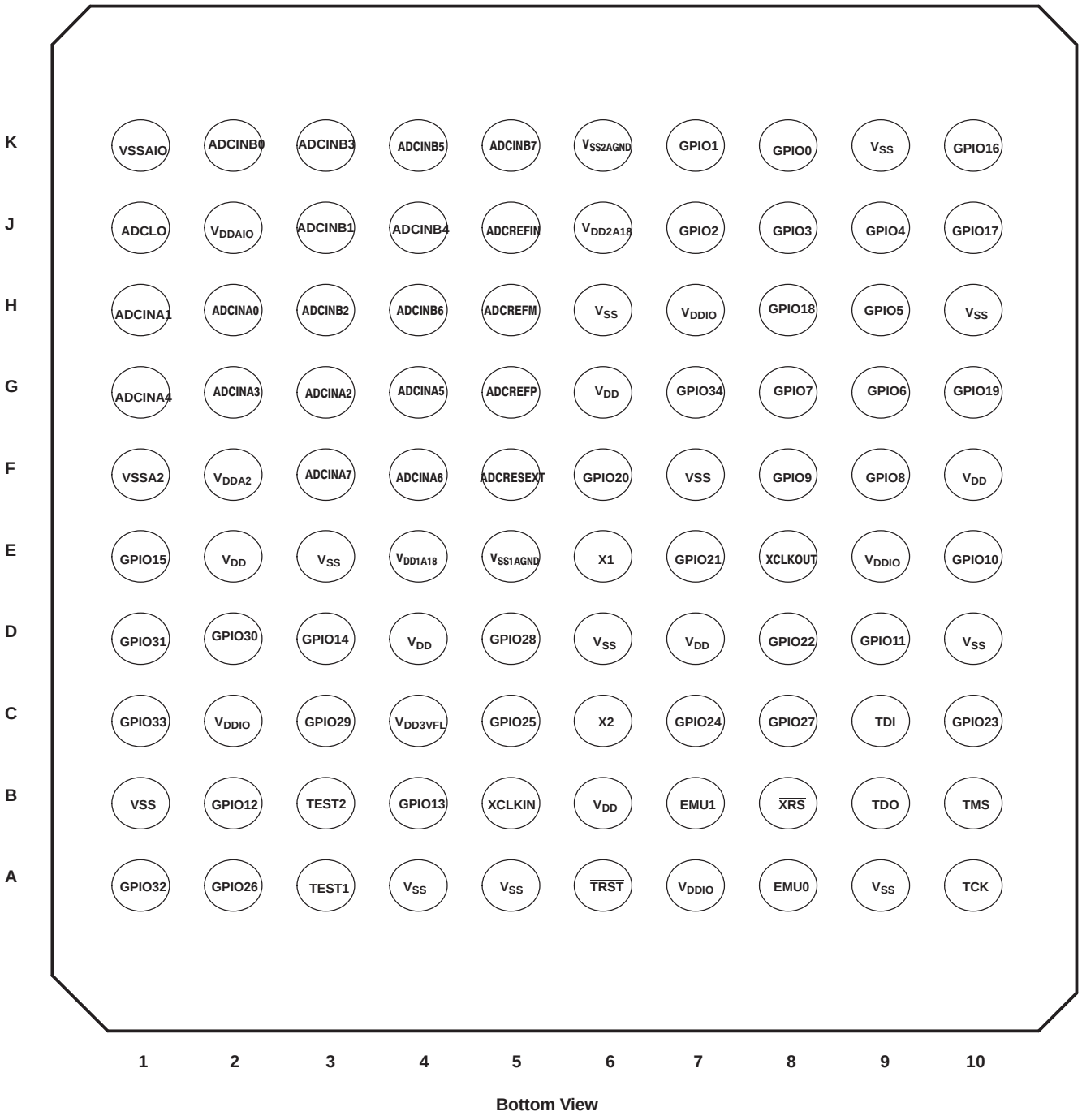


Figure 2-4. SM320F280x 100-Ball GGM and ZGM MicroStar™ BGA (Bottom View)

2.2 Signal Descriptions

Table 2-2 describes the signals on the 280x devices. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant.

Table 2-2. Signal Descriptions

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM BALL #	
JTAG			
$\overline{\text{TRST}}$	84	A6	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pull-down device. $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. In a low-noise environment, $\overline{\text{TRST}}$ may be left floating. In other instances, an external pulldown resistor is **highly recommended**. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board is validated for proper operation of the debugger and the application. (I, ↓)
TCK	75	A10	JTAG test clock with internal pullup (I, ↑)
TMS	74	B10	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (I, ↑)
TDI	73	C9	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (I, ↑)
TDO	76	B9	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (O/Z 8 mA drive)
EMU0	80	A8	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. (I/O/Z, 8 mA drive ↑)
EMU1	81	B7	Emulator pin 1. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. (I/O/Z, 8 mA drive, ↑)
FLASH			
VDD3VFL	96	C4	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times.
TEST1	97	A3	Test Pin. Reserved for Texas Instruments. Must be left unconnected. (I/O)
TEST2	98	B3	Test Pin. Reserved for Texas Instruments. Must be left unconnected. (I/O)
CLOCK			
XCLKOUT	66	E8	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by the bits 1, 0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. Unlike other GPIO pins, the XCLKOUT pin is not placed in high-impedance state during a reset. (O/Z, 8 mA drive).
XCLKIN	90	B5	External Oscillator Input. This pin is to feed a clock from an external 3.3-V oscillator. In this case, the X1 pin must be tied to GND. If a crystal/resonator is used (or if an external 1.8-V oscillator is used to feed clock to X1 pin), this pin must be tied to GND. (I)
X1	88	E6	Internal/External Oscillator Input. To use the internal oscillator, a quartz crystal or a ceramic resonator may be connected across X1 and X2. The X1 pin is referenced to the 1.8-V core digital power supply. A 1.8-V external oscillator may be connected to the X1 pin. In this case, the XCLKIN pin must be connected to ground. If a 3.3-V external oscillator is used with the XCLKIN pin, X1 must be tied to GND. (I)
X2	86	C6	Internal Oscillator Output. A quartz crystal or a ceramic resonator may be connected across X1 and X2. If X2 is not used it must be left unconnected. (O)
RESET			
$\overline{\text{XRS}}$	78	B8	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{\text{XRS}}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{\text{XRS}}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSP when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. (I/OD, ↑) The output buffer of this pin is an open-drain with an internal pullup (100 μA, typical). It is recommended that this pin be driven by an open-drain device.
ADC SIGNALS			
ADCINA7	16	F3	ADC Group A, Channel 7 input (I)
ADCINA6	17	F4	ADC Group A, Channel 6 input (I)

(1) I = Input, O = Output, Z = High impedance, OD = Open drain, ↑ = Pullup, ↓ = Pulldown

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM BALL #	
ADCINA5	18	G4	ADC Group A, Channel 5 input (I)
ADCINA4	19	G1	ADC Group A, Channel 4 input (I)
ADCINA3	20	G2	ADC Group A, Channel 3 input (I)
ADCINA2	21	G3	ADC Group A, Channel 2 input (I)
ADCINA1	22	H1	ADC Group A, Channel 1 input (I)
ADCINA0	23	H2	ADC Group A, Channel 0 input (I)
ADCINB7	34	K5	ADC Group B, Channel 7 input (I)
ADCINB6	33	H4	ADC Group B, Channel 6 input (I)
ADCINB5	32	K4	ADC Group B, Channel 5 input (I)
ADCINB4	31	J4	ADC Group B, Channel 4 input (I)
ADCINB3	30	K3	ADC Group B, Channel 3 input (I)
ADCINB2	29	H3	ADC Group B, Channel 2 input (I)
ADCINB1	28	J3	ADC Group B, Channel 1 input (I)
ADCINB0	27	K2	ADC Group B, Channel 0 input (I)
ADCLO	24	J1	Low Reference (connect to analog ground) (I)
ADCRESEXT	38	F5	ADC External Current Bias Resistor. Connect a 22-kΩ resistor to analog ground.
ADCREFIN	35	J5	External reference input (I)
ADCREFP	37	G5	Internal Reference Positive Output. Requires a low ESR (50 mΩ - 1.5 Ω) ceramic bypass capacitor of 2.2 µF to analog ground. (O)
ADCREFM	36	H5	Internal Reference Medium Output. Requires a low ESR (50 mΩ - 1.5 Ω) ceramic bypass capacitor of 2.2 µF to analog ground. (O)
CPU AND I/O POWER PINS			
V_{DDA2}	15	F2	ADC Analog Power Pin (3.3 V)
V_{SSA2}	14	F1	ADC Analog Ground Pin
V_{DDAIO}	26	J2	ADC Analog I/O Power Pin (3.3 V)
V_{SSAIO}	25	K1	ADC Analog I/O Ground Pin
V_{DD1A18}	12	E4	ADC Analog Power Pin (1.8 V)
$V_{SS1AGND}$	13	E5	ADC Analog Ground Pin
V_{DD2A18}	40	J6	ADC Analog Power Pin (1.8 V)
$V_{SS2AGND}$	39	K6	ADC Analog Ground Pin
V_{DD}	10	E2	CPU and Logic Digital Power Pins (1.8 V)
V_{DD}	42	G6	
V_{DD}	59	F10	
V_{DD}	68	D7	
V_{DD}	85	B6	
V_{DD}	93	D4	
V_{DDIO}	3	C2	Digital I/O Power Pin (3.3 V)
V_{DDIO}	46	H7	
V_{DDIO}	65	E9	
V_{DDIO}	82	A7	

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM BALL #	
V_{SS}	2	B1	Digital Ground Pins
V_{SS}	11	E3	
V_{SS}	41	H6	
V_{SS}	49	K9	
V_{SS}	55	H10	
V_{SS}	62	F7	
V_{SS}	69	D10	
V_{SS}	77	A9	
V_{SS}	87	D6	
V_{SS}	89	A5	
V_{SS}	94	A4	
GPIOA AND PERIPHERAL SIGNALS(2)			
GPIO0 EPWM1A - -	47	K8	General purpose input/output 0 (I/O/Z) (3) Enhanced PWM1 Output A and HRPWM channel (O) - -
GPIO1 EPWM1B SPISIMOD -	44	K7	General purpose input/output 1 (I/O/Z)(3) Enhanced PWM1 Output B (O) SPI-D slave in, master out (I/O) (not available on F2801/9501) -
GPIO2 EPWM2A - -	45	J7	General purpose input/output 2 (I/O/Z)(3) Enhanced PWM2 Output A and HRPWM channel (O) - -
GPIO3 EPWM2B SPISOMID -	48	J8	General purpose input/output 3 (I/O/Z)(3) Enhanced PWM2 Output B (O) SPI-D slave out, master in (I/O) (not available on F2801/9501) -
GPIO4 EPWM3A - -	51	J9	General purpose input/output 4 (I/O/Z)(3) Enhanced PWM3 output A and HRPWM channel (O) - -
GPIO5 EPWM3B SPICLKD ECAP1	53	H9	General purpose input/output 5 (I/O/Z)(3) Enhanced PWM3 output B (O) SPI-D clock (I/O) (not available on F2801/9501) Enhanced capture input/output 1 (I/O)
GPIO6 EPWM4A EPWMSYNCI EPWMSYNCO	56	G9	General purpose input/output 6 (I/O/Z)(3) Enhanced PWM4 output A and HRPWM channel (not available on F2801/9501) (O) External ePWM sync pulse input (I) External ePWM sync pulse output (O)
GPIO7 EPWM4B SPISTED ECAP2	58	G8	General purpose input/output 7 (I/O/Z)(3) Enhanced PWM4 output B (not available on F2801/9501) (O) SPI-D slave transmit enable (not available on F2801/9501 (I/O) Enhanced capture input/output 2 (I/O)
GPIO8 EPWM5A CANTXB $\overline{\text{ADCSOCAO}}$	60	F9	General purpose input/output 8 (I/O/Z)(3) Enhanced PWM5 output A (not available on F2801/9501) (O) Enhanced CAN-B transmit (not available on F2806/F2801/9501) (O) ADC start-of-conversion A (O)
GPIO9 EPWM5B SCITXDB ECAP3	61	F8	General purpose input/output 9 (I/O/Z)(3) Enhanced PWM5 output B (not available on F2801/9501) (O) SCI-B transmit data (not available on F2801/9501) (O) Enhanced capture input/output 3 (not available on F2801/9501) (I/O)

(2) All GPIO pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup, which can be selectively enabled/disabled on a per-pin basis. This feature only applies to the GPIO pins. The GPIO function (shown in Italics) is the default at reset. The peripheral signals that are listed under them are alternate functions.
(3) The pullups on GPIO0-GPIO11 pins are not enabled at reset.

Table 2-2. Signal Descriptions (continued)

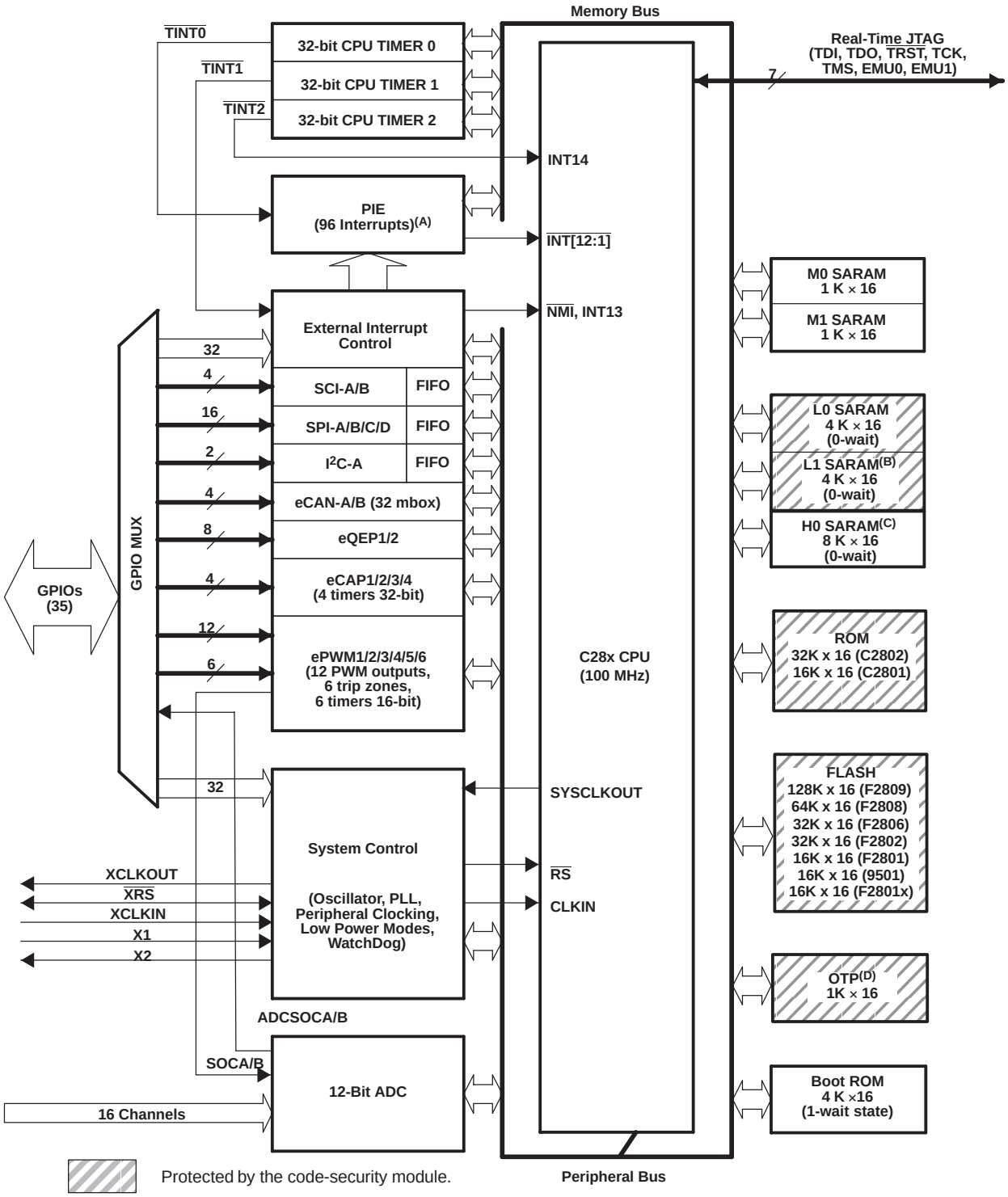
NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM BALL #	
GPIO10 EPWM6A CANRXB ADCSOCBO	64	E10	General purpose input/output 10 (I/O/Z)(3) Enhanced PWM6 output A (not available on F2801/9501) (O) Enhanced CAN-B receive (not available on F2806/F2801/9501) (I) ADC start-of-conversion B (O)
GPIO11 EPWM6B SCIRXDB ECAP4	70	D9	General purpose input/output 11 (I/O/Z)(3) Enhanced PWM6 output B (not available on F2801/9501) (O) SCI-B receive data (not available on F2801/9501) (I) Enhanced CAP Input/Output 4 (not available on F2801/9501) (I/O)
GPIO12 TZ1 CANTXB SPISIMOB	1	B2	General purpose input/output 12 (I/O/Z)(4) Trip Zone input 1 (I) Enhanced CAN-B transmit (not available on F2806/F2801/9501) (O) SPI-B Slave in, Master out (I/O)
GPIO13 TZ2 CANRXB SPISOMIB	95	B4	General purpose input/output 13 (I/O/Z)(4) Trip zone input 2 (I) Enhanced CAN-B receive (not available on F2806/F2801/9501) (I) SPI-B slave out, master in (I/O)
GPIO14 TZ3 SCITXDB SPICLKB	8	D3	General purpose input/output 14 (I/O/Z)(4) Trip zone input 3 (I) SCI-B transmit (not available on F2801/9501) (O) SPI-B clock input/output (I/O)
GPIO15 TZ4 SCIRXDB SPISTEB	9	E1	General purpose input/output 15 (I/O/Z)(4) Trip zone input (I) SCI-B receive (not available on F2801/9501) (I) SPI-B slave transmit enable (I/O)
GPIO16 SPISIMOA CANTXB TZ5	50	K10	General purpose input/output 16 (I/O/Z)(4) SPI-A slave in, master out (I/O) Enhanced CAN-B transmit (not available on F2806/F2801/9501) (O) Trip zone input 5 (I)
GPIO17 SPISOMIA CANRXB TZ6	52	J10	General purpose input/output 17 (I/O/Z)(4) SPI-A slave out, master in (I/O) Enhanced CAN-B receive (not available on F2806/F2801/9501) (I) Trip zone input 6(I)
GPIO18 SPICLKA SCITXDB - -	54	H8	General purpose input/output 18 (I/O/Z)(4) SPI-A clock input/output (I/O) SCI-B transmit (not available on F2801/9501) (O) - -
GPIO19 SPISTEA SCIRXDB - -	57	G10	General purpose input/output 19 (I/O/Z)(4) SPI-A slave transmit enable input/output (I/O) SCI-B receive (not available on F2801/9501) (I) - -
GPIO20 EQEP1A SPISIMOC CANTXB	63	F6	General purpose input/output 20 (I/O/Z)(4) Enhanced QEP1 input A (I) SPI-C slave in, master out (not available on F2801/9501) (I/O) Enhanced CAN-B transmit (not available on F2806/F2801/9501) (O)
GPIO21 EQEP1B SPISOMIC CANRXB	67	E7	General purpose input/output 21 (I/O/Z)(4) Enhanced QEP1 input A (I) SPI-C master in, slave out (not available on F2801/9501) (I/O) Enhanced CAN-B receive (not available on F2806/F2801/9501) (I)
GPIO22 EQEP1S SPICLKC SCITXDB	71	D8	General purpose input/output 22 (I/O/Z)(4) Enhanced QEP1 strobe (I/O) SPI-C clock (not available on F2801/9501) (I/O) SCI-B transmit (not available on F2801/9501) (O)
GPIO23 EQEP1I SPISTEC SCIRXDB	72	C10	General purpose input/output 23 (I/O/Z)(4) Enhanced QEP1 index (I/O) SPI-C slave transmit enable (not available on F2801/9501) (I/O) SCI-B receive (I) (not available on F2801/9501)

(4) The pullups on GPIO12-GPIO34 are enabled upon reset.

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM BALL #	
GPIO24 ECAP1 EQEP2A SPISIMOB	83	C7	General purpose input/output 24 (I/O/Z)(4) Enhanced capture 1 (I/O) Enhanced QEP2 input A (I) (not available on F2801/9501) SPI-B slave in, master out (I/O)
GPIO25 ECAP2 EQEP2B SPISOMIB	91	C5	General purpose input/output 25 (I/O/Z)(4) Enhanced capture 2 (I/O) Enhanced QEP2 input B (I) (not available on F2801/9501) SPI-B master in, slave out (I/O)
GPIO26 ECAP3 EQEP2I SPICLKB	99	A2	General purpose input/output 26 (I/O/Z)(4) Enhanced capture 3 (I/O) (not available on F2801/9501) Enhanced QEP2 index (I/O) (not available on F2801/9501) SPI-B clock (I/O)
GPIO27 ECAP4 EQEP2S SPISTEB	79	C8	General purpose input/output 27 (I/O/Z)(4) Enhanced capture 4 (I/O) (not available on F2801/9501) Enhanced QEP2 strobe (I/O) (not available on F2801) SPI-B slave transmit enable (I/O)
GPIO28 SCIRXDA - $\overline{TZ5}$	92	D5	General purpose input/output 28. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) SCI receive data (I) - Trip zone 5 (I)
GPIO29 SCITXDA - $\overline{TZ6}$	4	C3	General purpose input/output 29. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) SCI transmit data (O) - Trip zone 6 (I)
GPIO30 CANRXA - -	6	D2	General purpose input/output 30. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) Enhanced CAN-A receive data (I) - -
GPIO31 CANTXA - -	7	D1	General purpose input/output 31. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) Enhanced CAN-A transmit data (O) - -
GPIO32 SDAA EPWMSYNCI $\overline{ADCSOCAO}$	100	A1	General purpose input/output 32 (I/O/Z)(4) I2C data open-drain bidirectional port (I/OD) Enhanced PWM external sync pulse input (I) ADC start-of-conversion (O)
GPIO33 SCLA EPWMSYNCO $\overline{ADCSOCBO}$	5	C1	General-Purpose Input/Output 33 (I/O/Z)(4) I2C clock open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse output (O) ADC start-of-conversion (O)
GPIO34 - - -	43	G7	General-Purpose Input/Output 34 (I/O/Z)(4) - - -

3 Functional Overview



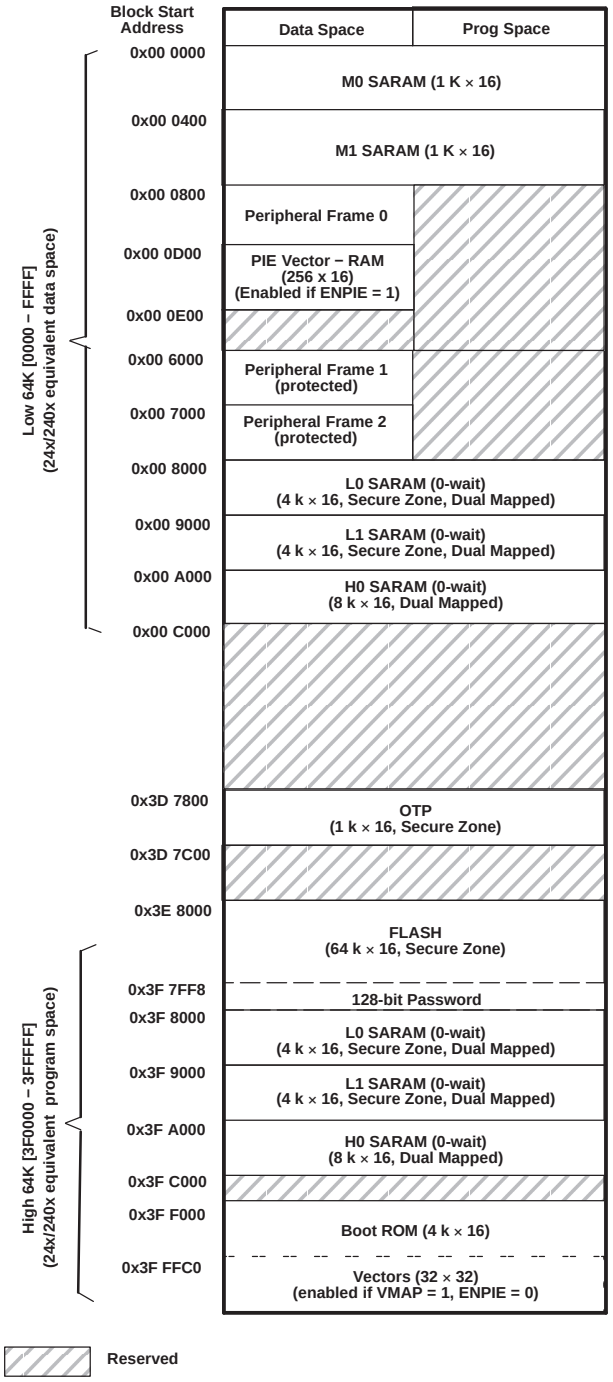
A. 43 of the possible 96 interrupts are used on the devices.

B. Not available in F2801/9501

C. Not available in F2806 or F2801/9501

Figure 3-1. Functional Block Diagram

3.1 Memory Map



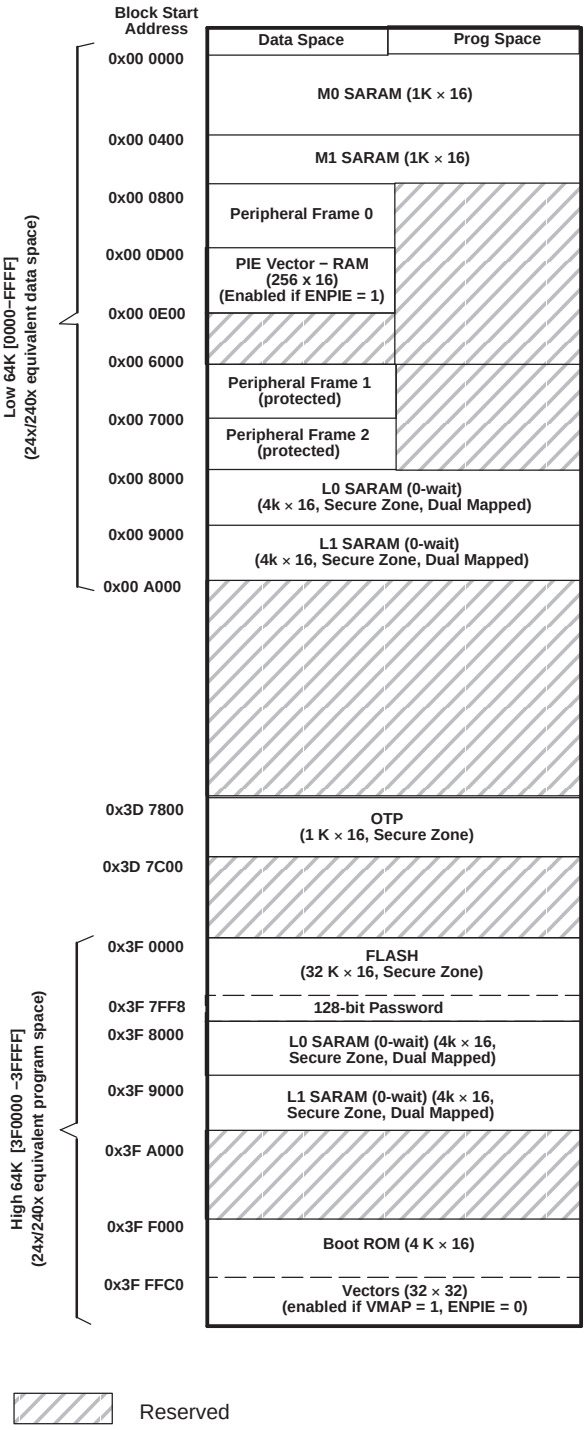
A. Memory blocks are not to scale.

B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.

C. " Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.

D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3-2. F2808 Memory Map



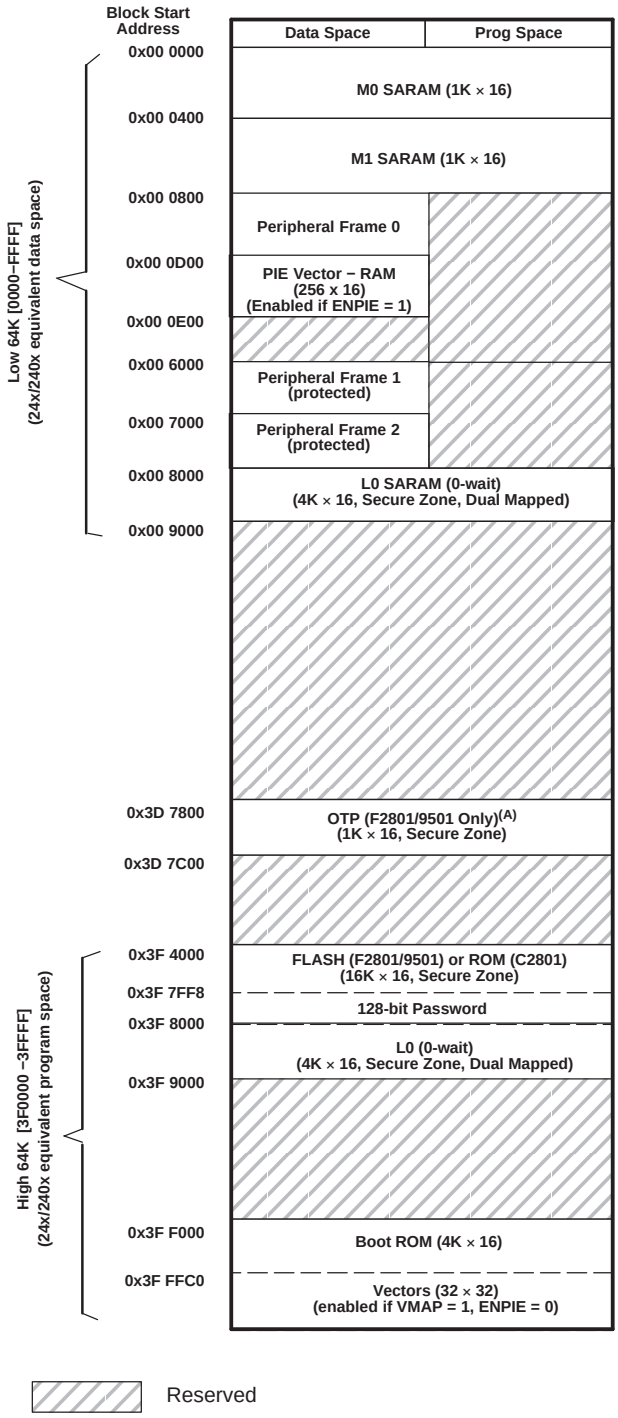
A. Memory blocks are not to scale.

B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.

C. " Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.

D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3-3. F2806 Memory Map



A. Memory blocks are not to scale.

B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.

C. " Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.

D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3-4. F2801/9501 Memory Map

Table 3-1. Addresses of Flash Sectors in F2808

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 0x3E BFFF	Sector D (16K x 16)
0x3E C000 0x3E FFFF	Sector C (16K x 16)
0x3F 0000 0x3F 3FFF	Sector B (16K x 16)
0x3F 4000 0x3F 7F7F	Sector A (16K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3-2. Addresses of Flash Sectors in F2806

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 0000 0x3F 1FFF	Sector D (8K x 16)
0x3F 2000 0x3F 3FFF	Sector C (8K x 16)
0x3F 4000 0x3F 5FFF	Sector B (8K x 16)
0x3F 6000 0x3F 7F7F	Sector A (8K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3-3. Addresses of Flash Sectors in F2801/9501

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 4000 0x3F 4FFF	Sector D (4K x 16)
0x3F 5000 0x3F 5FFF	Sector C (4K x 16)
0x3F 6000 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 0x3F 7F7F	Sector A (4K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

NOTE

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the code-security passwords are programmed. If security is not a concern, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data variables and should not contain program code.

Peripheral Frame 1 and Peripheral Frame 2 are grouped together so as to enable these blocks to be write/read peripheral block protected. The protected mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, appears in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected so as to make sure that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait states for the various spaces in the memory map area are listed in Table 3-4.

Table 3-4. Wait States

AREA	WAIT-STATES	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	Fixed
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Fixed. The eCAN peripheral can extend a cycle as needed.
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed
L0 & L1 SARAMs	0-wait	
OTP	Programmable, 1-wait minimum	Programmed via the Flash registers. 1-wait-state operation is possible at a reduced CPU frequency. See Section Section 3.2.5 for more information.
Flash	Programmable, 0-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at reduced CPU frequency. The CSM password locations are hardwired for 16 wait-states. See Section Section 3.2.5 for more information.
H0 SARAM	0-wait	Fixed
Boot-ROM	1-wait	Fixed

3.2 Brief Descriptions

3.2.1 C28x CPU

The C28x™ DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is an efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

3.2.2 Memory Bus (Harvard Bus Architecture)

As with many DSP type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed "Harvard Bus", enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

3.2.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments DSP family of devices, the 280x devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Two versions of the peripheral bus are supported on the 280x. One version only supports 16-bit accesses (called peripheral frame 2). The other version supports both 16- and 32-bit accesses (called peripheral frame 1).

3.2.4 Real-Time JTAG and Analysis

The 280x implements the standard IEEE 1149.1 JTAG interface. Additionally, the 280x supports real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The 280x implements the real-time mode in hardware within the CPU. This is a unique feature to the 280x, no software monitor is required. Additionally, special analysis hardware is provided which allows the user to set hardware breakpoint or data/address watch-points and generate various user-selectable break events when a match occurs.

3.2.5 Flash

The F2808 contains 64K x 16 of embedded flash memory, segregated into four 16K X 16 sectors. The F2806 has 32K X 16 of embedded flash, segregated into four 8K X 16 sectors. The F2801/UCD9501 devices contain 16K X 16 of embedded Flash (four 4K X 16 sectors). All three devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 - 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Note that addresses 0x3F7FF0 - 0x3F7FF5 are reserved for data variables and should not contain program code.

NOTE

The F2808/F2806/F2801 Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

3.2.6 M0, M1 SARAMs

All 280x devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

3.2.7 L0, L1, H0 SARAMs

The F2808 contains an additional 16K x 16 of single-access RAM, divided into 3 blocks (L0-4K, L1-4K, H0-8K). The F2806 contains an additional 8K x 16 of single-access RAM, divided into 2 blocks (L0-4K, L1-4K). The F2801/UCD9501 contain an additional 4K x 16 of single-access RAM (L0-4K). Each block can be independently accessed to minimize CPU pipeline stalls. Each block is mapped to both program and data space.

3.2.8 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math related algorithms.

Table 3-5. Boot Mode Selection

MODE	DESCRIPTION	GPIO18 SPICLKA SCITXDB	GPIO29 SCITXDA	GPIO34
Boot to Flash	Jump to Flash address 0x3F 7FF6 You must have programmed a branch instruction here prior to reset to redirect code execution as desired.	1	1	1
SCI-A Boot	Load a data stream from SCI-A	1	1	0
SPI-A Boot	Load from an external serial SPI EEPROM on SPI-A	1	0	1
I2C Boot	Load data from an external EEPROM at address 0x50 on the I2C bus	1	0	0
eCAN-A Boot	Call CAN_Boot to load from eCAN-A mailbox 1.	0	1	1
Boot to M0 SARAM	Jump to M0 SARAM address 0x00 0000.	0	1	0
Boot to OTP	Jump to OTP address 0x3D 7800	0	0	1
Parallel I/O Boot	Load data from GPIO0 - GPIO15	0	0	0

3.2.9 Security

The 280x devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit "KEY" value, which matches the value stored in the password locations within the Flash.

NOTE

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the Code Security Password is programmed. If security is not a concern, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data variables and should not contain program code.

The 128-bit password (at 0x3F 7FF8 - 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

NOTE

Code Security Module Disclaimer

The Code Security Module ("CSM") included on this device was designed to password protect the data stored in the associated memory (either ROM or Flash) and is warranted by Texas Instruments (Texas Instruments), in accordance with its standard terms and conditions, to conform to TI's published specifications for the warranty period applicable for this device.

Texas Instruments DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, Texas Instruments MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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3.2.10 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the 280x, 43 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

3.2.11 External Interrupts (XINT1, XINT2, XNMI)

The 280x supports three masked external interrupts (XINT1, XINT2, XNMI). XNMI can be connected to the INT13 or NMI interrupt of the CPU. Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled (including the XNMI). The masked interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. Unlike the 281x devices, there are no dedicated pins for the external interrupts. Rather, any Port A GPIO pin can be configured to trigger any external interrupt.

3.2.12 Oscillator and PLL

The 280x can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to the Electrical Specification section for timing details. The PLL block can be set in bypass mode.

3.2.13 Watchdog

The 280x devices contain a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

3.2.14 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except eCAN) and the ADC blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

3.2.15 Low-Power Modes

The 280x devices are full static CMOS devices. Three low-power modes are provided:

IDLE:	Place CPU into low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
STANDBY:	Turn off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
HALT:	Turn off oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. A reset or external signal can wake the device from this mode.

3.2.16 Peripheral Frames 0, 1, 2 (PFn)

The 280x segregate peripherals into three sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers (dual-mapped)
PF1:	eCAN:	eCAN Mailbox and Control Registers
	GPIO:	GPIO MUX Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers

	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Result Register
	I^2C:	Inter-Integrated Circuit Module and Registers

3.2.17 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

3.2.18 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for Real-Time OS (RTOS)/BIOS applications. CPU-Timer 1 is also reserved for Texas Instruments system functions. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

3.2.19 Control Peripherals

The 280x devices support the following peripherals which are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support HRPWM features.
eCAP:	The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
eQEP:	The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
ADC:	The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

3.2.20 Serial Port Peripherals

The 280x devices support the following serial communication peripherals:

- eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.
- SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the 280x, the SPI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.
- SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the 280x, the SCI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.
- I^2C: The inter-integrated circuit (I^2C) module provides an interface between a DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I^2C module. On the 280x, the I^2C contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

3.3 Register Map

The 280x devices contain three peripheral register spaces. The spaces are categorized as follows:

- Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 3-6
- Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3-7
- Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3-8

Table 3-6. Peripheral Frame 0 Registers(1)(2)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE(3)
Device Emulation Registers	0x0880 0x09FF	384	EALLOW protected
FLASH Registers(4)	0x0A80 0x0ADF	96	EALLOW protected CSM Protected
Code Security Module Registers	0x0AE0 0x0AEF	16	EALLOW protected
ADC Result Registers (dual-mapped)	0xB00 0xB0F	16	Not EALLOW protected
CPU-TIMER0/1/2 Registers	0x0C00 0x0C3F	64	Not EALLOW protected
PIE Registers	0x0CE0 0x0CFF	32	Not EALLOW protected
PIE Vector Table	0x0D00 0x0DFF	256	EALLOW protected

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) Missing segments of memory space are reserved and should not be used in applications.
(3) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(4) The Flash Registers are also protected by the Code Security Module (CSM).

Table 3-7. Peripheral Frame 1 Registers[1][2]

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
eCANA Registers	0x6000 0x60FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANA Mailbox RAM	0x6100 0x61FF	256 (128 x 32)	Not EALLOW-protected
eCANB Registers	0x6200 0x62FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANB Mailbox RAM	0x6300 0x63FF	256 (128 x 32)	Not EALLOW-protected
ePWM1 Registers	0x6800 0x683F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2
ePWM2 Registers	0x6840 0x687F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2.
ePWM3 Registers	0x6880 0x68BF	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2.
ePWM4 Registers	0x68C0 0x68FF	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2.
ePWM5 Registers	0x6900 0x693F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2.
ePWM6 Registers	0x6940 0x697F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4-2.
eCAP1 Registers	0x6A00 0x6A1F	32 (16 x 32)	Not EALLOW protected
eCAP2 Registers	0x6A20 0x6A3F	32 (16 x 32)	Not EALLOW protected
eCAP3 Registers	0x6A40 0x6A5F	32 (16 x 32)	Not EALLOW protected
eCAP4 Registers	0x6A60 0x6A7F	32 (16 x 32)	Not EALLOW protected
eQEP1 Registers	0x6B00 0x6B3F	64 (32 x 32)	Not EALLOW protected
eQEP2 Registers	0x6B40 0x6B7F	64 (32 x 32)	Not EALLOW protected
GPIO Control Registers	0x6F80 0x6FBF	128 (64 x 32)	EALLOW protected
GPIO Data Registers	0x6FC0 0x6FDF	32 (16 x 32)	Not EALLOW protected
GPIO Interrupt and LPM Select Registers	0x6FE0 0x6FFF	32 (16 x 32)	EALLOW protected

(1) The eCAN control registers only support 32-bit read/write operations. All 32-bit accesses are aligned to even address boundaries.
(2) Missing segments of memory space are reserved and should not be used in applications.

Table 3-8. Peripheral Frame 2 Registers(1)(2)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
System Control Registers	0x7010 0x702F	32	EALLOW Protected
SPI-A Registers	0x7040 0x704F	16	Not EALLOW Protected
SCI-A Registers	0x7050 0x705F	16	Not EALLOW Protected
External Interrupt Registers	0x7070 0x707F	16	Not EALLOW Protected
ADC Registers	0x7100 0x711F	32	Not EALLOW Protected
SPI-B Registers	0x7740 0x774F	16	Not EALLOW Protected
SCI-B Registers	0x7750 0x775F	16	Not EALLOW Protected
SPI-C Registers	0x7760 0x776F	16	Not EALLOW Protected
SPI-D Registers	0x7780 0x778F	16	Not EALLOW Protected
I^2C Registers	0x7900 0x792F	48	Not EALLOW Protected

(1) Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data may be returned or written).
(2) Missing segments of memory space are reserved and should not be used in applications.

3.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3-9.

Table 3-9. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION	
DEVICECNF	0x0880 0x0881	2	Device Configuration Register	
PARTID	0x0882	1	Part ID Register	0x002C(1) - F2801/9501 0x0034 - F2806 0x003C - F2808
REVID	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMX 0x0001 - Silicon Rev. A - TMX 0x0002 - Silicon Rev. B - TMS
PROTSTART	0x0884	1	Block Protection Start Address Register	
PROTRANGE	0x0885	1	Block Protection Range Address Register	

(1) The first byte (00) denotes flash devices. "FF" is reserved for future ROM devices. Other values are reserved for future devices.

3.5 Interrupts

Figure 3-5 shows how the various interrupt sources are multiplexed within the 280x devices.

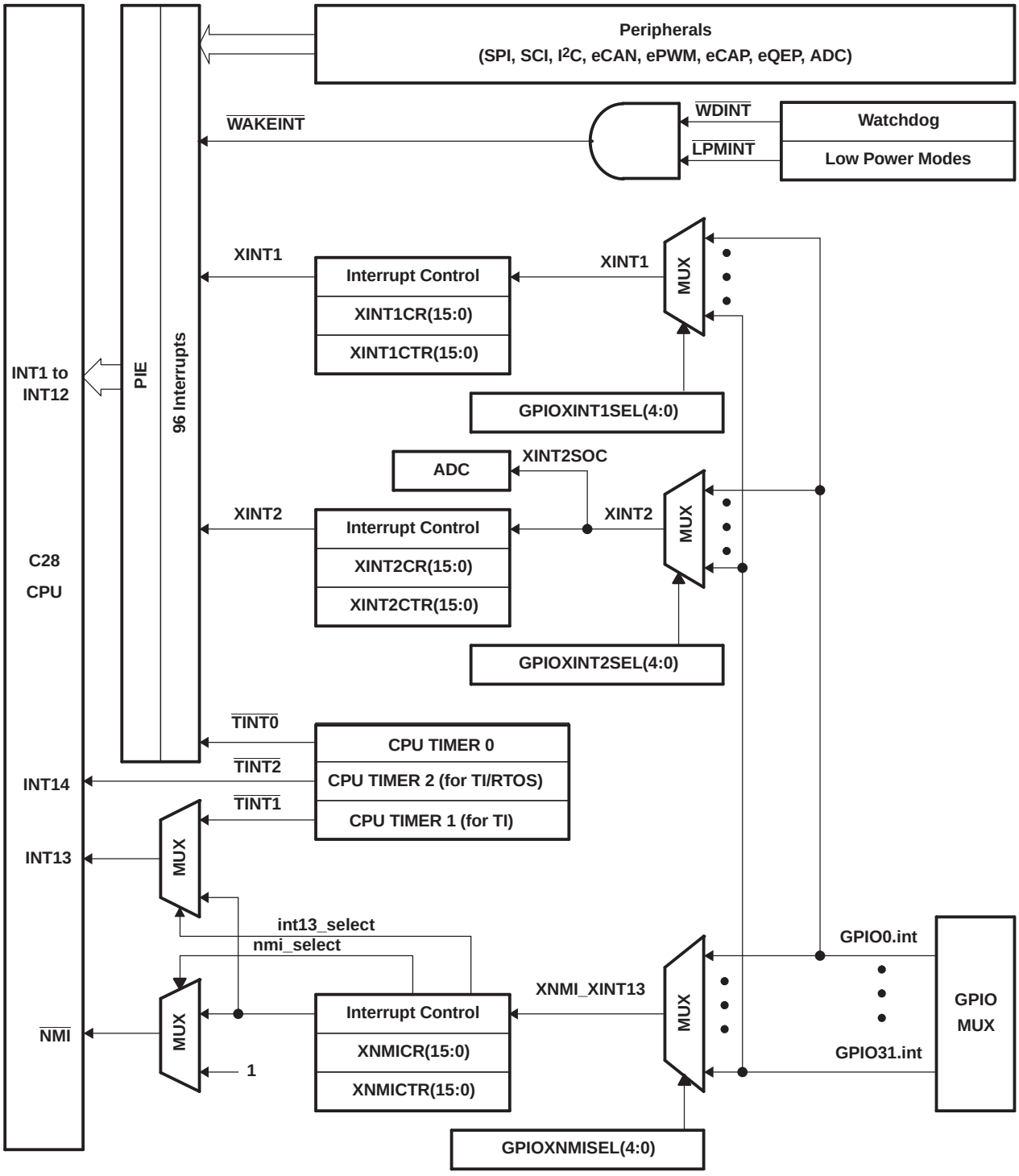


Figure 3-5. External and PIE Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the 280x, 43 of these are used by peripherals as shown in Table 3-10.

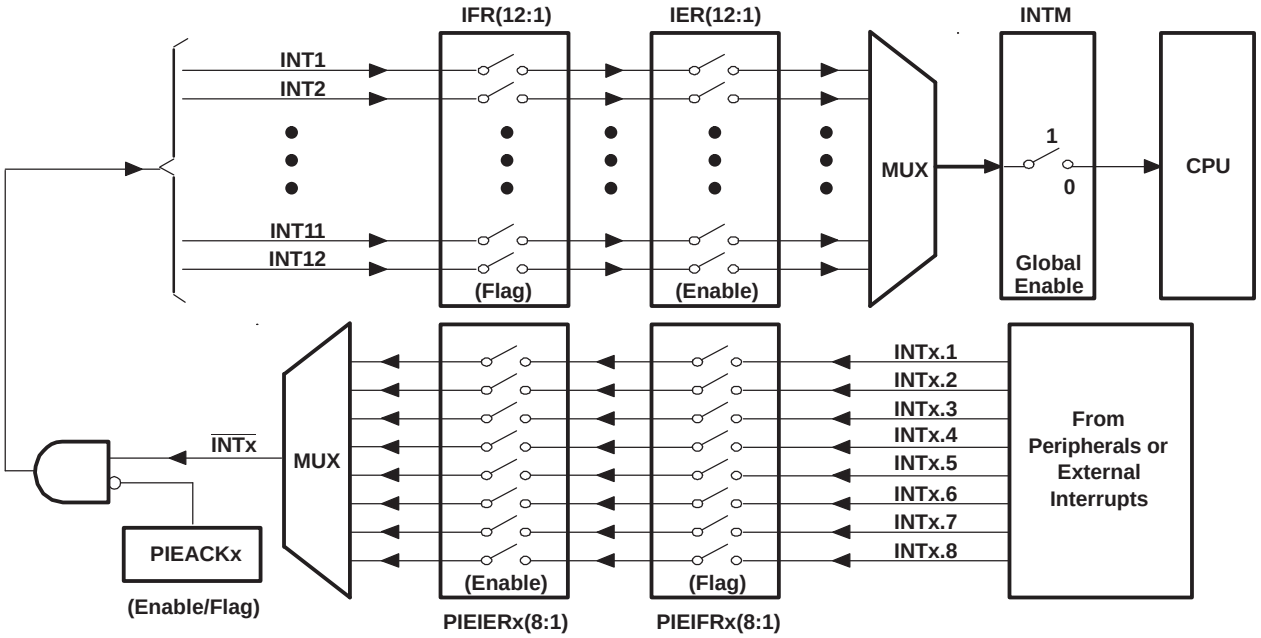


Figure 3-6. Multiplexing of Interrupts Using the PIE Block

Table 3-10. PIE Peripheral Interrupts(1)

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	reserved	SEQ2INT (ADC)	SEQ1INT (ADC)
INT2	reserved	reserved	EPWM6_TZINT (ePWM6)	EPWM5_TZINT (ePWM5)	EPWM4_TZINT (ePWM4)	EPWM3_TZINT (ePWM3)	EPWM2_TZINT (ePWM2)	EPWM1_TZINT (ePWM1)
INT3	reserved	reserved	EPWM6_INT (ePWM6)	EPWM5_INT (ePWM5)	EPWM4_INT (ePWM4)	EPWM3_INT (ePWM3)	EPWM2_INT (ePWM2)	EPWM1_INT (ePWM1)
INT4	reserved	reserved	reserved	reserved	ECAP4_INT (eCAP4)	ECAP3_INT (eCAP3)	ECAP2_INT (eCAP2)	ECAP1_INT (eCAP1)
INT5	reserved	reserved	reserved	reserved	reserved	reserved	EQEP2_INT (eQEP2)	EQEP1_INT (eQEP1)
INT6	SPITXINTD (SPI-D)	SPIRXINTD (SPI-D)	SPITXINTC (SPI-C)	SPIRXINTC (SPI-C)	SPITXINTB (SPI-B)	SPIRXINTB (SPI-B)	SPITXINTA (SPI-A)	SPIRXINTA (SPI-A)
INT7	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT8	reserved	reserved	reserved	reserved	reserved	reserved	I2CINT2A (I2C-A)	I2CINT1A (I2C-A)
INT9	ECAN1_INTB (CAN-B)	ECAN0_INTB (CAN-B)	ECAN1_INTA (CAN-A)	ECAN0_INTA (CAN-A)	SCITXINTB (SCI-B)	SCIRXINTB (SCI-B)	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT11	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT12	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

(1) Out of the 96 possible interrupts, 43 interrupts are currently used. The remaining interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
1) No peripheral within the group is asserting interrupts.
2) No peripheral interrupts are assigned to the group (example PIE group 12).

Table 3-11. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

3.5.1 External Interrupts

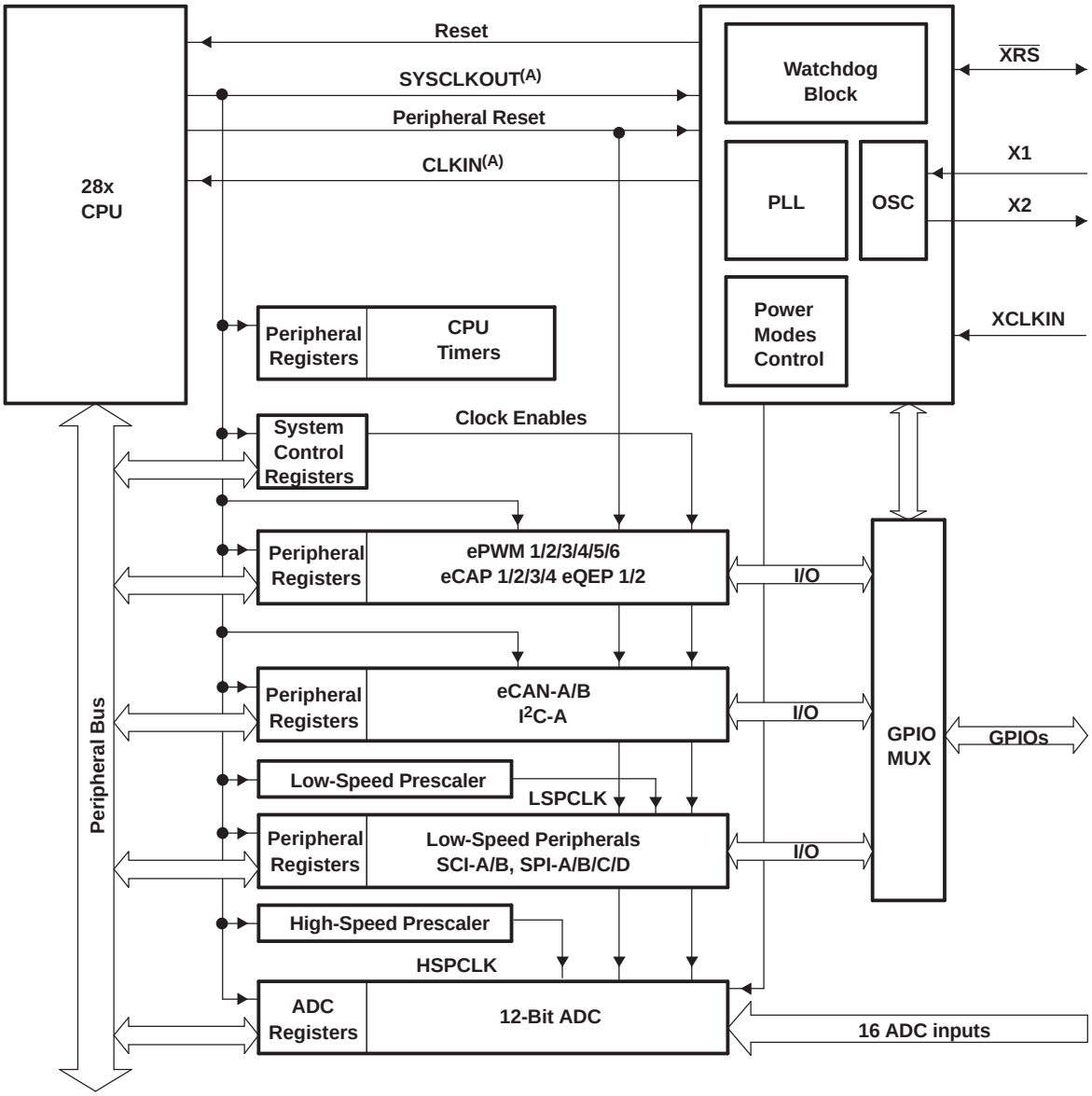
Table 3-12. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x7070	1	XINT1 control register
XINT2CR	0x7071	1	XINT2 control register
reserved	0x7072 0x7076	5	
XNMICR	0x7077	1	XNMI control register
XINT1CTR	0x7078	1	XINT1 counter register
XINT2CTR	0x7079	1	XINT2 counter register
reserved	0x707A 0x707E	5	
XNMICTR	0x707F	1	XNMI counter register

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

3.6 System Control

This section describes the 280x oscillator, PLL and clocking mechanisms, the watchdog function and the low power modes. Figure 3-7 shows the various clock and reset domains in the 280x devices that will be discussed.



A. CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 3-7. Clock and Reset Domains

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 3-13.

Table 3-13. PLL, Clocking, Watchdog, and Low-Power Mode Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XCLK	0x7010	1	XCLKOUT Pin Control, X1 and XCLKIN Status Register
PLLSTS	0x7011	1	PLL Status Register
reserved	0x7012 0x7019	8	
HISPCP	0x701A	1	High-Speed Peripheral Clock Prescaler Register (for HSPCLK)
LOSPCP	0x701B	1	Low-Speed Peripheral Clock Prescaler Register (for LSPCLK)
PCLKCR0	0x701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x701D	1	Peripheral Clock Control Register 1
LPMCR0	0x701E	1	Low Power Mode Control Register 0
reserved	0x701F 0x7020	1	
PLLCR	0x7021	1	PLL Control Register
SCSR	0x7022	1	System Control and Status Register
WDCNTR	0x7023	1	Watchdog Counter Register
reserved	0x7024	1	
WDKEY	0x7025	1	Watchdog Reset Key Register
reserved	0x7026 0x7028	3	
WDCR	0x7029	1	Watchdog Control Register
reserved	0x702A 0x702F	6	

(1) All of the registers in this table are EALLOW protected.

3.6.1 OSC and PLL Block

Figure 3-8 shows the OSC and PLL block on the 280x.

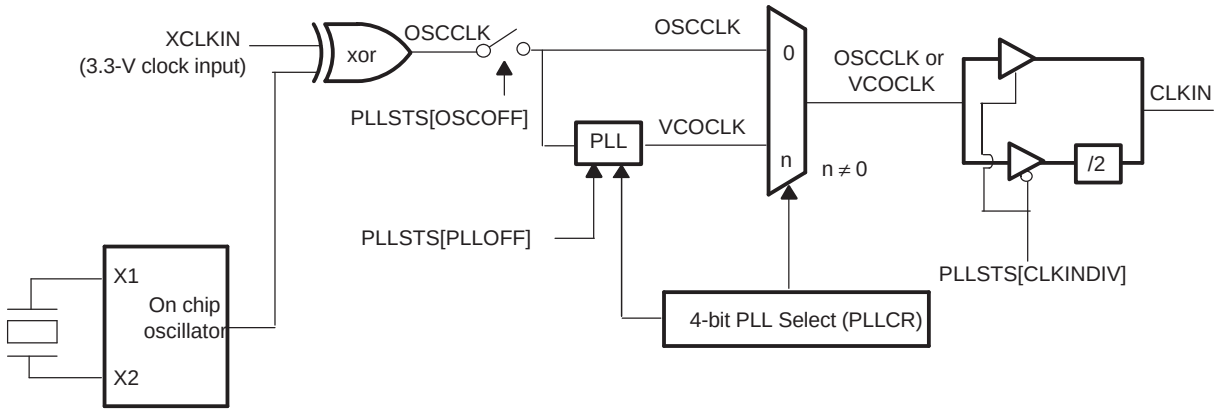


Figure 3-8. OSC and PLL Block Diagram

The on-chip oscillator circuit enables a crystal/resonator to be attached to the 280x devices using the X1 and X2 pins. If the on-chip oscillator is not used, an external oscillator can be used in either one of the following configurations:

1. A 3.3-V external oscillator can be directly connected to the XCLKIN pin. The X2 pin should be left unconnected and the X1 pin tied low. The logic-high level in this case should not exceed V_{DDIO}.
2. A 1.8-V external oscillator can be directly connected to the X1 pin. The X2 pin should be left

unconnected and the XCLKIN pin tied low. The logic-high level in this case should not exceed V_{DD}.

The three possible input-clock configurations are shown in Figure 3-9 through Figure 3-11

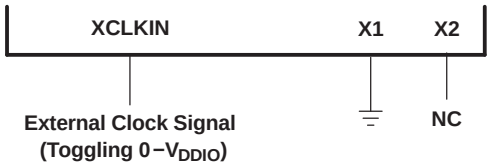


Figure 3-9. Using a 3.3-V External Oscillator

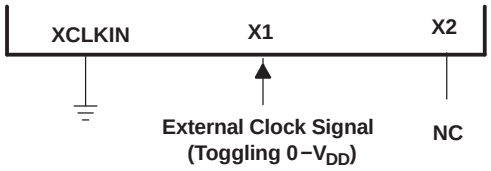


Figure 3-10. Using a 1.8-V External Oscillator

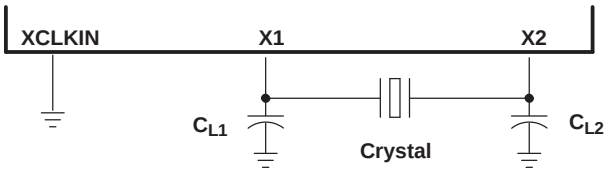


Figure 3-11. Using the Internal Oscillator

3.6.1.1 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 20 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 30 to 60 Ω

Texas Instruments recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

3.6.1.2 PLL-Based Clock Module

The 280x devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131072 OSCCLK cycles.

Table 3-14. PLLCR Register Bit Definitions

PLLCR[DIV](1)	PLLSTS[CLKINDIV]	SYSCLKOUT (CLKIN)(2)
0000 (PLL bypass)	0	OSCCLK/2
0000 (PLL bypass)	1	OSCCLK
0001	0	(OSCCLK*1)/2
0010	0	(OSCCLK*2)/2
0011	0	(OSCCLK*3)/2
0100	0	(OSCCLK*4)/2
0101	0	(OSCCLK*5)/2
0110	0	(OSCCLK*6)/2
0111	0	(OSCCLK*7)/2
1000	0	(OSCCLK*8)/2
1001	0	(OSCCLK*9)/2
1010	0	(OSCCLK*10)/2
1011-1111	0	reserved

(1) This register is EALLOW protected.
(2) CLKIN is the input clock to the CPU. SYSCLKOUT is the output clock from the CPU. The frequency of SYSCLKOUT is the same as CLKIN.

CAUTION

PLLSTS[CLKINDIV] can be set to 1 only if PLLCR is 0x0000. PLLCR should not be changed once PLLSTS[CLKINDIV] is set.

The PLL-based clock module provides two modes of operation:

- Crystal-operation - This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation - This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the X1 or the XCLKIN pin.

Table 3-15. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[CLKINDIV]	SYSCLKOUT (CLKIN)
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0	OSCCLK/2
		1	OSCCLK
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0	OSCCLK/2
		1	OSCCLK
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0	OSCCLK*n/2

3.6.1.3 Loss of Input Clock

In PLL-enabled and PLL-bypass mode, if the input clock OSCCLK is removed or absent, the PLL will still issue a "limp-mode" clock. The limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1-5 MHz. Limp mode is not specified to work from power-up, only after input clocks have been present initially. In PLL bypass mode, the limp mode clock from the PLL is automatically routed to the CPU if the input clock is removed or absent.

Normally, when the input clocks are present, the watchdog counter decrements to initiate a watchdog

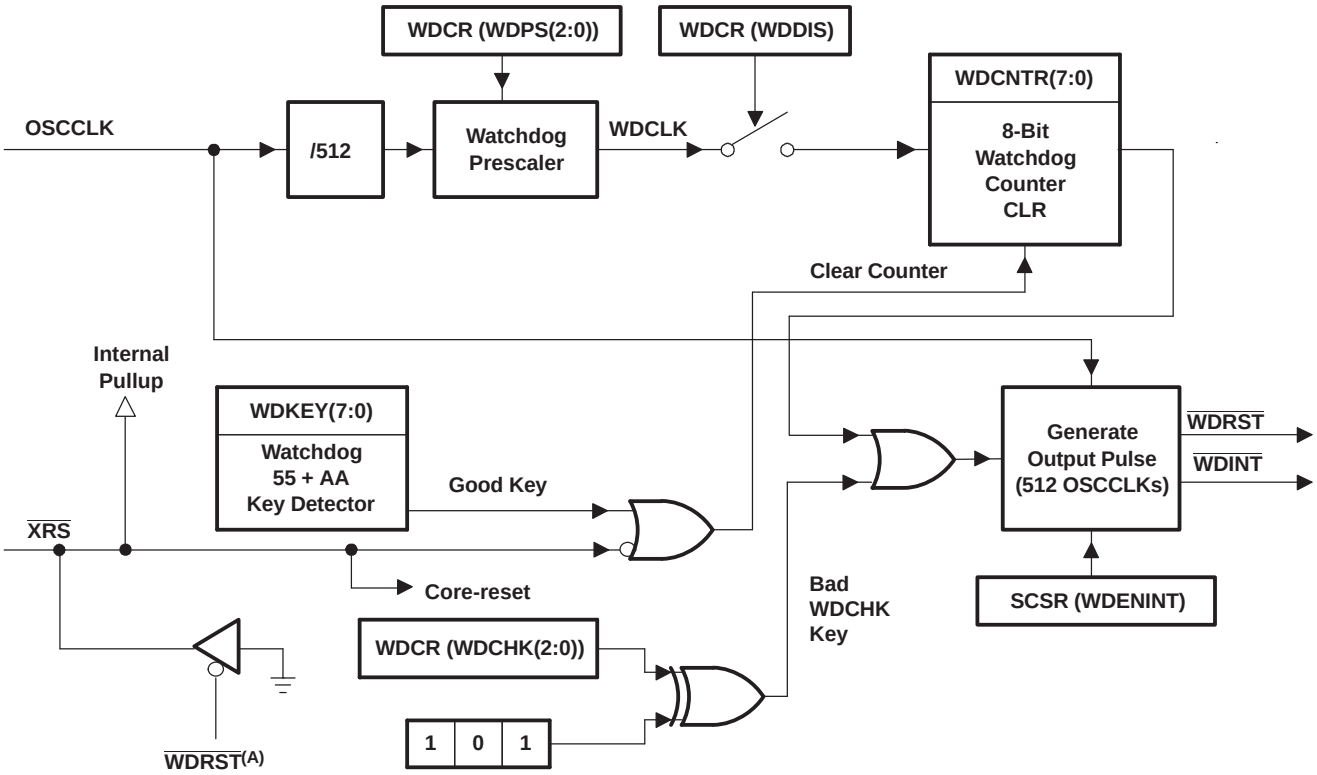
reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter stops decrementing (i.e., the watchdog counter does not change with the limp-mode clock). In addition to this, the device will be reset and the “Missing Clock Status” (MCLKSTS) bit will be set. These conditions could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedure for the system.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the DSP will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the DSP, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory and the V_{DD3VFL} rail.

3.6.2 Watchdog Block

The watchdog block on the 280x is similar to the one used on the 240x and 281x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 3-12 shows the various functional blocks within the watchdog module.



A. The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 3-12. Watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The WATCHDOG module will run off OSCCLK. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section Section 3.7, Low-Power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence so is the WATCHDOG.

3.7 Low-Power Modes Block

The low-power modes on the 280x are similar to the 240x devices. Table 3-16 summarizes the various modes.

Table 3-16. Low-Power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On(2)	$\overline{\text{XRS}}$, Watchdog interrupt, any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, debugger(3), XNMI
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, XNMI, debugger(3)

(1) The Exit column lists which signals or under what conditions the low power mode will be exited. A low signal, on any of the signals, will exit the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode will not be exited and the device will go back into the indicated low power mode.
(2) The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.
(3) On the C28x, the JTAG port can still function even if the CPU clock (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt or an XNMI that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: Only the $\overline{\text{XRS}}$ and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712) for more details.

4 Peripherals

The integrated peripherals of the 280x are described in the following subsections:

- Three 32-bit CPU-Timers
- Up to six enhanced PWM modules (ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6)
- Up to four enhanced capture modules (eCAP1, eCAP2, eCAP3, eCAP4)
- Up to two enhanced QEP modules (eQEP1, eQEP2)
- Enhanced analog-to-digital converter (ADC) module
- Up to two enhanced controller area network (eCAN) modules (eCAN-A, eCAN-B)
- Up to two serial communications interface modules (SCI-A, SCI-B)
- Up to four serial peripheral interface (SPI) modules (SPI-A, SPI-B, SPI-C, SPI-D)
- Inter-integrated circuit module (I^2C)
- Digital I/O and shared pin functions

4.1 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the 280x devices (CPU-TIMER0/1/2).

CPU-Timer 1 is reserved for Texas Instruments system functions and Timer 2 is reserved for DSP/BIOS™. CPU-Timer 0 can be used in user applications. These timers are different from the timers that are present in the ePWM modules.

NOTE

NOTE: If the application is not using DSP/BIOS, then CPU-Timer 2 can be used in the application.

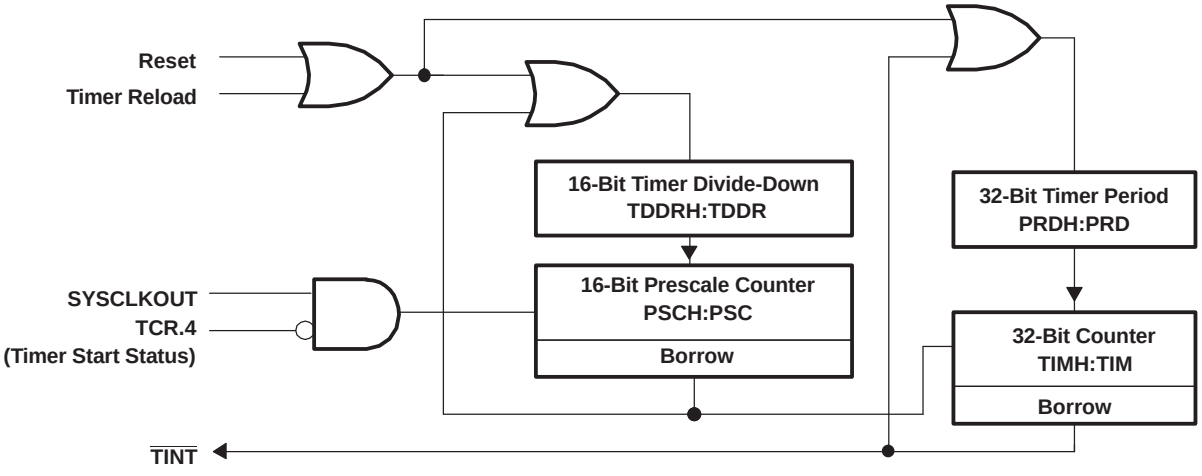
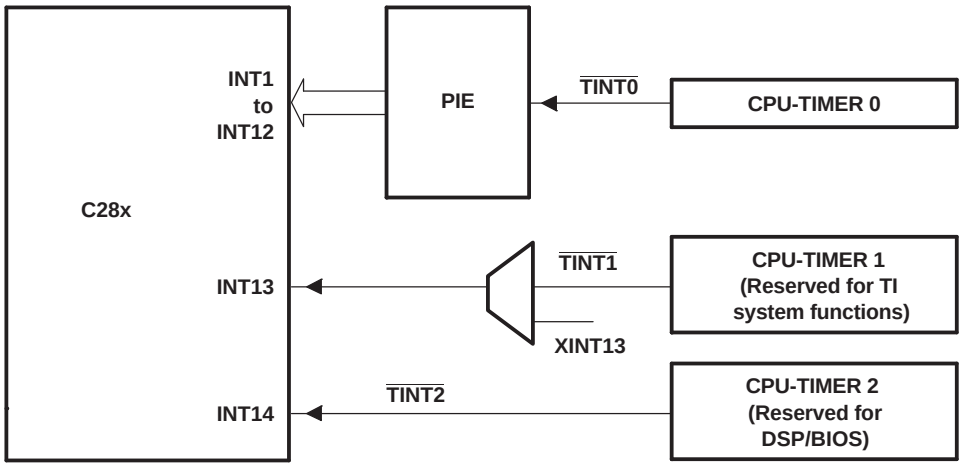


Figure 4-1. CPU-Timers

In the 280x devices, the timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 4-2.



A. The timer registers are connected to the memory bus of the C28x processor.

B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

C. While TIMER1 is reserved, INT13 is not reserved and the user can use XINT13 connected to INT13.

Figure 4-2. CPU-Timer Interrupt Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register "TIMH:TIM" is loaded with the value in the period register "PRDH:PRD". The counter register decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 4-1 are used to configure the timers. For more information, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

Table 4-1. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x0C04	1	CPU-Timer 0, Control Register
reserved	0x0C05	1	
TIMER0TPR	0x0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x0C0C	1	CPU-Timer 1, Control Register
reserved	0x0C0D	1	
TIMER1TPR	0x0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x0C14	1	CPU-Timer 2, Control Register
reserved	0x0C15	1	

Table 4-1. CPU-Timers 0, 1, 2 Configuration and Control Registers (continued)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER2TPR	0x0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x0C17	1	CPU-Timer 2, Prescale Register High
reserved	0x0C18 0x0C3F	40	

4.2 Enhanced PWM Modules (ePWM1/2/3/4/5/6)

The 280x device contains up to six enhanced PWM Modules (ePWM). Figure 4-3 shows a block diagram of multiple ePWM modules. Figure 4-4 shows the signal interconnections with the ePWM. See the *TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRU791) for more details.

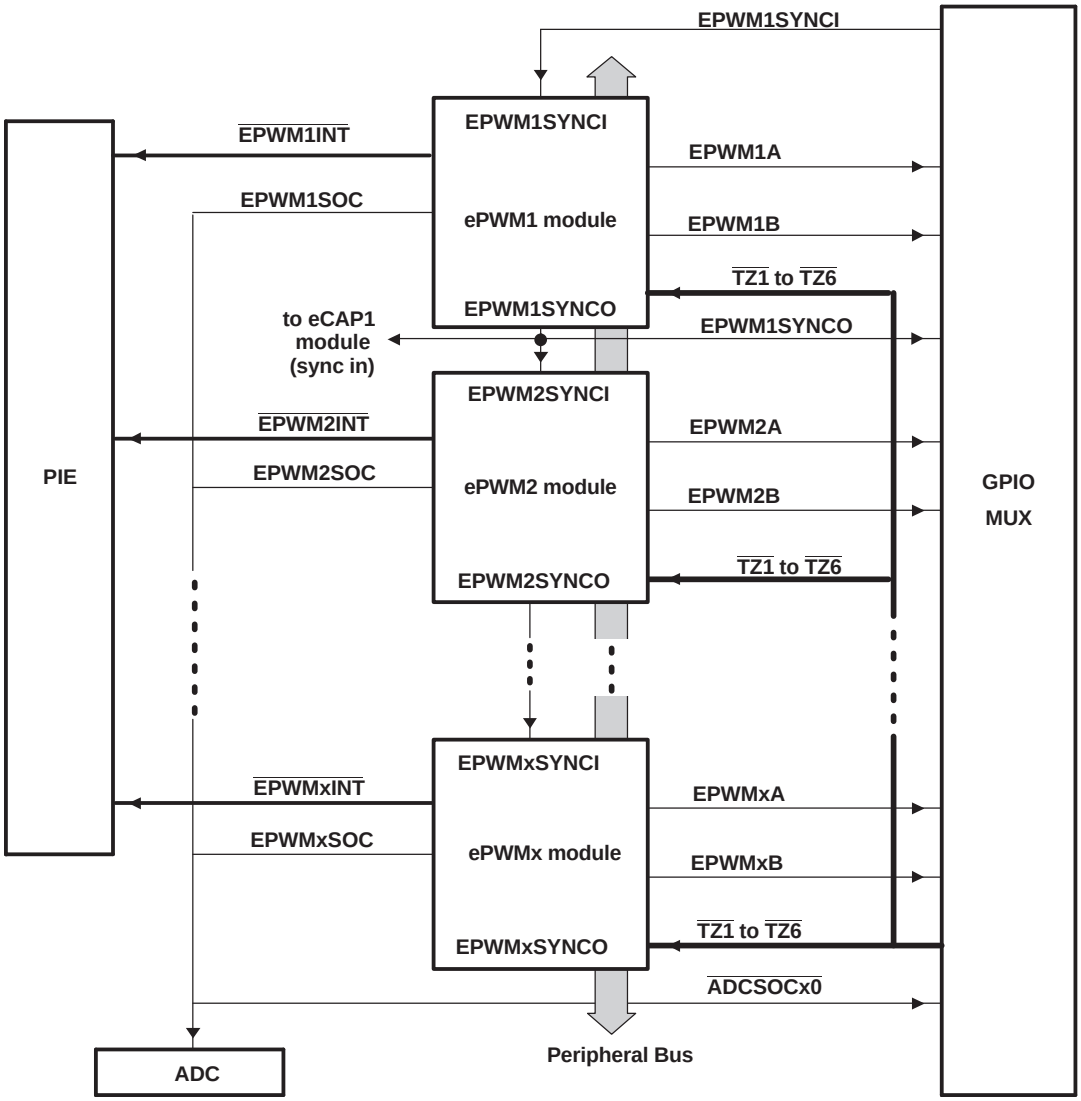


Figure 4-3. Multiple PWM Modules in a 280x System

Table 4-2 shows the complete ePWM register set per module.

Table 4-2. ePWM Control and Status Registers

NAME	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	0x6900	0x6940	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	0x6901	0x6941	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	N/A	N/A	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	0x6903	0x6943	1 / 0	Time Base Phase Register
TBCNT	0x6804	0x6844	0x6884	0x68C4	0x6904	0x6944	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	0x6905	0x6945	1 / 1	Time Base Period Register Set
CMPCTL	0x6807	0x6847	0x6887	0x68C7	0x6907	0x6947	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	N/A	N/A	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	0x6909	0x6949	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	0x690A	0x694A	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	0x690B	0x694B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	0x690C	0x694C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	0x690D	0x694D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	0x690E	0x694E	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	0x690F	0x694F	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	0x6910	0x6950	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	0x6911	0x6951	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	0x6912	0x6952	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6814	0x6854	0x6894	0x68D4	0x6914	0x6954	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	0x6915	0x6955	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	0x6916	0x6956	1 / 0	Trip Zone Flag Register
TZCLR	0x6817	0x6857	0x6897	0x68D7	0x6917	0x6957	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	0x6918	0x6958	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	0x6919	0x6959	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	0x691A	0x695A	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	0x691B	0x695B	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	0x691C	0x695C	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	0x691D	0x695D	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	0x691E	0x695E	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	N/A	N/A	1 / 0	HRPWM Configuration Register

(1) Registers that are EALLOW protected.

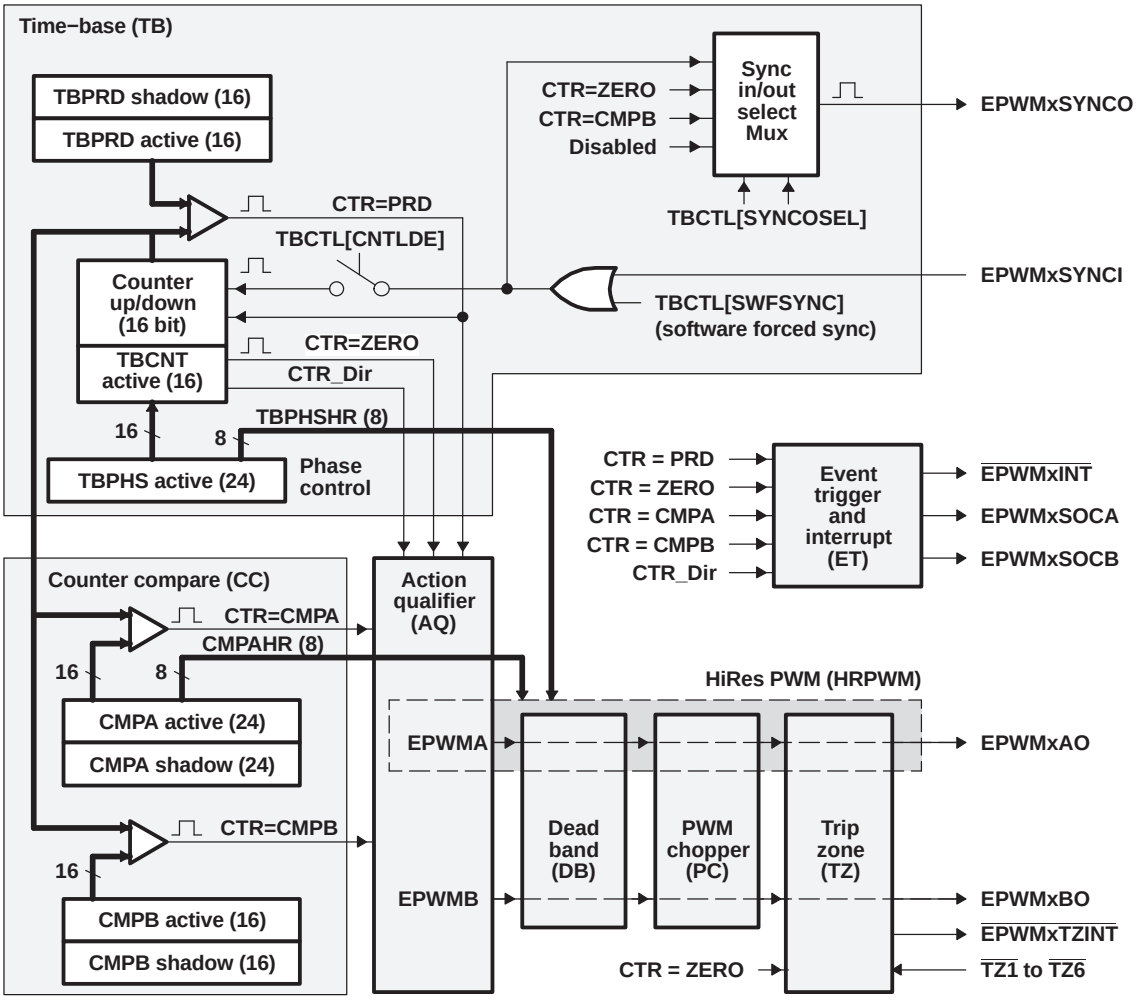


Figure 4-4. ePWM Sub-modules Showing Critical Internal Signal Interconects

4.3 Hi-Resolution PWM (HRPWM)

The HRPWM module offers PWM resolution (time granularity) which is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- Typically used when effective PWM resolution falls below ~ 9-10 bits. This occurs at PWM frequencies greater than ~200 KHz when using a CPU/System clock of 100 MHz.
- This capability can be utilized in both duty cycle and phase-shift control methods.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities are offered only on the A signal path of an ePWM module (i.e., on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

Only PWM channels ePWM 1A, 2A, 3A, 4A support HRPWM features. The remaining ePWM channels do not support the HRPWM features.

4.4 Enhanced CAP Modules (eCAP1/2/3/4)

The 280x device contains up to four enhanced capture (eCAP) modules. Figure 4-5 shows a functional block diagram of a module. See the *TMS320x280x Enhanced Capture (eCAP) Module Reference Guide* (literature number SPRU807) for more details.

The eCAP modules are clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1/2/3/4ENCLK) in the PCLKCR1 register are used to turn off the eCAP modules individually (for low power operation). Upon reset, ECAP1ENCLK, ECAP2ENCLK, ECAP3ENCLK, and ECAP4ENCLK are set to low, indicating that the peripheral clock is off.

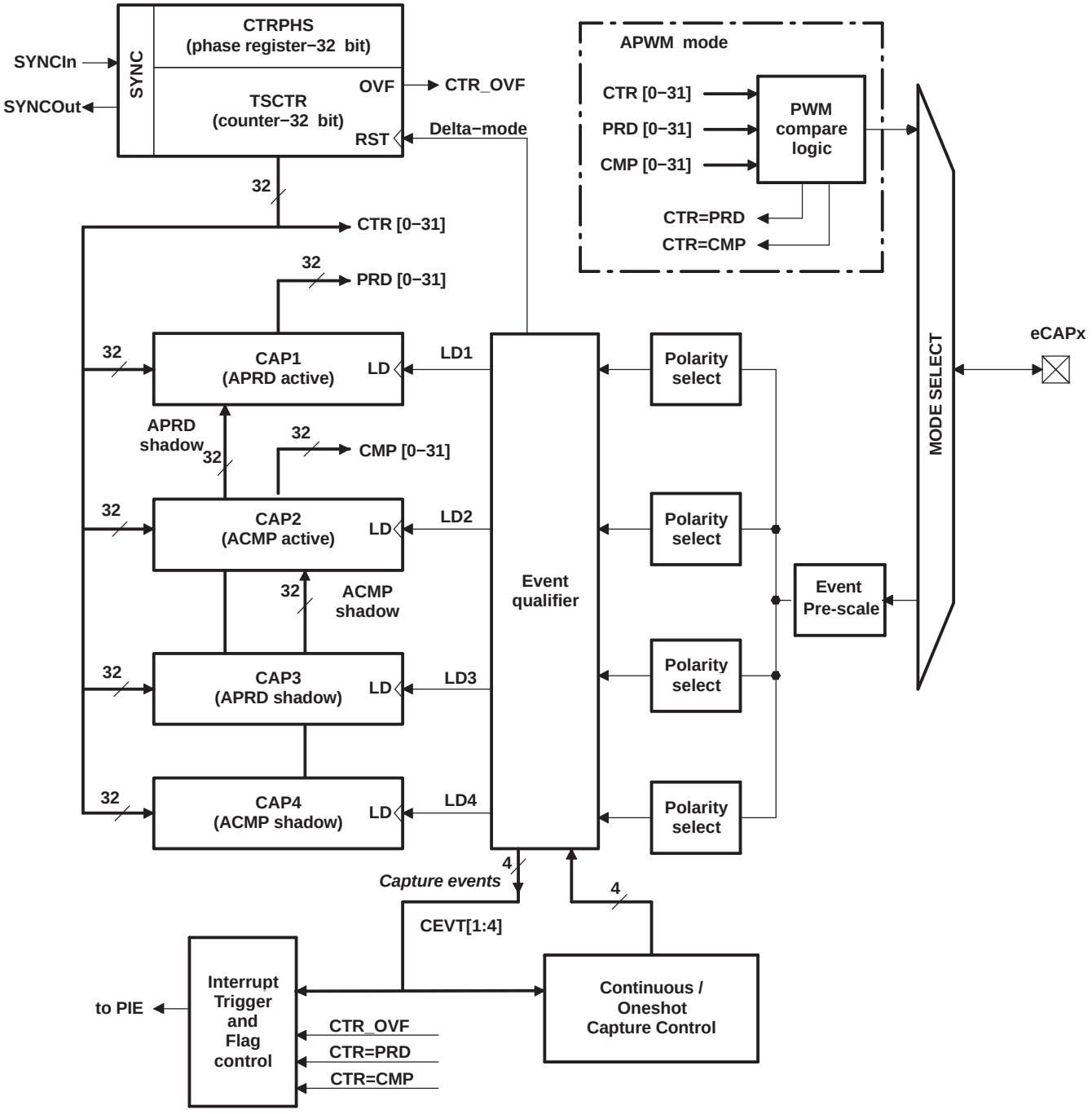


Figure 4-5. eCAP Functional Block Diagram

Table 4-3. eCAP Control and Status Registers

NAME	ECAP1	ECAP2	ECAP3	ECAP4	SIZE (x16)	DESCRIPTION
TSCTR	0x6A00	0x6A20	0x6A40	0x6A60	2	Time-Stamp Counter
CTRPHS	0x6A02	0x6A22	0x6A42	0x6A62	2	Counter Phase Offset Value Register
CAP1	0x6A04	0x6A24	0x6A44	0x6A64	2	Capture 1 Register
CAP2	0x6A06	0x6A26	0x6A46	0x6A66	2	Capture 2 Register
CAP3	0x6A08	0x6A28	0x6A48	0x6A68	2	Capture 3 Register
CAP4	0x6A0A	0x6A2A	0x6A4A	0x6A6A	2	Capture 4 Register
Reserved	0x6A0C-0x6A12	0x6A2C-0x6A32	0x6A4C-0x6A52	0x6A6C-0x6A72	8	
ECCTL1	0x6A14	0x6A34	0x6A54	0x6A74	1	Capture Control Register 1
ECCTL2	0x6A15	0x6A35	0x6A55	0x6A75	1	Capture Control Register 2
ECEINT	0x6A16	0x6A36	0x6A56	0x6A76	1	Capture Interrupt Enable Register
ECFLG	0x6A17	0x6A37	0x6A57	0x6A77	1	Capture Interrupt Flag Register
ECCLR	0x6A18	0x6A38	0x6A58	0x6A78	1	Capture Interrupt Clear Register
ECFRC	0x6A19	0x6A39	0x6A59	0x6A79	1	Capture Interrupt Force Register
Reserved	0x6A1A-0x6A1F	0x6A3A-0x6A3F	0x6A5A-0x6A5F	0x6A7A-0x6A7F	6	

4.5 Enhanced QEP Modules (eQEP1/2)

The 280x device contains up to two enhanced quadrature encoder (eQEP) modules. See the *TMS320x280x Enhanced Quadrature Encoder (eQEP) Module Reference Guide* (literature number SPRU790) for more details.

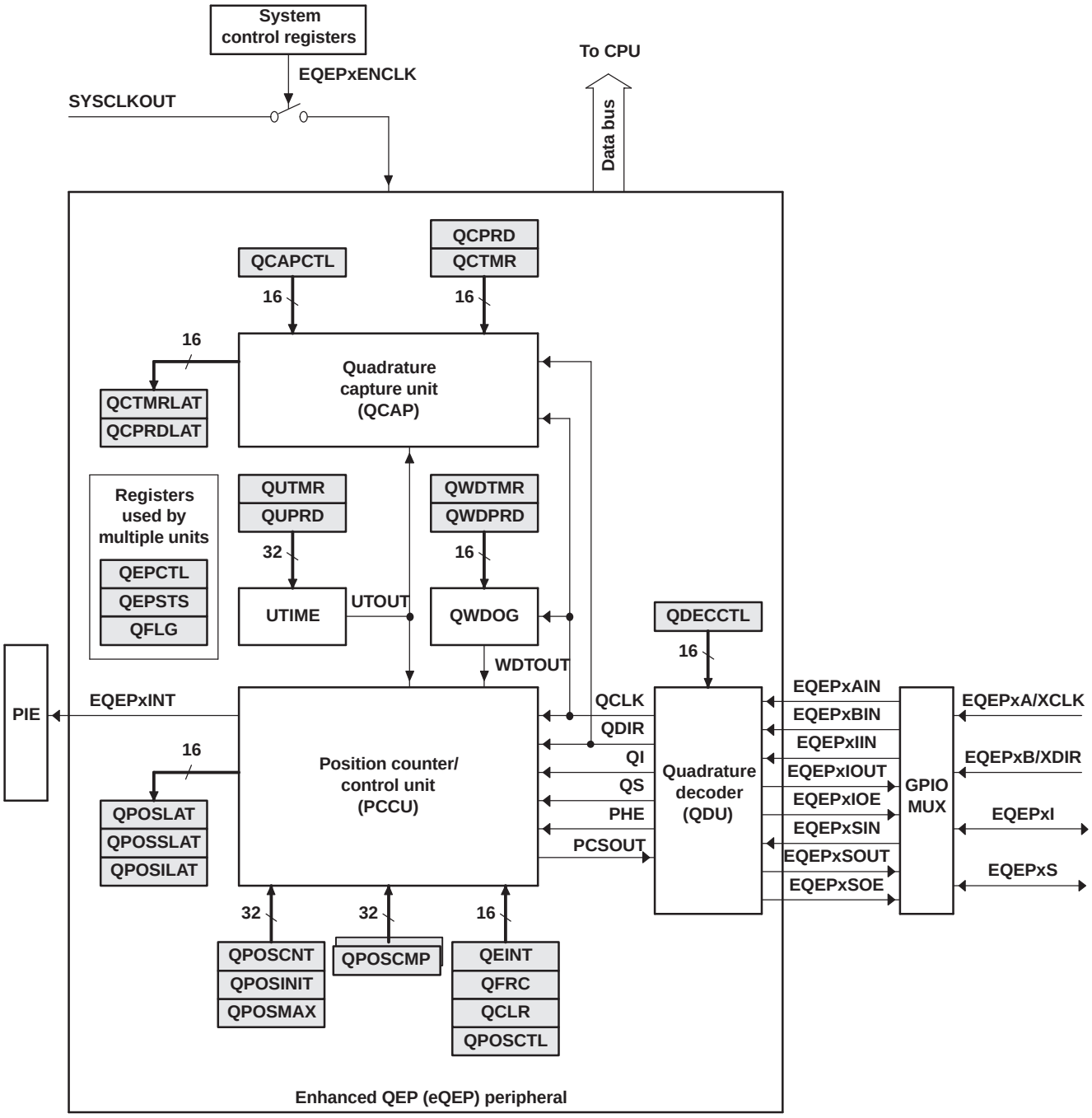


Figure 4-6. eQEP Functional Block Diagram

Table 4-4. eQEP Control and Status Registers

NAME	EQEP1 ADDRESS	EQEP2 ADDRESS	EQEP1 SIZE(x16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	0x6B40	2/0	eQEP Position Counter
QPOSINIT	0x6B02	0x6B42	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	0x6B44	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	0x6B46	2/1	eQEP Position-compare
QPOSILAT	0x6B08	0x6B48	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	0x6B4A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	0x6B4C	2/0	eQEP Position Latch
QUTMR	0x6B0E	0x6B4E	2/0	eQEP Unit Timer
QUPRD	0x6B10	0x6B50	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	0x6B52	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	0x6B53	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	0x6B54	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	0x6B55	1/0	eQEP Control Register
QCAPCTL	0x6B16	0x6B56	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	0x6B57	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	0x6B58	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	0x6B59	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	0x6B5A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	0x6B5B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	0x6B5C	1/0	eQEP Status Register
QCTMR	0x6B1D	0x6B5D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	0x6B5E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	0x6B5F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	0x6B60	1/0	eQEP Capture Period Latch
Reserved	0x6B21-0x6B3F	0x6B61-0x6B7F	31/0	

4.6 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 4-7. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0 V to 3 V (Voltages above 3 V produce full-scale conversion results.)
- Fast conversion rate: 160 ns at 12.5-MHz ADC clock, 6.25 MSPS
- 16-channel, MUXed inputs
- Autosequencing capability provides up to 16 "autoconversions" in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - \text{ADCLO}}{3}, \quad \text{when } 0\ \text{V} < \text{input} < 3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3\ \text{V}$$

A. All fractional values are truncated.

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W - software immediate start
  - ePWM start of conversion
  - XINT2 ADC start of conversion
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS.
- Sequencer can operate in "start/stop" mode, allowing multiple "time-sequenced triggers" to synchronize conversions.
- SOCA and SOCB triggers can operate independently in dual-sequencer mode.
- Sample-and-hold (S/H) acquisition time window has separate prescale control.

The ADC module in the 280x has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of 160 ns at 12.5-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 4-7 shows the block diagram of the ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

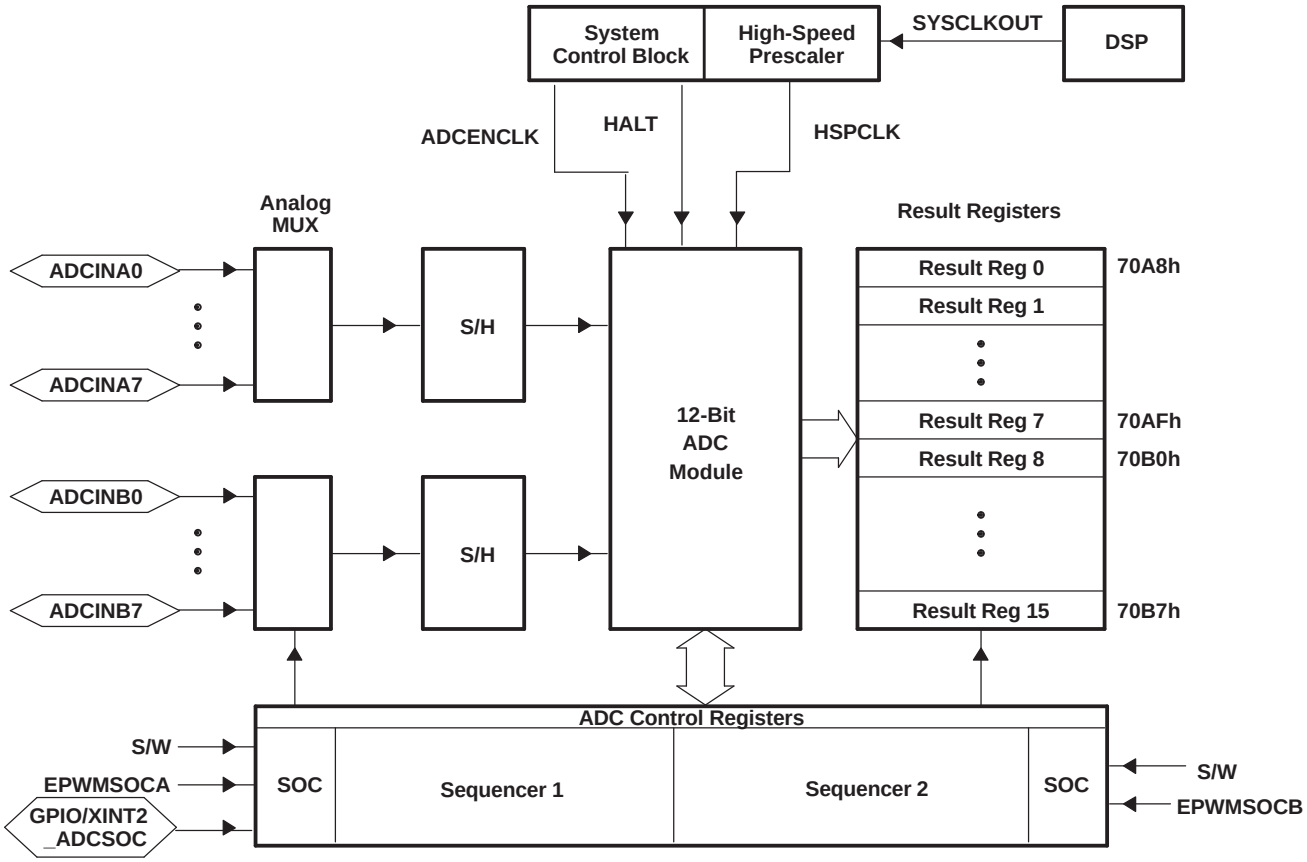


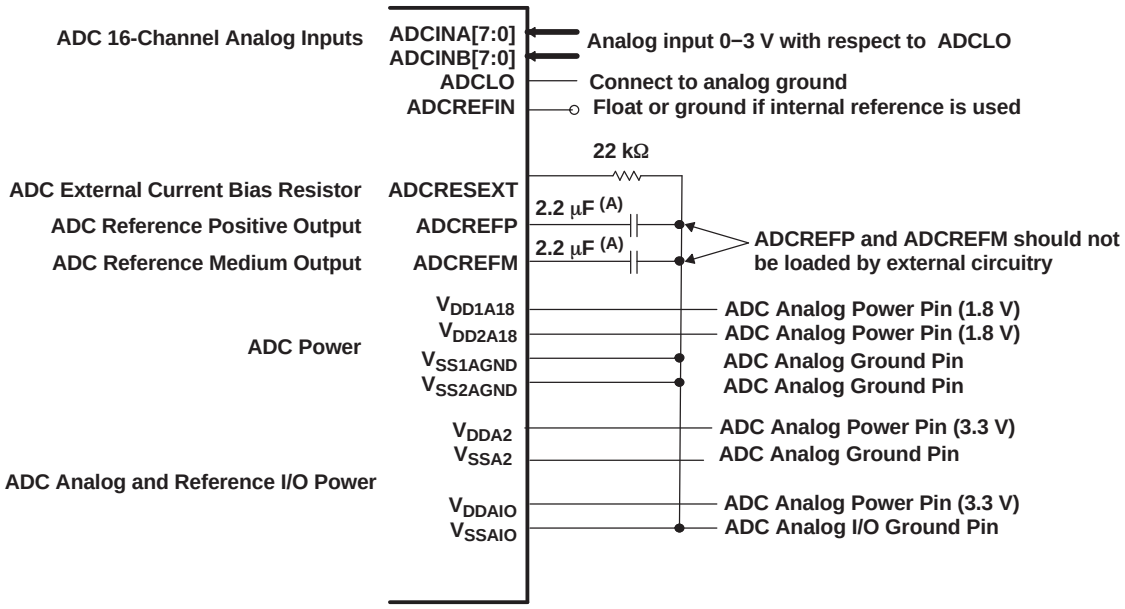
Figure 4-7. Block Diagram of the ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DD1A18}, V_{DD2A18} , V_{DDA2}, V_{DDAIO}) from the digital supply.Figure 4-8 shows the ADC pin connections for the 280x devices.

NOTE

1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).
2. The behavior of the ADC module based on the state of the ADCENCLK and HALT signals is as follows:
   - *ADCENCLK:* On reset, this signal will be low. While reset is active-low ($\overline{XRS}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module, however, will be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.
   - *HALT:* This mode only affects the analog module. It does not affect the registers. In this mode, the ADC module goes into low-power mode. This mode also will stop the clock to the CPU, which will stop the HSPCLK; therefore, the ADC register logic will be turned off indirectly.

Figure 4-8 shows the ADC pin-biasing for internal reference and Figure 4-9 shows the ADC pin-biasing for external reference.

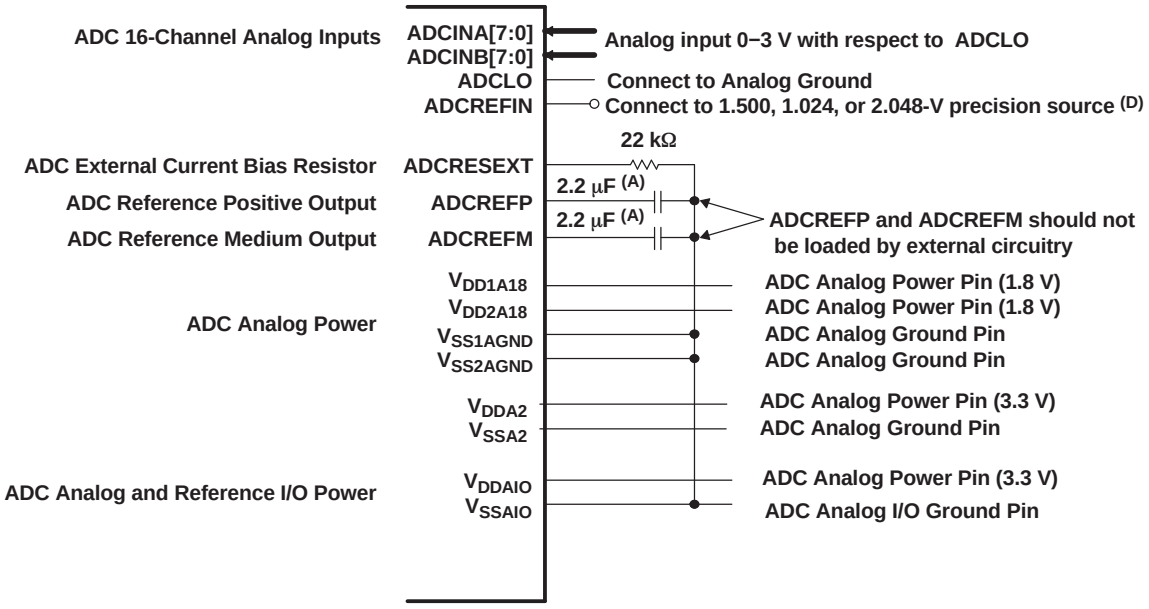


A. TAIYO YUDEN LMK212BJ225MG-T or equivalent

B. External decoupling capacitors are recommended on all power pins.

C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 4-8. ADC Pin Connections With Internal Reference



A. TAIYO YUDEN LMK212BJ225MG-T or equivalent

B. External decoupling capacitors are recommended on all power pins.

C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

D. External voltage on ADCREFIN is enabled by changing bits 15:14 in the ADC Reference Select register depending on the voltage used on this pin. Texas Instruments recommends Texas Instruments part REF3020 or equivalent for 2.048-V generation. Overall gain accuracy will be determined by accuracy of this voltage source.

Figure 4-9. ADC Pin Connections With External Reference

NOTE

The temperature rating of any recommended component must match the rating of the end product.

The ADC operation is configured, controlled, and monitored by the registers listed in Table 4-5.

Table 4-5. ADC Registers(1)

NAME	ADDRESS(1)	ADDRESS(2)	SIZE (x16)	DESCRIPTION
ADCTRL1	0x7100		1	ADC Control Register 1
ADCTRL2	0x7101		1	ADC Control Register 2
ADCMAXCONV	0x7102		1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x7103		1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x7104		1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x7105		1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x7106		1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x7107		1	ADC Auto-Sequence Status Register
ADCRESULT0	0x7108	0x0B00	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x7109	0x0B01	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x710A	0x0B02	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x710B	0x0B03	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x710C	0x0B04	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x710D	0x0B05	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x710E	0x0B06	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x710F	0x0B07	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x7110	0x0B08	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x7111	0x0B09	1	ADC Conversion Result Buffer Register 9
ADCRESULT10	0x7112	0x0B0A	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x7113	0x0B0B	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x7114	0x0B0C	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x7115	0x0B0D	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x7116	0x0B0E	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x7117	0x0B0F	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x7118		1	ADC Control Register 3
ADCST	0x7119		1	ADC Status Register
Reserved	0x711A 0x711B		2	
ADCREFSEL	0x711C		1	ADC Reference Select Register
ADCOFFTRIM	0x711D		1	ADC Offset Trim Register
Reserved	0x711E 0x711F		2	ADC Status Register

(1) The registers in this column are Peripheral Frame 2 Registers.
(2) The ADC result registers are dual mapped in the 280x DSP. Locations in Peripheral Frame 2 (0x7108-0x7117) are 2 wait states and left justified. Locations in Peripheral frame 0 space (0x0B00-0x0B0F) are 0 wait sates and right justified. During high speed/continuous conversion use of the ADC, use the 0 wait state locations for fast transfer of ADC results to user memory.

4.7 Enhanced Controller Area Network (eCAN) Modules (eCAN-A and eCAN-B)

The CAN module has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a SYSCLKOUT of 100 MHz, the smallest bit rate possible is 15.6 kbps.

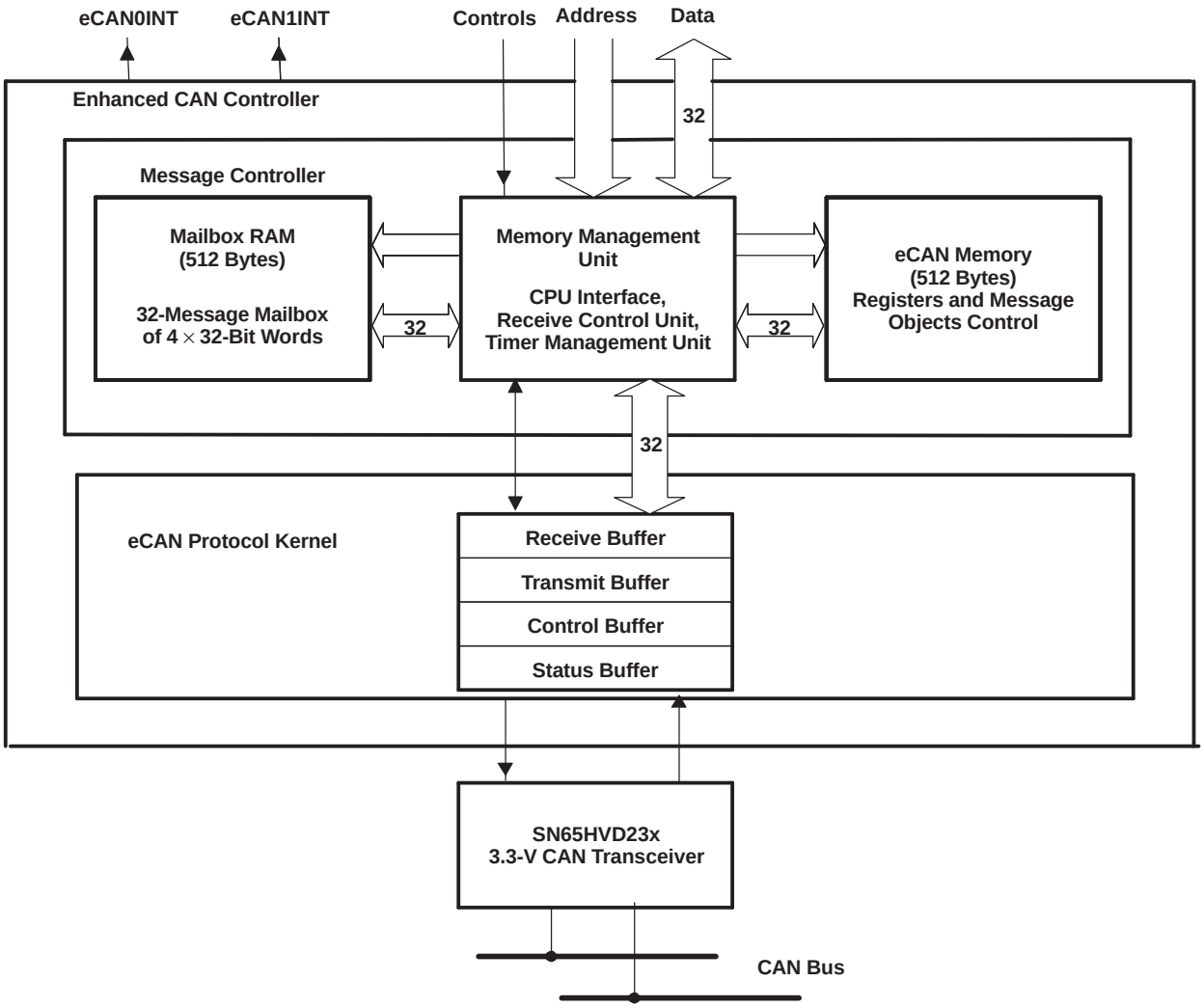


Figure 4-10. eCAN Block Diagram and Interface Circuit

Table 4-6. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	-40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	-40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	-40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	-40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	-40°C to 125°C
SN65HVD234	3.3 V	Standby & Sleep	Adjustable	None	–	-40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	-40°C to 125°C

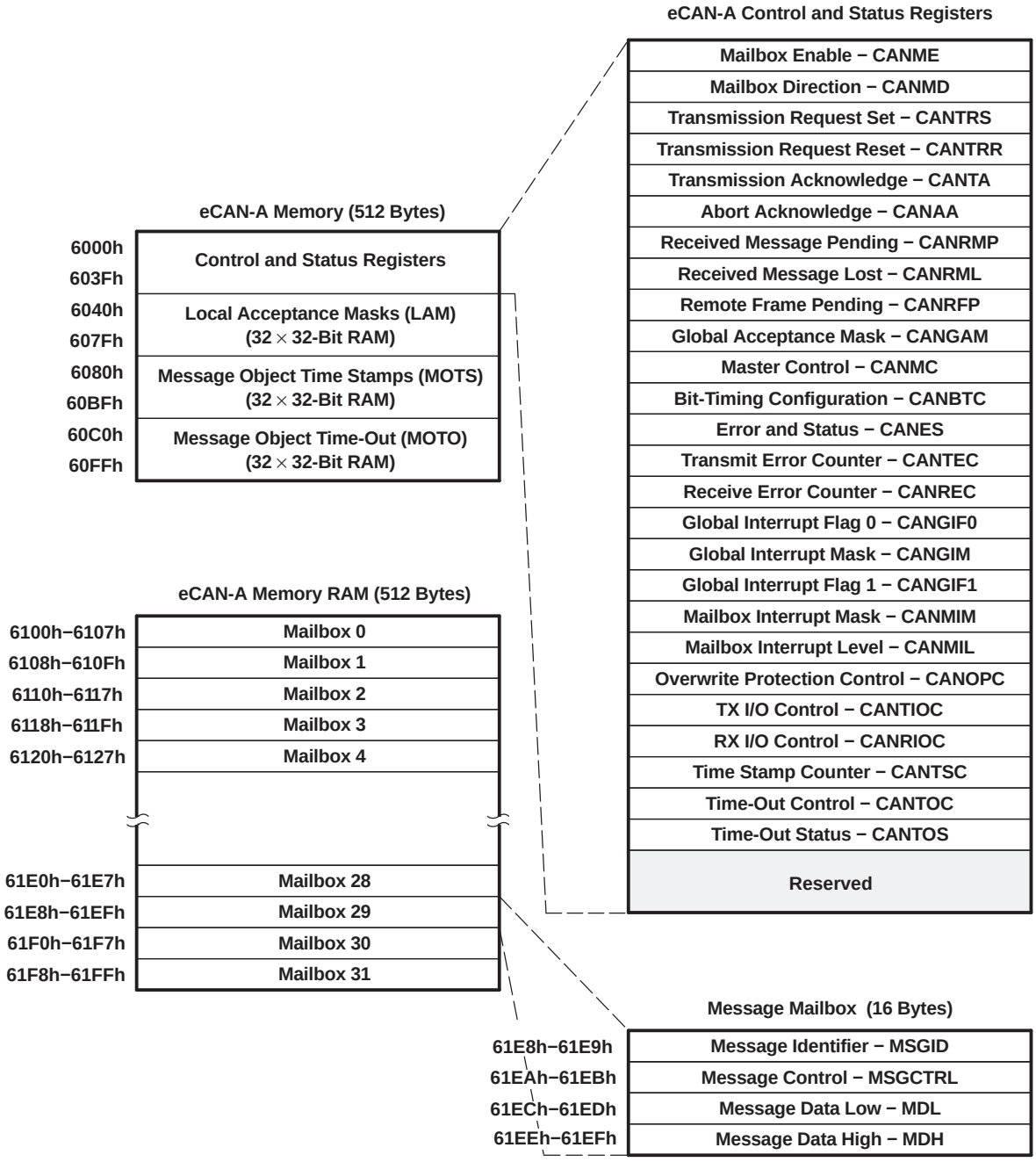


Figure 4-11. eCAN-A Memory Map

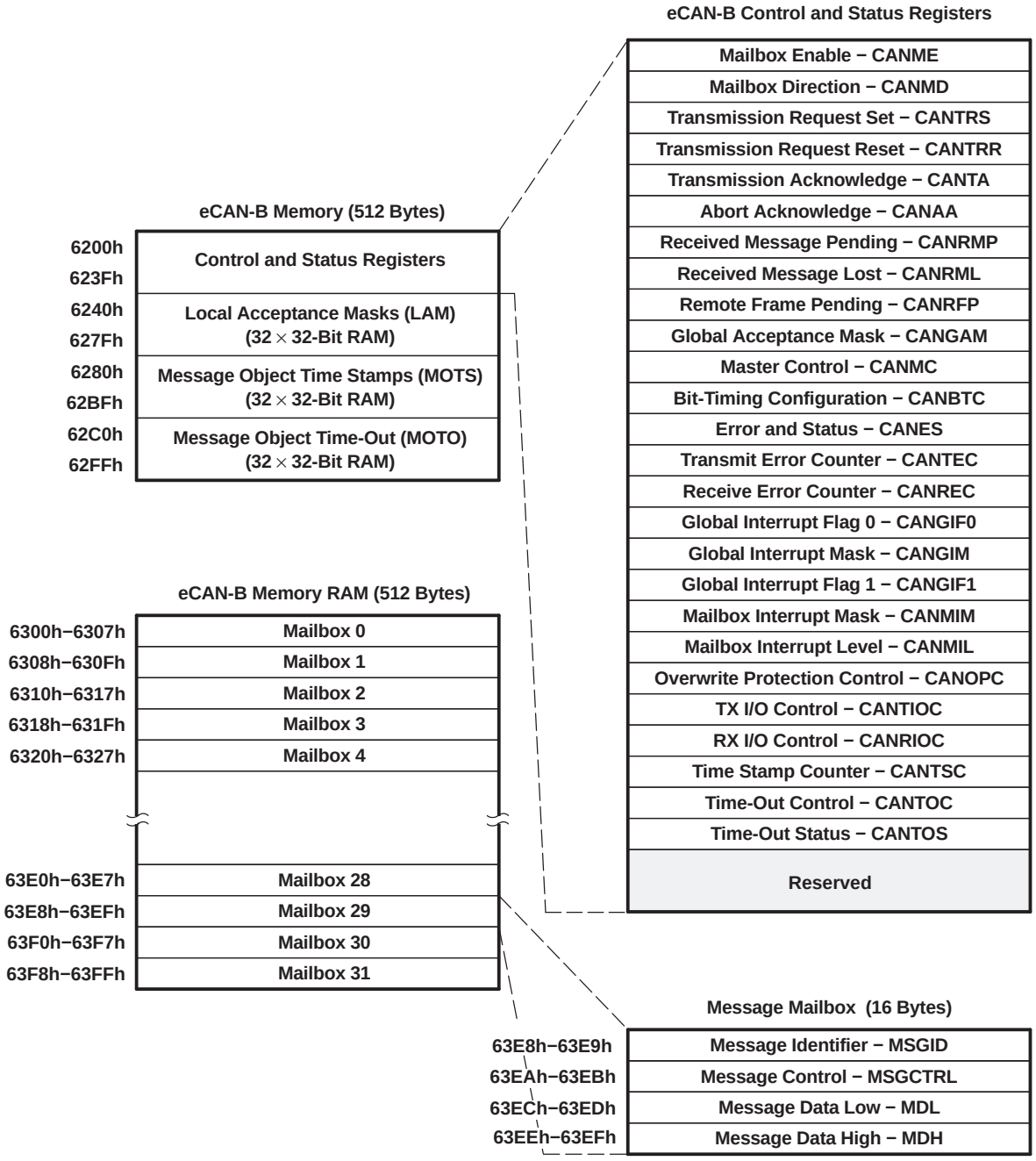


Figure 4-12. eCAN-B Memory Map

The CAN registers listed in Table 4-7 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 4-7. CAN Register Map(1)

REGISTER NAME	ECAN-A ADDRESS	ECAN-B ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	0x6200	1	Mailbox enable
CANMD	0x6002	0x6202	1	Mailbox direction
CANTRS	0x6004	0x6204	1	Transmit request set
CANTRR	0x6006	0x6206	1	Transmit request reset
CANTA	0x6008	0x6208	1	Transmission acknowledge
CANAA	0x600A	0x620A	1	Abort acknowledge
CANRMP	0x600C	0x620C	1	Receive message pending
CANRML	0x600E	0x620E	1	Receive message lost
CANRFP	0x6010	0x6210	1	Remote frame pending
CANGAM	0x6012	0x6212	1	Global acceptance mask
CANMC	0x6014	0x6214	1	Master control
CANBTC	0x6016	0x6216	1	Bit-timing configuration
CANES	0x6018	0x6218	1	Error and status
CANTEC	0x601A	0x621A	1	Transmit error counter
CANREC	0x601C	0x621C	1	Receive error counter
CANGIF0	0x601E	0x621E	1	Global interrupt flag 0
CANGIM	0x6020	0x6220	1	Global interrupt mask
CANGIF1	0x6022	0x6222	1	Global interrupt flag 1
CANMIM	0x6024	0x6224	1	Mailbox interrupt mask
CANMIL	0x6026	0x6226	1	Mailbox interrupt level
CANOPC	0x6028	0x6228	1	Overwrite protection control
CANTIOC	0x602A	0x622A	1	TX I/O control
CANRIOC	0x602C	0x622C	1	RX I/O control
CANTSC	0x602E	0x622E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	0x6230	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	0x6232	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

4.8 Serial Communications Interface (SCI) Modules (SCI-A, SCI-B)

The 280x devices include two serial communications interface (SCI) modules. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- $\text{Max bit rate} = \frac{100\ \text{MHz}}{16} = 6.25 \times 10^6\ \text{b/s}$
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 16-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4-8 and Table 4-9.

Table 4-8. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x7050	1	SCI-A Communications Control Register
SCICTL1A	0x7051	1	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	SCI-A Control Register 2
SCIRXSTA	0x7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Table 4-9. SCI-B Registers(1)(2)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRB	0x7750	1	SCI-B Communications Control Register
SCICTL1B	0x7751	1	SCI-B Control Register 1
SCIHBAUDB	0x7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x7754	1	SCI-B Control Register 2
SCIRXSTB	0x7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUFB	0x7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB(2)	0x775A	1	SCI-B FIFO Transmit Register
SCIFFRXB(2)	0x775B	1	SCI-B FIFO Receive Register
SCIFFCTB(2)	0x775C	1	SCI-B FIFO Control Register
SCIPRIB	0x775F	1	SCI-B Priority Control Register

(1) Registers in this table are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Figure 4-13 shows the SCI module block diagram.

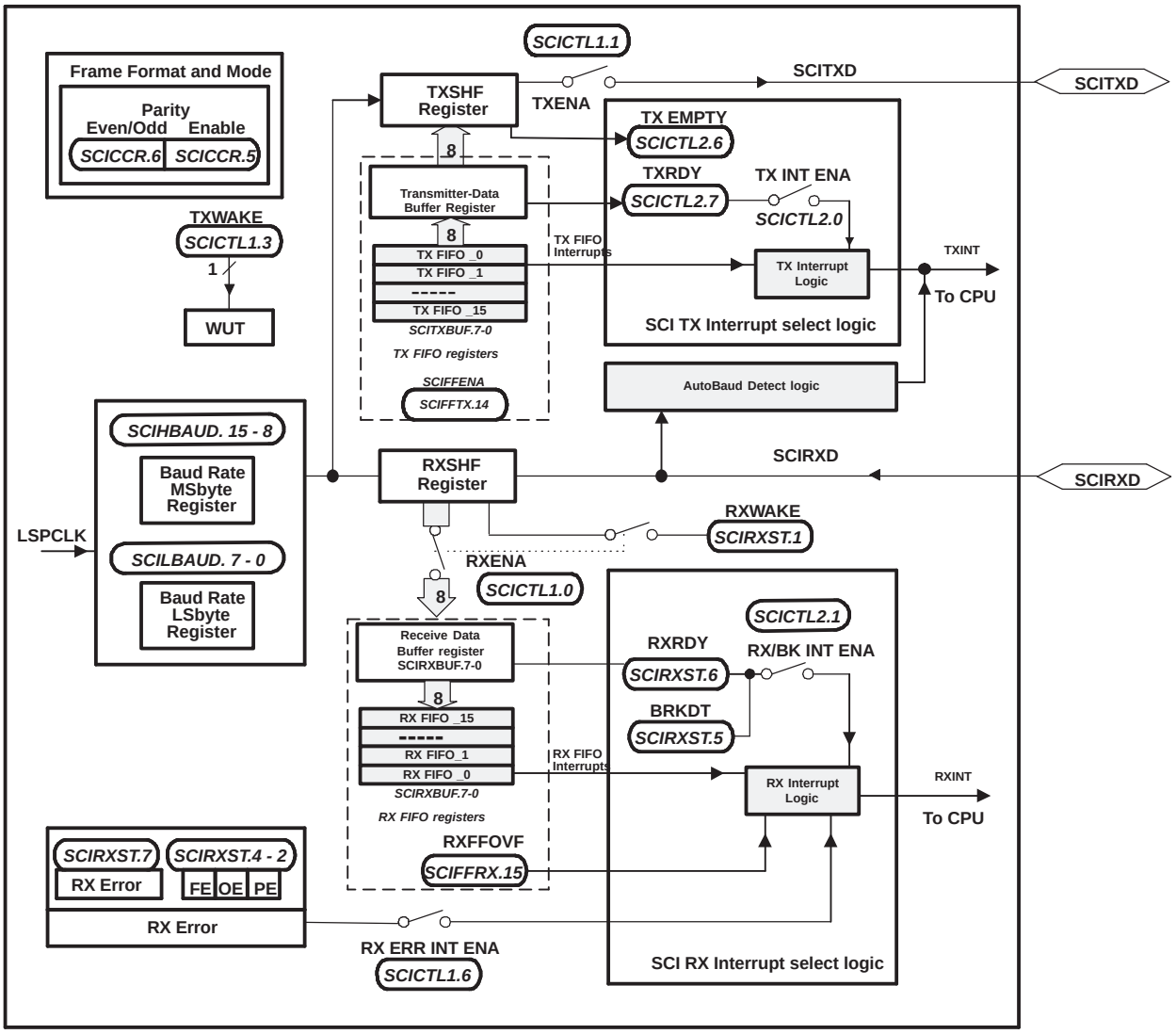


Figure 4-13. Serial Communications Interface (SCI) Module Block Diagram

4.9 Serial Peripheral Interface (SPI) Modules (SPI-A, SPI-B, SPI-C, SPI-D)

The 280x devices include the four-pin serial peripheral interface (SPI) module. Up to four SPI modules (SPI-A, SPI-B, SPI-C, and SPI-D) are available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave
  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR = 3 to 127}$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR = 0,1, 2}$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 16-level transmit/receive FIFO
- Delayed transmit control

The SPI port operation is configured and controlled by the registers listed in Table 4-10.

Table 4-10. SPI-A Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
SPICCR	0x7040	1	SPI-A Configuration Control Register
SPICTL	0x7041	1	SPI-A Operation Control Register
SPISTS	0x7042	1	SPI-A Status Register
SPIBRR	0x7044	1	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	SPI-A Serial Data Register
SPIFFTX	0x704A	1	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	SPI-A FIFO Control Register
SPIPRI	0x704F	1	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4-11. SPI-B Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
SPICCR	0x7740	1	SPI-B Configuration Control Register
SPICTL	0x7741	1	SPI-B Operation Control Register
SPISTS	0x7742	1	SPI-B Status Register
SPIBRR	0x7744	1	SPI-B Baud Rate Register
SPIRXEMU	0x7746	1	SPI-B Receive Emulation Buffer Register
SPIRXBUF	0x7747	1	SPI-B Serial Input Buffer Register
SPITXBUF	0x7748	1	SPI-B Serial Output Buffer Register
SPIDAT	0x7749	1	SPI-B Serial Data Register
SPIFFTX	0x774A	1	SPI-B FIFO Transmit Register
SPIFFRX	0x774B	1	SPI-B FIFO Receive Register
SPIFFCT	0x774C	1	SPI-B FIFO Control Register
SPIPRI	0x774F	1	SPI-B Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4-12. SPI-C Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
SPICCR	0x7760	1	SPI-C Configuration Control Register
SPICTL	0x7761	1	SPI-C Operation Control Register
SPISTS	0x7762	1	SPI-C Status Register
SPIBRR	0x7764	1	SPI-C Baud Rate Register
SPIRXEMU	0x7766	1	SPI-C Receive Emulation Buffer Register
SPIRXBUF	0x7767	1	SPI-C Serial Input Buffer Register
SPITXBUF	0x7768	1	SPI-C Serial Output Buffer Register
SPIDAT	0x7769	1	SPI-C Serial Data Register
SPIFFTX	0x776A	1	SPI-C FIFO Transmit Register
SPIFFRX	0x776B	1	SPI-C FIFO Receive Register
SPIFFCT	0x776C	1	SPI-C FIFO Control Register
SPIPRI	0x776F	1	SPI-C Priority Control Register

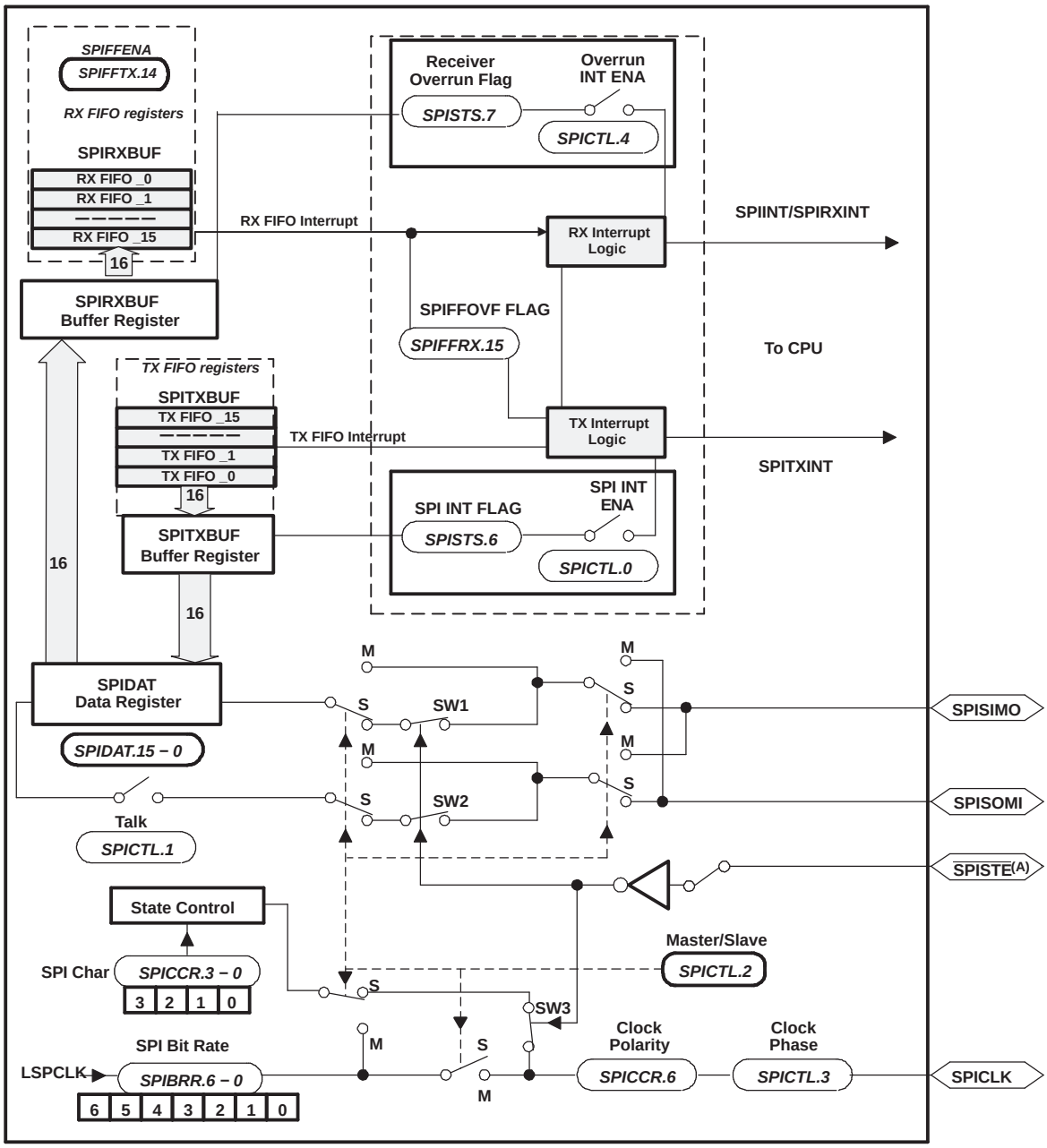
(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4-13. SPI-D Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
SPICCR	0x7780	1	SPI-D Configuration Control Register
SPICTL	0x7781	1	SPI-D Operation Control Register
SPISTS	0x7782	1	SPI-D Status Register
SPIBRR	0x7784	1	SPI-D Baud Rate Register
SPIRXEMU	0x7786	1	SPI-D Receive Emulation Buffer Register
SPIRXBUF	0x7787	1	SPI-D Serial Input Buffer Register
SPITXBUF	0x7788	1	SPI-D Serial Output Buffer Register
SPIDAT	0x7789	1	SPI-D Serial Data Register
SPIFFTX	0x778A	1	SPI-D FIFO Transmit Register
SPIFFRX	0x778B	1	SPI-D FIFO Receive Register
SPIFFCT	0x778C	1	SPI-D FIFO Control Register
SPIPRI	0x778F	1	SPI-D Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4-14 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

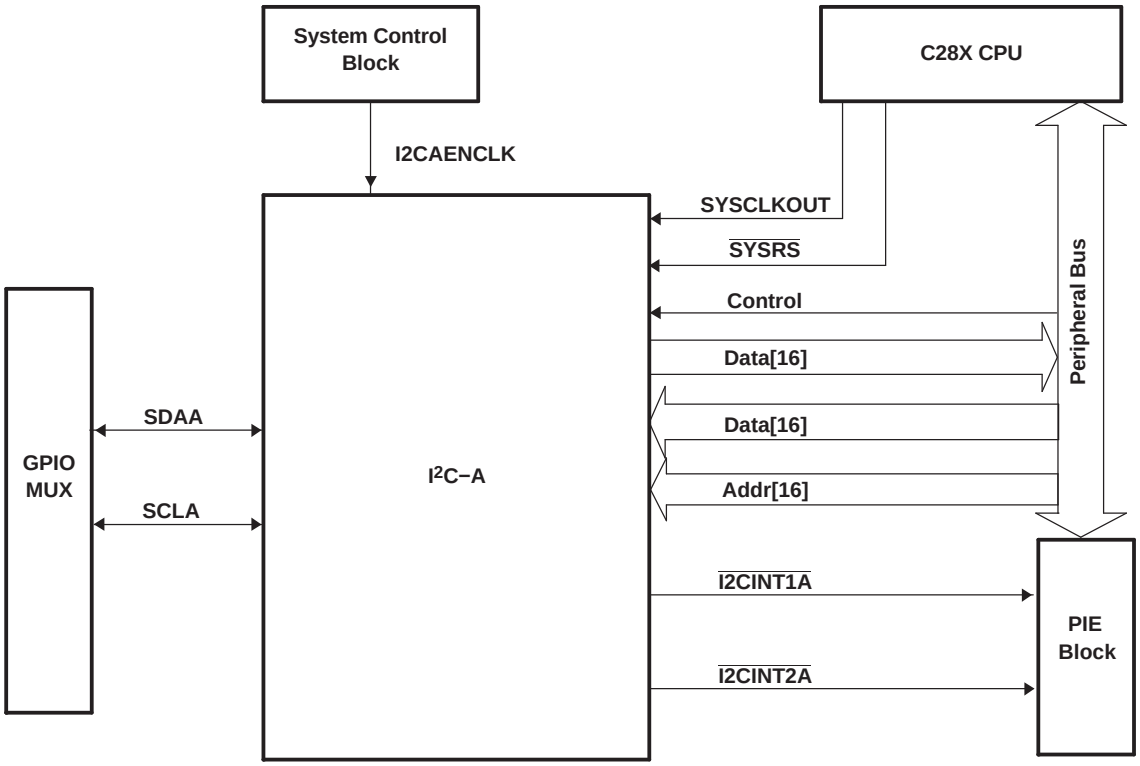
Figure 4-14. SPI Module Block Diagram (Slave Mode)

4.10 Inter-Integrated Circuit (I^2C)

The 280x device contains one I^2C Serial Port. Figure 4-15 shows how the I^2C peripheral module interfaces within the 280x device.

The I^2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)
- One 16-bit receive FIFO and one 16-bit transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



A. The I²C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I²C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I²C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 4-15. I²C Peripheral Module Interfaces

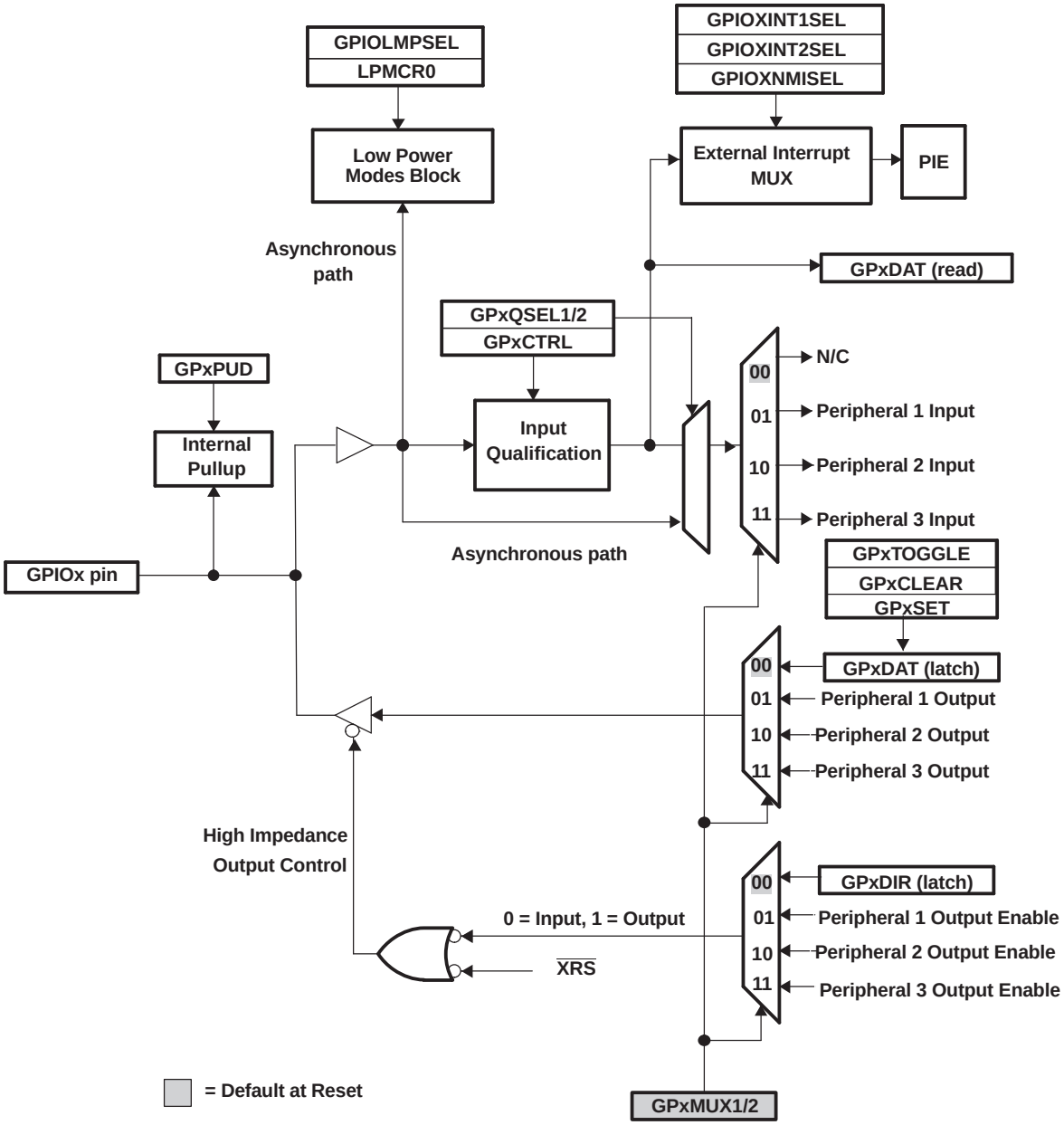
The registers in Table 4-14 configure and control the I²C port operation.

Table 4-14. I²C-A Registers

NAME	ADDRESS	DESCRIPTION
I2COAR	0x7900	I²C own address register
I2CIER	0x7901	I²C interrupt enable register
I2CSTR	0x7902	I²C status register
I2CCLKL	0x7903	I²C clock low-time divider register
I2CCLKH	0x7904	I²C clock high-time divider register
I2CCNT	0x7905	I²C data count register
I2CDRR	0x7906	I²C data receive register
I2CSAR	0x7907	I²C slave address register
I2CDXR	0x7908	I²C data transmit register
I2CMDR	0x7909	I²C mode register
I2CISRC	0x790A	I²C interrupt source register
I2CPSC	0x790C	I²C prescaler register
I2CFFTX	0x7920	I²C FIFO transmit register
I2CFFRX	0x7921	I²C FIFO receive register
I2CRSR	-	I²C receive shift register (not accessible to the CPU)
I2CXSR	-	I²C transmit shift register (not accessible to the CPU)

4.11 GPIO MUX

On the 280x, the GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging IO capability. The GPIO MUX block diagram per pin is shown in Figure 4-16. Because of the open drain capabilities of the I^2C pins, the GPIO MUX block diagram for these pins differ. See the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712) for details.



A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

Figure 4-16. GPIO MUX Block Diagram

The 280x supports 34 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 4-15 shows the GPIO register mapping.

Table 4-15. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
reserved	0x6F8E 0x6F8F	2	
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 35)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 35)
GPBQSEL2	0x6F94	2	reserved
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 35)
GPBMUX2	0x6F98	2	reserved
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 35)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 35)
reserved	0x6F9E 0x6F9F	2	reserved
reserved	0x6FA0 0x6FBF	32	
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO Data Register (GPIO32 to 35)
GPBSET	0x6FCA	2	GPIO Data Set Register (GPIO32 to 35)
GPBCLEAR	0x6FCC	2	GPIO Data Clear Register (GPIO32 to 35)
GPBTOGGLE	0x6FCE	2	GPIO Data Toggle Register (GPIO32 to 35)
reserved	0x6FD0 0x6FDF	16	
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
reserved	0x6FE3 0x6FE7	5	
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)
reserved	0x6FEA 0x6FFF	22	

Table 4-16. F2808 GPIO MUX Table

GPAMUX1/2[1] REGISTER BITS	DEFAULT AT RESET PRIMARY I/O FUNCTION (GPxMUX1/2 BITS = 0,0)	PERIPHERAL SELECTION 1[2] (GPxMUX1/2 BITS = 0,1)	PERIPHERAL SELECTION 2 (GPxMUX1/2 BITS = 1,0)	PERIPHERAL SELECTION 3 (GPxMUX1/2 BITS = 1,1)
GPAMUX1				
1-0	GPIO0	EPWM1A (O)	Reserved[3]	Reserved[3]
3-2	GPIO1	EPWM1B (O)	SPISIMOD (I/O)	Reserved[3]
5-4	GPIO2	EPWM2A (O)	Reserved[3]	Reserved[3]
7-6	GPIO3	EPWM2B (O)	SPISOMID (I/O)	Reserved[3]
9-8	GPIO4	EPWM3A (O)	Reserved[3]	Reserved[3]
11-10	GPIO5	EPWM3B (O)	SPICLKD (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SPISTED (I/O)	ECAP2 (I/O)
17-16	GPIO8	EPWM5A (O)	CANTXB (O)	$\overline{\text{ADCSOCAO}}$ (O)
19-18	GPIO9	EPWM5B (O)	SCITXDB (O)	ECAP3 (I/O)
21-20	GPIO10	EPWM6A (O)	CANRXB (I)	$\overline{\text{ADCSOCBO}}$ (O)
23-22	GPIO11	EPWM6B (O)	SCIRXDB (I)	ECAP4 (I/O)
25-24	GPIO12	$\overline{\text{TZ1}}$ (I)	CANTXB (O)	SPISIMOB (I/O)
27-26	GPIO13	$\overline{\text{TZ2}}$ (I)	CANRXB (I)	SPISOMIB (I/O)
29-28	GPIO14	$\overline{\text{TZ3}}$ (I)	SCITXDB (O)	SPICLKB (I/O)
31-30	GPIO15	$\overline{\text{TZ4}}$ (I)	SCIRXDB (I)	SPISTEB (I/O)
GPAMUX2				
1-0	GPIO16	SPISIMOA (I/O)	CANTXB (O)	$\overline{\text{TZ5}}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	CANRXB (I)	$\overline{\text{TZ6}}$ (I)
5-4	GPIO18	SPICLKA (I/O)	SCITXDB (O)	Reserved[3]
7-6	GPIO19	SPISTEA (I/O)	SCIRXDB (I)	Reserved[3]
9-8	GPIO20	EQEP1A (I)	SPISIMOC (I/O)	CANTXB (O)
11-10	GPIO21	EQEP1B (I)	SPISOMIC (I/O)	CANRXB (I)
13-12	GPIO22	EQEP1S (I/O)	SPICLKC (I/O)	SCITXDB (O)
15-14	GPIO23	EQEP1I (I/O)	SPISTEC (I/O)	SCIRXDB (I)
17-16	GPIO24	ECAP1 (I/O)	EQEP2A (I)	SPISIMOB (I/O)
19-18	GPIO25	ECAP2 (I/O)	EQEP2B (I)	SPISOMIB (I/O)
21-20	GPIO26	ECAP3 (I/O)	EQEP2I (I/O)	SPICLKB (I/O)
23-22	GPIO27	ECAP4 (I/O)	EQEP2S (I/O)	SPISTEB (I/O)
25-24	GPIO28	SCIRXDA (I)	Reserved[3]	$\overline{\text{TZ5}}$ (I)
27-26	GPIO29	SCITXDA (O)	Reserved[3]	$\overline{\text{TZ6}}$ (I)
29-28	GPIO30	CANRXA (I)	Reserved[3]	Reserved[3]
31-30	GPIO31	CANTXA (O)	Reserved[3]	Reserved[3]
GPBMUX1				
1-0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3-2	GPIO33	SCLA (I/OC)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5-4	GPIO34	Reserved[3]	Reserved[3]	Reserved[3]

(1) GPxMUX1/2 refers to the appropriate MUX register for the pin; GPAMUX1, GPAMUX2 or GPBMUX1.
(2) This table pertains to the 2808 device. Some peripherals may not be available in the 2806 or 2801 devices. See the pin descriptions for more detail.
(3) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2=0,0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2=0,1 and 1,0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.

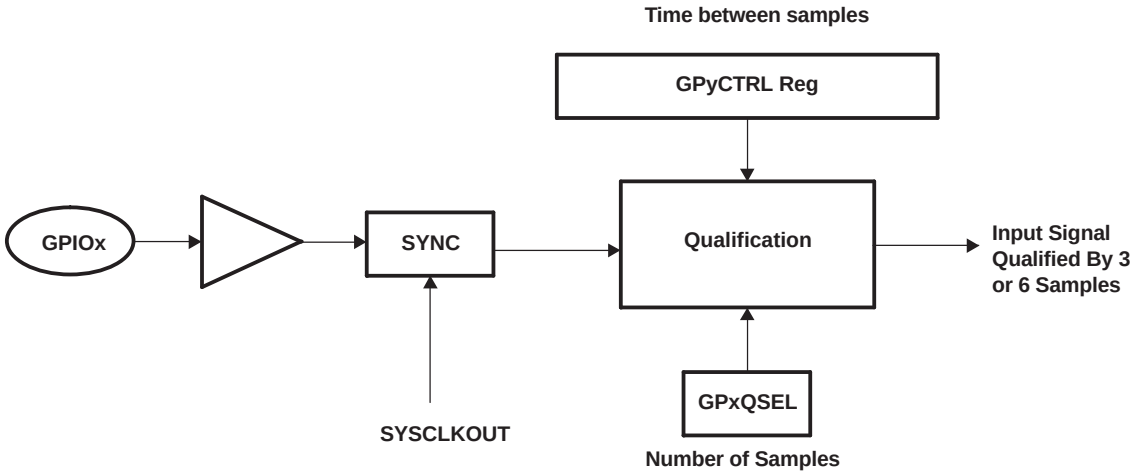


Figure 4-17. Qualification Using Sampling Window

- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2=1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the 280x device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

5 Device Support

Texas Instruments (Texas Instruments) offers an extensive line of development tools for the C28x™ generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 280x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- 2808 eZdsp™
- JTAG-based emulators - SPI515, XDS510PP, XDS510PP Plus, XDS510USB™
- Universal 5-V dc power supply
- Documentation and cables

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully and the quality and reliability of the device have been demonstrated fully. Texas Instruments standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Texas Instruments device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PBK) and temperature range (for example, A). Figure 5-1 provides a legend for reading the complete device name for any family member.

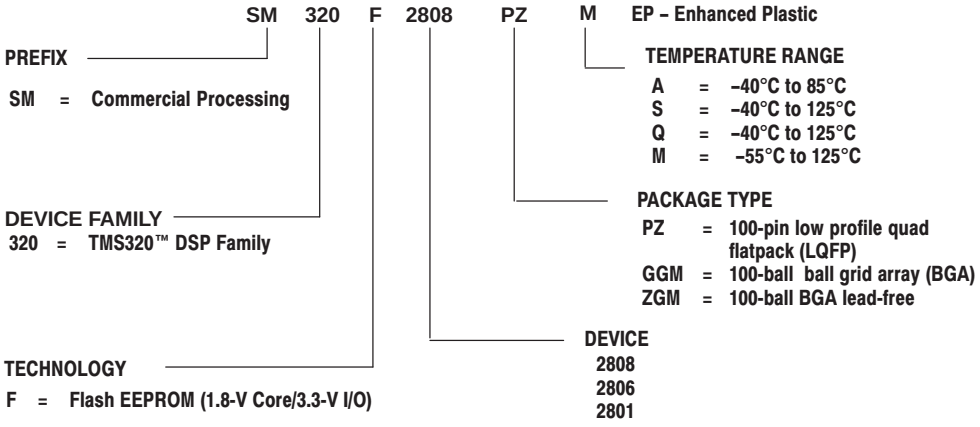


Figure 5-1. Example of SM320x280x Device Nomenclature

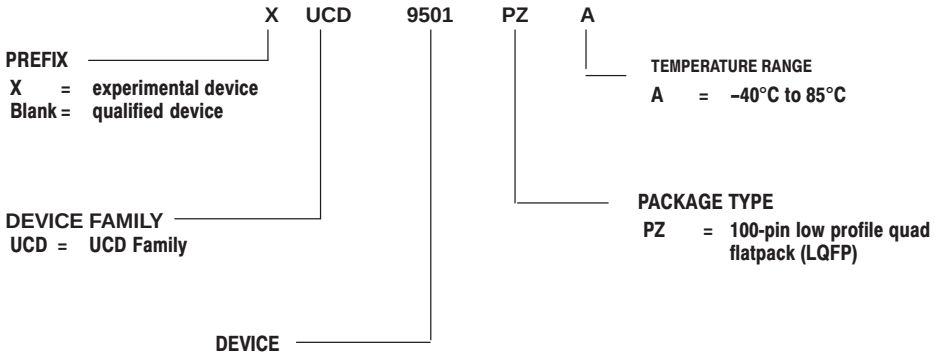


Figure 5-2. Example of UCD Device Nomenclature

5.2 Documentation Support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications. TMS320x280x device reference guides are applicable to the UCD9501 device as well. Useful reference documentation includes:

SPRU051: TMS320x281x, 280x Serial Communication Interface (SCI) Reference Guide

Describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

SPRU059: TMS320x281x, 280x Serial Peripheral Interface (SPI) Reference Guide

Describes the SPI - a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the

device at a programmed bit-transfer rate. The SPI is used for communications between the DSP controller and external peripherals or another controller.

SPRU074: TMS320x281x, 280x Enhanced Controller Area Network (eCAN) Reference Guide

Describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments. With 32 fully configurable mailboxes and time-stamping feature, the eCAN module provides a versatile and robust serial communication interface. The eCAN module implemented in the 281x DSP is compatible with the CAN 2.0B standard (active).

SPRU430: TMS320C28x DSP CPU and Instruction Set Reference Guide

Describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

SPRU513: TMS320C28x Assembly Language Tools User's Guide

Describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514: TMS320C28x Optimizing C Compiler User's Guide

describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU566: TMS320x281x, 280x Peripheral Reference Guide

Describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRU608: The TMS320C28x Instruction Set Simulator Technical Overview

Describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

SPRU625: TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide

Describes development using DSP/BIOS.

SPRU712: TMS320x280x System Control and Interrupts Reference Guide

Describes the various interrupts and system control features of the 280x digital signal processors (DSPs).

SPRU716: TMS320x280x Analog-to-Digital Converter (ADC) Reference Guide

Describes the ADC module. The module is a 12-bit pipelined ADC. The analog circuits of this converter, referred to as the core in this document, include the front-end analog multiplexers (MUXs), sample-and-hold (S/H) circuits, the conversion core, voltage regulators, and other analog supporting circuits. Digital circuits, referred to as the wrapper in this document, include programmable conversion sequencer, result registers, interface to analog circuits, interface to device peripheral bus, and interface to other on-chip modules.

SPRU722: TMS320x280x Boot ROM Reference Guide

Describes the purpose and features of the bootloader (factory-programmed boot-loading software). It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRU790: TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide

Describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

SPRU791: TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide

The PWM peripheral is an essential part of controlling many of the power related systems found in both commercial and industrial equipments. This guide describes the main areas that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion. The PWM peripheral can be considered as performing a DAC function, where the duty cycle is equivalent to a DAC analog value, it is sometimes referred to as a Power DAC.

SPRU807: TMS320x280x Enhanced Capture (eCAP) Module Reference Guide

Describes the enhanced capture module. It includes the module description and registers.

SPRU924: High-Resolution Pulse Width Modulator (HRPWM) describes the operation of the high-resolution extension to the pulse width modulator (HRPWM)

SPRA550: 3.3 V DSP for Digital Motor Control describes a scenario of a 3.3-V-only motor controller indicating that for most applications, no significant issue of interfacing between 3.3 V and 5 V exists. On-chip 3.3-V analog-to-digital converter (ADC) versus 5-V ADC is also discussed. Guidelines for component layout and printed circuit board (PCB) design that can reduce system noise and EMI effects are summarized.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Updated information on the TMS320 DSP controllers can be found on the worldwide web at: **http://www.ti.com**.

To send comments regarding this data manual (literature number SPRS230), use the *comments@books.sc.ti.com* email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the **http://www.ti.com/sc/docs/pic/home.htm** site.

6 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320F280x DSPs.

6.1 Absolute Maximum Ratings(1)(2)

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges.

Supply voltage range, V_{DDIO}, V_{DD3VFL}	with respect to V_{SS}	-0.3 V to 4.6 V
Supply voltage range, V_{DDA2}, V_{DDAIO}	with respect to V_{SSA}	-0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	-0.3 V to 2.5 V
Supply voltage range, V_{DD1A18}, V_{DD2A18}	with respect to V_{SSA}	-0.3 V to 2.5 V
Supply voltage range, V_{SSA2}, V_{SSAIO}, $V_{SS1AGND}$, $V_{SS2AGND}$	with respect to V_{SS}	-0.3 V to 0.3 V
Input voltage range, V_{IN}		-0.3 V to 4.6 V
Output voltage range, V_O		-0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(3)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		±20 mA
Operating ambient temperature ranges, T_A(4)		-55°C to 125°C
Junction temperature range, T_j(4)		-55°C to 150°C
Storage temperature range, T_{stg}(4)		- 65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA. This includes the analog inputs which have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA2} or below V_{SSA2}.
(4) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24x and TMS320F281x Devices Application Report* (literature number SPRA963)

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		3.14	3.3	3.47	V
Device supply voltage CPU, V_{DD}		1.71	1.8	1.89	V
Supply ground, V_{SS}, V_{SSIO}			0		V
ADC supply voltage (3.3 V), V_{DDA2}, V_{DDAIO}		3.14	3.3	3.47	V
ADC supply voltage (1.8 V), V_{DD1A18}, V_{DD2A18}		1.71	1.8	1.89	V
Flash supply voltage, V_{DD3VFL}		3.14	3.3	3.47	V
Device clock frequency (system clock), $f_{SYSCLKOUT}$		2		100	MHz
High-level input voltage, V_{IH}		2		V_{DDIO}	V
Low-level input voltage, V_{IL}				0.8	
High-level output source current, V_{OH} = 2.4 V, I_{OH}	All I/Os except Group 2			-4	mA
	Group 2(1)			-8	
Low-level output sink current, V_{OL} = V_{OL} MAX, I_{OL}	All I/Os except Group 2			4	mA
	Group 2(1)			8	
Ambient temperature, T_A		-55		125	°C

(1) Group 2 pins are as follows: GPIO28, GPIO29, GPIO30, GPIO31, TDO, XCLKOUT, EMU0, and EMU1

6.3 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}MAX$		2.4			V
			I_{OH} = 50 µA		V_{DDIO} - 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}MAX$				0.4	V
I_{IL}	Input current (low level)	With pullup	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)	-80	-140	-190	µA
		Pullup disabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	With pullup	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$				±2	µA
		Pullup disabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$		38	50	80	
I_{OZ}	Output current, high-impedance state (off-state)		$V_O = V_{DDIO}$ or 0 V				±2	µA
C_I	Input capacitance					2		pF

6.4 Current Consumption

Table 6-1. SM320F2808 Current Consumption by Power-Supply Pins at 100-MHz SYSCLKOUT

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO}(1)		I_{DD3VFL}		I_{DDA18}(2)		I_{DDA33}(3)	
		TYP(4)	MAX	TYP(4)	MAX	TYP	MAX	TYP(4)	MAX	TYP(4)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4/5/6 • eCAP1/2/3/4 • eQEP1/2 • eCAN-A • SCI-A/B • SPI-A • ADC • I^2C All PWM pins are toggled at 100 kHz. Data is continuously transmitted out of the SCI-A, SCI-B, and eCAN-A ports. The hardware multiplier is exercised. Code is running out of flash with 3 wait states. XCLKOUT is turned off.	195 mA	230 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	Flash is powered down. XCLKOUT is turned off. The following peripheral clocks are enabled: • eCAN-A • SCI-A • SPI-A • I^2C	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) I_{DDA18} includes current into V_{DD1A18} and V_{DD2A18} pins.
(3) I_{DDA33} includes current into V_{DDA2} and V_{DDAIO} pins.
(4) The TYP numbers are applicable over room temperature and nominal voltage.

CAUTION

The peripheral - I/O multiplexing implemented in the 280x devices prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

Table 6-2. F2806 Current Consumption by Power-supply Pins at 100 MHz SYSCLKOUT

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DD3VFL}		I_{DDA18} (2)		I_{DDA33} (3)	
		TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4/5/6 • eCAP1/2/3/4 • eQEP1/2 • eCAN-A • SCI-A/B • SPI-A • ADC • I^2C All PWM pins are toggled at 100 kHz. Data is continuously transmitted out of the SCI-A, SCI-B, and eCAN-A ports. The hardware multiplier is exercised. Code is running out of flash with 3 wait states. XCLKOUT is turned off	195 mA	230 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	Flash is powered down. XCLKOUT is turned off. The following peripheral clocks are enabled: • eCAN-A • SCI-A • SPI-A • I^2C	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) I_{DDA18} includes current into V_{DD1A18} and V_{DD2A18} pins.
(3) I_{DDA33} includes current into V_{DDA2} and V_{DDAIO} pins.
(4) The TYP numbers are applicable over room temperature and nominal voltage.

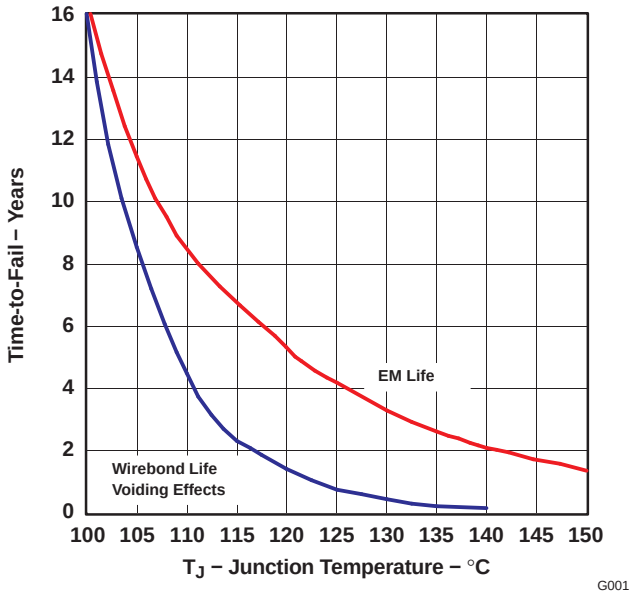


Figure 6-1. Wirebond / EM Life for SM320F280xPZMEP

CAUTION

The peripheral - I/O multiplexing implemented in the 280x devices prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

Table 6-3. F2801/UCD9501 Current Consumption by Power-supply Pins at 100-MHz SYSCLKOUT

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DD3VFL}		I_{DDA18} (2)		I_{DDA33} (3)	
		TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3 • eCAP1/2 • eQEP1 • eCAN-A • SCI-A • SPI-A • ADC • I^2C All PWM pins are toggled at 100 kHz. Data is continuously transmitted out of the SCI-A, SCI-B, and eCAN-A ports. The hardware multiplier is exercised. Code is running out of flash with 3 wait states. XCLKOUT is turned off.	180 mA	210 mA	15 mA	27 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) I_{DDA18} includes current into V_{DD1A18} and V_{DD2A18} pins.
(3) I_{DDA33} includes current into V_{DDA2} and V_{DDAIO} pins.
(4) The TYP numbers are applicable over room temperature and nominal voltage.

Table 6-3. F2801/UCD9501 Current Consumption by Power-supply Pins at 100-MHz SYSCLKOUT (continued)

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DD3VFL}		I_{DDA18} (2)		I_{DDA33} (3)	
		TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX	TYP (4)	MAX
IDLE	Flash is powered down. XCLKOUT is turned off. The following peripheral clocks are enabled: • eCAN-A • SCI-A • SPI-A • I^2C	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

6.4.1 Reducing Current Consumption

280x devices have a richer peripheral mix compared to the 281x family. While the McBSP has been removed, the following new peripherals have been added on the 280x:

- 3 SPI modules
- 1 CAN module
- 1 I^2C module

The two event manager modules of the 281x have been enhanced and replaced with separate ePWM (6), eCAP (4) and eQEP (2) modules, providing tremendous flexibility in applications. Like 281x, 280x DSPs incorporate a unique method to reduce the device current consumption. Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 6-4 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 6-4. Typical Current Consumption by Various Peripherals (at 100 MHz) (1)

PERIPHERAL MODULE	I_{DD} CURRENT REDUCTION (mA)
ADC	8 (2)
I2C	5
eQEP	5
ePWM	5
eCAP	2
SCI	4
SPI	5
eCAN	11

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA18}) as well.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 110 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

6.4.2 Current Consumption Graphs

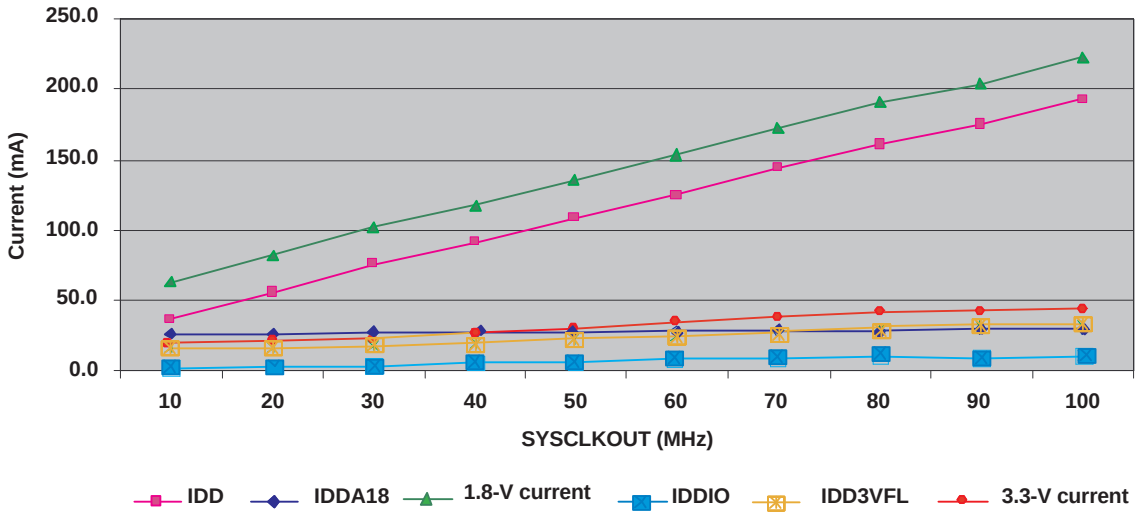


Figure 6-2. Typical Operational Current Versus Frequency (F2808)

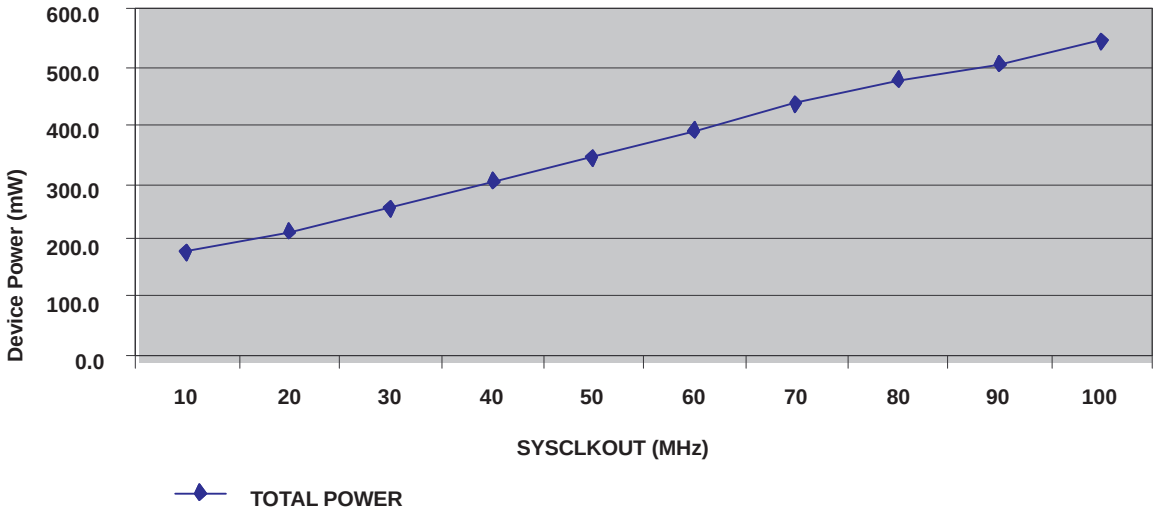


Figure 6-3. Typical Operational Power Versus Frequency (F2808)

6.5 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

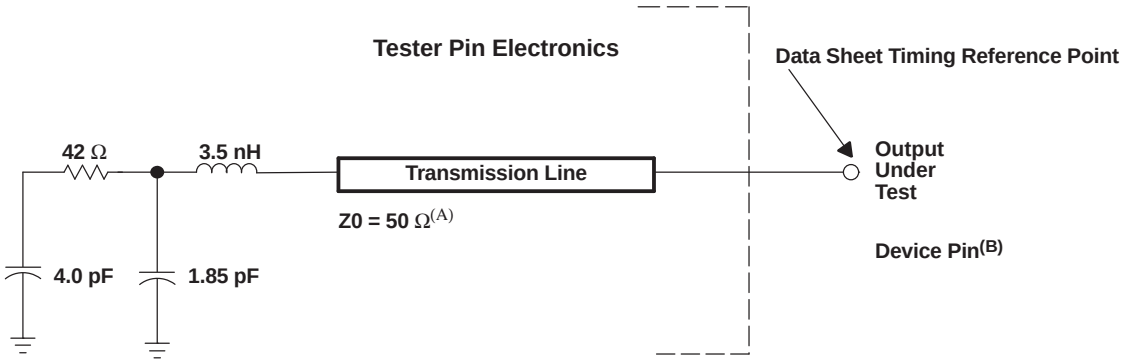
6.5.1 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

6.5.2 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 6-4. 3.3-V Test Load Circuit

6.5.3 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 280x DSPs. Table 6-5 lists the cycle times of various clocks.

Table 6-5. TMS320x280x Clock Table and Nomenclature

		MIN	NOM	MAX	UNIT
On-chip oscillator clock	$t_{c(OSC)}$, Cycle time	28.6		50	ns
	Frequency	20		35	MHz
XCLKIN(1)	$t_{c(CI)}$, Cycle time	10		250	ns
	Frequency	4		100	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	10		500	ns
	Frequency	2		100	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	10		2000	ns
	Frequency	0.5		100	MHz
HSPCLK(2)	$t_{c(HCO)}$, Cycle time	10	20(3)		ns
	Frequency		50(3)	100	MHz
LSPCLK(2)	$t_{c(LCO)}$, Cycle time	10	40(3)		ns
	Frequency		25(3)	100	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	80			ns
	Frequency			12.5	MHz

(1) This also applies to the X1 pin if a 1.8-V oscillator is used.
(2) Lower LSPCLK and HSPCLK will reduce device power consumption.
(3) This is the default reset value if SYSCLKOUT = 100 MHz.

6.6 Clock Requirements and Characteristics

Table 6-6. Input Clock Frequency

PARAMETER				MIN	TYP	MAX	UNIT
f_x	Input clock frequency	Resonator (X1/X2)		20		35	MHz
		Crystal (X1/X2)		20		35	
		External oscillator/clock source (XCLKIN or X1 pin)	Without PLL	4		100	
			With PLL	5		30	
f_l	Limp mode clock frequency range				1-5		MHz

Table 6-7. XCLKIN(1) Timing Requirements - PLL Enabled

NO.			MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	33.3	200	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

(1) This applies to the X1 pin also.

Table 6-8. XCLKIN(1) Timing Requirements - PLL Disabled

NO.				MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		10	250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 100 MHz		2	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 100 MHz		2	ns

(1) This applies to the X1 pin also.

Table 6-8. XCLKIN Timing Requirements - PLL Disabled (continued)

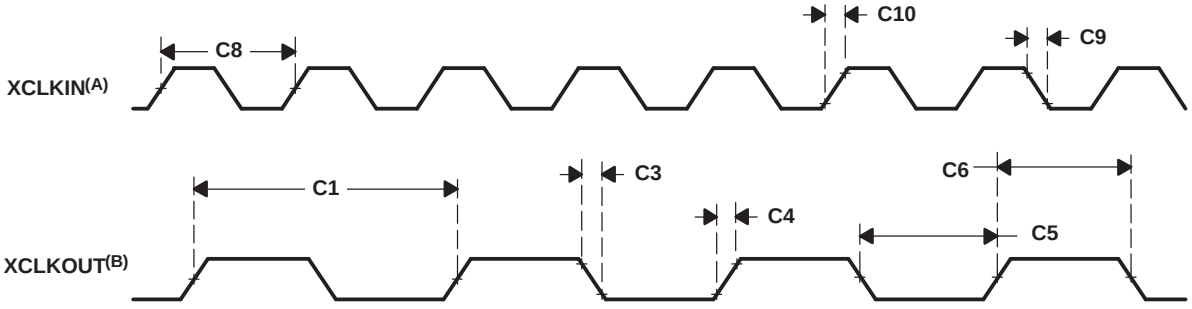
NO.			MIN	MAX	UNIT
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

The possible configuration modes are shown in Table 3-15.

Table 6-9. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1)(2)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	10			ns
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H-2		H+2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H-2		H+2	ns
	t_p	PLL lock time			$131072t_{c(OSCCLK)}$ (3)	cycles

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$
(3) OSCCLK is either the output of the on-chip oscillator or the output from an external oscillator.



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.

B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 6-5. Clock Timing

6.7 Power Sequencing

No requirements are placed on the power up/down sequence of the various power pins to ensure the correct reset state for all the modules. However, if the 3.3-V transistors in the level shifting output buffers of the I/O pins are powered prior to the 1.8-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

There are some requirements on the $\overline{XRS}$ pin:

1. During power up, the $\overline{XRS}$ pin must be held low for $t_{w(RSL1)}$ after the input clock is stable (see Table 6-11). This is to enable the entire device to start from a known condition.
2. During power down, the $\overline{XRS}$ pin must be pulled low at least 8 µs prior to V_{DD} reaching 1.5 V. This is to enhance flash reliability.

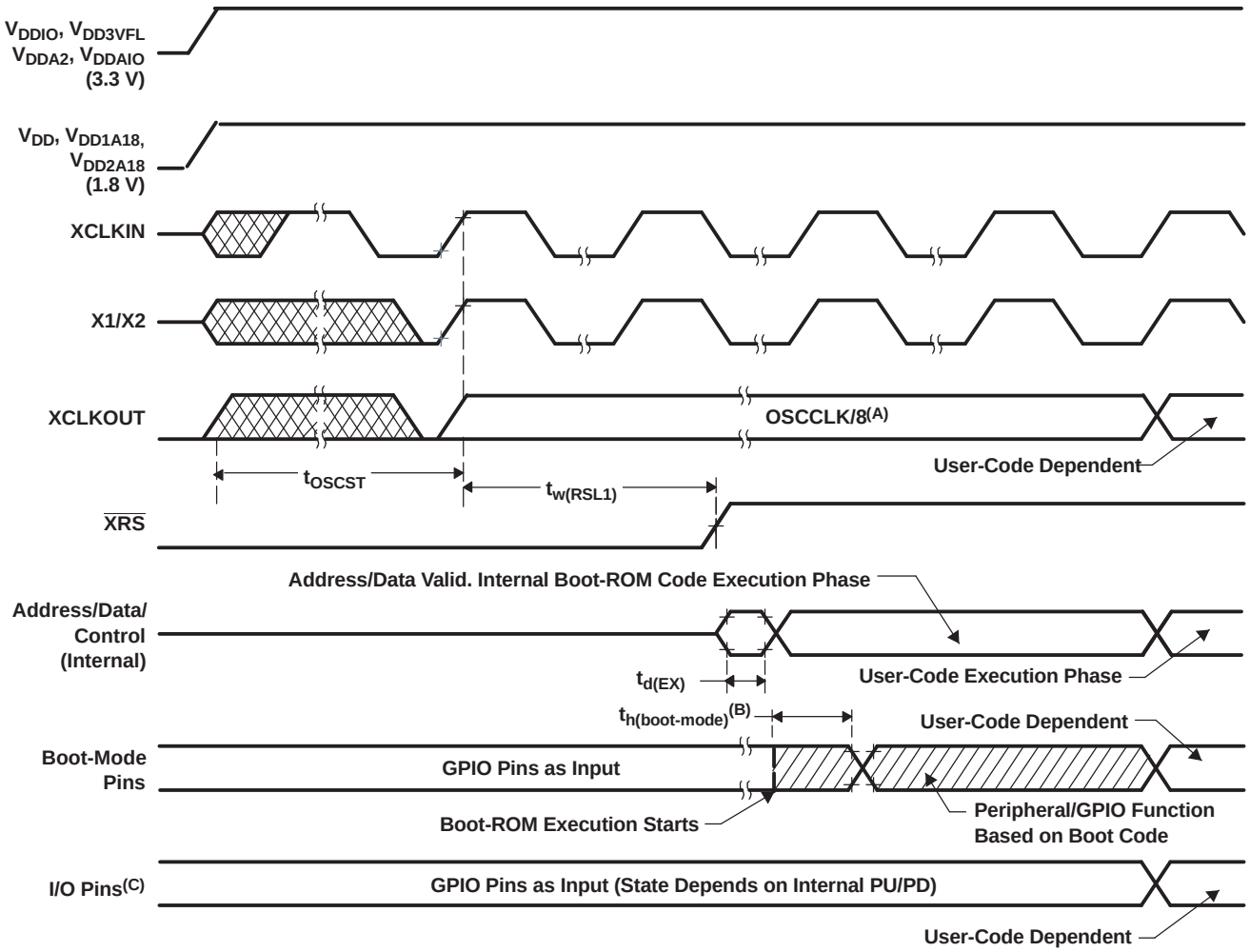
Additionally it is recommended that no voltage larger than a diode drop (0.7 V) should be applied to any pin prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.

6.7.1 Power Management and Supervisory Circuit Solutions

Table 6-10 lists the power management and supervisory circuit solutions for 280x DSPs. LDO selection depends on the total power consumed in the end application. Go to www.power.ti.com for a complete list of Texas Instruments power ICs or select Texas Instruments DSP Power Solutions for links to the *DSP Power Selection Guide* (slub006a.pdf) and links to specific power reference designs.

Table 6-10. Power Management and Supervisory Circuit Solutions

SUPPLIER	TYPE	PART	DESCRIPTION
Texas Instruments	LDO	TPS767D301	Dual 1-A low-dropout regulator (LDO) with supply voltage supervisor (SVS)
Texas Instruments	LDO	TPS70202	Dual 500/250-mA LDO with SVS
Texas Instruments	LDO	TPS766xx	250-mA LDO with PG
Texas Instruments	SVS	TPS3808	Open Drain SVS with programmable delay
Texas Instruments	SVS	TPS3803	Low-cost Open-drain SVS with 5 μS delay
Texas Instruments	LDO	TPS799xx	200-mA LDO in WCSP package
Texas Instruments	LDO	TPS736xx	400-mA LDO with 40 mV of V_{DO}
Texas Instruments	DC/DC	TPS62110	High V_{in} 1.2-A dc/dc converter in 4x4 QFN package
Texas Instruments	DC/DC	TPS6230x	500-mA converter in WCSP package



A. Upon power up, SYSCLKOUT is OSCCLK/2. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = OSCCLK/8 during this phase.

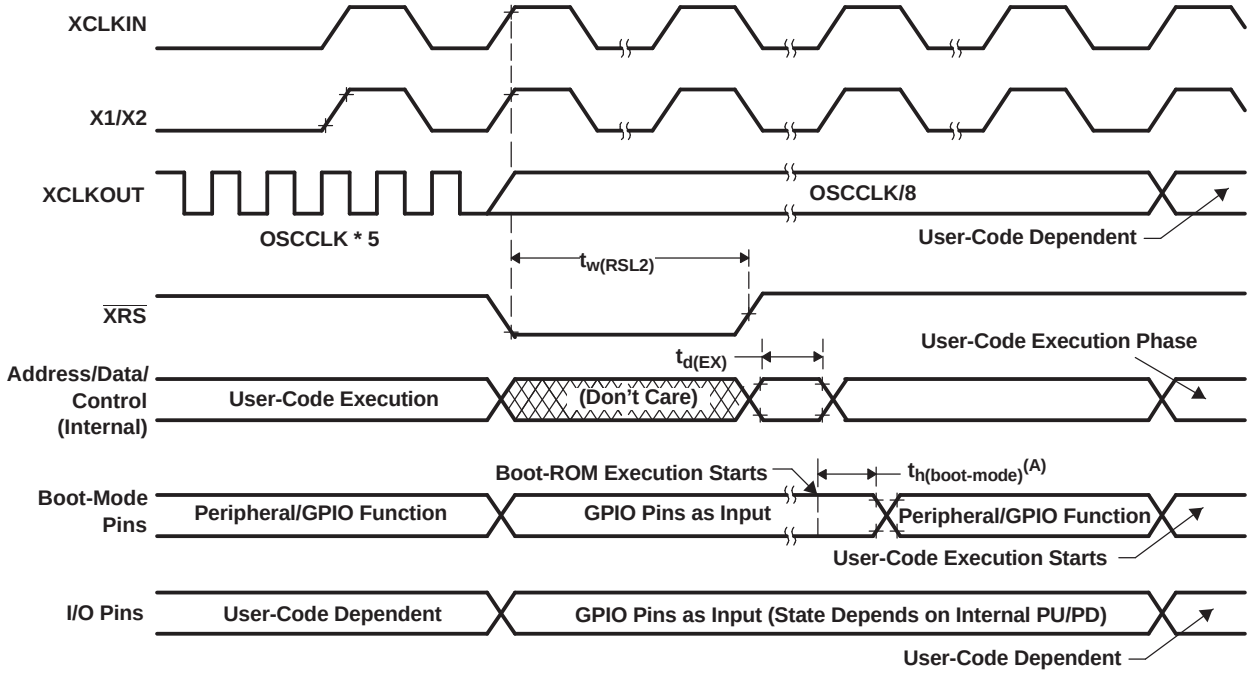
B. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 6-6. Power-on Reset

Table 6-11. Reset ($\overline{XRS}$) Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(RSL1)}$ (1)	Pulse duration, stable XCLKIN to $\overline{XRS}$ high		$8t_{c(OSCCLK)}$			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low	Warm reset	$8t_{c(OSCCLK)}$			cycles
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(OSCCLK)}$		cycles
t_{OSCST} (2)	Oscillator start-up time		1	10		ms
$t_{h(boot-mode)}$	Hold time for boot-mode pins		$200t_{c(OSCCLK)}$			cycles

(1) In addition to the $t_{w(RSL1)}$ requirement, $\overline{XRS}$ has to be low at least for 1 ms after V_{DD} reaches 1.5 V.
(2) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

Figure 6-8 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete (which takes 131072 OSCCLK cycles), SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

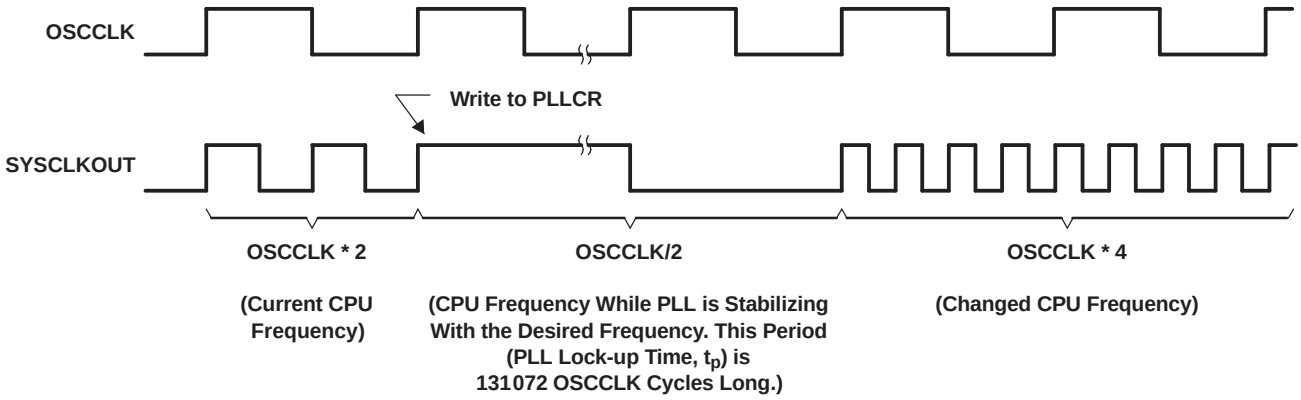


Figure 6-8. Example of Effect of Writing Into PLLCR Register

6.8 General-Purpose Input/Output (GPIO)

6.8.1 GPIO - Output Timing

Table 6-12. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8	ns
t_{fGPO}	Toggling frequency, GPO pins			25	MHz

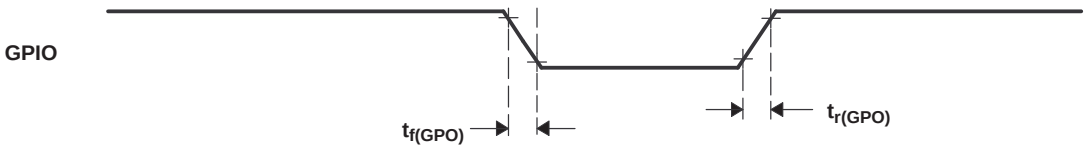
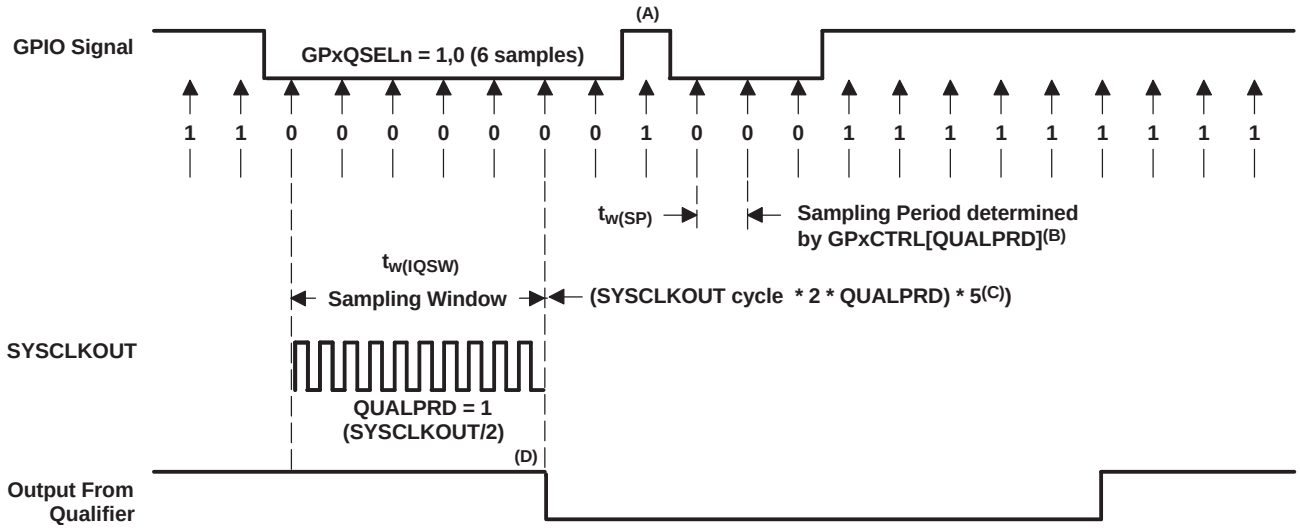


Figure 6-9. General-Purpose Output Timing

6.8.2 GPIO - Input Timing



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled)..

B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 6-10. Sampling Mode

Table 6-13. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) - 1)		cycles
$t_{w(GPI)}$(2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 5, if QUALPRD = 0

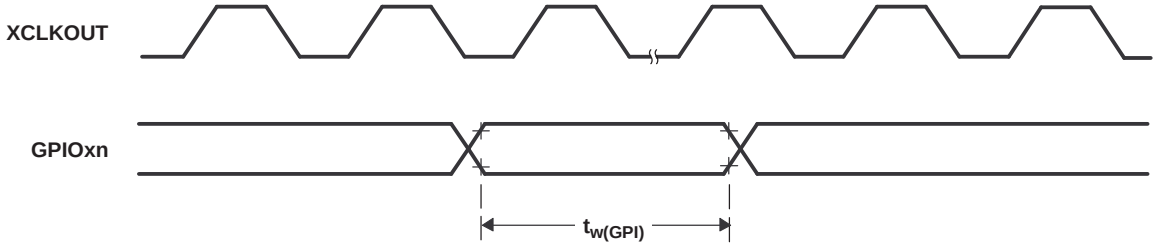


Figure 6-11. General-Purpose Input Timing

NOTE

The pulse-width requirement for general-purpose input is applicable for the XINT2_ADCSOC signal as well.

6.8.4 Low-Power Mode Wakeup Timing

Table 6-14 shows the timing requirements, Table 6-15 shows the switching characteristics, and Figure 6-12 shows the timing diagram for IDLE mode.

Table 6-14. IDLE Mode Timing Requirements(1)

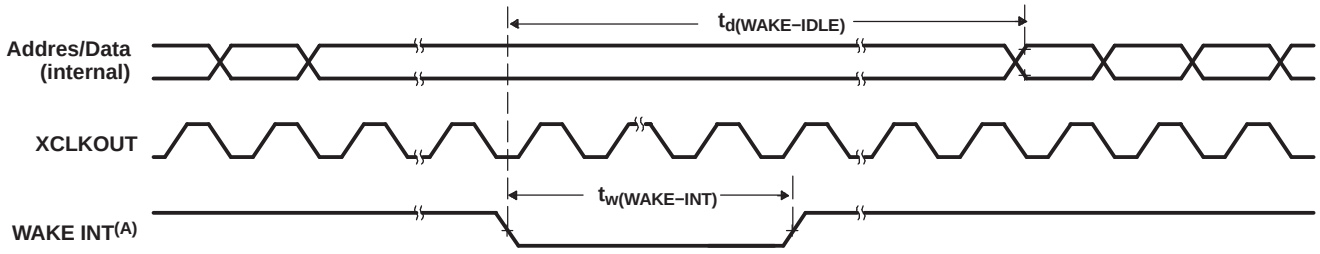
			MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$			cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$			

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-15. IDLE Mode Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)					
	• Wake-up from Flash – Flash module in active state	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier			$1050t_{c(SCO)}$	cycles
		With input qualifier			$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 6-13.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up) signal involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$, XNMI, or $\overline{\text{XRS}}$.

Figure 6-12. IDLE Entry and Exit Timing

Table 6-16. STANDBY Mode Timing Requirements

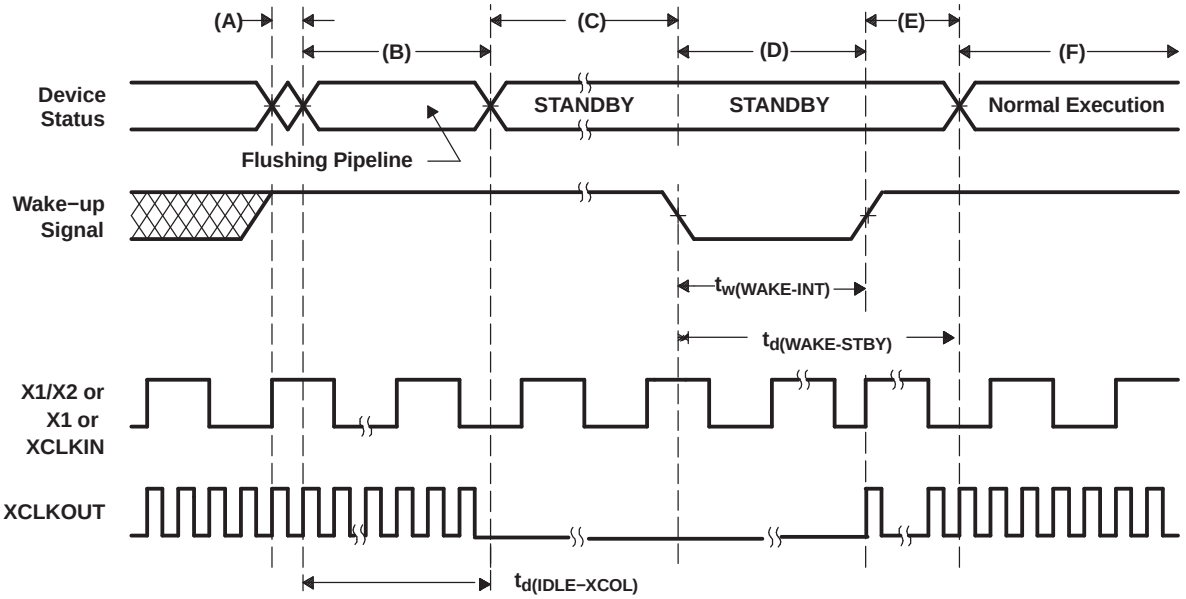
		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$			cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$			

(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 6-17. STANDBY Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume (1)					cycles
	• Wake up from flash – Flash module in active state	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier			$1125t_{c(SCO)}$	cycles
		With input qualifier			$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.

B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles before being turned off. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.

D. The external wake-up signal is driven active.

E. After a latency period, the STANDBY mode is exited.

F. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-13. STANDBY Entry and Exit Timing Diagram

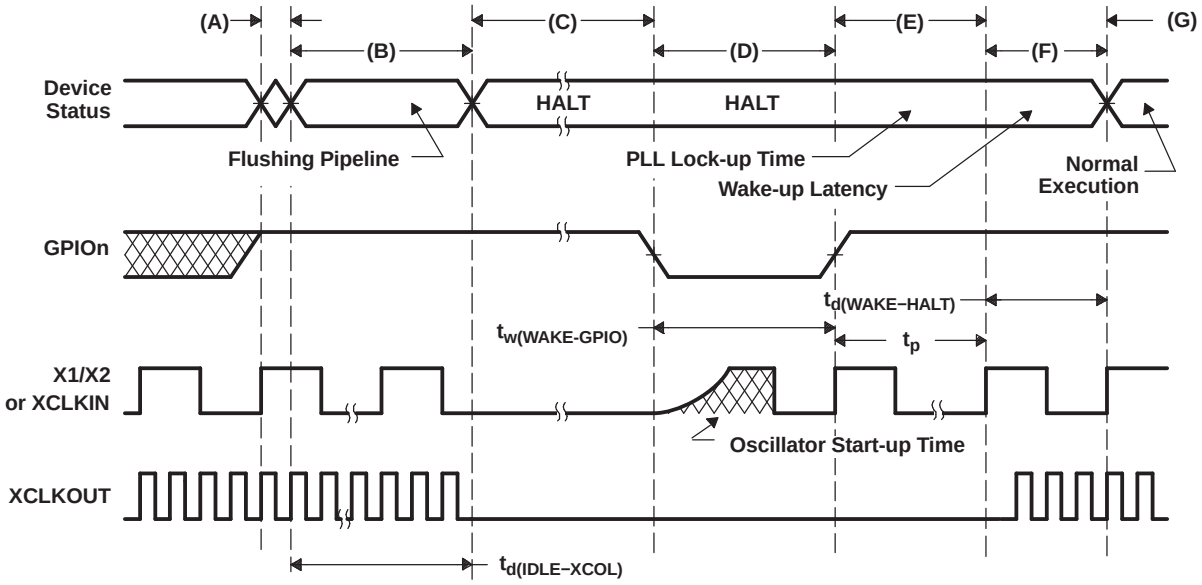
Table 6-18. HALT Mode Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$ (1)			cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$t_{oscst} + 8t_{c(OSCCLK)}$			cycles

(1) See Table 6-11 for an explanation of t_{oscst}.

Table 6-19. HALT Mode Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time			$131072t_{c(OSCCLK)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state			$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM			$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for approximately 32 cycles before the oscillator is turned off and the CLKIN to the core is stopped. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power.

D. When the GPIOn pin is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. When GPIOn is deactivated, it initiates the PLL lock sequence, which takes 131,072 OSCCLK (X1/X2 or X1 or XCLKIN) cycles.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

G. Normal operation resumes.

Figure 6-14. HALT Wake Up Using GPIOn

6.9 Enhanced Control Peripherals

6.9.1 Enhanced Pulse Width Modulator (ePWM) Timing

PWM refers to PWM outputs on ePWM1-6. Table 6-20 shows the PWM timing requirements and Table 6-21, switching characteristics.

Table 6-20. ePWM Timing Requirements(1)

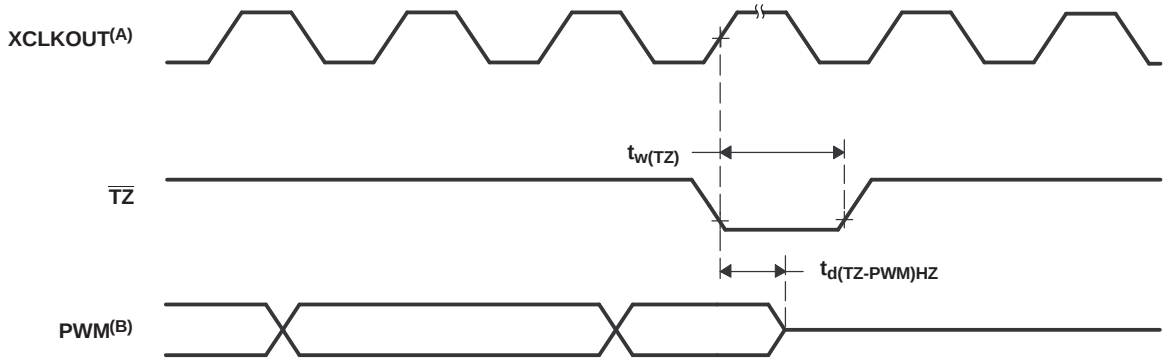
		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-21. ePWM Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

6.9.2 Trip-Zone Input Timing



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-15. PWM Hi-Z Characteristics

Table 6-22. Trip-Zone input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-23 shows the high-resolution PWM switching characteristics.

Table 6-23. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)

	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) Maximum MEP step size is based on worst-case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the Texas Instruments software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

Table 6-24 shows the eCAP timing requirement and Table 6-25 shows the eCAP switching characteristics.

Table 6-24. Enhanced Capture (eCAP) Timing Requirement(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-25. eCAP Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

Table 6-26 shows the eQEP timing requirement and Table 6-27 shows the eQEP switching characteristics.

Table 6-26. Enhanced Quadrature Encoder Pulse (eQEP) Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2(1t_{c(SCO)} + t_{w(IQSW)})$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-27. eQEP Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment			$4t_{c(SCO)}$	cycles
$t_{d(PXCSOUT)QEP}$	Delay time, QEP input edge to position compare sync output			$6t_{c(SCO)}$	cycles

Table 6-28. External ADC Start-of-Conversion Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCAL)}$	Pulse duration, $\overline{\text{ADCSOCAO}}$ low	$32t_{c(HCO)}$		cycles

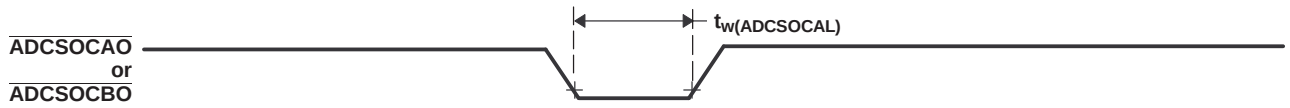


Figure 6-16. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

6.9.3 External Interrupt Timing

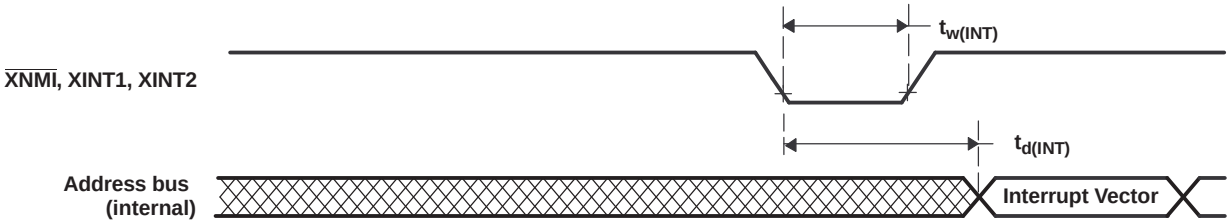


Figure 6-17. External Interrupt Timing

Table 6-29. External Interrupt Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-30. External Interrupt Switching Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

6.9.4 I2C Electrical Specification and Timing

Table 6-31. I2C Timing

		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately		400	kHz
v_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3 mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	1.3		µs
t_{HIGH}	High period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	0.6		µs
I_I	Input current with an input voltage between 0.1 V_{DDIO} and 0.9 V_{DDIO} MAX		-10	10	µA

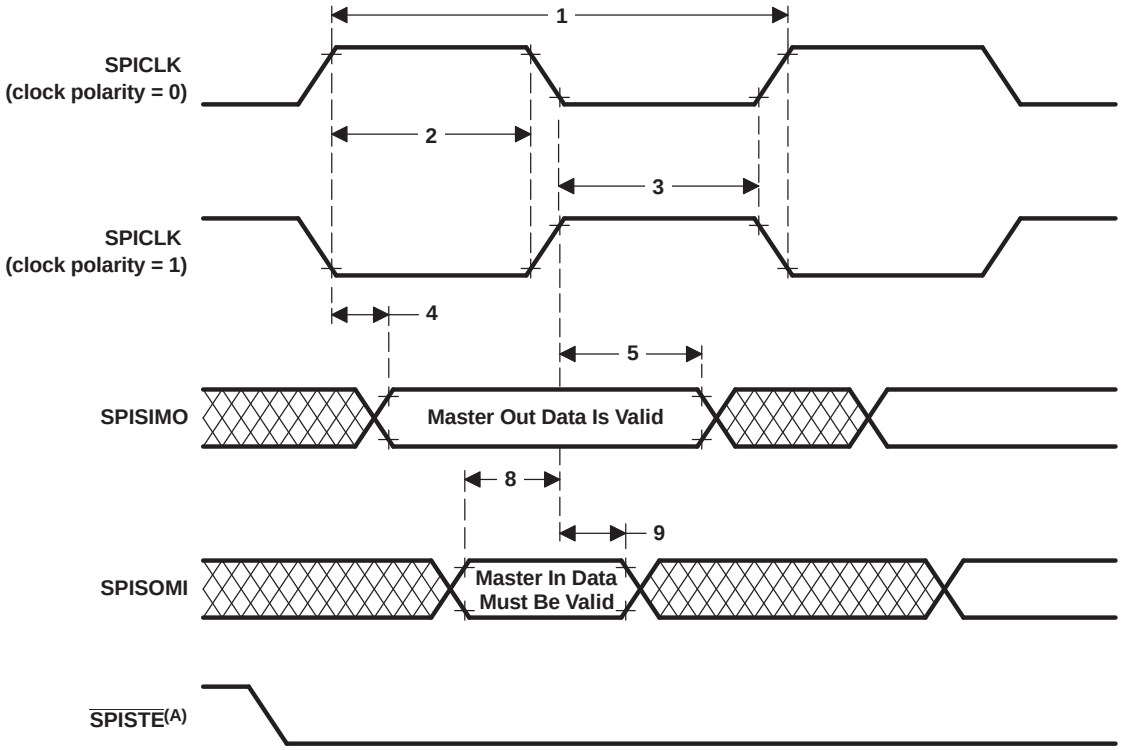
6.9.5 Serial Peripheral Interface (SPI) Master Mode Timing

Table 6-32 lists the master mode timing (clock phase = 0) and Table 6-33 lists the timing (clock phase = 1). Figure 6-18 and Figure 6-19 show the timing waveforms.

Table 6-32. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)}M$ - $0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ - 10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ - 10	$0.5_{tc(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$-10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M}$ - 10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$- 10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		10		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		10		10	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ -10		
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ -10		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	35		35		ns
9	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.25t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$- $0.5t_{c(LCO)}$- 10		
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.25t_{c(SPC)M}$ - 10		$0.5t_{c(SPC)M}$- $0.5t_{c(LCO)}$- 10		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).



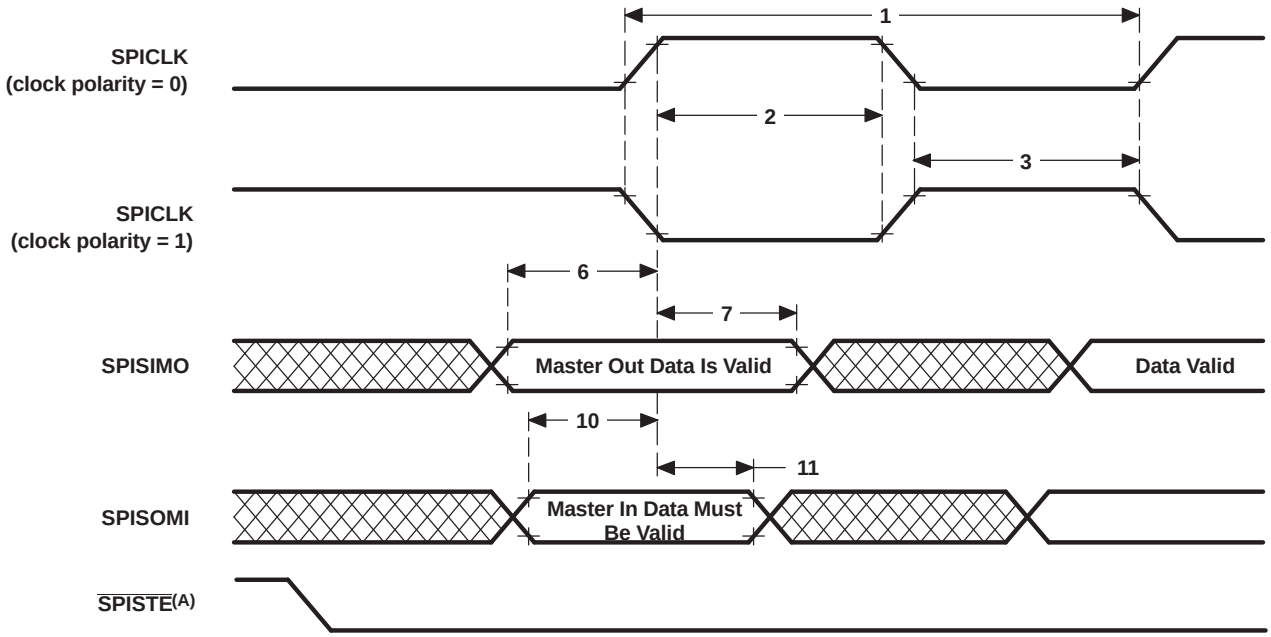
A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-18. SPI Master Mode External Timing (Clock Phase = 0)

Table 6-33. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c\ (LCO)}$-10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c\ (LCO)}$-10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO}$	ns
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5_{tc(SPC)M}$ + $0.5t_{c(LCO)}$ -10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
6	$t_{su(SIMO-SPCH)M}$	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
	$t_{su(SIMO-SPCL)M}$	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ -10		ns
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	35		35		ns
11	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.25t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ -10		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.25_{tc(SPC)M}$ -10		$0.5_{tc(SPC)M}$ -10		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX
Slave mode transmit 12.5 MHz MAX, slave mode receive 12.5 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-19. SPI Master External Timing (Clock Phase = 1)

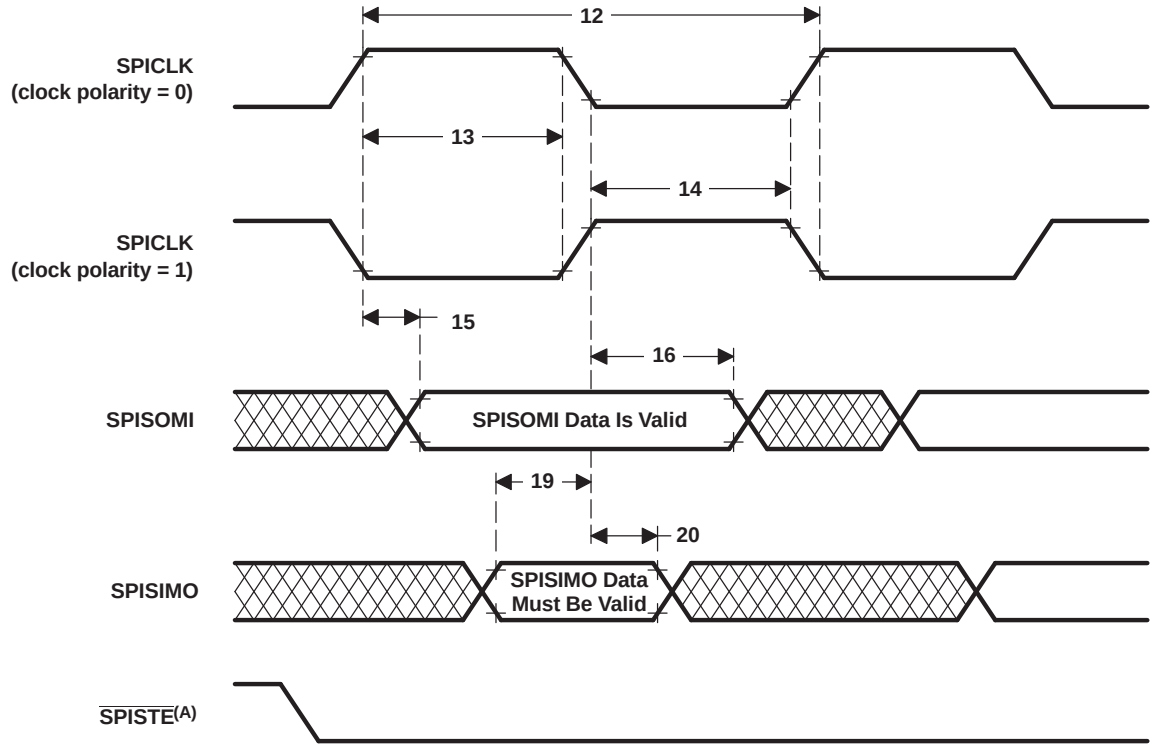
6.9.6 SPI Slave Mode Timing

Table 6-34 lists the slave mode external timing (clock phase = 0) and Table 6-35 (clock phase = 1). Figure 6-20 and Figure 6-21 show the timing waveforms.

Table 6-34. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLKCycle time, SPICLK	$4t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		35	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		35	ns
16	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		ns
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	35		ns
20	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



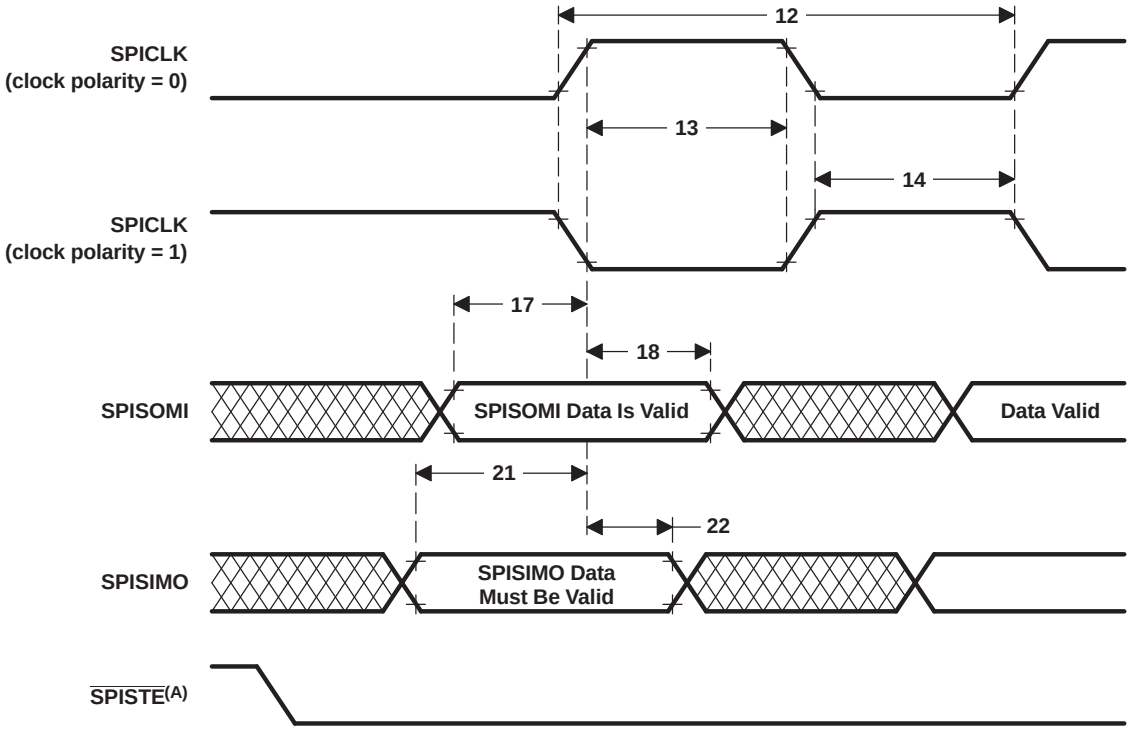
A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ (minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-20. SPI Slave Mode External Timing (Clock Phase = 0)

Table 6-35. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
17	$t_{su(SOMI-SPCH)S}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$0.125t_{c(SPC)S}$		ns
	$t_{su(SOMI-SPCL)S}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1	$0.125t_{c(SPC)S}$		ns
18	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		ns
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	35		ns
22	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-21. SPI Slave Mode External Timing (Clock Phase = 1)

6.9.7 On-Chip Analog-to-Digital Converter

Table 6-36. ADC Electrical Characteristics (over recommended operating conditions)(1)(2)

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock		1			kHz
				12.5	MHz
ACCURACY					
INL (Integral nonlinearity)	1-12.5 MHz ADC clock (6.25 MSPS)			±1.5	LSB
DNL (Differential nonlinearity)(3)	1-12.5 MHz ADC clock (6.25 MSPS)			±1	LSB
Offset error (4)		-60		+60	LSB
Offset error with hardware trimming			±4		LSB
Overall gain error with internal reference (5)		-60		+60	LSB
Overall gain error with external reference		-60		+60	LSB
Channel-to-channel offset variation			±4		LSB
Channel-to-channel gain variation			±4		LSB
ANALOG INPUT					
Analog input voltage (ADCINx to ADCLO) (6)		0		3	V
ADCLO		-5	0	5	mV
Input capacitance			10		pF
Input leakage current				±5	µA
INTERNAL VOLTAGE REFERENCE (5)					
$V_{ADCREFP}$ - ADCREFP output voltage at the pin based on internal reference			1.275		V
$V_{ADCREFM}$ - ADCREFM output voltage at the pin based on internal reference			0.525		V
Voltage difference, ADCREFP - ADCREFM			0.75		V
Temperature coefficient			50		PPM/°C
EXTERNAL VOLTAGE REFERENCE(5)(7)					
$V_{ADCREFIN}$ - External reference voltage input on ADCREFIN pin 0.2% or better accurate reference recommended	ADCREFSEL[15:14] = 11b		1.024		V
	ADCREFSEL[15:14] = 10b		1.500		V
	ADCREFSEL[15:14] = 01b		2.048		V
AC SPECIFICATIONS					
SINAD (100 kHz) Signal-to-noise ratio + distortion			67.5		dB
SNR (100 kHz) Signal-to-noise ratio			68		dB
THD (100 kHz) Total harmonic distortion			-79		dB
ENOB (100 kHz) Effective number of bits			10.9		Bits
SFDR (100 kHz) Spurious free dynamic range			83		dB

(1) Tested at 12.5 MHz ADCCLK.
(2) All voltages listed in this table are with respect to V_{SSA2}.
(3) Texas Instruments specifies that the ADC will have no missing codes.
(4) 1 LSB has the weighted value of 3.0/4096 = 0.732 mV.
(5) A single internal/external band gap reference sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference. The total gain error listed for the internal reference is inclusive of the movement of the internal bandgap over temperature. Gain error over temperature for the external reference option will depend on the temperature profile of the source used.
(6) Voltages above V_{DDA} + 0.3 V or below V_{SS} - 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.
(7) Texas Instruments recommends using high precision external reference Texas Instruments part REF3020/3120 or equivalent for 2.048-V reference.

6.9.7.1 ADC Power-Up Control Bit Timing

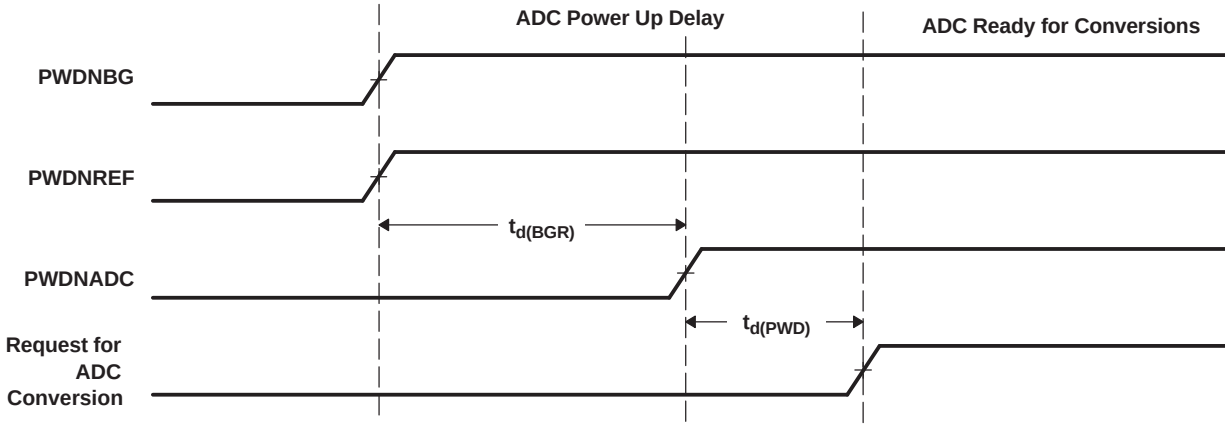


Figure 6-22. ADC Power-Up Control Bit Timing

Table 6-37. ADC Power-Up Delays

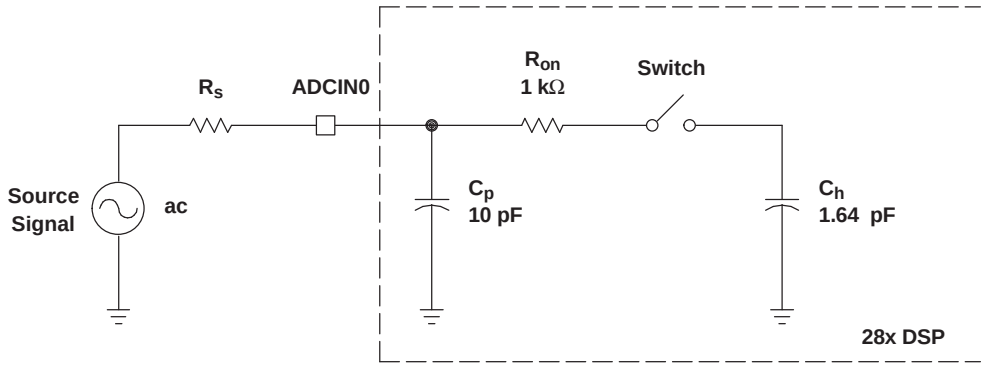
	PARAMETER(1)	MIN	TYP	MAX	UNIT
$t_{d(BGR)}$	Delay time for band gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled.		5		ms
$t_{d(PWD)}$	Delay time for power-down control to be stable. Bit delay time for band-gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled. Bit 5 of the ADCTRL3 register (PWDNADC)must be set to 1 before any ADC conversions are initiated.	20	50		µs
				1	ms

(1) Timings maintain compatibility to the 281x ADC module. The 280x ADC also supports driving all 3 bits at the same time and waiting $t_{d(BGR)}$ ms before first conversion.

Table 6-38. Current Consumption for Different ADC Configurations (at 12.5-MHz ADCCLK)(1)(2)

ADC OPERATING MODE	CONDITIONS	V_{DDA18}	$V_{DDA3.3}$	UNIT
Mode A (Operational Mode):	• BG and REF enabled • PWD disabled	30	2	mA
Mode B:	• ADC clock enabled • BG and REF enabled • PWD enabled	9	0.5	ma
Mode C:	• ADC clock enabled • BG and REF disabled • PWD enabled	5	20	µA
Mode D:	• ADC clock disabled • BG and REF disabled • PWD enabled	5	15	µA

(1) Test Conditions:
SYSCLKOUT = 100 MHz
ADC module clock = 12.5 MHz
ADC performing a continuous conversion of all 16 channels in Mode A
(2) V_{DDA18} includes current into V_{DD1A18} and V_{DD2A18}. $V_{DDA3.3}$ includes current into V_{DDA2} and V_{DDAIO}.



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}):	**1 kΩ**
Sampling Capacitor (C_h):	**1.64 pF**
Parasitic Capacitance (C_p):	**10 pF**
Source Resistance (R_s):	**50 Ω**

Figure 6-23. ADC Analog Input Impedance Model

6.9.7.2 Definitions

Reference Voltage

The on-chip ADC has a built-in reference, which provides the reference voltages for the ADC.

Analog Inputs

The on-chip ADC consists of 16 analog inputs, which are sampled either one at a time or two channels at a time. These inputs are software-selectable.

Converter

The on-chip ADC uses a 12-bit four-stage pipeline architecture, which achieves a high sample rate with low power consumption.

Conversion Modes

The conversion can be performed in two different conversion modes:

- Sequential sampling mode (SMODE = 0)
- Simultaneous sampling mode (SMODE = 1)

6.9.7.3 Sequential Sampling Mode (Single-Channel) (SMODE = 0)

In sequential sampling mode, the ADC can continuously convert input signals on any of the channels (Ax to Bx). The ADC can start conversions on event triggers from the ePWM, software trigger, or from an external ADCSOC signal. If the SMODE bit is 0, the ADC will do conversions on the selected channel on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled at every falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

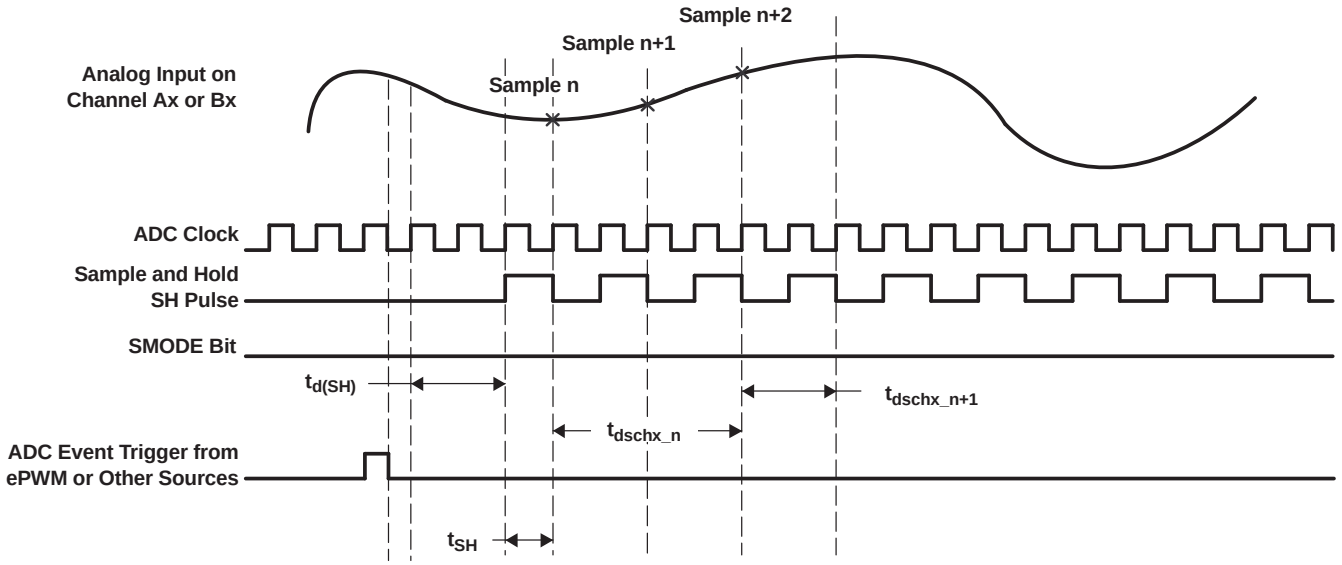


Figure 6-24. Sequential Sampling Mode (Single-Channel) Timing

Table 6-39. Sequential Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 12.5 MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 80 nS	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/Acquisition Width	(1 + Acqps) * $t_{c(ADCCLK)}$		80 ns with Acqps = 0	Acqps value = 0-15 ADCTRL1[8:11]
$t_{d(schx\_n)}$	Delay time for first result to appear in Result register	$4t_{c(ADCCLK)}$		320 ns	
$t_{d(schx\_n+1)}$	Delay time for successive results to appear in Result register		(2 + Acqps) * $t_{c(ADCCLK)}$	160 ns	

6.9.7.4 Simultaneous Sampling Mode (Dual-Channel) (SMODE = 1)

In simultaneous mode, the ADC can continuously convert input signals on any one pair of channels (A0/B0 to A7/B7). The ADC can start conversions on event triggers from the ePWM, software trigger, or from an external ADCSOC signal. If the SMODE bit is 1, the ADC will do conversions on two selected channels on every Sample/Hold pulse. The conversion time and latency of the result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled simultaneously at the falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

NOTE

In simultaneous mode, the ADCIN channel pair select has to be A0/B0, A1/B1, ..., A7/B7, and not in other combinations (such as A1/B3, etc.).

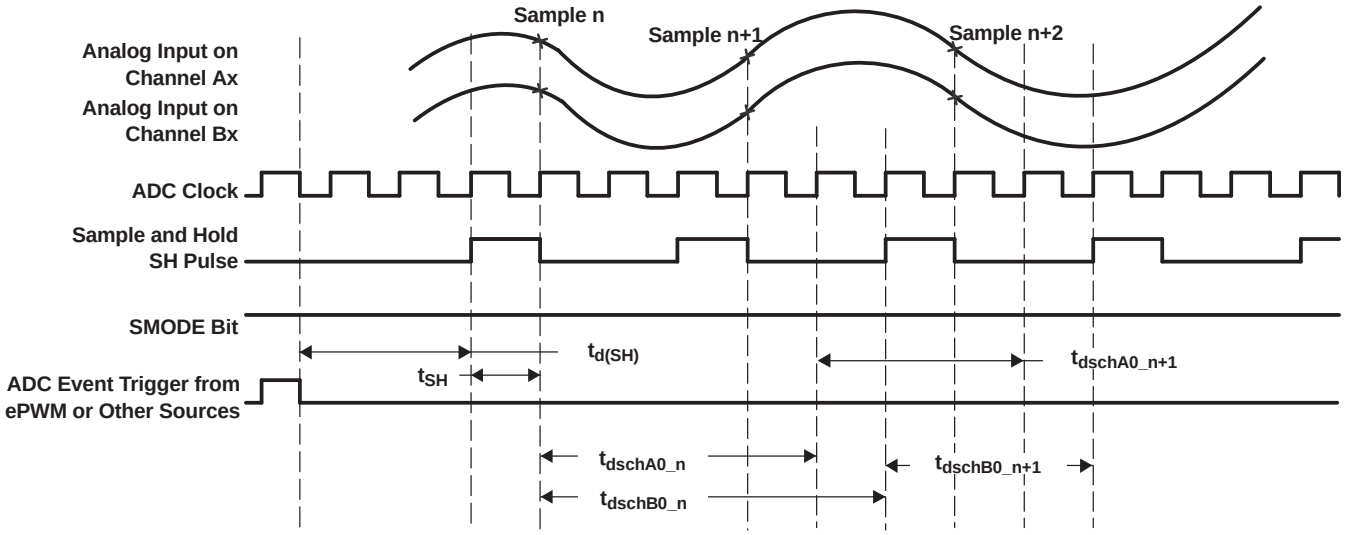


Figure 6-25. Simultaneous Sampling Mode Timing

Table 6-40. Simultaneous Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 12.5 MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 80 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	2.5 $t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/Acquisition Width	(1 + Acqps) x $t_{c(ADCCLK)}$		80 ns with Acqps = 0	Acqps value = 0-15 ADCTRL1[8:11]
$t_{d(schA0\_n)}$	Delay time for first result to appear in Result register	4 $t_{c(ADCCLK)}$		320 ns	
$t_{d(schB0\_n)}$	Delay time for first result to appear in Result register	5 $t_{c(ADCCLK)}$		400 ns	
$t_{d(schA0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) x $t_{c(ADCCLK)}$	240 ns	
$t_{d(schB0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) x $t_{c(ADCCLK)}$	240 ns	

6.10 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

6.11 Flash Timing

Table 6-41. Flash Endurance

			MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	-55°C to 125°C (ambient)	100	1000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	-55°C to 125°C (ambient)			1	write

Table 6-42. Flash Parameters at 100-MHz SYSCLKOUT

	PARAMETER(1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Time	16-Bit Word			50		µs
	16K Sector			500		ms
	8K Sector			250		ms
	4K Sector			125		ms
Erase Time	16K Sector			10		S
	8K Sector			10		S
	4K Sector			10		S
$I_{DD3VFLP}$	V_{DD3VFL} current consumption during the Erase/Program cycle	Erase		75		mA
		Program		35		mA
I_{DDP}	V_{DD} current consumption during Erase/Program cycle			140		mA
I_{DDIOP}	V_{DDIO} current consumption during Erase/Program cycle			20		mA

(1) Typical parameters as seen at room temperature using flash API version 3.00 including function call overhead.

Table 6-43. Flash/OTP Access Timing

PARAMETER(1)		MIN	TYP	MAX	UNIT
$t_{a(fp)}$	Paged flash access time	36			ns
$t_{a(fr)}$	Random flash access time	36			ns
$t_{a(OTP)}$	OTP access time	60			ns

(1) For 100 MHz, PAGE WS = 3 and RANDOM WS = 3; for 75 MHz, PAGE WS = 2, and RANDOM WS = 2.

Equations to compute the page wait state and random wait state in Table 6-44 are as follows:

$$\text{Flash Page Wait-State} = \left[\left(\frac{t_{a(fp)}}{t_{c(SCO)}}\right) - 1\right] \text{(round up to the next highest integer) or 0, whichever is larger}$$

$$\text{Flash Random Wait-State} = \left[\left(\frac{t_{a(fr)}}{t_{c(SCO)}}\right) - 1\right] \text{(round up to the next highest integer) or 1, whichever is larger}$$

Table 6-44. Minimum Required Wait-States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	PAGE WAIT-STATE	RANDOM WAIT STATE(1)
100	10	3	3
75	13.33	2	2
50	20	1	1
30	33.33	1	1
25	40	0	1
15	66.67	0	1
4	250	0	1

(1) Random wait state must be greater than or equal to 1.

7 Mechanical Data

Table 7-1 and Table 7-2 show the thermal data.
The mechanical package diagram(s) that follow the tables reflect the most current released mechanical data available for the designated device(s).

Table 7-1. F280x Thermal Model 100-pin GGM Results

	Air Flow			
PARAMETER	**0 lfm**	**150 lfm**	**250 lfm**	**500 lfm**
θ_{JA}[°C/W] High k PCB	30.58	29.31	28.09	26.62
Ψ_{JT}[°C/W]	0.4184	0.32	0.3725	0.4887
θ_{JC}	12.08			
θ_{JB}	16.46			

Table 7-2. F280x Thermal Model 100-pin PZ Results

	Air Flow			
PARAMETER	**0 lfm**	**150 lfm**	**250 lfm**	**500 lfm**
θ_{JA}[°C/W] High k PCB	48.16	40.06	37.96	35.17
Ψ_{JT}[°C/W]	0.3425	0.85	1.0575	1.410
θ_{JC}	12.89			
θ_{JB}	29.58			

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SM320F2801PZMEP	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SM320F2808PZMEP	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06619-01XE	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06619-03XE	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

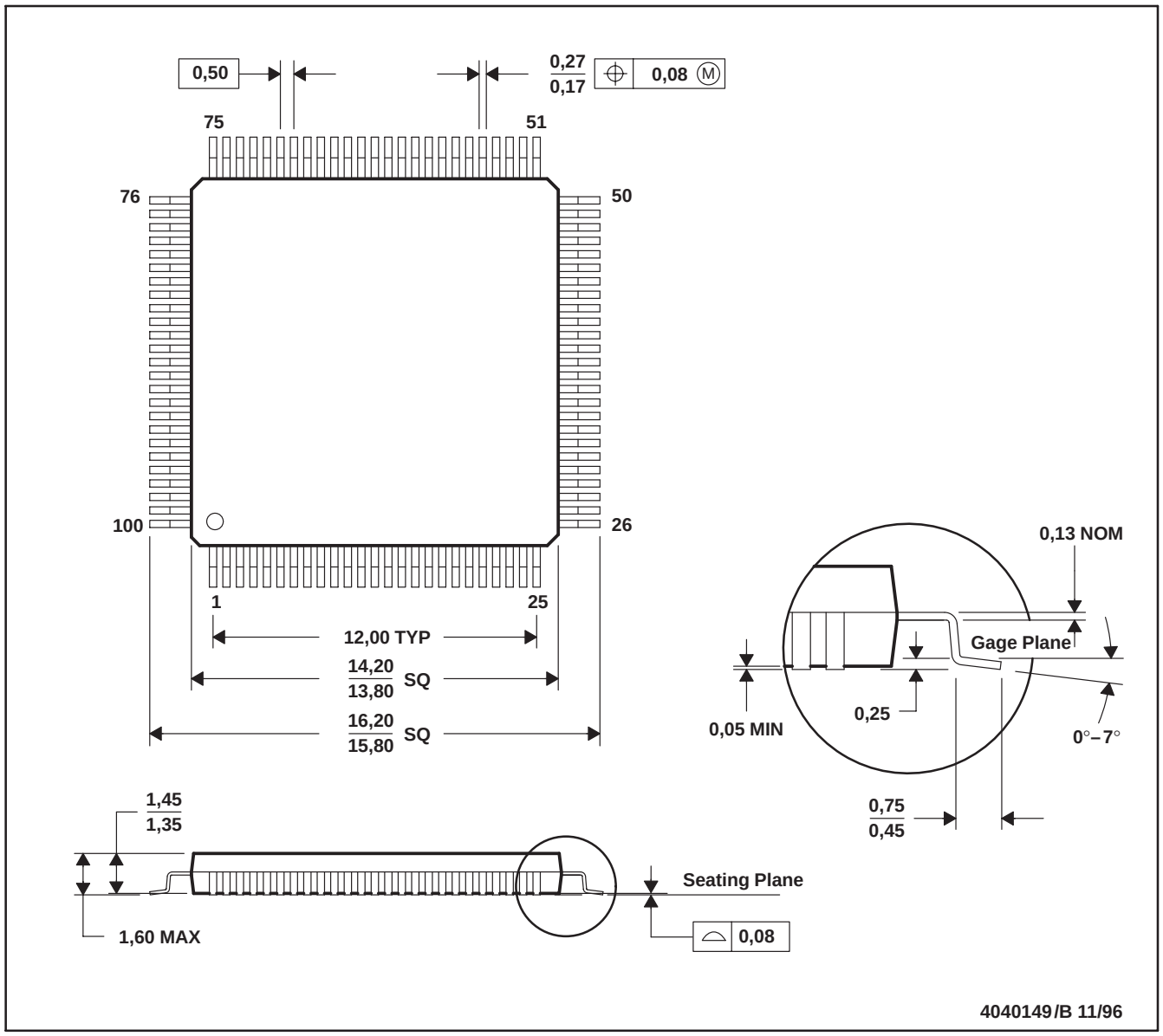
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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