SN74AVCH8T245 8-Bit Dual-Supply Bus Transceiver With Configurable Level-Shifting, Voltage Translation, and 3-State Outputs

1 Features

- Control Inputs (DIR and $\overline{OE}$) V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- V_{CC} Isolation Feature
- Fully Configurable Dual-Rail Design
- I/Os Are 4.6-V Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates:
  - 320 Mbps (V_{CCA} ≥ 1.8 V and V_{CCB} ≥ 1.8 V)
  - 170 Mbps (V_{CCA} ≤ 1.8 V or V_{CCB} ≤ 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecommunications

3 Description

The SN74AVCH8T245 is an 8-bit noninverting bus transceiver that uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}, which accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH8T245 is designed for asynchronous communication between data buses. The device transmits data from either the A bus to the B bus, or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVCH8T245	TVSOP (24)	5.00 mm × 4.40 mm
	TSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

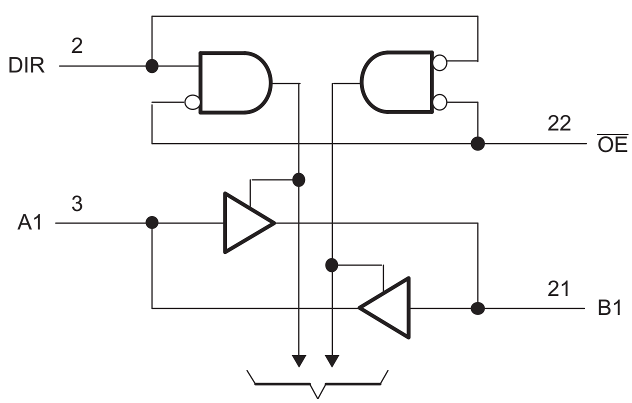


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2007) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted the Ordering Information table. See the POA at the end of the data sheet. 1

5 Description (continued)

The SN74AVCH8T245 is designed so that the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA}.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device.

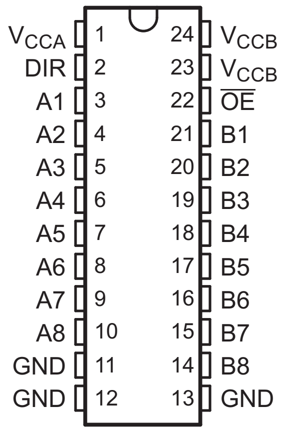
The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is at GND, then the outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

The SN74AVCH8T245 solution is compatible with a single-supply system and can be replaced later with a '245 function, with minimal printed circuit board redesign.

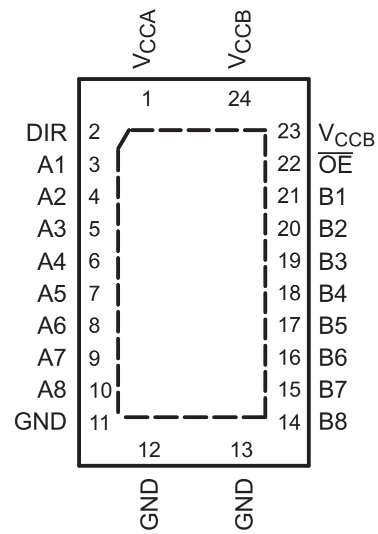
To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions

DGV or PW Package
24-Pin TVSOP or TSSOP
Top View



RHL Package
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	I	Direction-control signal. Referenced to V_{CCA}.
GND	11, 12, 13	—	Ground
$\overline{OE}$	22	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23, 24	—	B-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage[(2)]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state[(2)]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state[(2)(3)]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See [1][2]

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.2	3.6	V
V_{CCB}	Supply voltage			1.2	3.6	V
V_{IH}	High-level input voltage[1]	Data inputs	V_{CCI} = 1.2 V to 1.95 V	V_{CCI} × 0.65		V
			V_{CCI} = 1.95 V to 2.7 V	1.6		
			V_{CCI} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage[1]	Data inputs	V_{CCI} = 1.2 V to 1.95 V		V_{CCI} × 0.35	V
			V_{CCI} = 1.95 V to 2.7 V		0.7	
			V_{CCI} = 2.7 V to 3.6 V		0.8	
V_{IH}	High-level input voltage	DIR and $\overline{OE}$ (referenced to V_{CCA})	V_{CCI} = 1.2 V to 1.95 V	V_{CCA} × 0.65		V
			V_{CCI} = 1.95 V to 2.7 V	1.6		
			V_{CCI} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	DIR and $\overline{OE}$ (referenced to V_{CCA})	V_{CCI} = 1.2 V to 1.95 V		V_{CCA} × 0.35	V
			V_{CCI} = 1.95 V to 2.7 V		0.7	
			V_{CCI} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage	Control Inputs		0	3.6	V
V_O	Output voltage[2]	Active state		0	V_{CCO}	V
		3-state		0	3.6	
I_{OH}	High-level output current		V_{CCO} = 1.2 V		–3	mA
			V_{CCO} = 1.4 V to 1.6 V		–6	
			V_{CCO} = 1.65 V to 1.95 V		–8	
			V_{CCO} = 2.3 V to 2.7 V		–9	
			V_{CCO} = 3 V to 3.6 V		–12	
I_{OL}	Low-level output current		V_{CCO} = 1.2 V		3	mA
			V_{CCO} = 1.4 V to 1.6 V		6	
			V_{CCO} = 1.65 V to 1.95 V		8	
			V_{CCO} = 2.3 V to 2.7 V		9	
			V_{CCO} = 3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.

7.4 Thermal Information

THERMAL METRIC[1]		SN74AVCH8T245			UNIT
		DGV (TVSOP)	PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	95.5	92	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	29.3	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	46.7	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	1.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.5	46.2	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage(1)	I_{OH} = –100 µA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V		V_{CCO} – 0.2			V
		I_{OH} = –3 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.2 V			0.95		
		I_{OH} = –6 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.4 V		1.05			
		I_{OH} = –8 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.65 V		1.2			
		I_{OH} = –9 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 2.3 V		1.75			
		I_{OH} = –12 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 3 V		2.3			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V				0.2	V
		I_{OL} = 3 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.2 V			0.15		
		I_{OL} = 6 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.4 V				0.35	
		I_{OL} = 8 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.65 V				0.45	
		I_{OL} = 9 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 2.3 V				0.55	
		I_{OL} = 12 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 3 V				0.7	
I_I	Control inputs	V_I = V_{CCA} or GND	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V			±0.025	±1	µA
I_{BHL}	Bus-hold low sustaining current(2)	V_I = 0.42 V	V_{CCA} = V_{CCB} = 1.2 V			25		µA
		V_I = 0.49 V	V_{CCA} = V_{CCB} = 1.4 V		15			
		V_I = 0.58 V	V_{CCA} = V_{CCB} = 1.65 V		25			
		V_I = 0.7 V	V_{CCA} = V_{CCB} = 2.3 V		45			
		V_I = 0.8 V	V_{CCA} = V_{CCB} = 3.3 V		100			
I_{BHH}	Bus-hold high sustaining current(3)	V_I = 0.78 V	V_{CCA} = V_{CCB} = 1.2 V			–25		µA
		V_I = 0.91 V	V_{CCA} = V_{CCB} = 1.4 V		–15			
		V_I = 1.07 V	V_{CCA} = V_{CCB} = 1.65 V		–25			
		V_I = 1.6 V	V_{CCA} = V_{CCB} = 2.3 V		–45			
		V_I = 2 V	V_{CCA} = V_{CCB} = 3.3 V		–100			
I_{BHLO}	Bus-hold low overdrive current(4)	V_I = 0 to V_{CC}	V_{CCA} = V_{CCB} = 1.2 V			50		µA
			V_{CCA} = V_{CCB} = 1.6 V		125			
			V_{CCA} = V_{CCB} = 1.95 V		200			
			V_{CCA} = V_{CCB} = 2.7 V		300			
			V_{CCA} = V_{CCB} = 3.6 V		500			
I_{BHHO}	Bus-hold high overdrive current(5)	V_I = 0 to V_{CC}	V_{CCA} = V_{CCB} = 1.2 V			–50		µA
			V_{CCA} = V_{CCB} = 1.6 V		–125			
			V_{CCA} = V_{CCB} = 1.95 V		–200			
			V_{CCA} = V_{CCB} = 2.7 V		–300			
			V_{CCA} = V_{CCB} = 3.6 V		–500			
I_{off}	Input/output power-off leakge current	V_I = 0 V to 3.6 V, V_O= 0 V to 3.6 V	V_{CCA} = 0 V, V_{CCB} = 0 V to 3.6 V	A Port		±0.1	±5	µA
			V_{CCA} = 0 V to 3.6 V, V_{CCB} = 0 V	B Port		±0.1	±5	

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(3) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(4) An external driver must source at least I_{BHLO} to switch this node from low to high.
(5) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Electrical Characteristics (continued)

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{OZ}	Off-state output current [1][6][7]	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$	$V_{CCA} = V_{CCB}$ = 3.6 V	A Port, B Port		±0.5	±5	μA
		$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE}$ = Don't Care	V_{CCA} = 0 V, V_{CCB} = 3.6 V	B Port			±5	
			V_{CCA} = 3.6 V, V_{CCB} = 0 V	A Port			±5	
I_{CCA}	Supply current A port[6]	$V_I = V_{CCI}$ or GND, I_O = 0	$V_{CCA} = V_{CCB}$ = 1.2 V to 3.6 V				8	μA
			V_{CCA} = 0 V, V_{CCB} = 3.6 V				–2	
			V_{CCA} = 3.6 V, V_{CCB} = 0 V				8	
I_{CCB}	Supply current B port[6]	$V_I = V_{CCI}$ or GND, I_O = 0	$V_{CCA} = V_{CCB}$ = 1.2 V to 3.6 V				8	μA
			V_{CCA} = 0 V, V_{CCB} = 3.6 V				8	
			V_{CCA} = 3.6 V, V_{CCB} = 0 V				–2	
I_{CCA} + I_{CCB}	Combined supply current[6]	$V_I = V_{CCI}$ or GND, I_O = 0	$V_{CCA} = V_{CCB}$ = 1.2 V to 3.6 V				16	μA
C_i	Input capacitance control pins	V_I = 3.3 V or GND	$V_{CCA} = V_{CCB}$ = 3.3 V			3.5	4.5	pF
C_{io}	Input/output capacitance a or b port	V_O = 3.3 V or GND	$V_{CCA} = V_{CCB}$ = 3.3 V			6	7	pF

(6) V_{CCI} is the V_{CC} associated with the input port.
(7) For I/O ports, the parameter I_{OZ} includes the input leakage current.

7.6 Switching Characteristics, V_{CCA} = 1.2 V

T_A = 25°C (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		3.1		ns
				V_{CCB} = 1.5 V		2.6		
				V_{CCB} = 1.8 V		2.5		
				V_{CCB} = 2.5 V		3		
				V_{CCB} = 3.3 V		3.5		
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		3.1		ns
				V_{CCB} = 1.5 V		2.7		
				V_{CCB} = 1.8 V		2.5		
				V_{CCB} = 2.5 V		2.4		
				V_{CCB} = 3.3 V		2.3		
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		5.3		ns
				V_{CCB} = 1.5 V		5.3		
				V_{CCB} = 1.8 V		5.3		
				V_{CCB} = 2.5 V		5.3		
				V_{CCB} = 3.3 V		5.3		
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		5.1		ns
				V_{CCB} = 1.5 V		4		
				V_{CCB} = 1.8 V		3.5		
				V_{CCB} = 2.5 V		3.2		
				V_{CCB} = 3.3 V		3.1		
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.8		ns
				V_{CCB} = 1.5 V		4.8		
				V_{CCB} = 1.8 V		4.8		
				V_{CCB} = 2.5 V		4.8		
				V_{CCB} = 3.3 V		4.8		
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.7		ns
				V_{CCB} = 1.5 V		4		
				V_{CCB} = 1.8 V		4.1		
				V_{CCB} = 2.5 V		4.3		
				V_{CCB} = 3.3 V		5.1		

7.7 Switching Characteristics, V_{CCA}= 1.5 V ± 0.1 V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.7		ns
				V_{CCB} = 1.5 V	0.5		5.4	
				V_{CCB} = 1.8 V	0.5		4.6	
				V_{CCB} = 2.5 V	0.5		4.9	
				V_{CCB} = 3.3 V	0.5		6.8	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.6		ns
				V_{CCB} = 1.5 V	0.5		5.4	
				V_{CCB} = 1.8 V	0.5		5.1	
				V_{CCB} = 2.5 V	0.5		4.7	
				V_{CCB} = 3.3 V	0.5		4.5	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		3.7		ns
				V_{CCB} = 1.5 V	1.1		8.7	
				V_{CCB} = 1.8 V	1.1		8.7	
				V_{CCB} = 2.5 V	1.1		8.7	
				V_{CCB} = 3.3 V	1.1		8.7	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.8		ns
				V_{CCB} = 1.5 V	1.1		7.6	
				V_{CCB} = 1.8 V	1.1		7.1	
				V_{CCB} = 2.5 V	1.1		5.6	
				V_{CCB} = 3.3 V	1.1		5.2	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		3.1		ns
				V_{CCB} = 1.5 V	0.5		8.6	
				V_{CCB} = 1.8 V	0.5		8.6	
				V_{CCB} = 2.5 V	0.5		8.6	
				V_{CCB} = 3.3 V	0.5		8.6	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.1		ns
				V_{CCB} = 1.5 V	0.5		8.4	
				V_{CCB} = 1.8 V	0.5		7.6	
				V_{CCB} = 2.5 V	0.5		7.2	
				V_{CCB} = 3.3 V	0.5		7.8	

7.8 Switching Characteristics, V_{CCA}= 1.8 V ± 0.15 V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.5		ns
				V_{CCB} = 1.5 V	0.5		5.1	
				V_{CCB} = 1.8 V	0.5		4.4	
				V_{CCB} = 2.5 V	0.5		4	
				V_{CCB} = 3.3 V	0.5		3.9	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.5		ns
				V_{CCB} = 1.5 V	0.5		4.6	
				V_{CCB} = 1.8 V	0.5		4.4	
				V_{CCB} = 2.5 V	0.5		3.9	
				V_{CCB} = 3.3 V	0.5		3.7	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		3		ns
				V_{CCB} = 1.5 V	1		6.8	
				V_{CCB} = 1.8 V	1		6.8	
				V_{CCB} = 2.5 V	1		6.8	
				V_{CCB} = 3.3 V	1		6.8	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.6		ns
				V_{CCB} = 1.5 V	1.1		8.2	
				V_{CCB} = 1.8 V	1		6.7	
				V_{CCB} = 2.5 V	0.5		5.1	
				V_{CCB} = 3.3 V	0.5		4.5	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.8		ns
				V_{CCB} = 1.5 V	0.5		7.1	
				V_{CCB} = 1.8 V	0.5		7.1	
				V_{CCB} = 2.5 V	0.5		7.1	
				V_{CCB} = 3.3 V	0.5		7.1	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.9		ns
				V_{CCB} = 1.5 V	0.5		7.8	
				V_{CCB} = 1.8 V	0.5		6.9	
				V_{CCB} = 2.5 V	0.5		6	
				V_{CCB} = 3.3 V	0.5		5.8	

7.9 Switching Characteristics, V_{CCA}= 2.5 V ± 0.2 V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.4		ns
				V_{CCB} = 1.5 V	0.5		4.7	
				V_{CCB} = 1.8 V	0.5		3.9	
				V_{CCB} = 2.5 V	0.5		3.1	
				V_{CCB} = 3.3 V	0.5		2.8	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		3		ns
				V_{CCB} = 1.5 V	0.5		4.9	
				V_{CCB} = 1.8 V	0.5		4	
				V_{CCB} = 2.5 V	0.5		3.1	
				V_{CCB} = 3.3 V	0.5		2.9	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.2		ns
				V_{CCB} = 1.5 V	0.5		4.8	
				V_{CCB} = 1.8 V	0.5		4.8	
				V_{CCB} = 2.5 V	0.5		4.8	
				V_{CCB} = 3.3 V	0.5		4.8	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
				V_{CCB} = 1.5 V	1.1		7.9	
				V_{CCB} = 1.8 V	0.5		6.4	
				V_{CCB} = 2.5 V	0.5		4.6	
				V_{CCB} = 3.3 V	0.5		4	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.8		ns
				V_{CCB} = 1.5 V	0.5		5.1	
				V_{CCB} = 1.8 V	0.5		5.1	
				V_{CCB} = 2.5 V	0.5		5.1	
				V_{CCB} = 3.3 V	0.5		5.1	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.6		ns
				V_{CCB} = 1.5 V	0.5		7.1	
				V_{CCB} = 1.8 V	0.5		6.3	
				V_{CCB} = 2.5 V	0.5		5.1	
				V_{CCB} = 3.3 V	0.5		3.9	

7.10 Switching Characteristics, V_{CCA} = 3.3 V ± 0.3 V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.3		ns
				V_{CCB} = 1.5 V	0.5		4.5	
				V_{CCB} = 1.8 V	0.5		3.7	
				V_{CCB} = 2.5 V	0.5		2.9	
				V_{CCB} = 3.3 V	0.5		2.5	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		3.5		ns
				V_{CCB} = 1.5 V	0.5		6.8	
				V_{CCB} = 1.8 V	0.5		3.9	
				V_{CCB} = 2.5 V	0.5		2.8	
				V_{CCB} = 3.3 V	0.5		2.5	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		2		ns
				V_{CCB} = 1.5 V	0.5		4	
				V_{CCB} = 1.8 V	0.5		4	
				V_{CCB} = 2.5 V	0.5		4	
				V_{CCB} = 3.3 V	0.5		4	
t_{PZH}, t_{PZL}	Enable time: to high level and to low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
				V_{CCB} = 1.5 V	1.1		7.8	
				V_{CCB} = 1.8 V	0.5		6.2	
				V_{CCB} = 2.5 V	0.5		4.5	
				V_{CCB} = 3.3 V	0.5		3.9	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.7		ns
				V_{CCB} = 1.5 V	0.5		4	
				V_{CCB} = 1.8 V	0.5		4	
				V_{CCB} = 2.5 V	0.5		4	
				V_{CCB} = 3.3 V	0.5		4	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.4		ns
				V_{CCB} = 1.5 V	0.5		6.9	
				V_{CCB} = 1.8 V	0.5		6	
				V_{CCB} = 2.5 V	0.5		4.8	
				V_{CCB} = 3.3 V	0.5		4.2	

7.11 Operating Characteristics

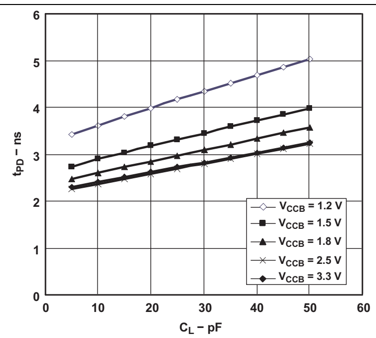
T_A= 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		TYP	UNIT
C_{pdA}	Power dissipation capacitance per transceiver(1) port A - outputs enabled	A	B	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	pF
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	
	Power dissipation capacitance per transceiver(1) port A - outputs disabled	A	B	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	
	Power dissipation capacitance per transceiver(1) port A - outputs enabled	B	A	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	
					V_{CCA} = V_{CCB} = 1.5 V	12	
					V_{CCA} = V_{CCB} = 1.8 V	12	
					V_{CCA} = V_{CCB} = 2.5 V	13	
					V_{CCA} = V_{CCB} = 3.3 V	14	
	Power dissipation capacitance per transceiver(1) port A - outputs disabled	B	A	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	
C_{pdB}	Power dissipation capacitance per transceiver(1) port B - outputs enabled	A	B	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	pF
					V_{CCA} = V_{CCB} = 1.5 V	12	
					V_{CCA} = V_{CCB} = 1.8 V	12	
					V_{CCA} = V_{CCB} = 2.5 V	13	
					V_{CCA} = V_{CCB} = 3.3 V	14	
	Power dissipation capacitance per transceiver(1) port B - outputs disabled	A	B	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	
	Power dissipation capacitance per transceiver(1) port B - outputs enabled	B	A	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	
	Power dissipation capacitance per transceiver(1) port B - outputs disabled	B	A	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
					V_{CCA} = V_{CCB} = 1.5 V	1	
					V_{CCA} = V_{CCB} = 1.8 V	1	
					V_{CCA} = V_{CCB} = 2.5 V	1	
					V_{CCA} = V_{CCB} = 3.3 V	1	

(1) See to TI application report, *CMOS Power Consumption and Cpd Calculation* (SCAA035).

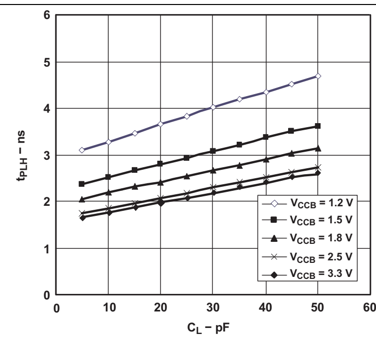
7.12 Typical Characteristics

T_A = 25°C



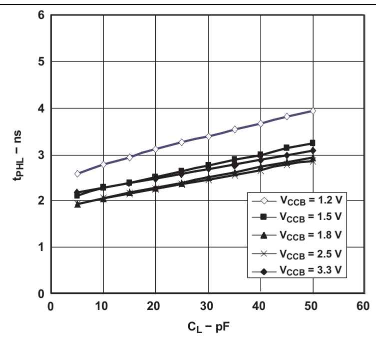
V_{CCA} = 1.2 V

Figure 1. Typical Propagation Delay (A to B) vs Load Capacitance



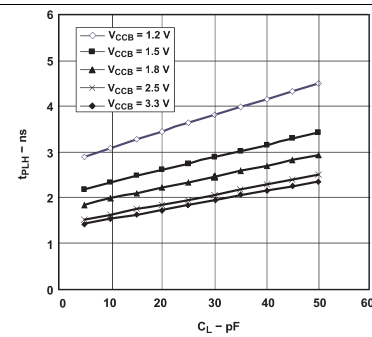
V_{CCA} = 1.5 V

Figure 2. Typical Propagation Delay (A to B) vs Load Capacitance



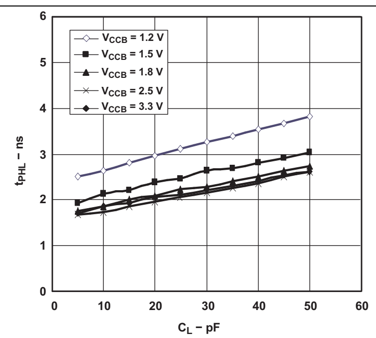
V_{CCA} = 1.5 V

Figure 3. Typical Propagation Delay (A to B) vs Load Capacitance



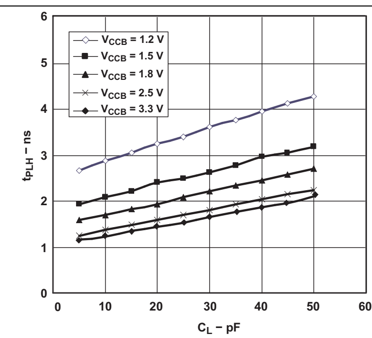
V_{CCA} = 1.8 V

Figure 4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8 V

Figure 5. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 2.5 V

Figure 6. Typical Propagation Delay (A to B) vs Load Capacitance

Typical Characteristics (continued)

$T_A = 25°C$

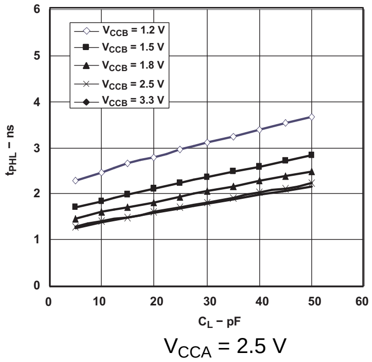


Figure 7. Typical Propagation Delay (A to B) vs Load Capacitance

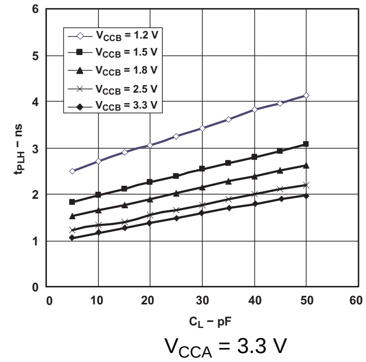


Figure 8. Typical Propagation Delay (A to B) vs Load Capacitance

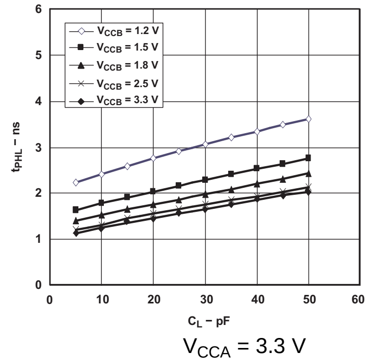
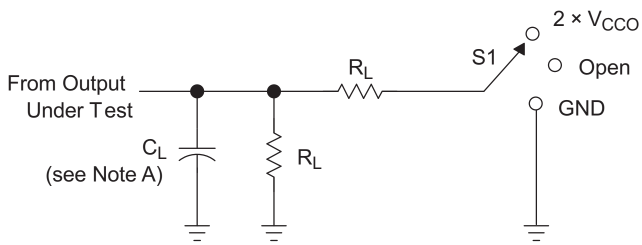


Figure 9. Typical Propagation Delay (A to B) vs Load Capacitance

8 Parameter Measurement Information

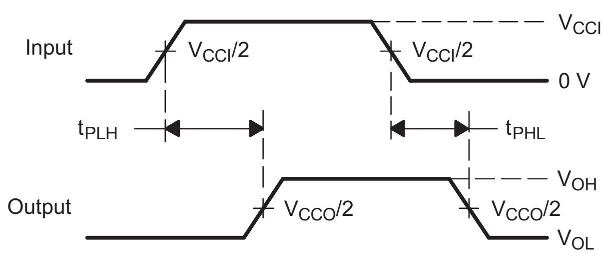


LOAD CIRCUIT

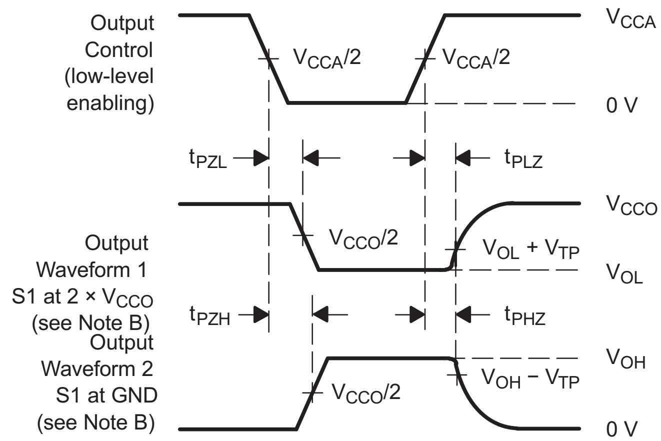
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kW	0.1 V
1.5 V ± 0.1 V	15 pF	2 kW	0.1 V
1.8 V ± 0.15 V	15 pF	2 kW	0.15 V
2.5 V ± 0.2 V	15 pF	2 kW	0.15 V
3.3 V ± 0.3 V	15 pF	2 kW	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 10. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74AVCH8T245 is an 8-bit, dual supply noninverting bidirectional voltage level translator. Pins A1 through A4, and the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA}, while pins B1 through B4 are referenced to V_{CCB}. Both the A port and B port can accept I/O voltages ranging from 1.2 V to 3.6 V. With $\overline{OE}$ set to low, a high on DIR allows data transmission from Port A to Port B, and a low on DIR allows data transmission from Port B to Port A. When $\overline{OE}$ is set to high, both Port A and Port B outputs are in the high-impedance state. See *AVC Logic Family Technology and Application* (SCEA006).

9.2 Functional Block Diagram

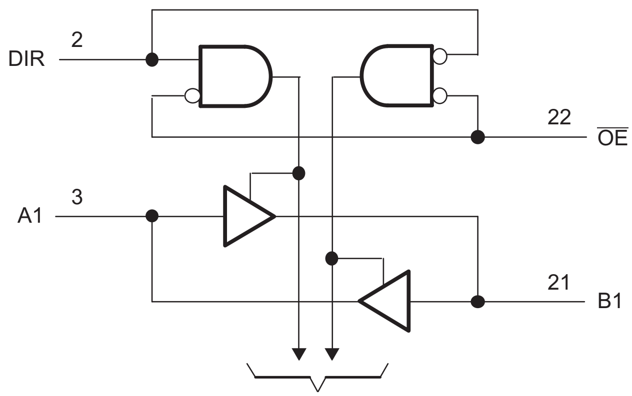


Figure 11. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V, making the device suitable for translating between any of the low voltage nodes: 1.2 V, 1.8 V, 2.5 V, and 3.3 V.

Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

9.3.2 Supports High-Speed Translation

SN74AVCH8T245 can support high data rate applications, which can be calculated from the maximum propagation delay. This is also dependent on output load. The translated signal data rate can be up to 320 Mbps when both V_{CCA} and V_{CCB} are at least 1.8 V.

9.3.3 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the SN74AVCH8T245 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

9.3.4 Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. See *Bus-Hold Circuit* (SCLA015).

9.3.5 V_{CC} Isolation Feature

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports will be in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This prevents false logic levels from being presented to either bus.

9.4 Device Functional Modes

Table 2 lists the functional modes of the SN74AVCH8T245.

Table 2. Function Table (Each 8-Bit Section)

CONTROL INPUTS[(1)]		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVCH8T245 device is ideal for data transmission which direction is different with each channel. The maximum data rate can be up to 320 Mbps when device voltage power supply is more than 1.8 V.

10.2 Typical Application

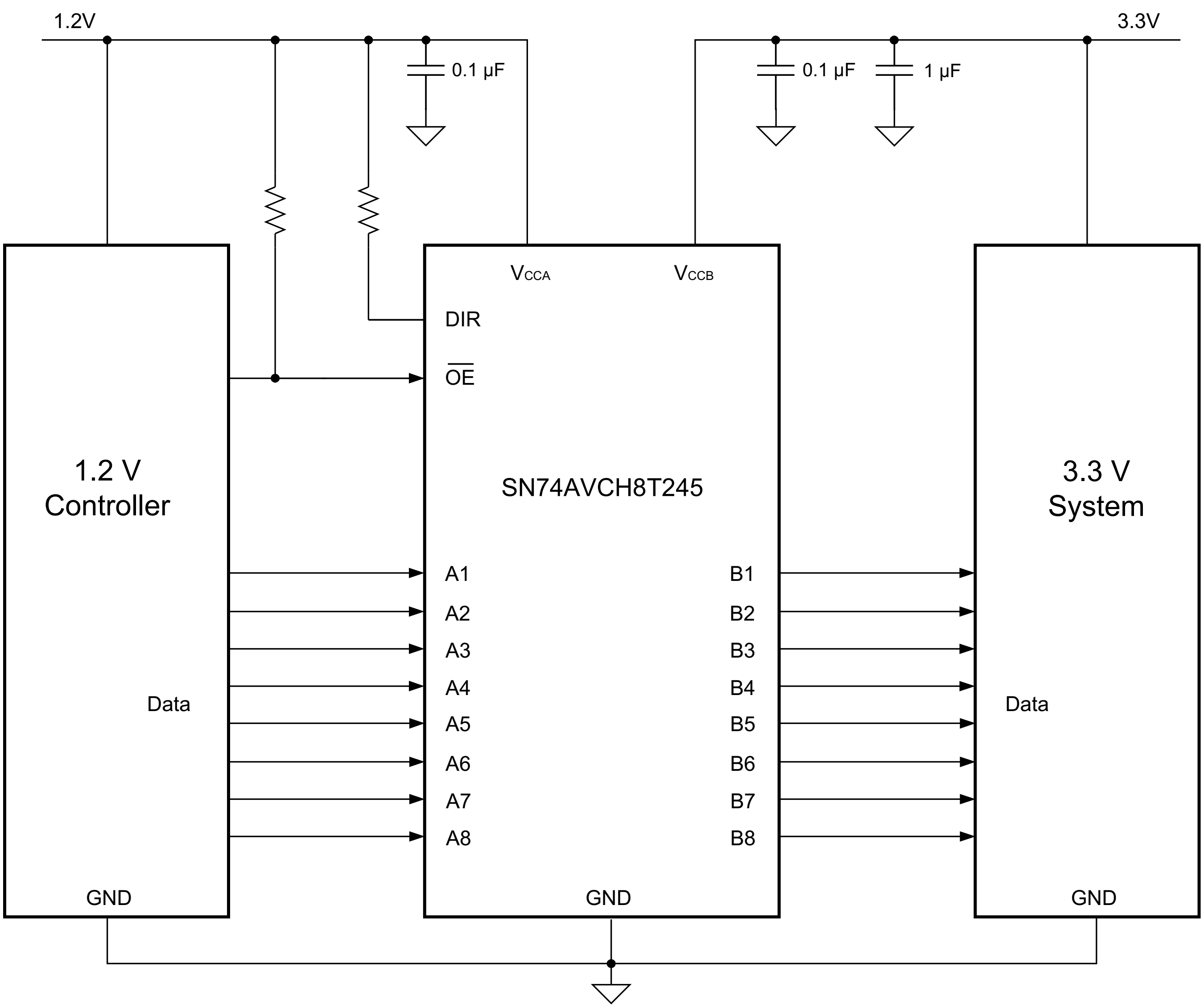


Figure 12. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage	1.2 V to 3.6 V
Output voltage	1.2 V to 3.6 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVCH8T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVCH8T245 device is driving to determine the output voltage range.

10.2.3 Application Curves

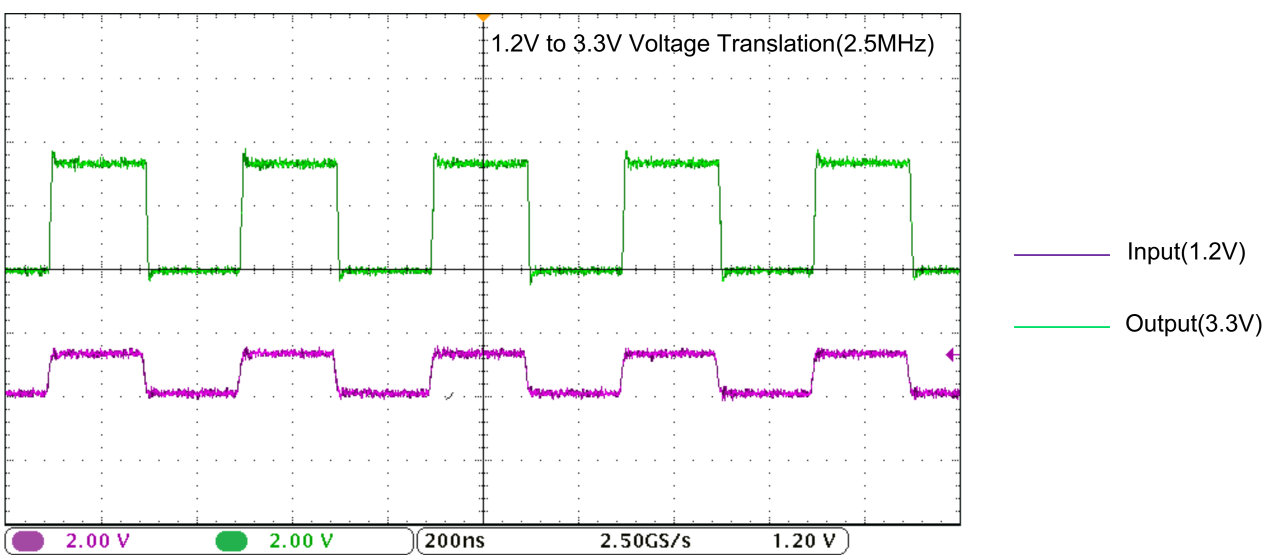


Figure 13. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The output-enable ($\overline{OE}$) input circuit is designed so that it is referenced to V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

V_{CCA} or V_{CCB} can be powered up first. If the SN74LVCH8T245 is powered up in a permanently enabled state (for example $\overline{OE}$ is always kept low), pullup resistors are recommended at the input. This ensures proper, glitch-free, power-up. See *Designing with SN4LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters* (SLVA746). In addition, the $\overline{OE}$ pin may be shorted to GND if the application does not require use of the high-impedance state at any time.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, TI recommends following the common printed-circuit board layout guidelines.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

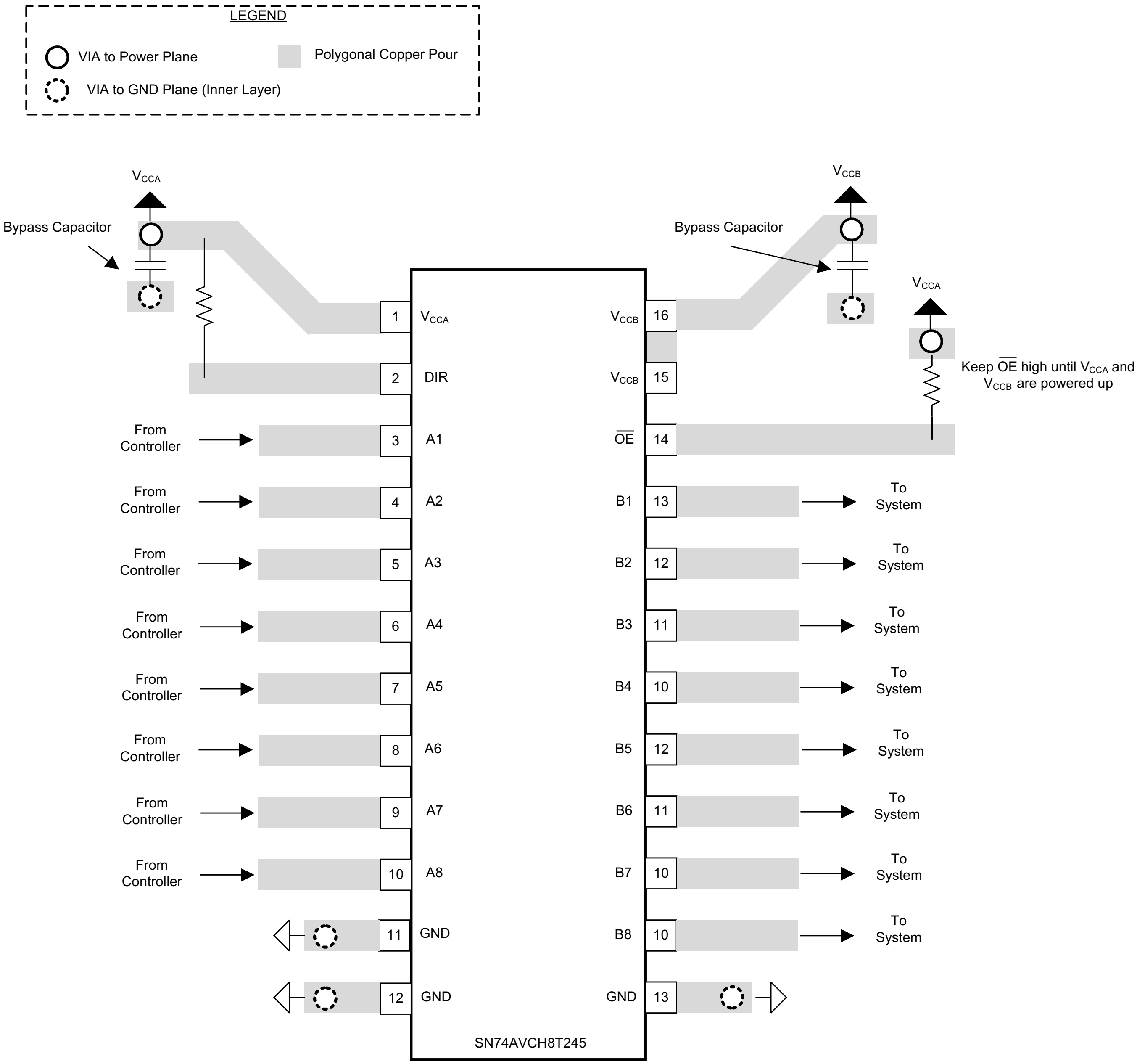


Figure 14. SN74AVCH8T245 Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*, SLVA746
- *Bus-Hold Circuit*, SCLA015
- *AVC Logic Family Technology and Applications*, SCEA006
- *CMOS Power Consumption and Cpd Calculation*, SCAA035

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCH8T245PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
74AVCH8T245RHLRG4	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WP245	Samples
SN74AVCH8T245DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245RHLR	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WP245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

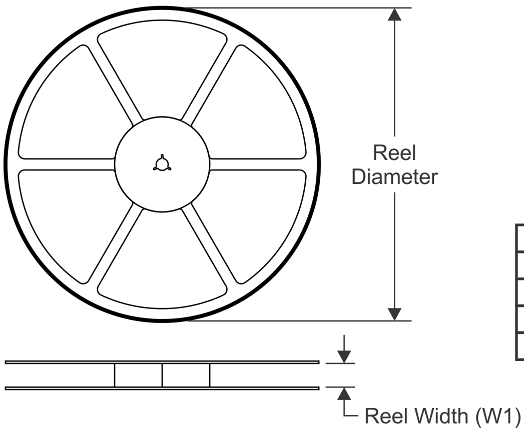
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

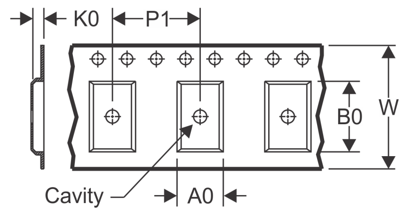
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

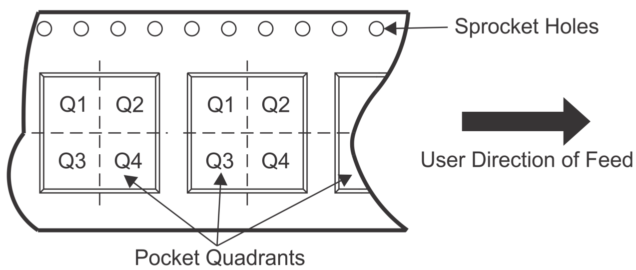


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

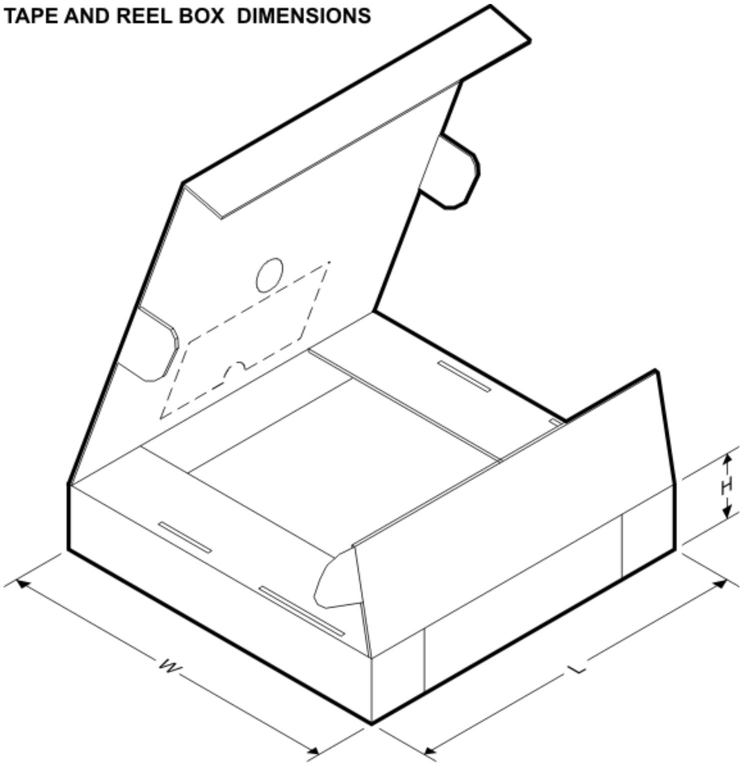
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AVCH8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

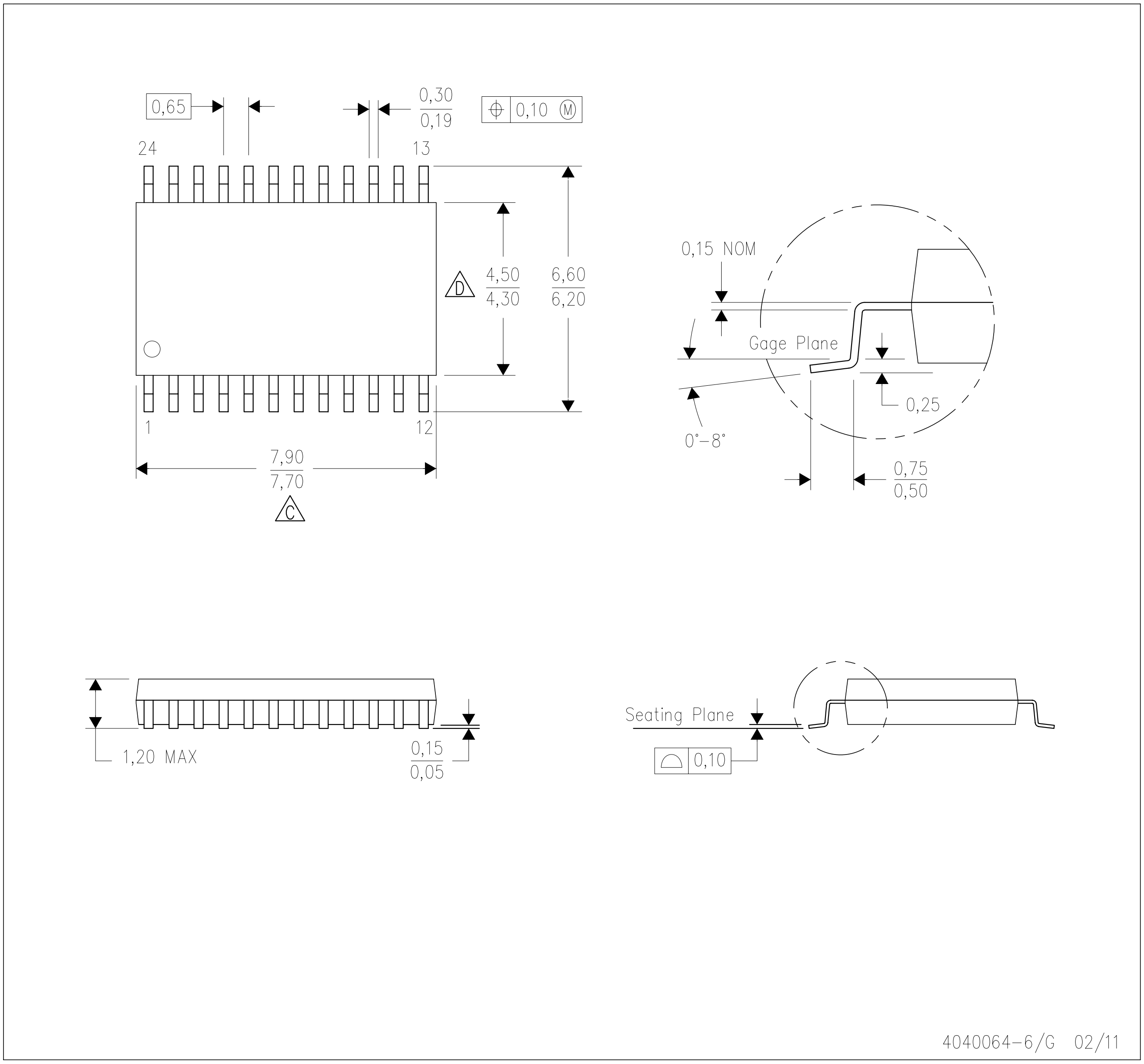
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

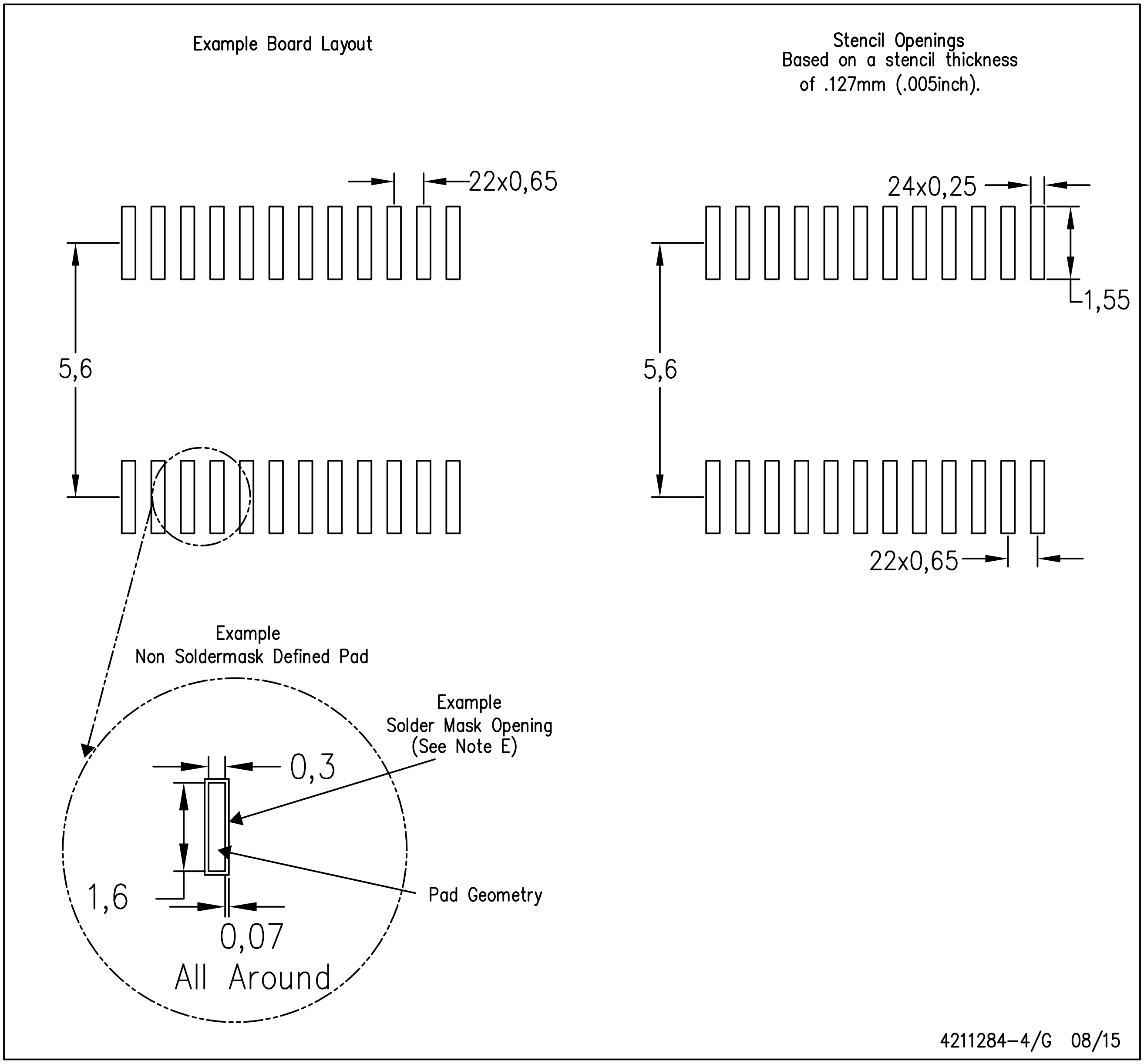
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH8T245DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74AVCH8T245PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74AVCH8T245RHLR	VQFN	RHL	24	1000	210.0	185.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



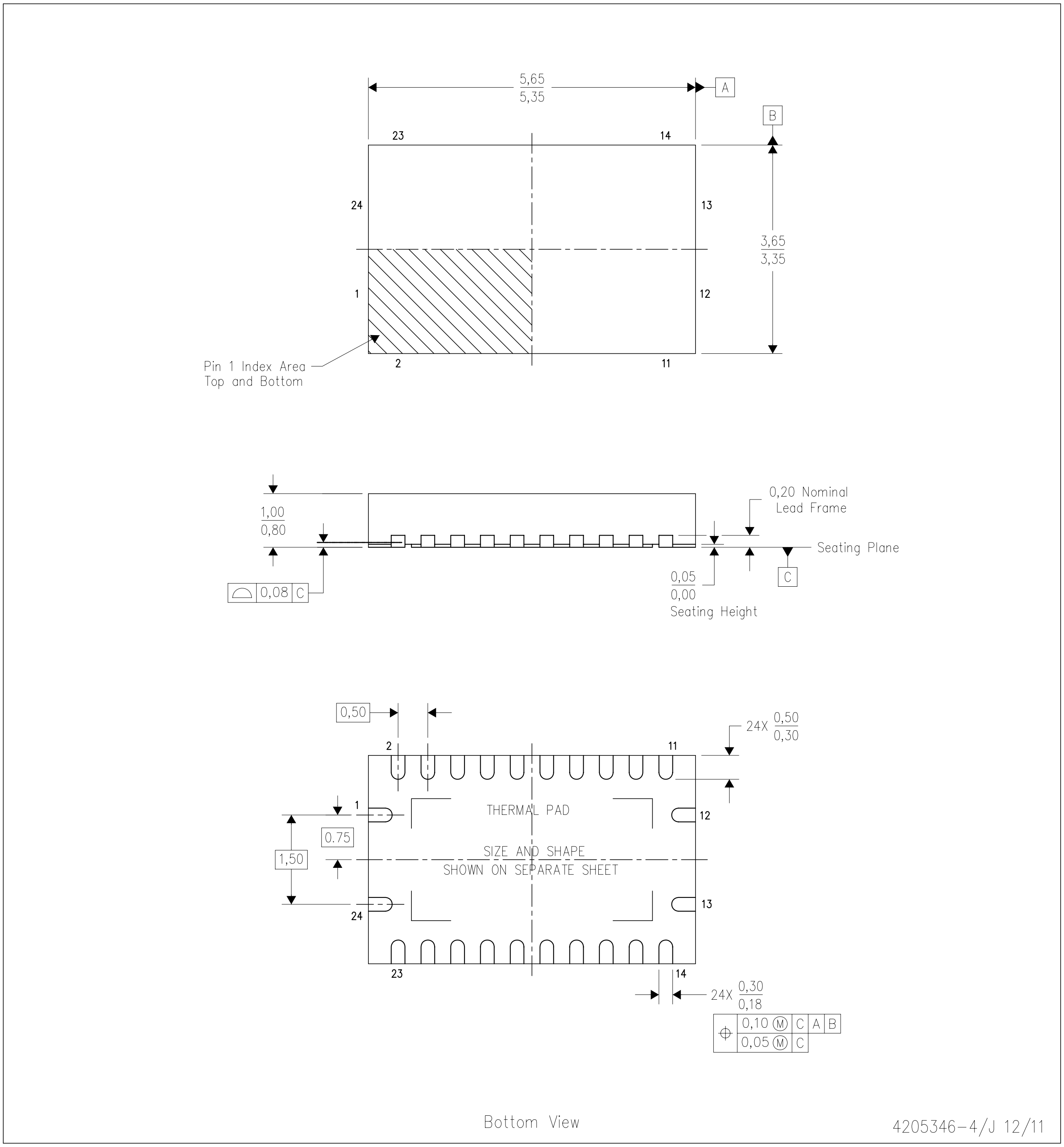
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. JEDEC MO–241 package registration pending.

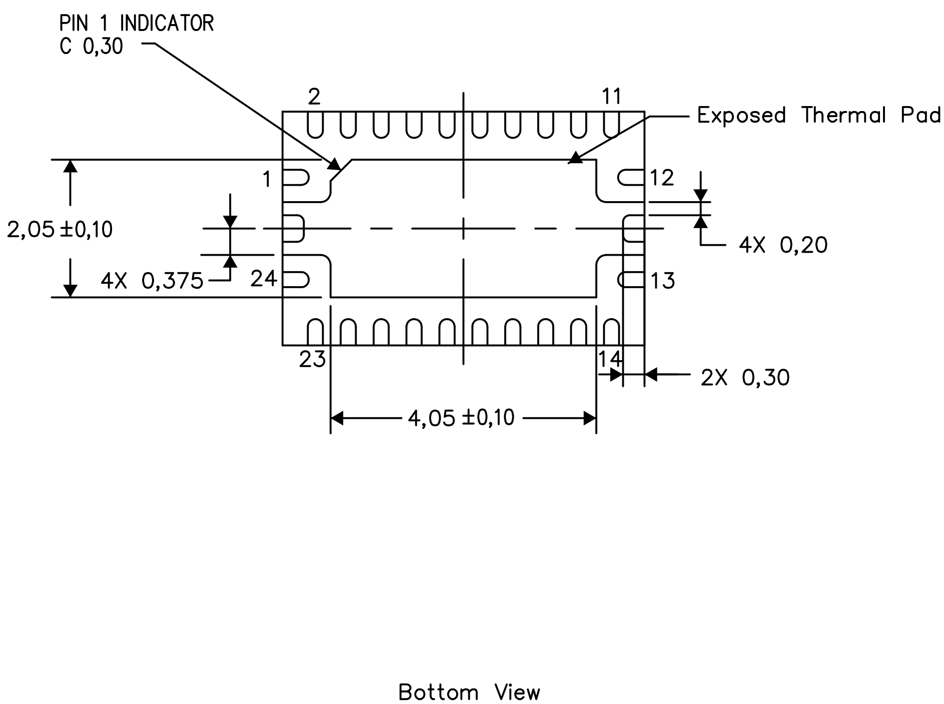
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

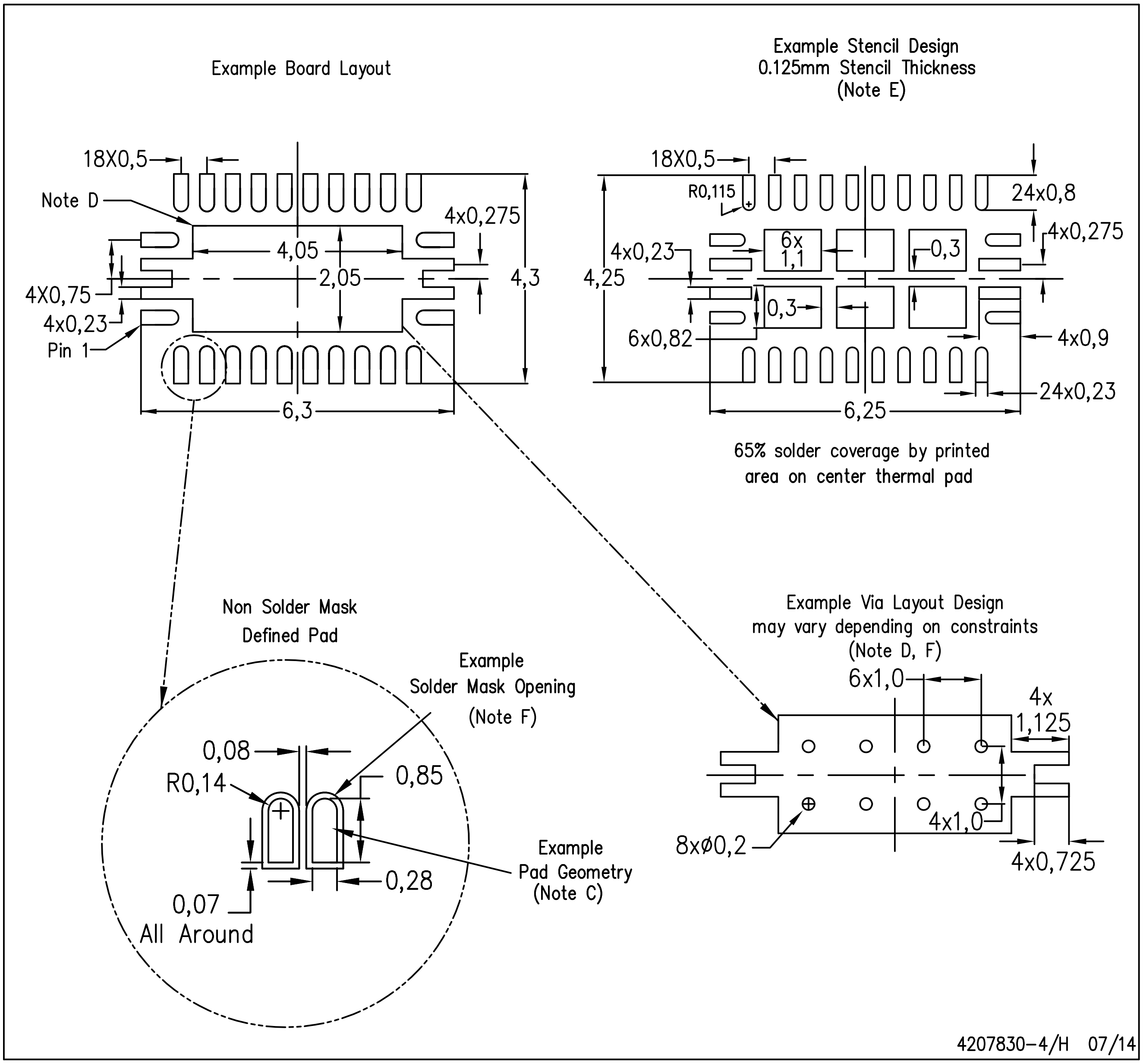


Exposed Thermal Pad Dimensions

4206363-4/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265