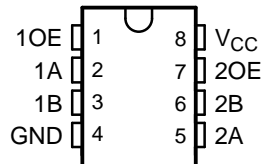


## FEATURES

- Undershoot Protection for OFF Isolation on A and B Ports up to -2 V
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typ)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 5$  pF Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3 \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, ClassII
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating

D, DGK, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74CBT3305C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active undershoot-protection circuitry on the A and B ports of the device provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3305C is organized as two 1-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube	SN74CBT3305CD	CU305C
		Tape and reel	SN74CBT3305CDR	
	VSSOP – DGK	Tape and reel	SN74CBT3305CDGKR	SNR
	TSSOP – PW	Tube	SN74CBT3305CPW	CU305C
		Tape and reel	SN74CBT3305CPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**SN74CBT3305C**  
**DUAL FET BUS SWITCH**  
**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

SCDS125B–SEPTEMBER 2003–REVISED AUGUST 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

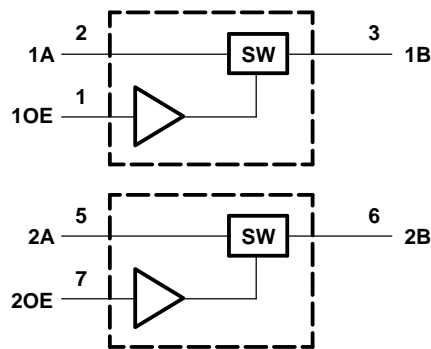
This device is fully specified for partial-power-down application using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

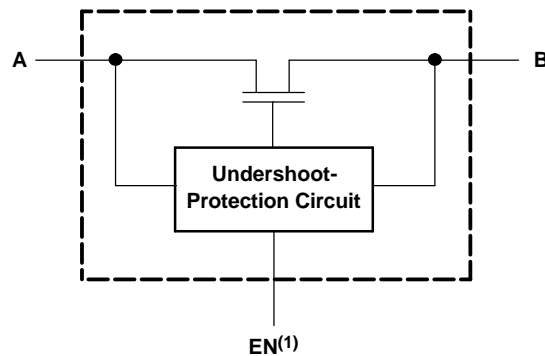
**FUNCTION TABLE**  
**(EACH BUS SWITCH)**

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)**



(1) EN is the internal enable signal applied to the switch.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current		-50	mA
		$V_{IN} < 0$		
$I_{I/OK}$	I/O port clamp current		-50	mA
		$V_{I/O} < 0$		
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>	D package		97
		DGK package		179
		PW package		149
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2	5.5	V
$V_{IL}$	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CBT3305C

## DUAL FET BUS SWITCH

### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS125B–SEPTEMBER 2003–REVISED AUGUST 2005

#### Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IK}$	Control inputs	$V_{CC} = 4.5\text{ V}$ ,	$I_{IN} = -18\text{ mA}$				-1.8	V	
$V_{IKU}$	Data inputs	$V_{CC} = 5\text{ V}$ ,	0 mA > $I_I \geq -50\text{ mA}$ , $V_{IN} = V_{CC}$ or GND, Switch OFF				-2	V	
$I_{IN}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{IN} = V_{CC}$ or GND				$\pm 1$	$\mu\text{A}$	
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$ to 5.5 V, $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND				$\pm 10$	$\mu\text{A}$	
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0$ to 5.5 V, $V_I = 0$				10	$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_{IO} = 0$ , $V_{IN} = V_{CC}$ or GND, Switch ON or OFF				3	$\mu\text{A}$	
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND				2.5	mA	
$C_{in}$	Control inputs	$V_{IN} = 3\text{ V}$ or 0					3	pF	
$C_{io(OFF)}$		$V_{IO} = 3\text{ V}$ or 0,	Switch OFF, $V_{IN} = V_{CC}$ or GND				5	pF	
$C_{io(ON)}$		$V_{IO} = 3\text{ V}$ or 0,	Switch ON, $V_{IN} = V_{CC}$ or GND				12.5	pF	
$r_{on}$ <sup>(5)</sup>		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ ,	$I_O = -15\text{ mA}$			8	12	$\Omega$
			$V_I = 0$	$I_O = 64\text{ mA}$			3	6	
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 30\text{ mA}$			3	6	
			$V_I = 2.4\text{ V}$ ,	$I_O = -15\text{ mA}$			5	10	

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND

(5) Measured by the voltage drop between the A and B terminals at the indicate current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

#### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A	0.24		0.15		ns
$t_{en}$	OE	A or B	4.4		1.5	4.1	ns
$t_{dis}$	OE	A or B	5.1		1.5	4.8	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

#### Undershoot Characteristics

See Figure 1 and Figure 2

PARAMETER	TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5\text{ V}$ ,	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

(1) All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

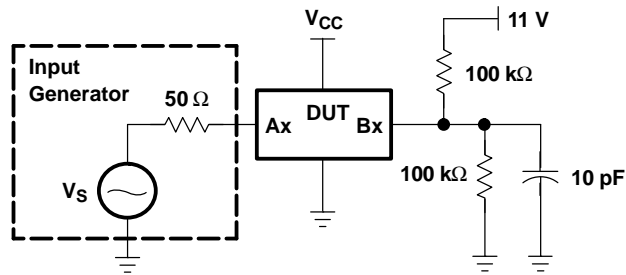


Figure 1. Device Test Setup

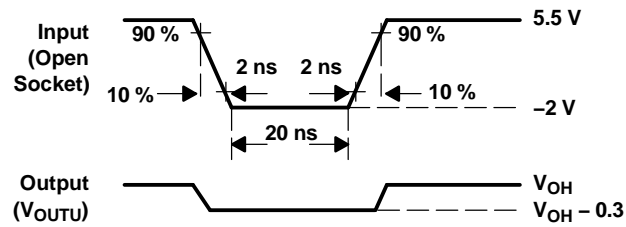
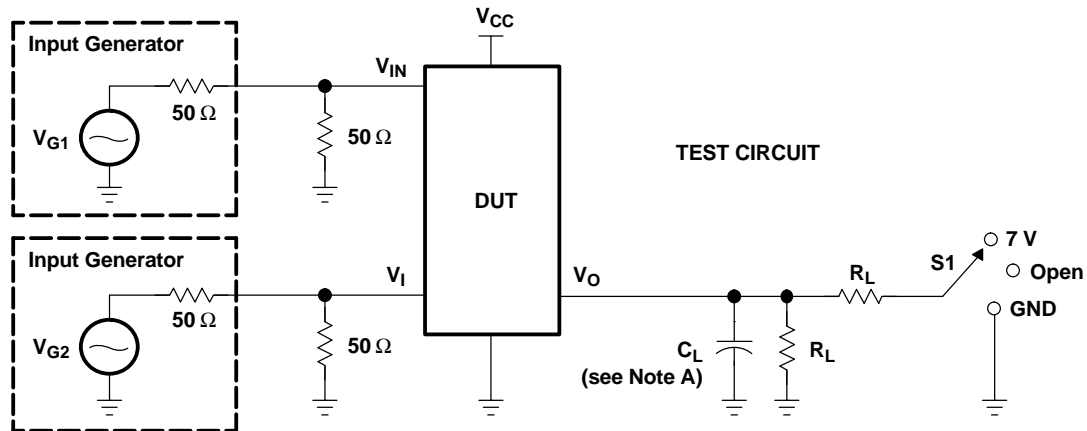
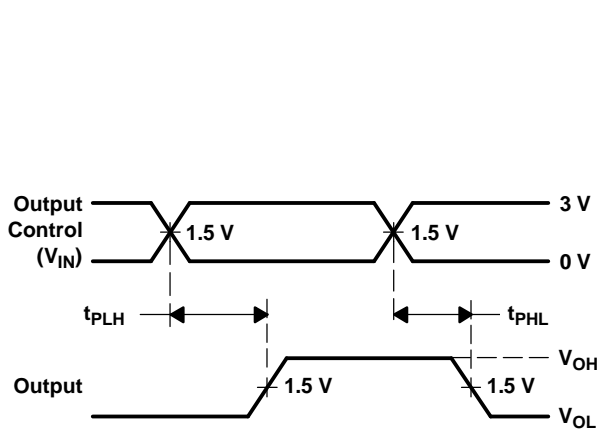


Figure 2. Transient Input Voltage ( $V_I$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

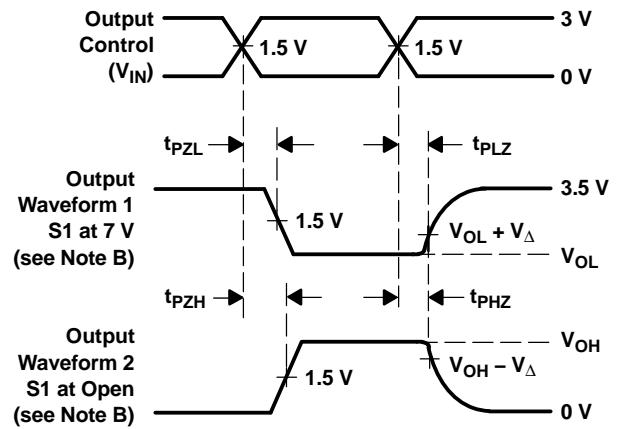
PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
	4 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub>	50 pF	0.3 V
	4 V	Open	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES (t<sub>pd(s)</sub>)



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3305CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C	<a href="#">Samples</a>
SN74CBT3305CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C	<a href="#">Samples</a>
SN74CBT3305CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C	<a href="#">Samples</a>
SN74CBT3305CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C	<a href="#">Samples</a>
SN74CBT3305CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU305C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3305CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3305CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3305CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3305CDR	SOIC	D	8	2500	340.5	338.1	20.6
SN74CBT3305CDR	SOIC	D	8	2500	367.0	367.0	35.0
SN74CBT3305CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

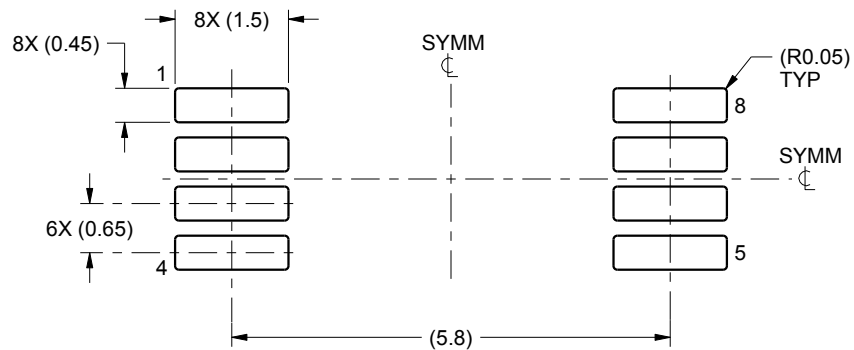


# EXAMPLE BOARD LAYOUT

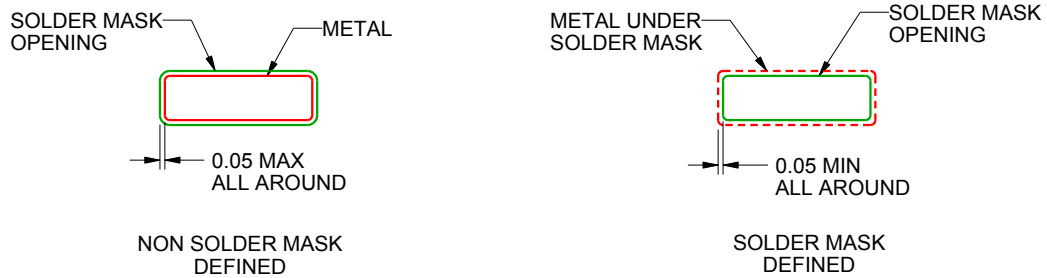
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

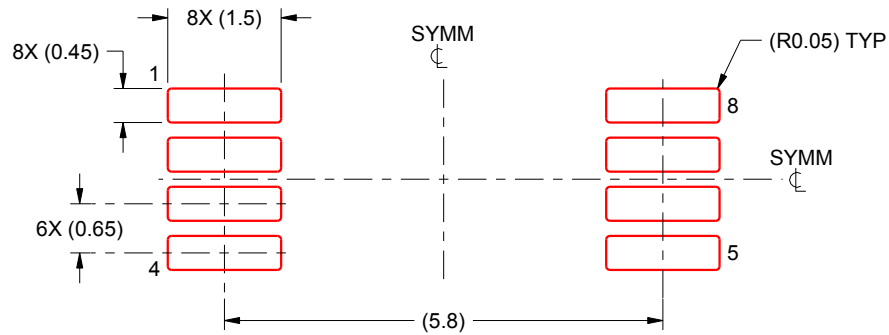
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

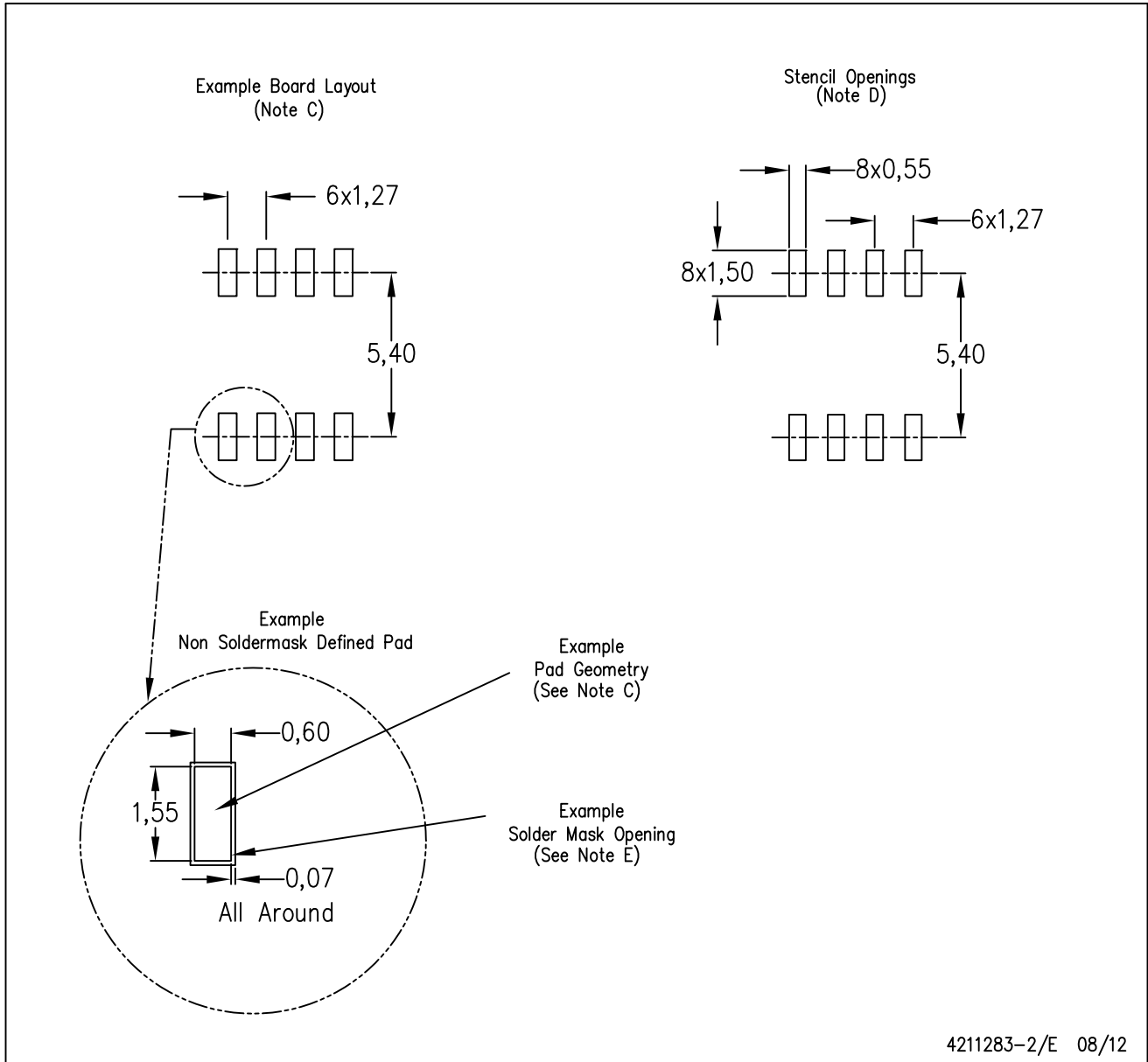
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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