SNx4CBT3383 10-Bit Bus-Exchange Switch

1 Features

- High-Bandwidth Data Path (Up to 200 MHz)
- Low and Flat ON-State Resistance (r_{ON}) Characteristics Over Operating Range (r_{ON} = 5 Ω Typical)
- Control Inputs Can Be Driven by TTL or 5-V and 3.3-V CMOS Outputs
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input and Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 6 pF Typical)
- V_{CC} Operating Range From 4.5 V to 5 V
- Low Power Consumption (I_{CC} = 50 µA Maximum)

2 Applications

- Enterprise Servers
- Ethernet Switches
- Routers
- Servers
- Industrial PCs

3 Description

The SN74CBT3383 and SN54CBT3383 devices provide ten bits of high-speed TTL-compatible bus switching or exchanging. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The devices operate as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when $\overline{BX}$ is high. The switches are connected when $\overline{BE}$ is low.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBT3383DB	SSOP (24)	8.40 mm × 5.30 mm
SN74CBT3383DBQ	SSOP (24)	8.65 mm × 3.90 mm
SN74CBT3383DW	SOIC (24)	15.40 mm × 7.50 mm
SN74CBT3383PW	TSSOP (24)	7.80 mm × 4.40 mm
SNJ54CBT3383JT	CDIP (24)	32.00 mm × 6.92 mm
SN54CBT3383W	CFP (24)	14.35 × 9.08 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

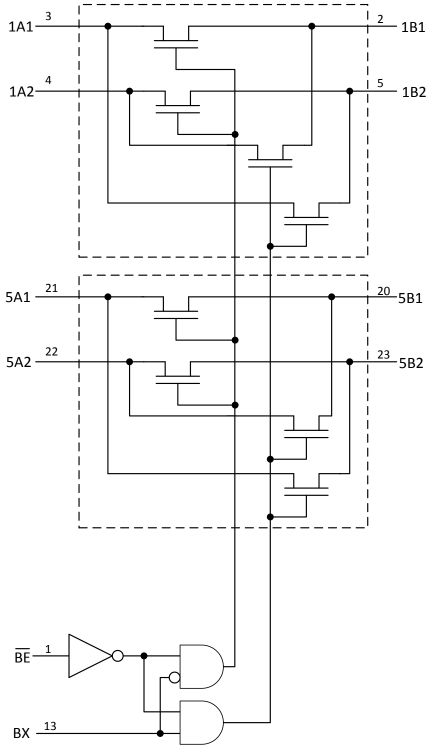


Table of Contents

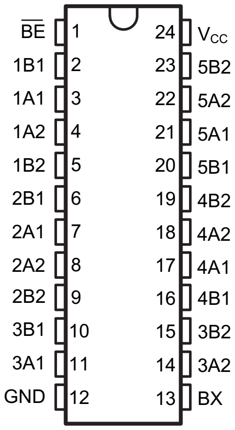
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (July 2004) to Revision P	Page
• Added *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information*.	1

5 Pin Configuration and Functions

DB, DBQ, DW, JT, W, or PW Package
24-Pin SSOP, SOIC, CDIP, CFP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{BE}$	I	Active-low input enable pin
2	1B1	I/O	Transceiver I/O pin
3	1A1	I/O	Transceiver I/O pin
4	1A2	I/O	Transceiver I/O pin
5	1B2	I/O	Transceiver I/O pin
6	2B1	I/O	Transceiver I/O pin
7	2A1	I/O	Transceiver I/O pin
8	2A2	I/O	Transceiver I/O pin
9	2B2	I/O	Transceiver I/O pin
10	3B1	I/O	Transceiver I/O pin
11	3A1	I/O	Transceiver I/O pin
12	GND	—	Ground
13	BX	I	Output select pin
14	3A2	I/O	Transceiver I/O pin
15	3B2	I/O	Transceiver I/O pin
16	4B1	I/O	Transceiver I/O pin
17	4A1	I/O	Transceiver I/O pin
18	4A2	I/O	Transceiver I/O pin
19	4B2	I/O	Transceiver I/O pin
20	5B1	I/O	Transceiver I/O pin
21	5A1	I/O	Transceiver I/O pin
22	5A2	I/O	Transceiver I/O pin
23	5B2	I/O	Transceiver I/O pin
24	V_{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage[2]	–0.5	7	V
I_O	Continuos channel current		128	mA
I_{IK}	Input clamp current ($V_{I/O}$<0)		–50	mA
T_J	Junction temperature	–65	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	SN74CBT3383	0	70.0	°C
		SN54CBT3383	–55.0	125.0	

6.4 Thermal Information

THERMAL METRIC[1]		SN74CBT3383				UNIT
		DB (SSOP)	DBQ (SSOP)	DW (SOIC)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.0	61.0	46.0	88.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	22.1	19.9	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.0	-	19.33	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = –18 mA						–1.2	V
I_I		V_{CC} = 5.5 V, V_I = 5.5 V or GND		SN54CBT3383				±5	µA
				SN74CBT3383				±1	
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND						50	µA
ΔI_{CC}(2)	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND						2.5	mA
C_i	Control inputs	V_I = 3 V or 0		SN74CBT3383			3		pF
		V_I = 2.5 V		SN54CBT3383				5	
$C_{io(OFF)}$		V_O = 3 V or 0, $\overline{BE}$ = V_{CC}		SN74CBT3383			6		pF
		V_O = 2.5 V, $\overline{BE}$ = V_{CC}		SN54CBT3383				6	
r_{on}(3)		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA	SN54CBT3383		5	9.2	Ω
					SN74CBT3383		5	7	
				I_I = 30 mA	SN74CBT3383		5	7	
			V_I = 2.4 V, I_I = 15 mA	SN54CBT3383			10	17	
				SN74CBT3383			10	15	

(1) Typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}(1)	A or B	B or A	SN54CBT3383		1.5	ns
			SN74CBT3383		0.25	
t_{pd}	BX	A or B	SN54CBT3383	1	10.2	ns
			SN74CBT3383	1	9.2	
t_{en}	$\overline{BE}$	A or B	SN54CBT3383	1	10.8	ns
			SN74CBT3383	1	8.6	
t_{dis}	$\overline{BE}$	A or B	SN54CBT3383	1	8.2	ns
			SN74CBT3383	1	7.5	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

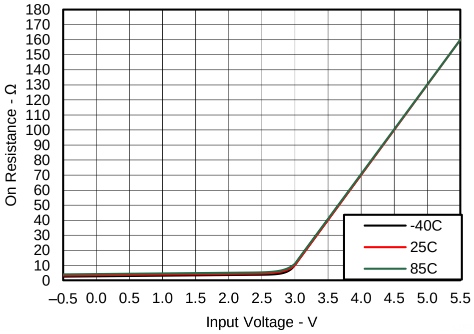
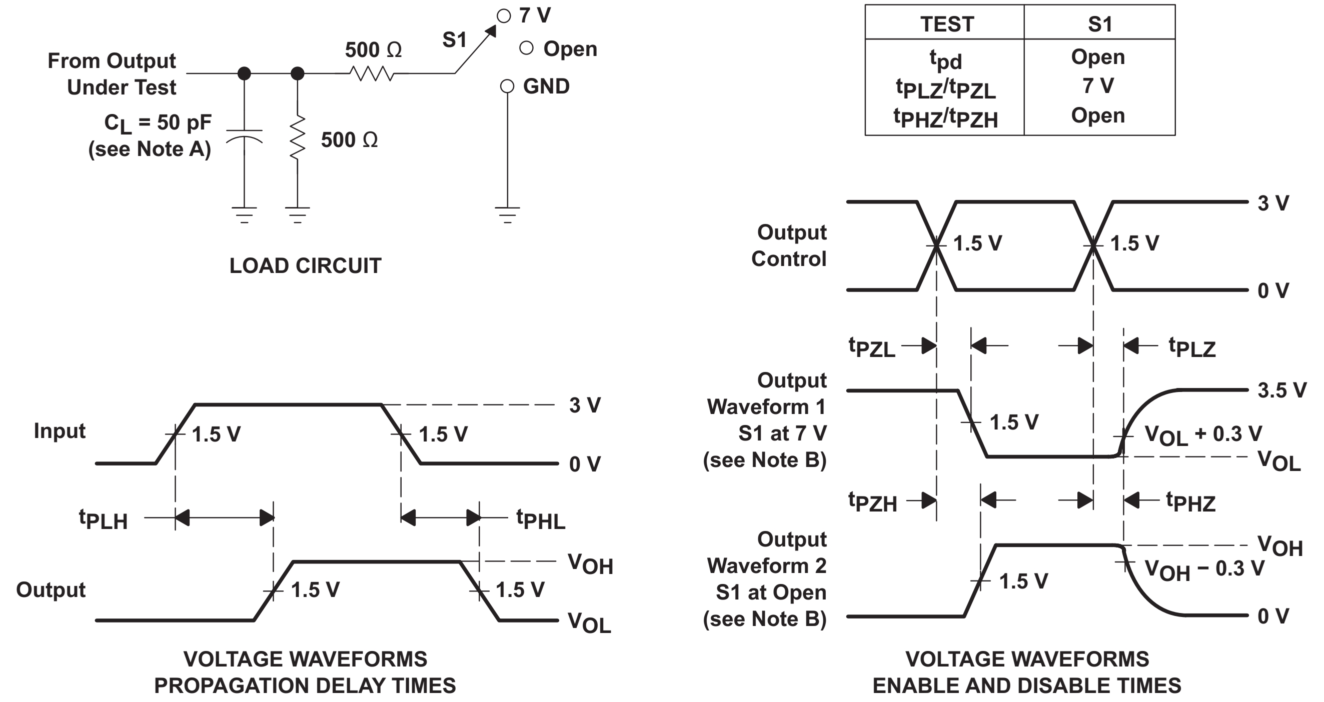


Figure 1. ON-Resistance (R_{ON}) for I_I = 64 mA Across V_I

7 Parameter Measurement Information



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

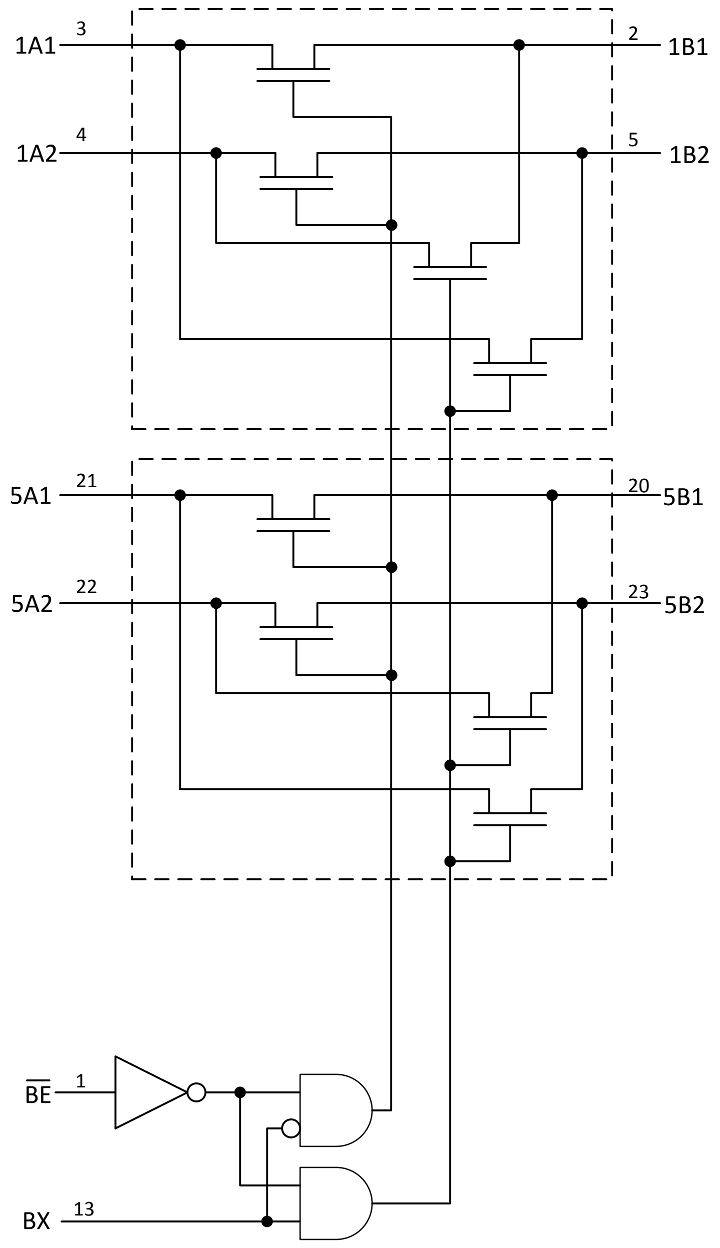
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNX4CBT3383 provides ten high-speed CMOS TTL-compatible bus switches. The low ON-resistance of the SNX4CBT3383 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the 1A and 1B pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a 5-wide, 2-to-1 multiplexer, to create low delay barrel shifters, and so forth.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Data Flow With Near-Zero Propagation Delay

The SN74CBT3383 features a low propagation delay or t_{pd} that works great for multiple rail information transfer from 1A1to 1B1 and 1A2 to 1B2 for example. However, the SNX4CBT3383 also features BUS exchange functionality, which allows for bidirectional data transfers from the inputs and outputs connected on the B side. By enabling the BX pin, the outputs are now crossed, or exchanged, and data can now flow from 1A1 to 1B2 and 1A2 to 1B1 with little to no propagation delay. This can be used to enable byte swapping of buses within a system or to create a 5-wide, 2-to-1 multiplexer.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4CBT3383.

Table 1. Function Table

INPUTS		INPUTS / OUTPUT	
$\overline{BE}$	BX	1A1-5A1	1A2-5A2
L	L	1B1-5B1	1B2-5B2
L	H	1B2-5B2	1B1-5B1
H	X	Z	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBT3383 can be used to multiplex up to 5 channels simultaneously in a 2:1 configuration. The application shown here is a 2-bit bus being multiplexed between two devices. The $\overline{BE}$ and BX pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires only one bit control or exchange, remember to tie the unused bit to high or low. By using another bus controller you can enable exchange across A1 and A2 to B1 and B2, allowing for greater system communication.

9.2 Typical Application

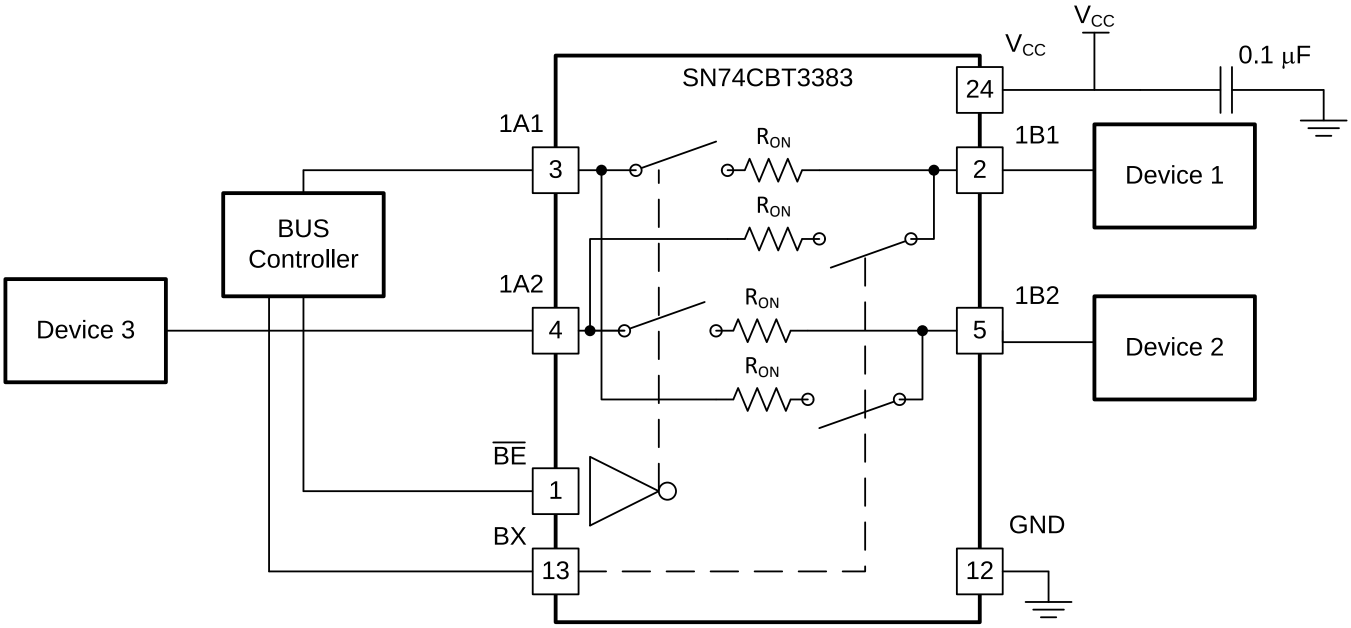


Figure 3. 1:2 Multiplexer or Bus and Selector Using 1 Bus Controller

9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions.*
2. Recommended Output Conditions:
   - Load currents must not exceed 128 mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 200 MHz.
   - Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

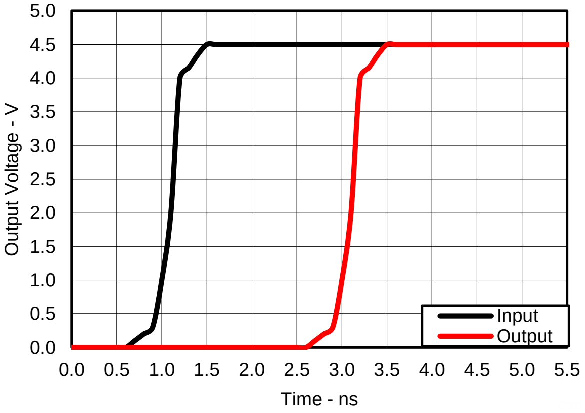
Typical Application (continued)

9.2.2 Detailed Design Procedure

The 2-bit bus is connected directly to the 1A1, 1A2 on the SN74CBT3383, which essentially combines in the bus controller to form a single input or split bus bits. When $\overline{BE}$ is low and BX is low, the selected bus is using 1A1 and 1B1 as inputs and outputs. This means that Device 1 is connected to the bus controller and Device 2 is connected to Device 3 when $\overline{BE}$ is low and BX is low. While keeping $\overline{BE}$ low and using BX high, we can enable communication from the bus controller to Device 2 and from Device 1 to Device 3. This setup is especially useful when two controllers or devices need to share the same data from Device 1 and Device 2 and the bus addresses are limited or hard coded.

The 0.1-μF capacitor on V_{CC} is a decoupling capacitor and should be placed as close as possible to the device.

9.2.3 Application Curve



V_{CC} = 4.5 V

Figure 4. Propagation Delay (t_{pd}) Simulation Results

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

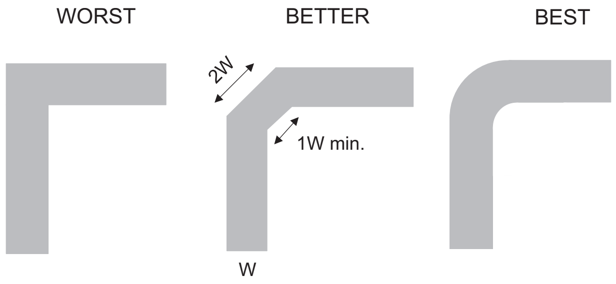


Figure 5. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see *Voltage Clamps Made Easy*, SCEA045.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74CBT3383	Click here	Click here	Click here	Click here	Click here
SN54CBT3383	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9668801QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668801QKA SNJ54CBT3383W	Samples
5962-9668801QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668801QLA SNJ54CBT3383JT	Samples
SN74CBT3383DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74CBT3383DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383	Samples
SN74CBT3383DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383	Samples
SN74CBT3383DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383	Samples
SN74CBT3383DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383	Samples
SN74CBT3383DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383	Samples
SN74CBT3383PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383	Samples
SN74CBT3383PWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SN74CBT3383PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383	Samples
SN74CBT3383PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383	Samples
SNJ54CBT3383JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668801QLA SNJ54CBT3383JT	Samples
SNJ54CBT3383W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9668801QKA SNJ54CBT3383W	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54CBT3383, SN74CBT3383 :

- Catalog: SN74CBT3383

- Military: SN54CBT3383

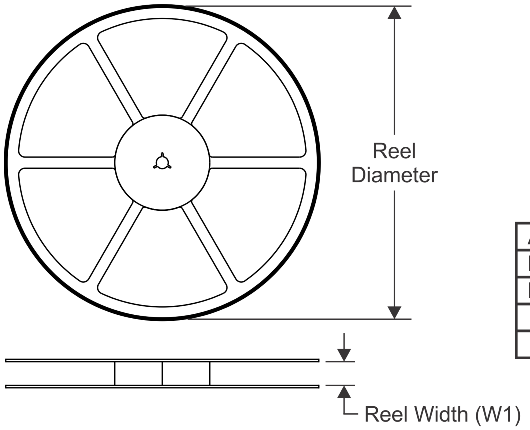
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

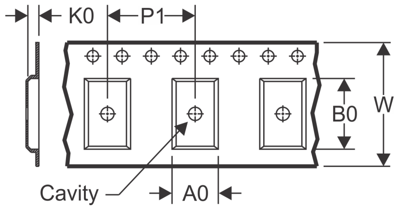
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

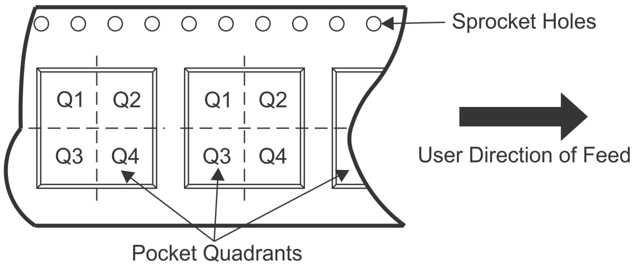


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

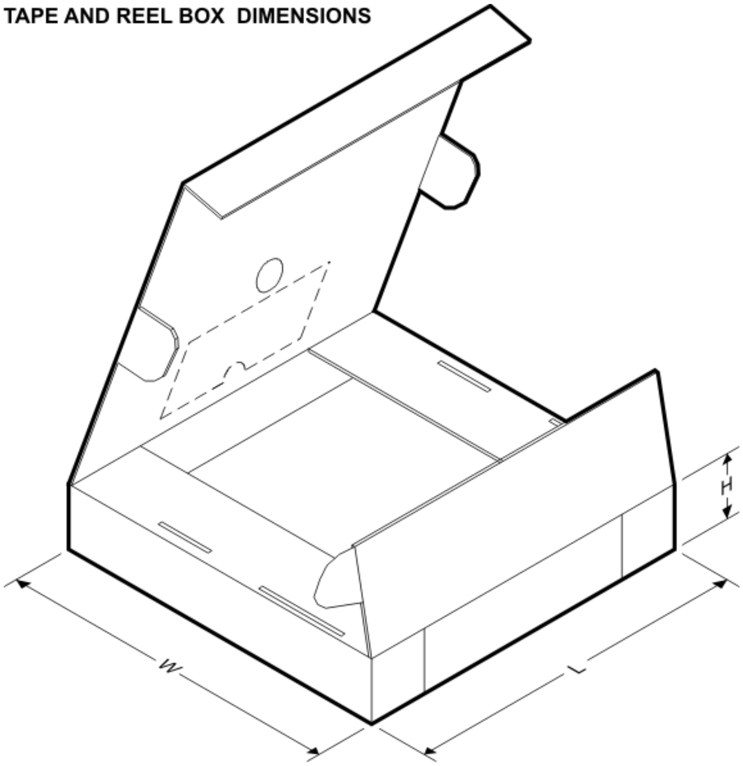
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3383DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3383DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74CBT3383DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3383PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



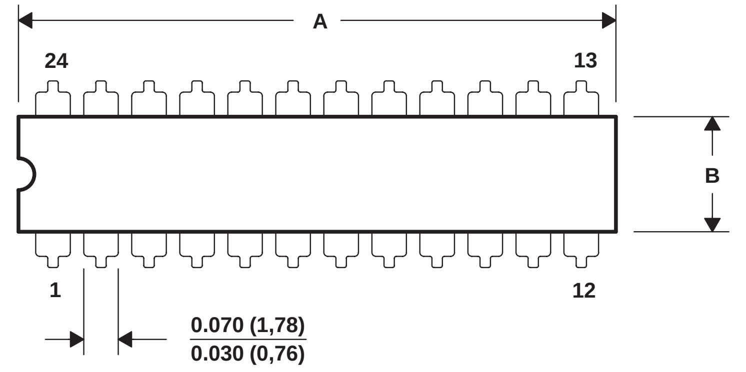
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3383DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74CBT3383DBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74CBT3383DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74CBT3383PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

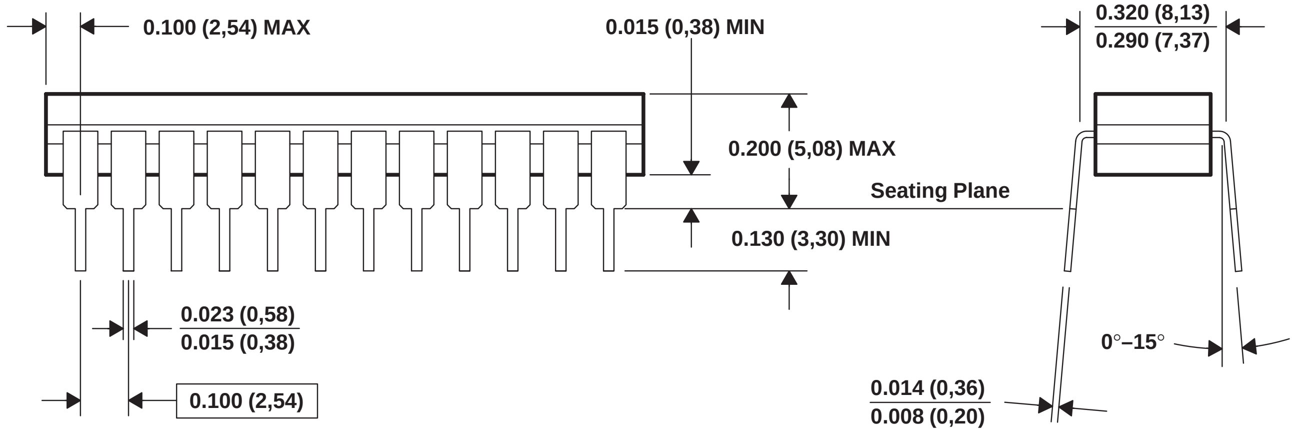
JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



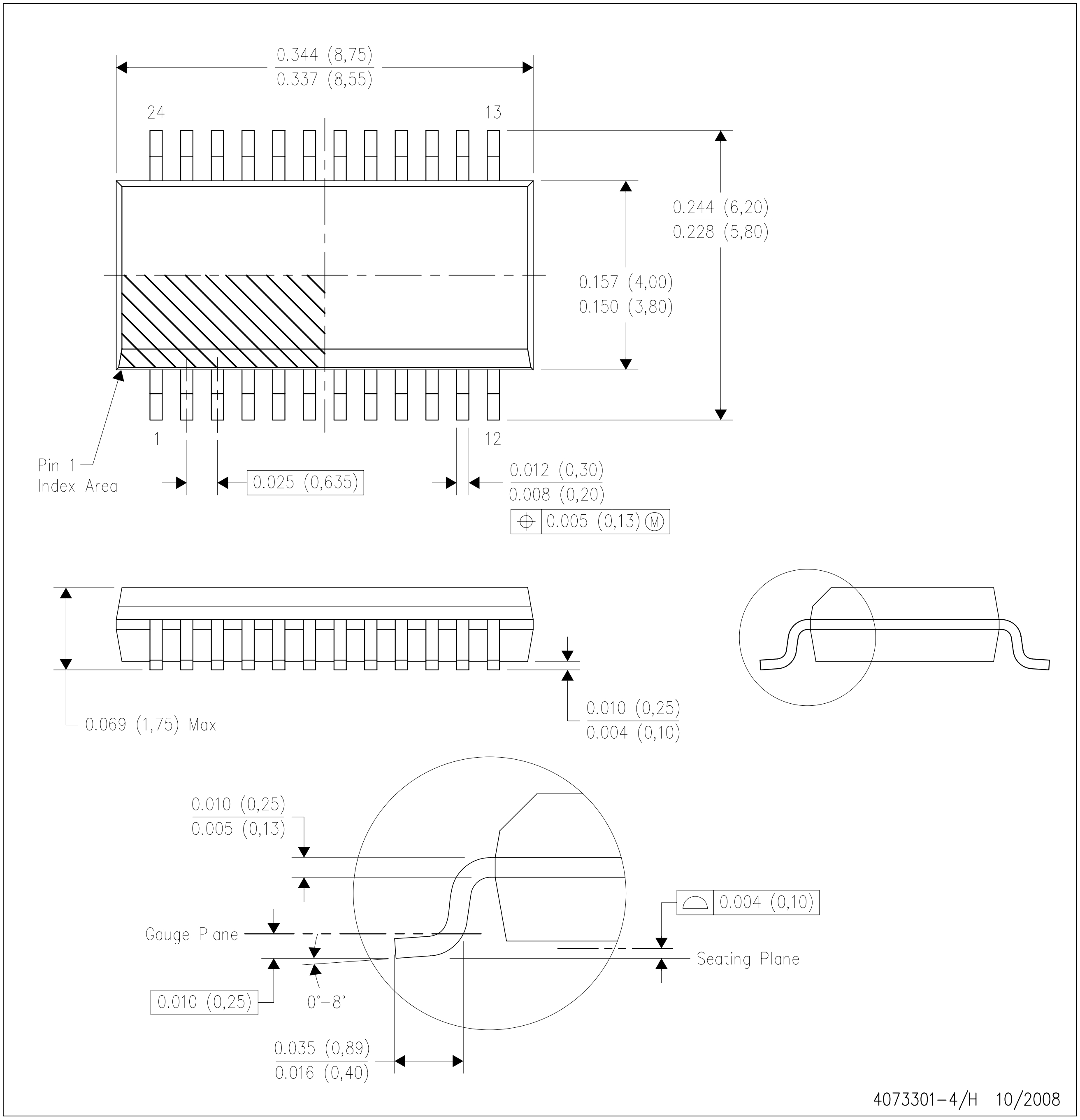
PINS ** / DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)



4040110/C 08/96

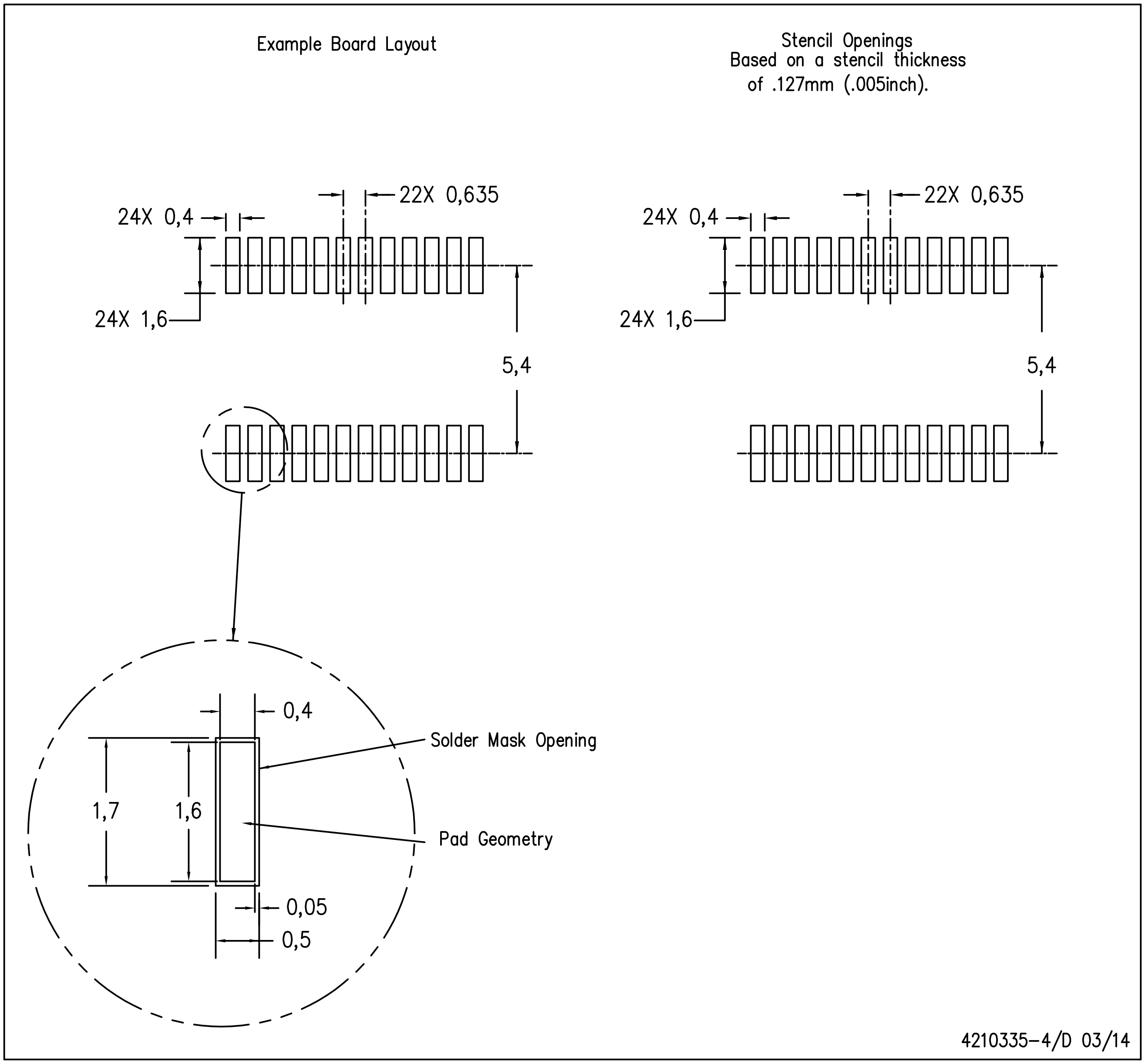
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

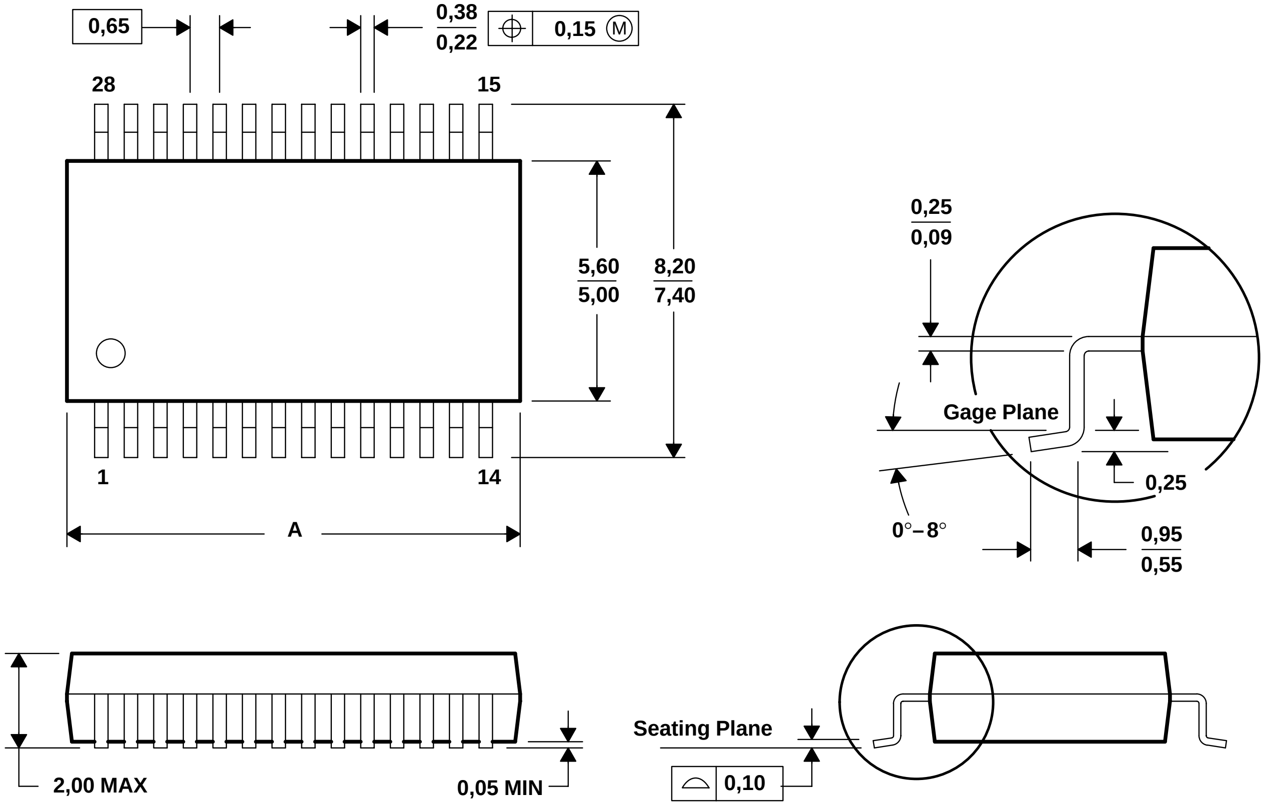
DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN

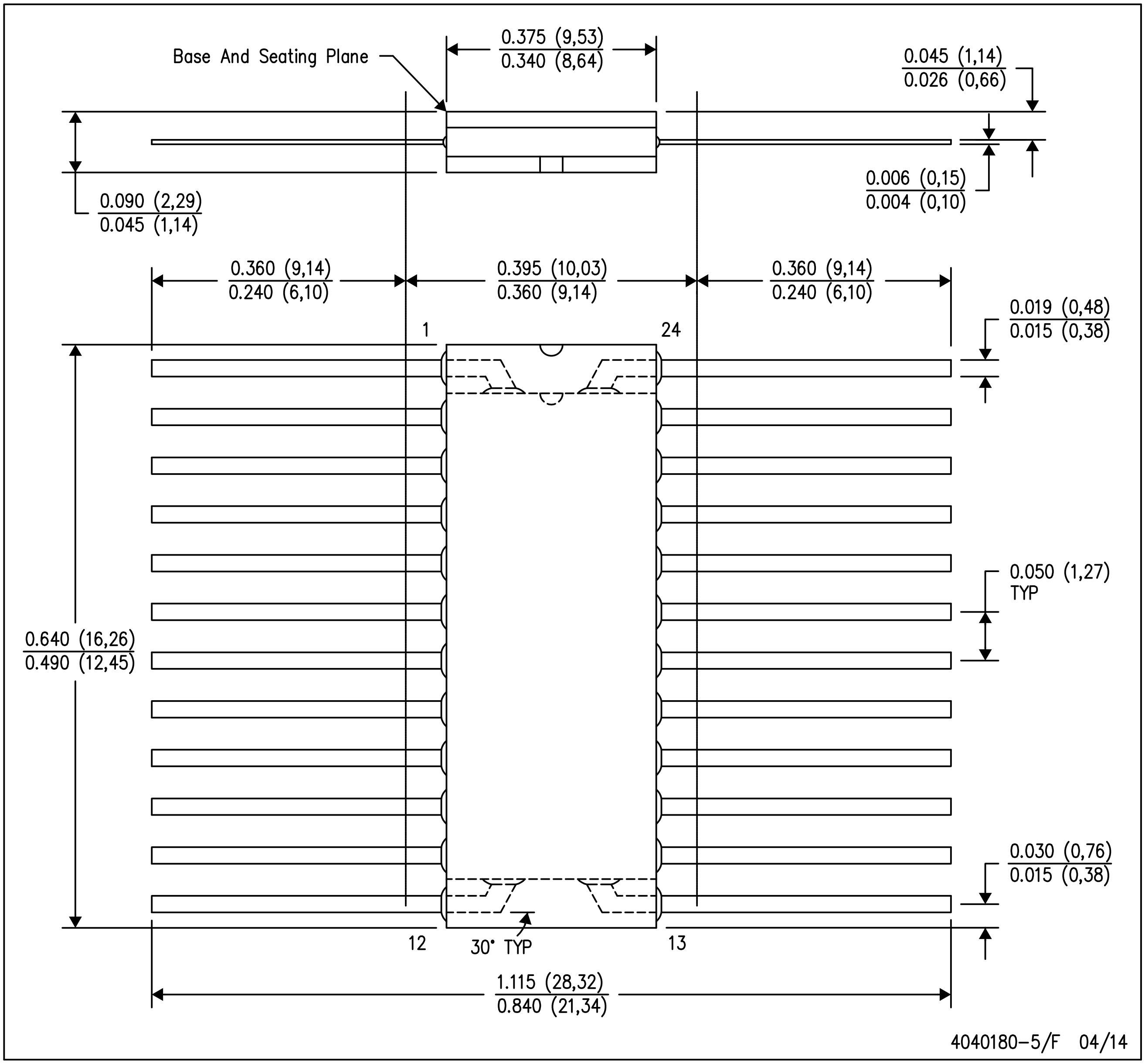


PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

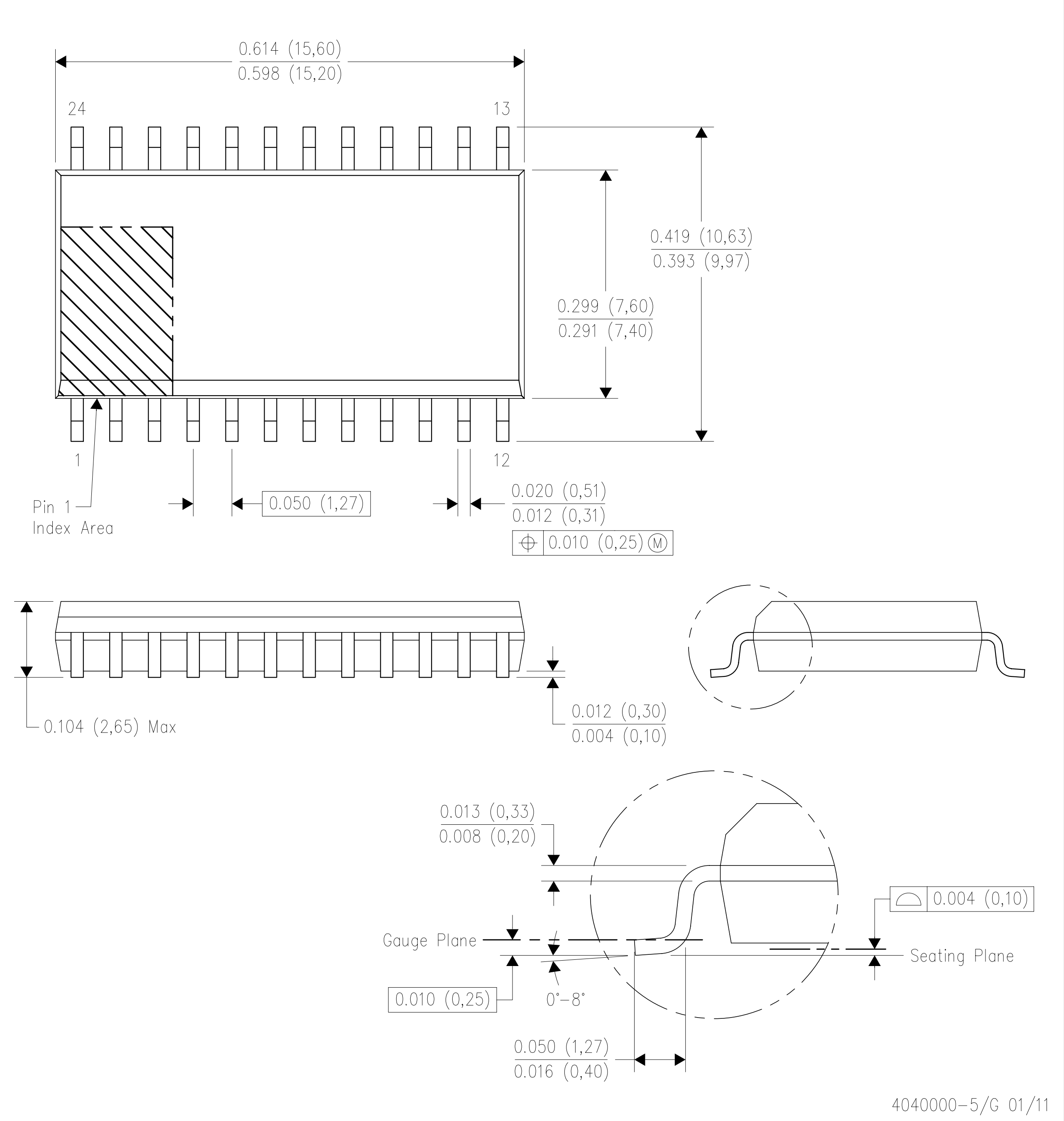
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

W (R–GDFP–F24) CERAMIC DUAL FLATPACK



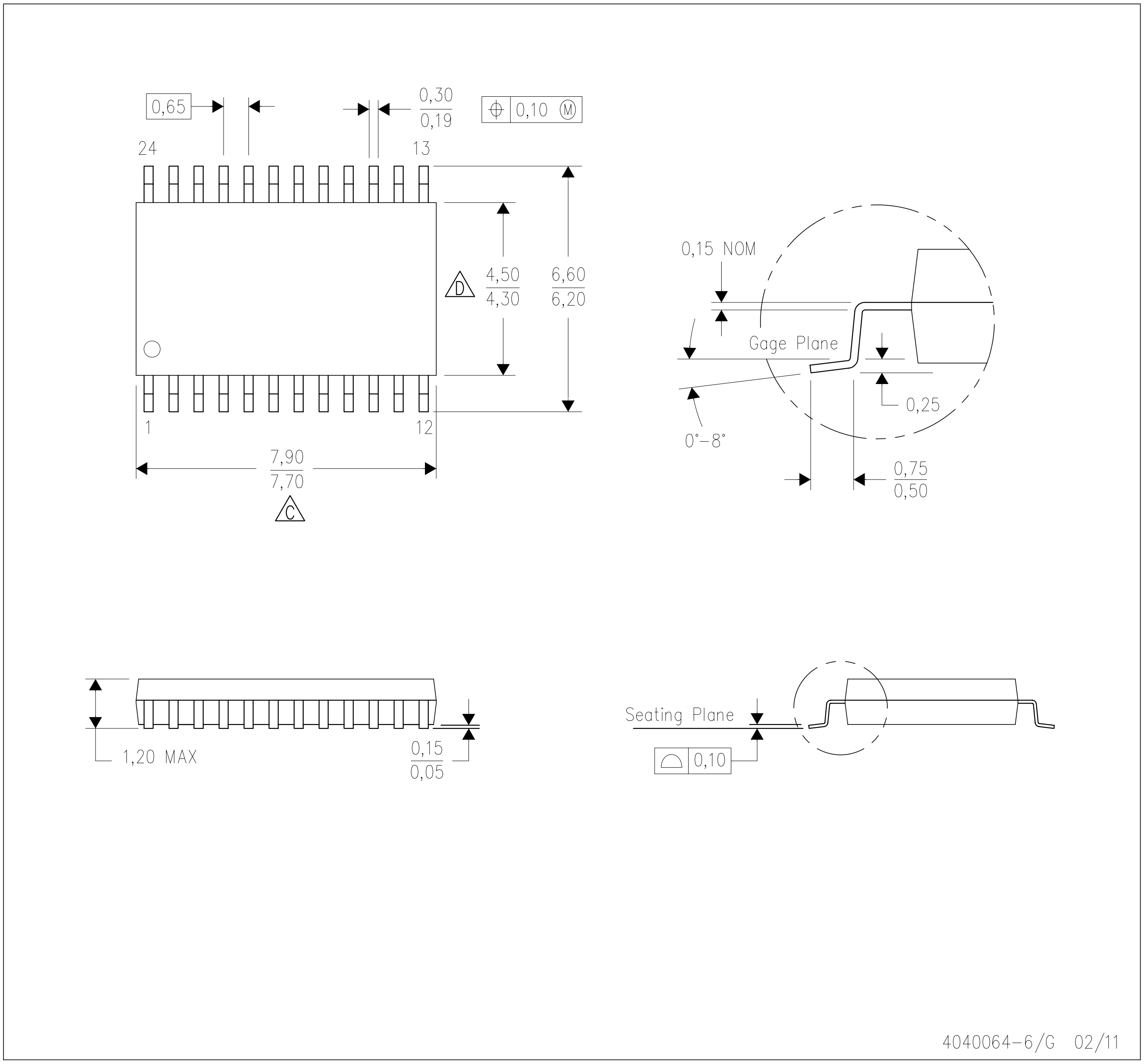
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil–Std 1835 GDFP2–F20

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

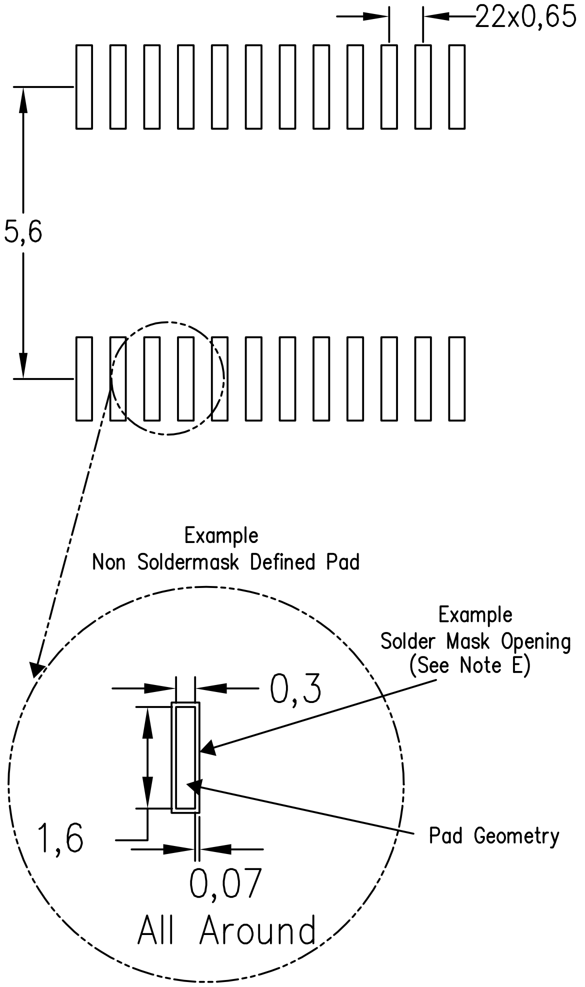
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



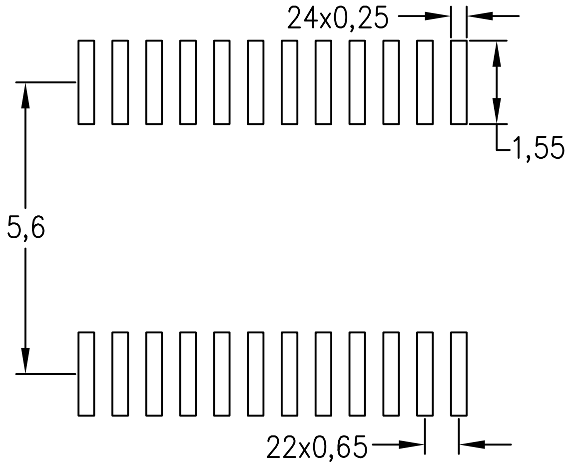
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4211284-4/G 08/15

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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