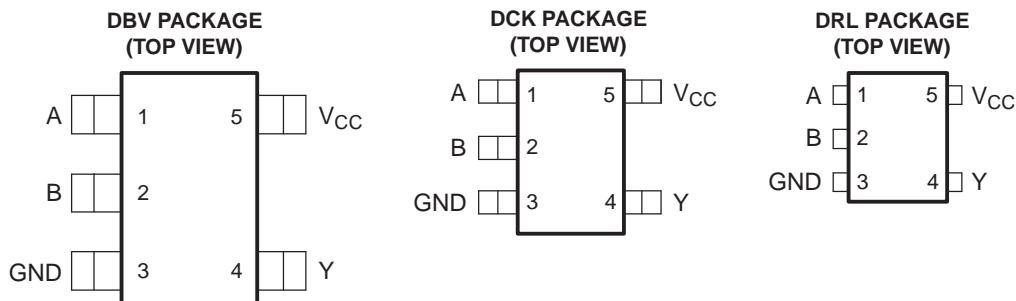


FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
 - **Extended Temperature Performance of –55°C to 125°C**
 - **Enhanced Diminishing Manufacturing Sources (DMS) Support**
 - **Enhanced Product-Change Notification**
 - **Qualification Pedigree** ⁽¹⁾
 - **Operating Range of 2 V to 5.5 V**
 - **Max t_{pd} of 8.5 ns at 5 V**
 - **Low Power Consumption, 10 μ A Max I_{CC}**
 - **\pm 8 mA Output Drive at 5 V**
 - **Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time**
 - **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SC-70) - DCK Reel of 3000	SN74AHC1G02MDCKREP	CGC

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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SN74AHC1G02-EP SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS708—FEBRUARY 2008

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Output voltage range ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-20 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O = 0$ to V_{CC}		± 20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 25 mA
	Continuous current through V_{CC} or GND	V_{CC} or GND		± 50 mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCK package		252 °C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-Level output current	$V_{CC} = 2\text{ V}$	-50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3$	-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5$	-8	
I_{OL}	Low-Level output current	$V_{CC} = 2\text{ V}$	50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
T_A	Operating free-air temperature	-55	125	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AHC1G02-EP SINGLE 2-INPUT POSITIVE-NOR GATE

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Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I _{OL} = 4 mA	3 V		0.36		0.44		
	I _{OL} = 8 mA	4.5 V		0.36		0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, O = 0	5.5 V			1	10	μA	
C _i	V _I = V _{CC} or GND	5 V		4	10	10	pF	

Switching Characteristics

over operating free-air temperature range, V_{CC} = 3.3 ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			T _A = -55°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 50 pF		8.1	11.4	1	13	ns
t _{PHL}					8.1	11.4	1	13	

Switching Characteristics

over operating free-air temperature range, V_{CC} = 5 ± 0.5 V (unless otherwise noted) (see Figure 1)

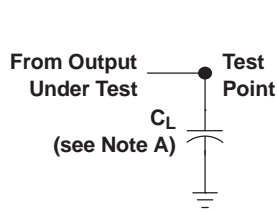
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			T _A = -55°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 50 pF		5.1	7.5	1	8.5	ns
t _{PHL}					5.1	7.5	1	8.5	

Operating Characteristics

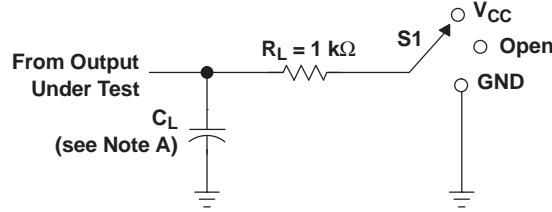
V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	15	pF

PARAMETER MEASUREMENT INFORMATION

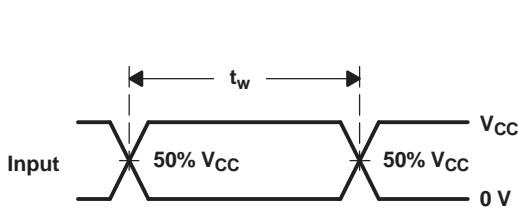


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

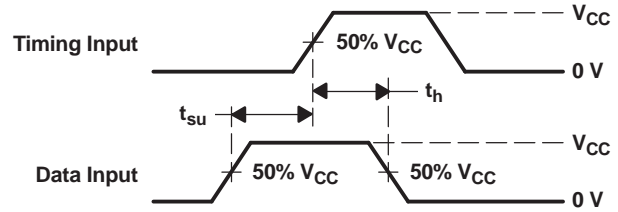


LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

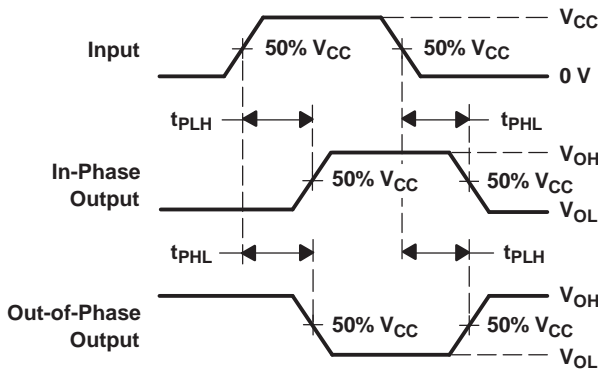
TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZH}	V _{CC}
t _{PHZ} /t _{PZH}	GND
Open Drain	V _{CC}



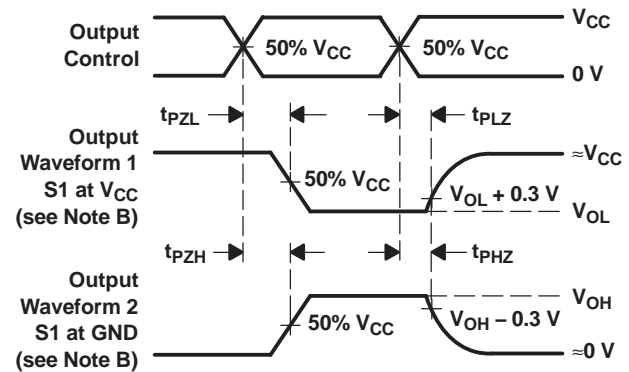
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G02MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G02MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

DCK (R-PDSO-G5)

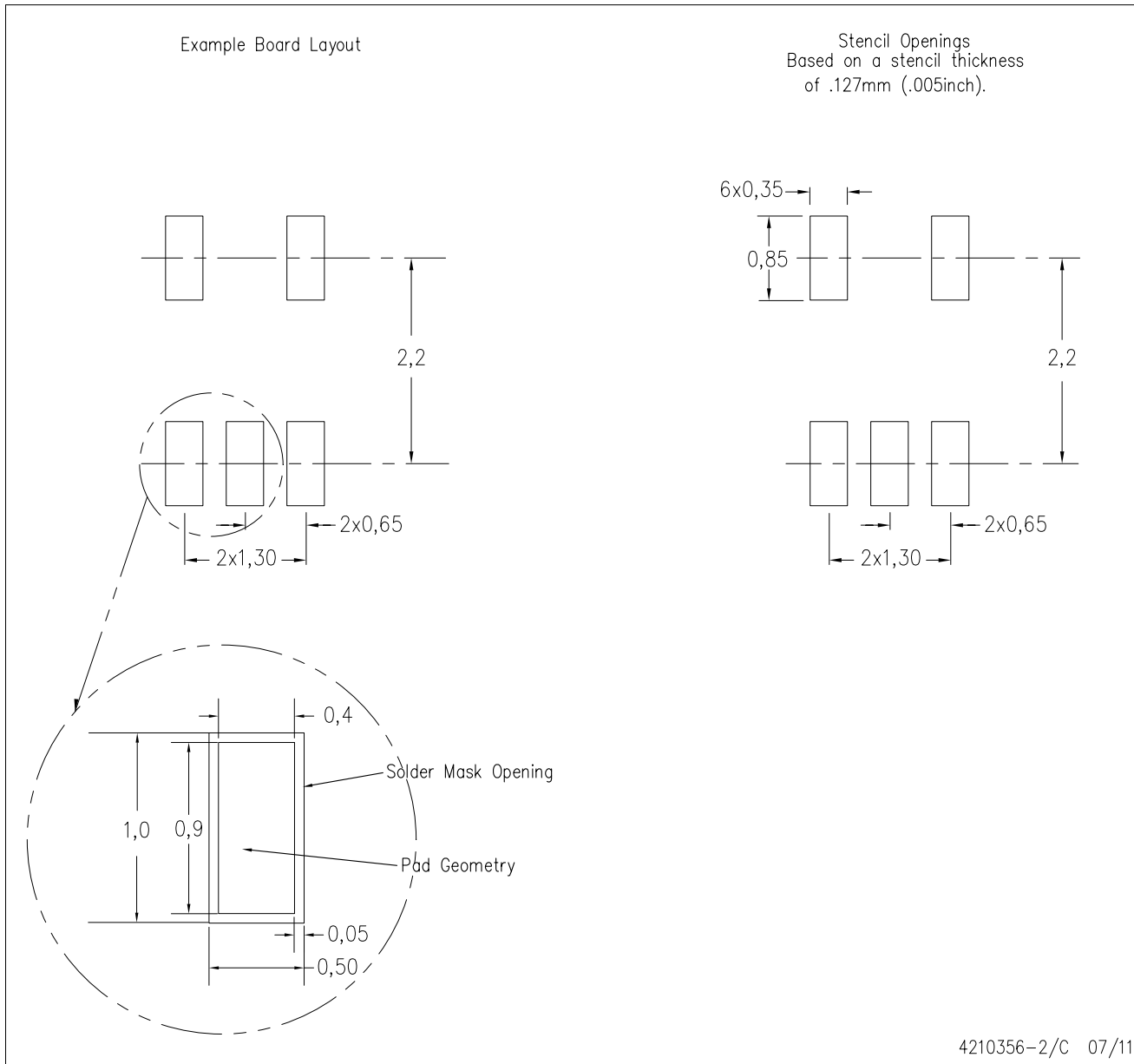
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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