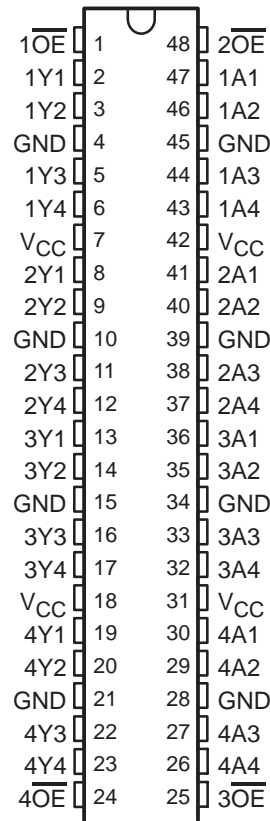


# SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD-17

SN54ABT162244 . . . WD PACKAGE  
SN74ABT162244 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description/ordering information

The 'ABT162244 devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ABT162244DL	ABT162244
		Tape and reel	SN74ABT162244DLR	
	TSSOP – DGG	Tape and reel	SN74ABT162244DGGR	ABT162244
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74ABT162244DGVR	AH2244
	CFP – WD	Tube	SNJ54ABT162244WD	SNJ54ABT162244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABT162244, SN74ABT162244

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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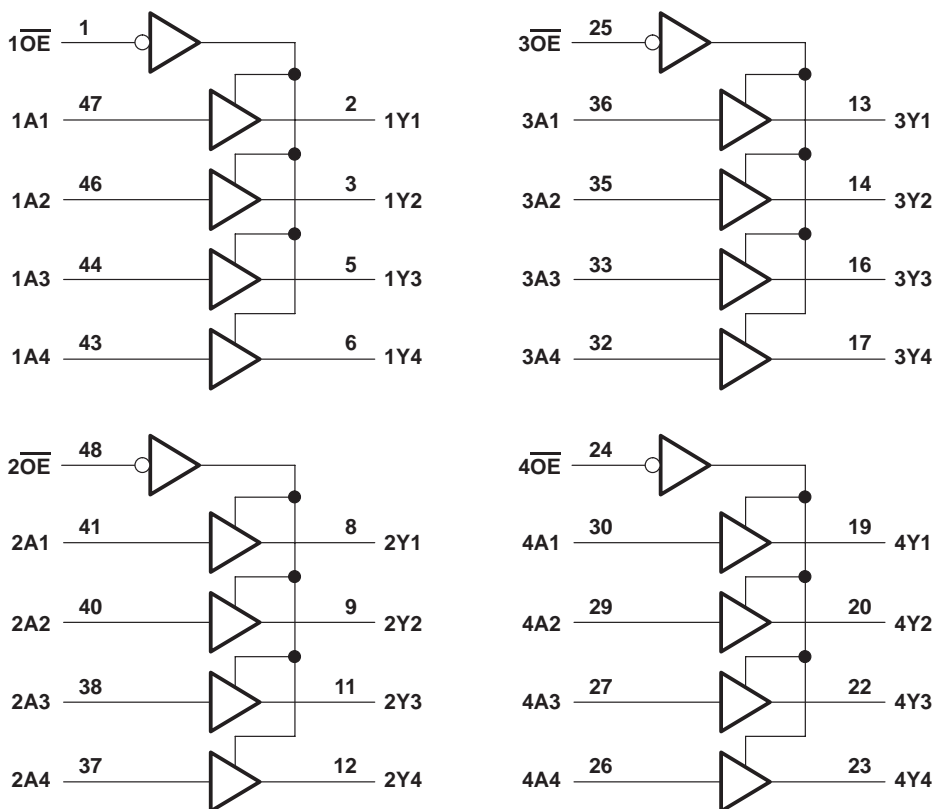
#### description/ordering information (continued)

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

#### logic diagram (positive logic)



# SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V	
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V	
Current into any output in the low state, $I_O$ .....	30 mA	
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2):	DGG package .....	70°C/W
	DGV package .....	58°C/W
	DL package .....	63°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54ABT162244		SN74ABT162244		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–3		–12	mA
$I_{OL}$	Low-level output current		8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

- NOTES: 3. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ABT162244, SN74ABT162244

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT162244		SN74ABT162244		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA			3.35		3.35		3.35	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA			3.85		3.85		3.85		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA			3.1		3.1			3.1
I <sub>OH</sub> = -12 mA				2.6*				2.6		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 8 mA			0.4			0.8	0.65	V
		I <sub>OL</sub> = 12 mA							0.8	
V <sub>hys</sub>				100					mV	
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	µA	
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA	
I <sub>OZPD</sub>	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA	
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	µA	
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	µA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50	50	µA	
I <sub>O</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-25 -55 -100		-25 -100		-25 -100	mA	
I <sub>CC</sub> ‡	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			2		2	2	mA	
		Outputs low			30		30	30		
		Outputs disabled			2		2	2		
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			50		50	µA	
			Outputs disabled			50		50		
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50		50	50		
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF	
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			8					pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.



**SN54ABT162244, SN74ABT162244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT162244					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
t <sub>PLH</sub>	A	Y	1	2.5	3.6	1	4.1	ns	
t <sub>PHL</sub>			1	3.1	4.7	1	5.3		
t <sub>PZH</sub>	$\overline{OE}$	Y	1	3.2	4.8	1	5.6	ns	
t <sub>PZL</sub>			1	3.2	4.7	1	5.5		
t <sub>PHZ</sub>	$\overline{OE}$	Y	1	3.2	5.3	1	6.3	ns	
t <sub>PLZ</sub>			1	3.1	4.6	1	4.9		

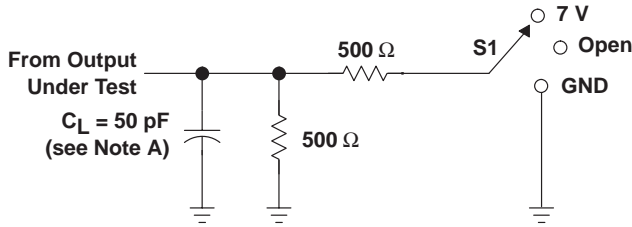
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT162244					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
t <sub>PLH</sub>	A	Y	1	2.5	3.2	1	3.9	ns	
t <sub>PHL</sub>			1	3.1	4	1	4.8		
t <sub>PZH</sub>	$\overline{OE}$	Y	1	3.2	4.2	1	5.4	ns	
t <sub>PZL</sub>			1	3.2	4.1	1	5.1		
t <sub>PHZ</sub>	$\overline{OE}$	Y	1	3.2	4	1	4.6	ns	
t <sub>PLZ</sub>			1	3.1	3.9	1	4.5		

**SN54ABT162244, SN74ABT162244**  
**16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

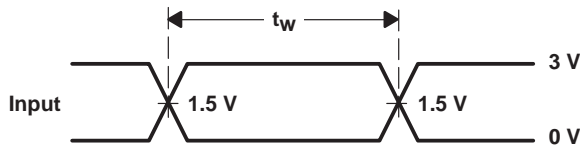
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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

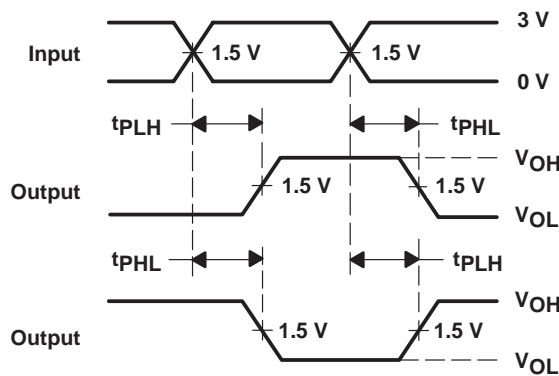
**LOAD CIRCUIT**



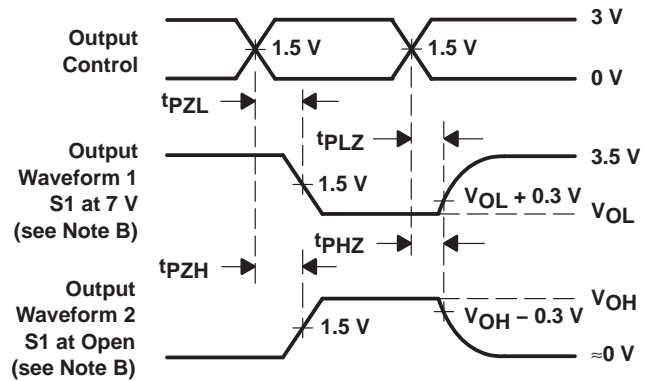
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9458701QXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9458701QX A SNJ54ABT162244 WD	<a href="#">Samples</a>
74ABT162244DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162244	<a href="#">Samples</a>
SN74ABT162244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162244	<a href="#">Samples</a>
SN74ABT162244DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH2244	<a href="#">Samples</a>
SN74ABT162244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162244	<a href="#">Samples</a>
SN74ABT162244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162244	<a href="#">Samples</a>
SN74ABT162244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162244	<a href="#">Samples</a>
SNJ54ABT162244WD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9458701QX A SNJ54ABT162244 WD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT162244, SN74ABT162244 :**

- Catalog: [SN74ABT162244](#)
- Military: [SN54ABT162244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABT162244DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABT162244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

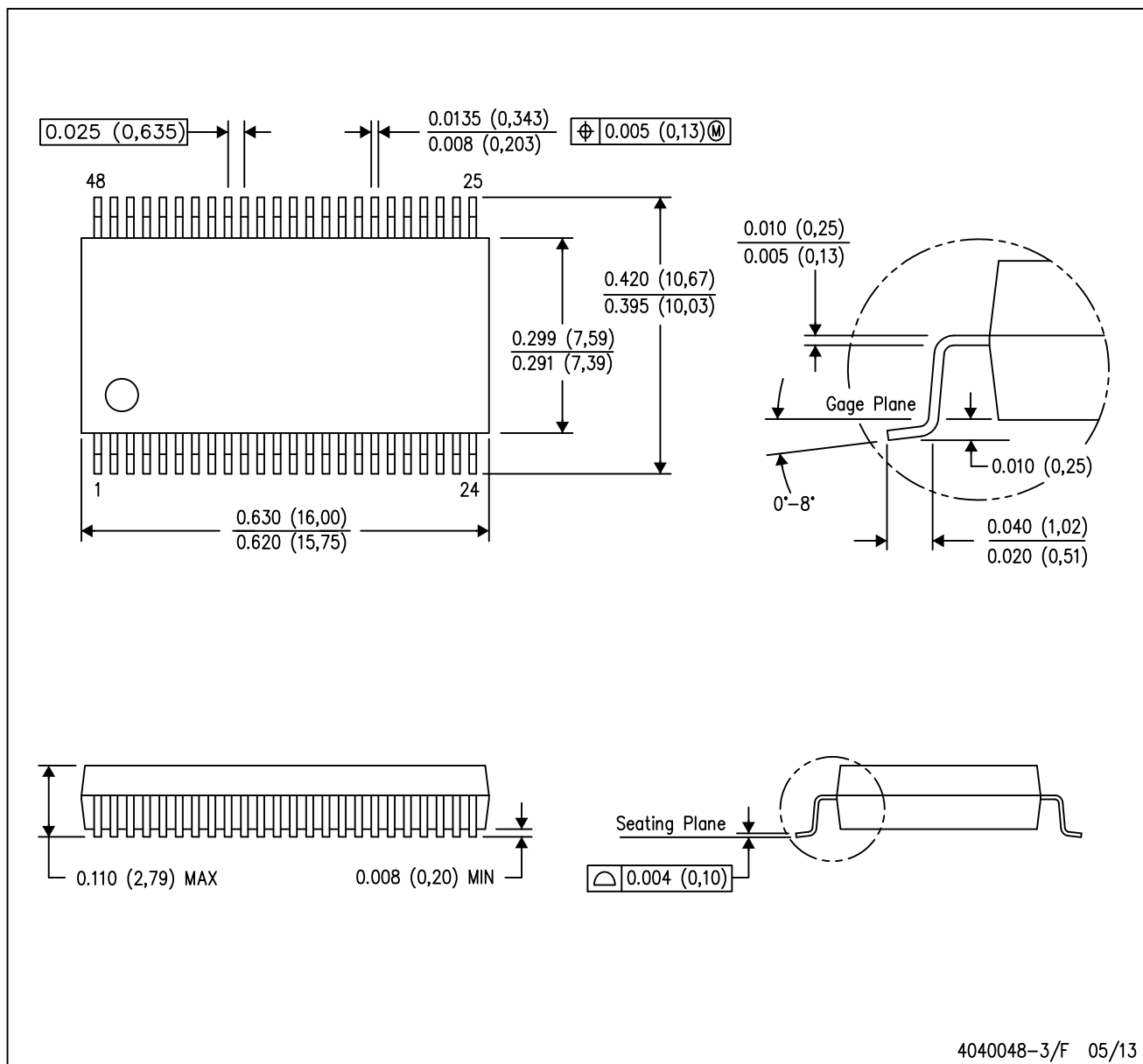
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT162244DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74ABT162244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

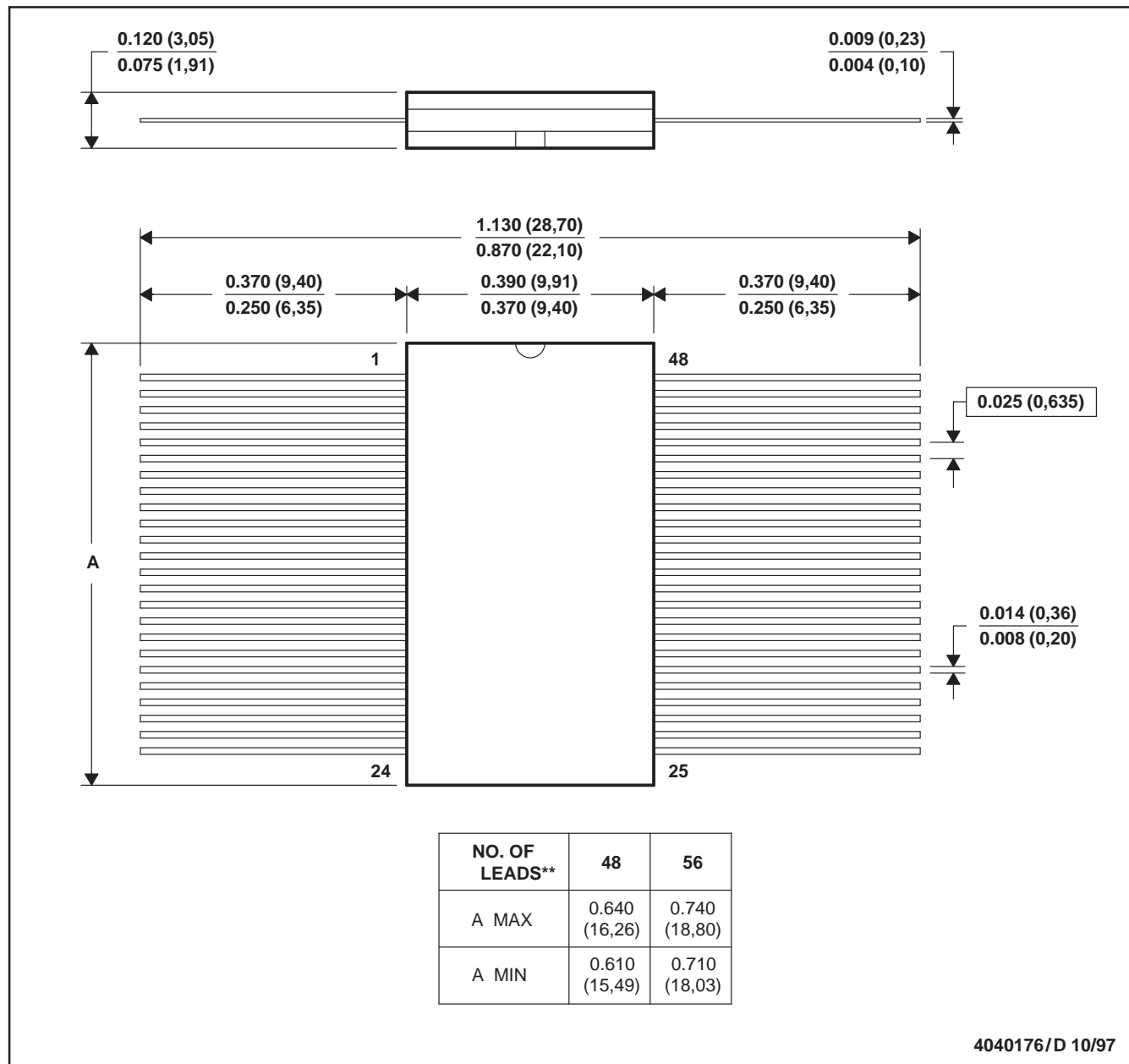


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

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