

SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

SDAS018C – DECEMBER 1982 – REVISED JANUARY 1995

- High Capacitive-Drive Capability
- Typical Delay Time of 3.2 ns ($C_L = 50$ pF) and Typical Power Dissipation of Less Than 13 mW Per Gate
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

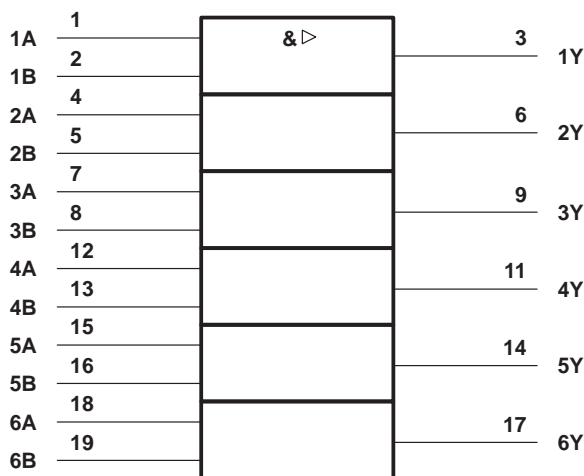
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

The SN54AS808B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS808B is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each driver)

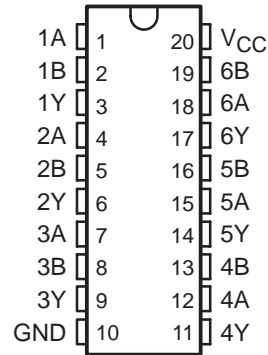
| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | H |
| L | X | L |
| X | L | L |

logic symbol†

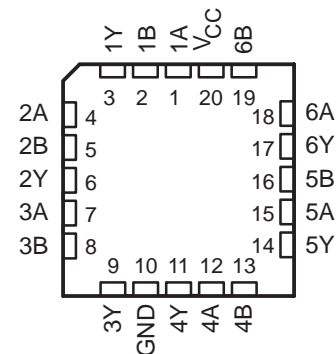


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

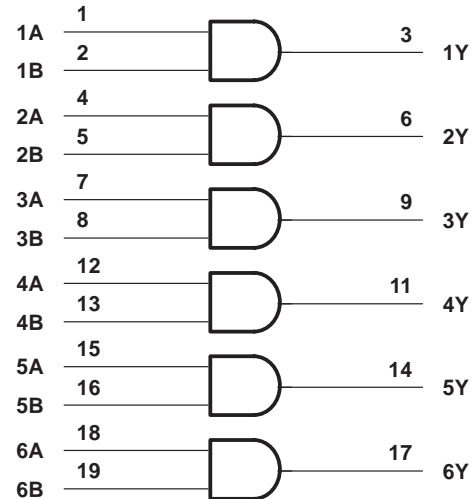
SN54AS808B . . . J PACKAGE
SN74AS808B . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS808B . . . FK PACKAGE
(TOP VIEW)



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54AS808B | -55°C to 125°C |
| SN74AS808B | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS808B | | | SN74AS808B | | | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -40 | | | -48 | mA |
| I_{OL} | Low-level output current | | | 40 | | | 48 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS808B | | | SN74AS808B | | | UNIT | |
|--------------|---|--------------------------|------|------|--------------|------|------|------|-----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | | -1.2 | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V | |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -3\text{ mA}$ | | | 2.4 | 3.2 | 2.4 | | 3.2 |
| | | $I_{OH} = -40\text{ mA}$ | | | 2 | | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -48\text{ mA}$ | | | 2 | | | | |
| | | $I_{OL} = 40\text{ mA}$ | | | 0.25 | 0.5 | | | |
| | | $I_{OL} = 48\text{ mA}$ | | | | | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | | | 0.1 | mA | |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | | | 20 | μA | |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -0.5 | | | -0.5 | mA | |
| I_{O}^{\S} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -50 | | -200 | -50 | | -200 | mA | |
| I_{CCH} | $V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$ | | 8 | 13 | | 8 | 13 | mA | |
| I_{CCL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0$ | | 20 | 33 | | 20 | 33 | mA | |

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$ | | | | UNIT |
|-----------|-----------------|----------------|---|-----|------------|-----|------|
| | | | SN54AS808B | | SN74AS808B | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | Y | 1 | 6.5 | 1 | 6 | ns |
| t_{PHL} | | | 1 | 6.5 | 1 | 6 | |

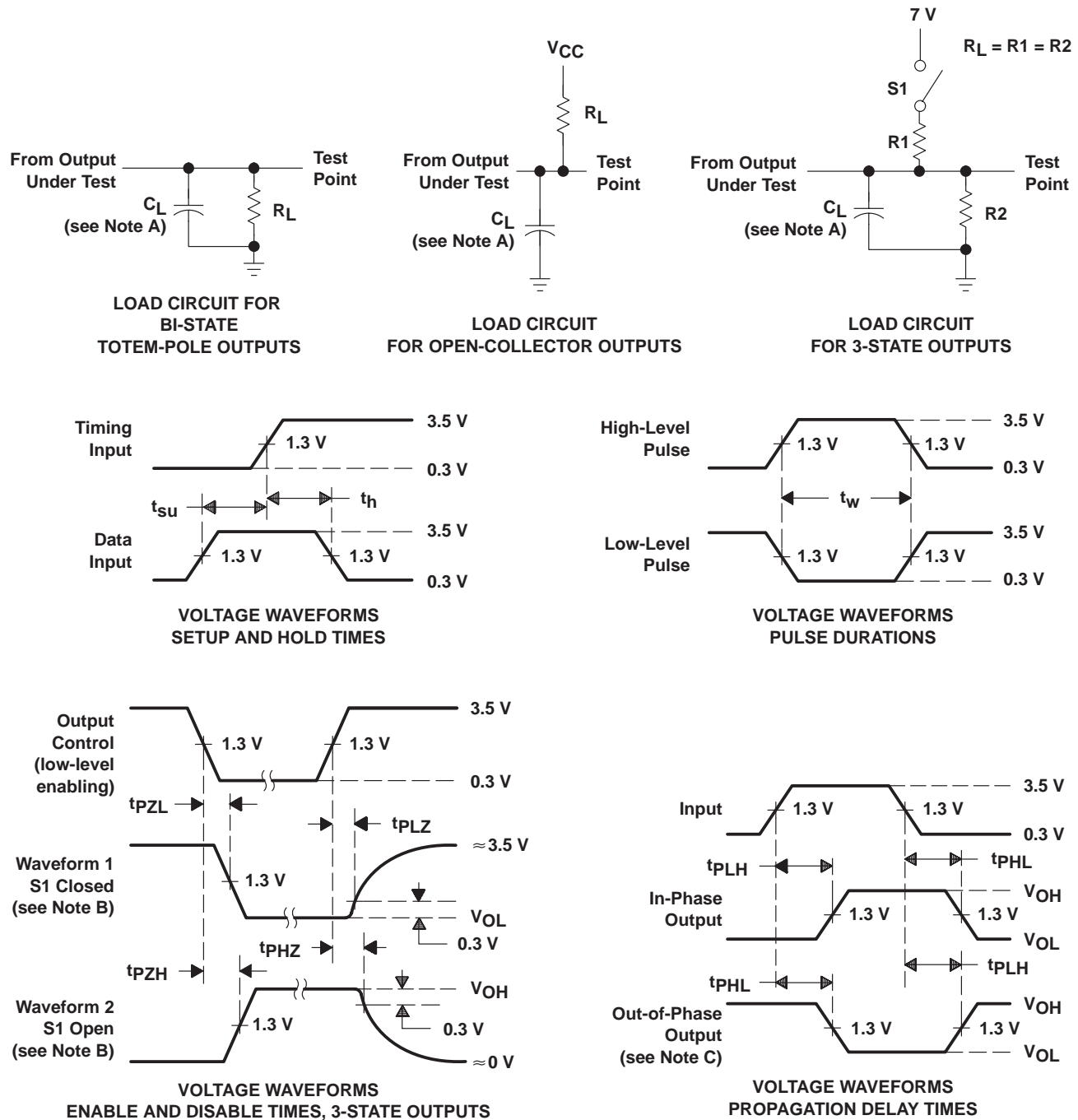
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-88522012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 88522012A SNJ54AS 808BFK | Samples |
| 5962-8852201RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8852201RA SNJ54AS808BJ | Samples |
| 5962-8852201SA | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SN54AS808BJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54AS808BJ | Samples |
| SN74AS808BDW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS808B | Samples |
| SN74AS808BDWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS808B | Samples |
| SN74AS808BDWR | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS808BDWRE4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS808BDWRG4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS808BN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS808BN | Samples |
| SN74AS808BN3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74AS808BNE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS808BN | Samples |
| SNJ54AS808BFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 88522012A SNJ54AS 808BFK | Samples |
| SNJ54AS808BJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8852201RA SNJ54AS808BJ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AS808B, SN74AS808B :

● Catalog: [SN74AS808B](#)

● Military: [SN54AS808B](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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