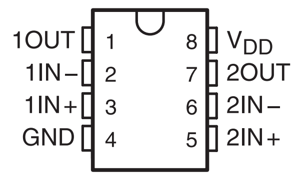
DUAL MICROPOWER LinCMOS™ VOLTAGE COMPARATORS

Check for Samples: TLC3702-Q1

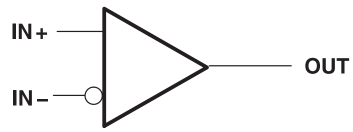
FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 100-V Machine Model (C = 200 pF, R = 0); Exceeds 1500-V Charged Device Model (C = 200 pF, R = 0)
- Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, I_O = ± 8 mA
- Very Low Power . . . 100 μW Typ at 5 V
- Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive
- Single-Supply Operation . . . 3 V to 16 V
- On-Chip ESD Protection

D OR PW PACKAGE
(TOP VIEW)



SYMBOL (EACH COMPARATOR)



DESCRIPTION

The TLC3702-Q1 consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use one-twentieth of the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

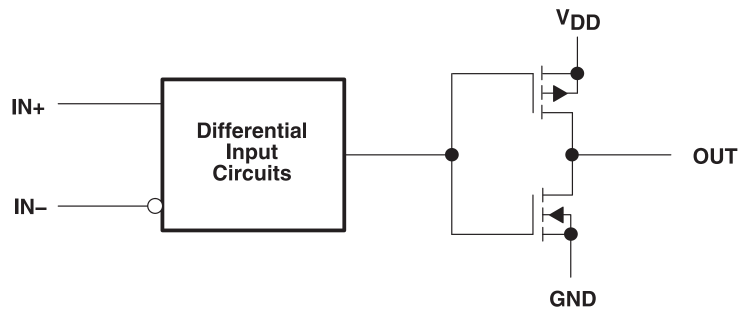
The TLC3702-Q1 is characterized for operation over the full automotive temperature range of −40°C to 125°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOP − D	Tape and reel	TLC3702QDRQ1	3702Q1
	TSSOP − PW	Tape and reel	TLC3702QPWRQ1	3702Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM (EACH COMPARATOR)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage range, V_{DD} (2)		−0.3 V to 18 V	V
Differential input voltage, V_{ID} (3)		±18	V
Input voltage range, V_I		−0.3 V to V_{DD}	V
Output voltage range, V_O		−0.3 V to V_{DD}	V
Input current, I_I		±5	mA
Output current, I_O (each output)		±20	mA
Total supply current into V_{DD}		40	mA
Total current out of GND		40	mA
Continuous total power dissipation		See Thermal Table	
Operating free-air temperature range, T_A		−40 to 125	°C
Storage temperature range, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package	260	°C
	PW package	260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Differential voltages are at IN+ with respect to IN −.

THERMAL INFORMATION

THERMAL METRIC (1)		TLC3702QDRQ1	TLC3702QPWRQ1	UNITS
		D (8 PINS)	PW (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	117.7	181.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	63.9	49.9	
θ_{JB}	Junction-to-board thermal resistance	57..8	110.1	
ψ_{JT}	Junction-to-top characterization parameter	15.3	2.4	
ψ_{JB}	Junction-to-board characterization parameter	57.3	108.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4	5	16	V
V_{IC}	Common-mode input voltage	0		V_{DD}- 1.5	V
I_{OH}	High-level output current			-20	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS(1)

at specified operating free-air temperature range, V_{DD}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min, See (2)	25°C		1.2	5	mV
			−40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			−40°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−40°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5			V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		19	40	µA
			−40°C to 125°C			90	

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.
(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

SWITCHING CHARACTERISTICS

at recommended operating conditions, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(PLH)}$	Propagation response time, low-to-high-level output (1)	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4 V step at IN+			1.1		
$t_{(PHL)}$	Propagation response time, high-to-low-level output (1)	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

(1) Simultaneous switching of inputs causes degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ Process

The LinCMOS process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Further questions should be directed to the nearest TI field sales office.

Electrostatic Discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, for example, during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented in the following sections.

All input and output pins on LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

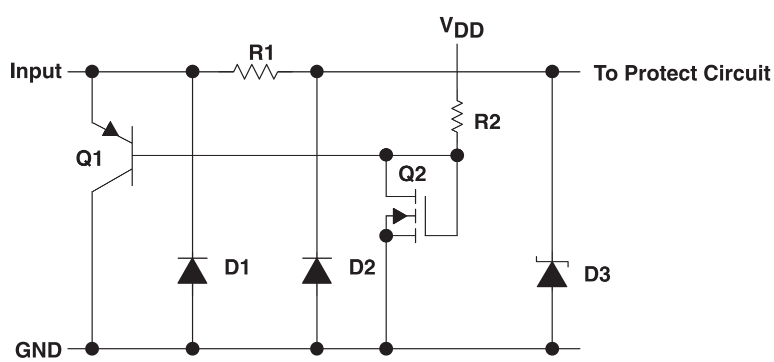


Figure 1. LinCMOS™ ESD-Protection Schematic

Input Protection Circuit Operation

TI's patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

Positive ESD Transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

Negative ESD Transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is −0.3 V to −1 V (the forward voltage of D1 and D2).

Circuit-Design Considerations

LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 2 and Figure 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

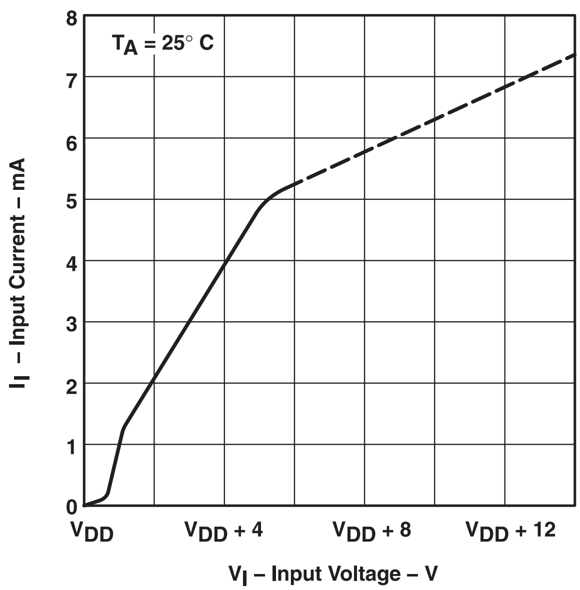


Figure 2.

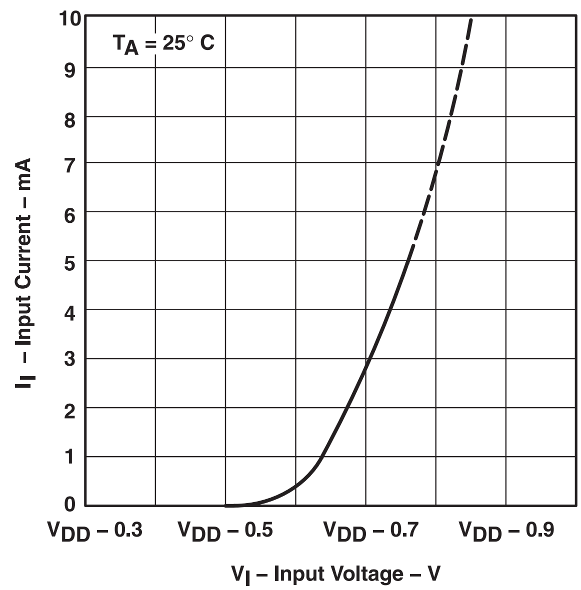
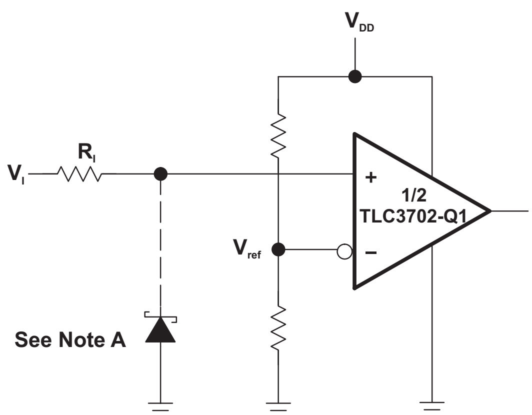


Figure 3.



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

A. If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3702-Q1 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier and comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, and so forth.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed to provide greater accuracy, as shown in Figure 5(b) for the V_{ICR} test. This slewing is done instead of changing the input voltages.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R8 and R9 provide an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

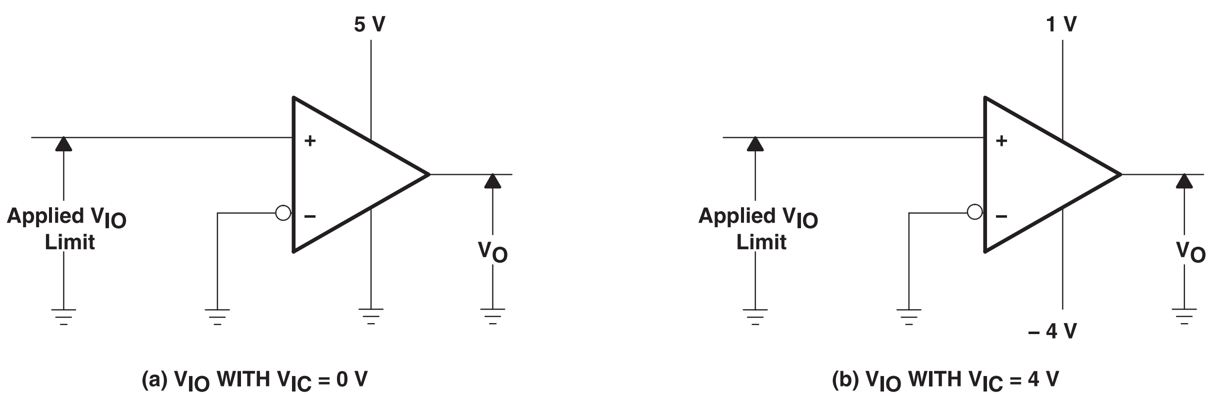


Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION (continued)

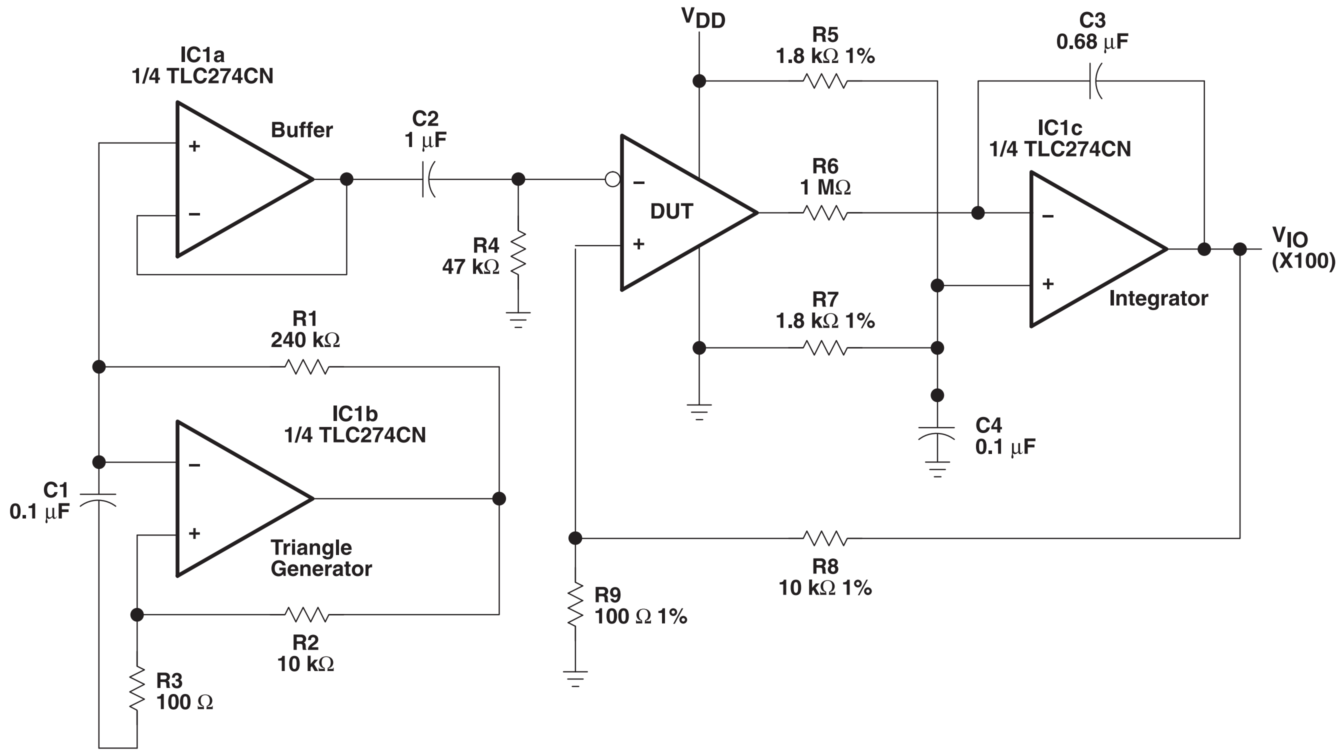
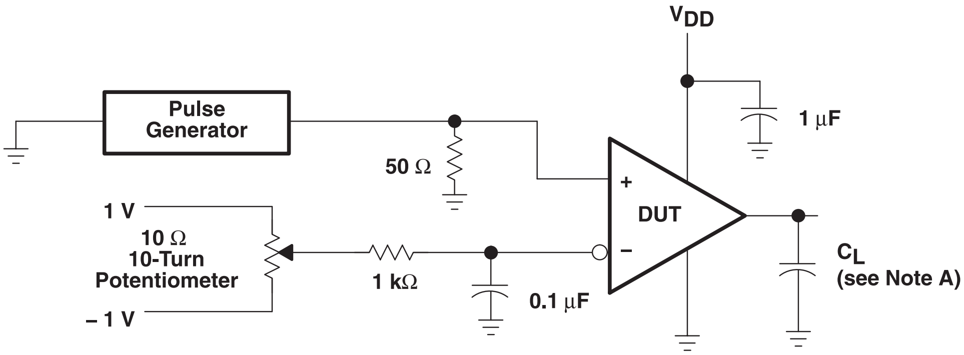


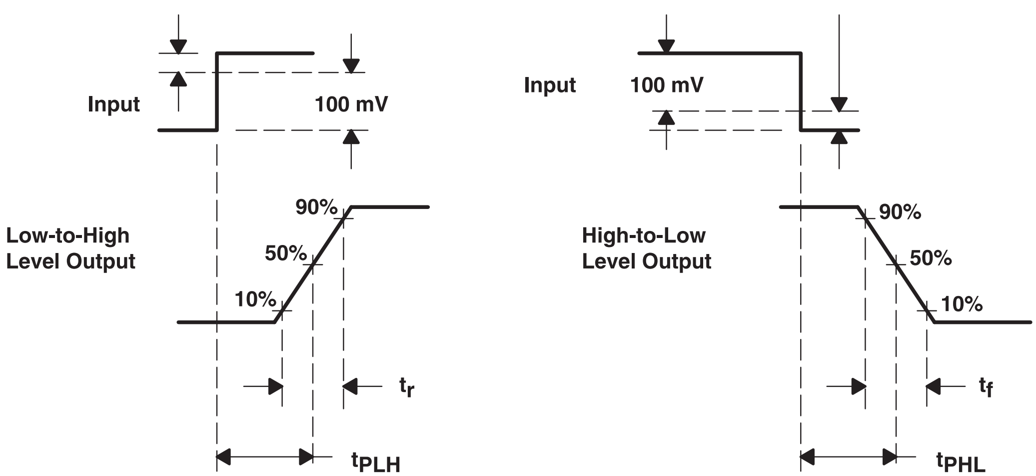
Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 8
I_{IB}	Input bias current	vs Free-air temperature	Figure 9
CMRR	Common-mode rejection ratio	vs Free-air temperature	Figure 10
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	Figure 11
V_{OH}	High-level output current	vs Free-air temperature	Figure 12
		vs High-level output current	Figure 13
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 14
		vs Free-air temperature	Figure 15
t_t	Transition time	vs Load capacitance	Figure 16
	Supply current response	vs Time	Figure 17
	Low-to-high-level output response	Low-to-high level output propagation delay time	Figure 18
	High-to-low level output response	High-to-low level output propagation delay time	Figure 19
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	Figure 20
t_{PHL}	High-to-low level output propagation delay time	vs Supply voltage	Figure 21
I_{DD}	Supply current	vs Frequency	Figure 22
		vs Supply voltage	Figure 23
		vs Free-air temperature	Figure 24

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

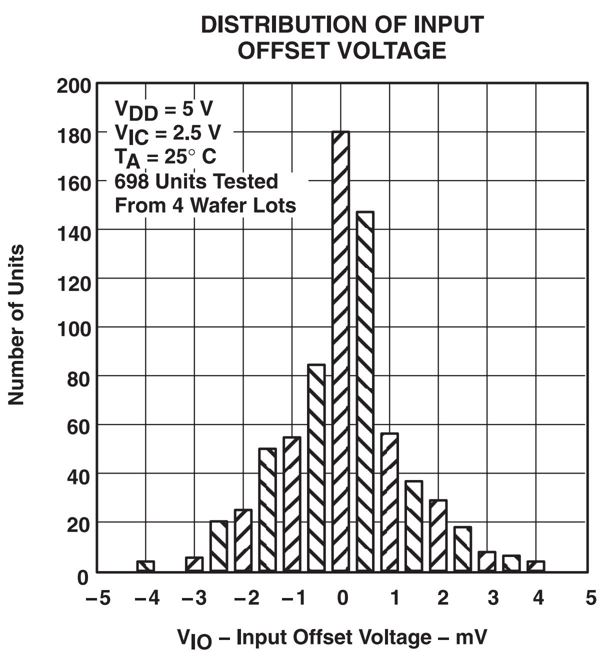


Figure 8.

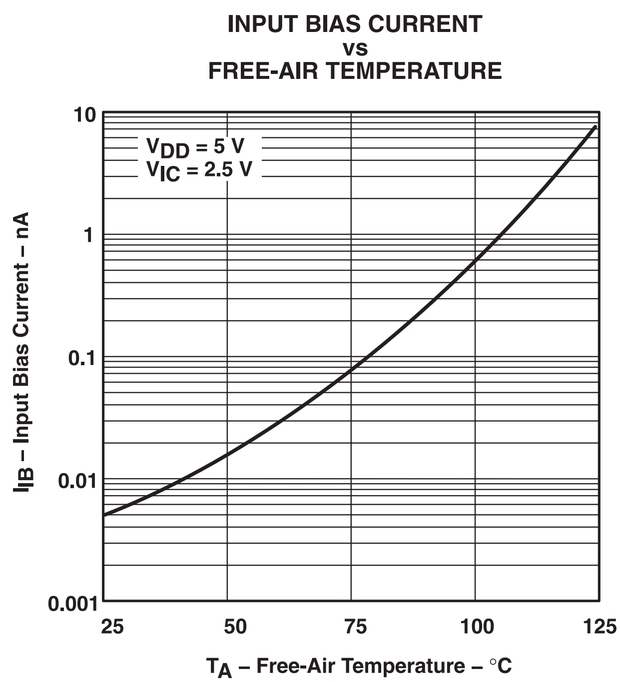


Figure 9.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

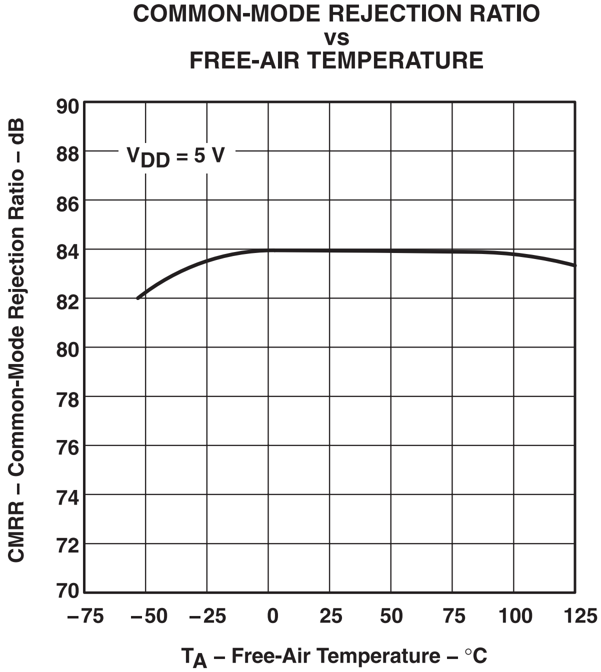


Figure 10.

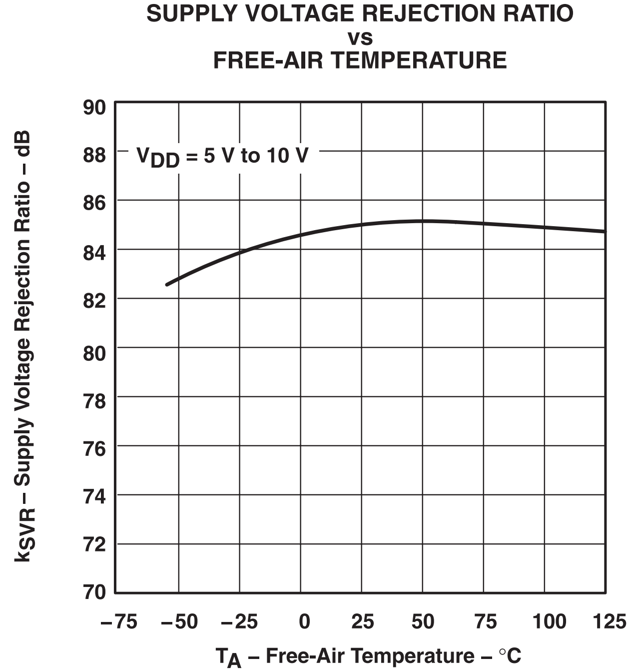


Figure 11.

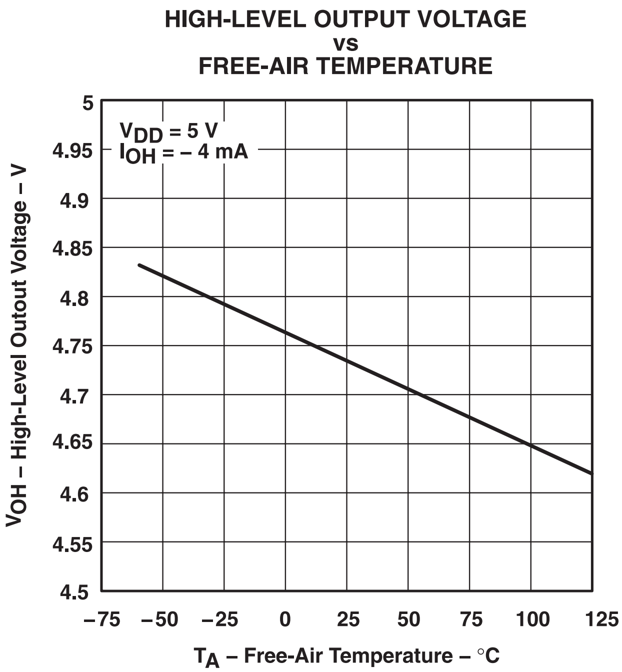


Figure 12.

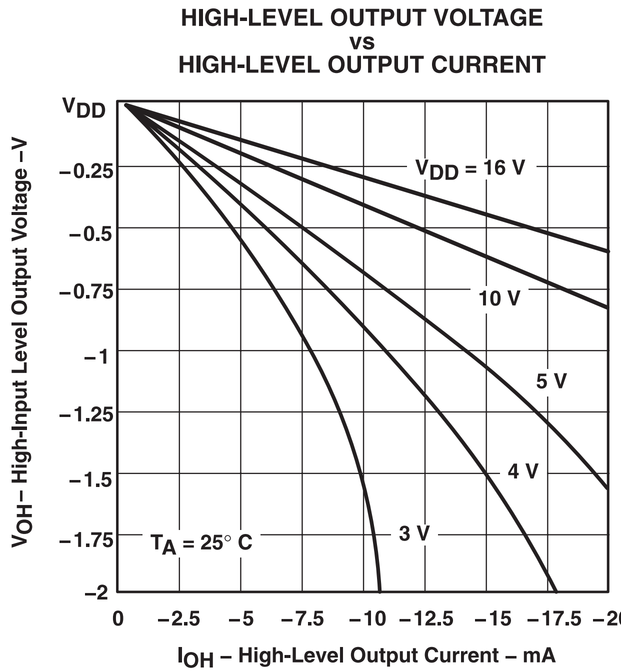


Figure 13.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

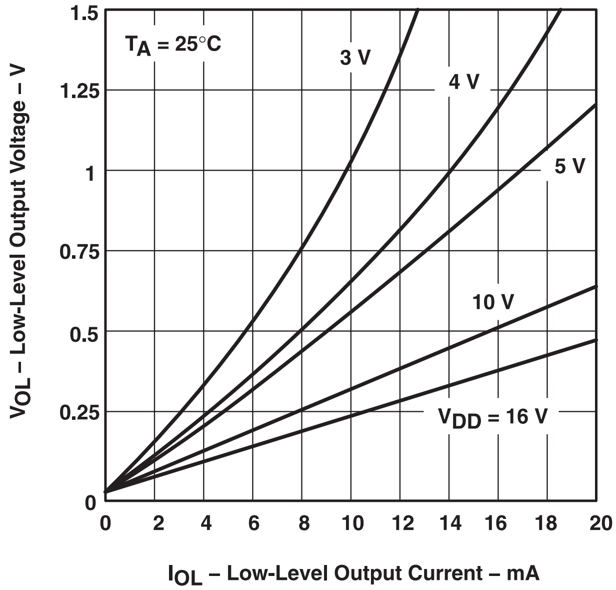


Figure 14.

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

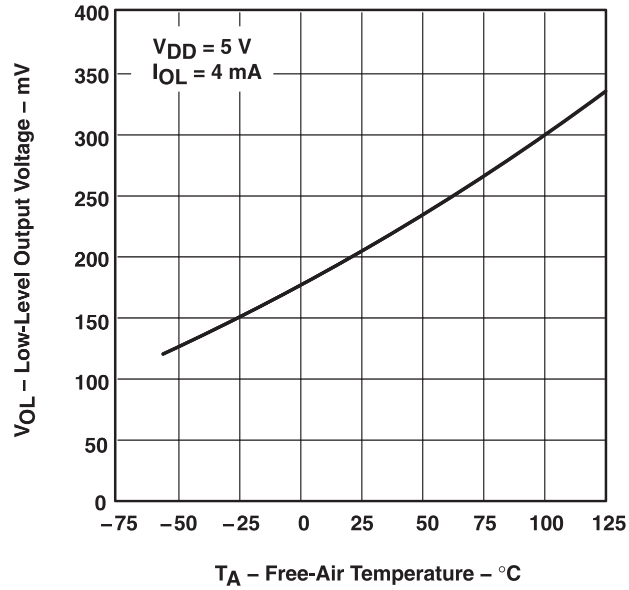


Figure 15.

OUTPUT TRANSITION TIME
vs
LOAD CAPACITANCE

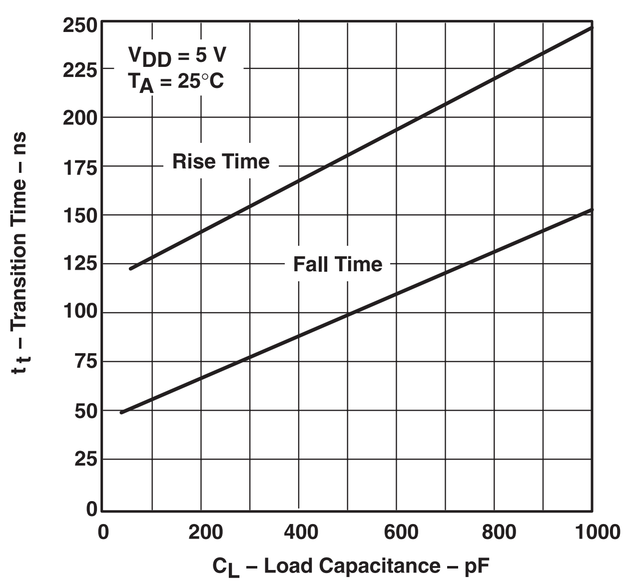


Figure 16.

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

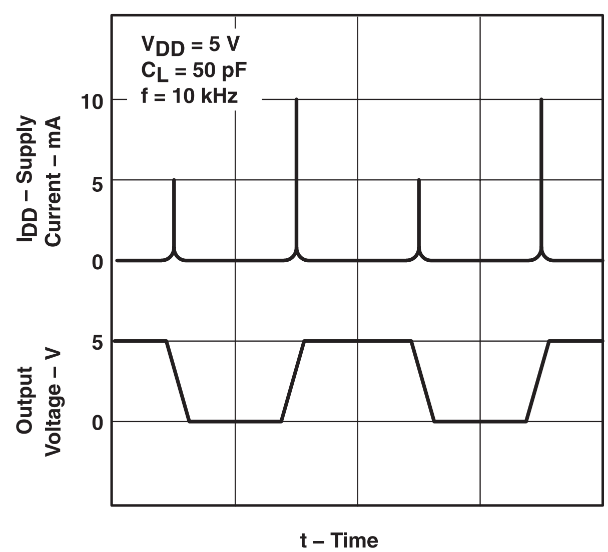


Figure 17.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

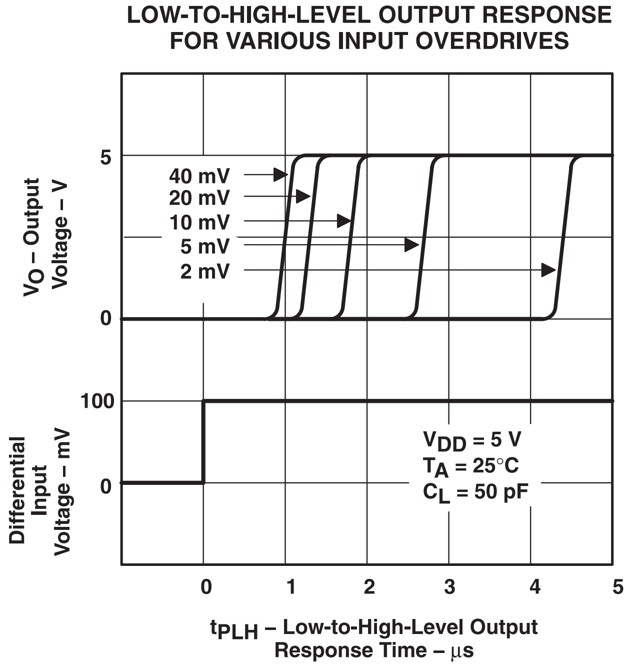


Figure 18.

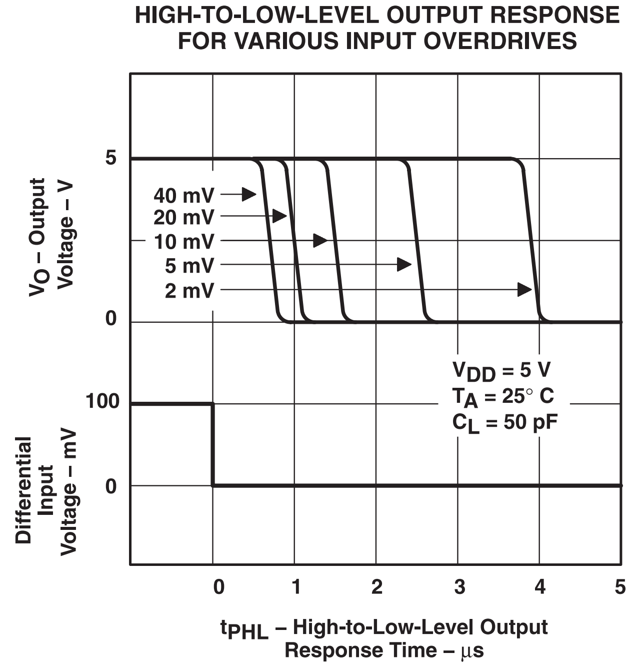


Figure 19.

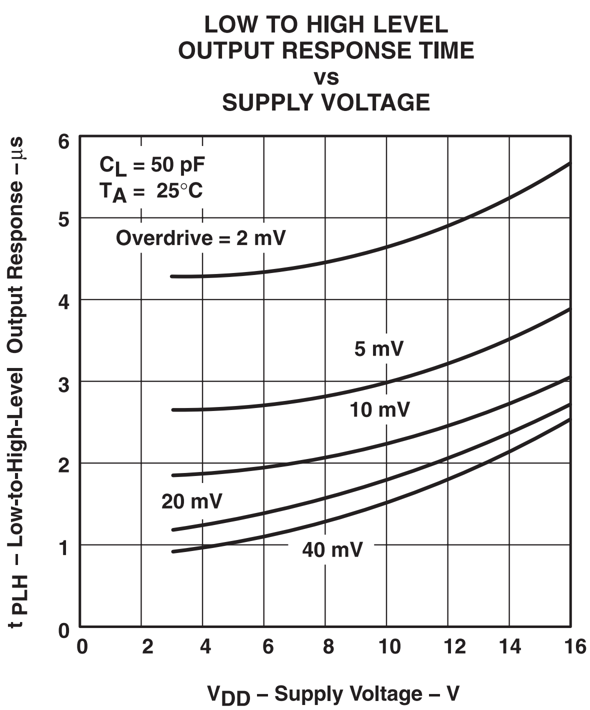


Figure 20.

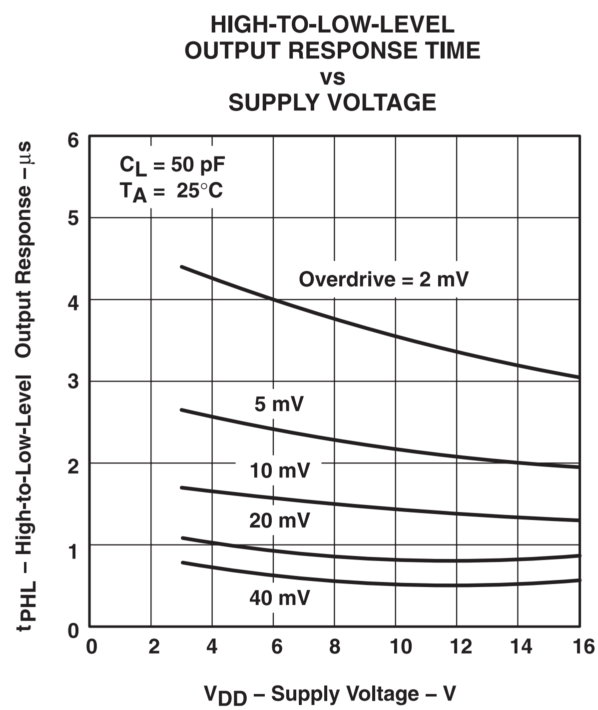


Figure 21.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY

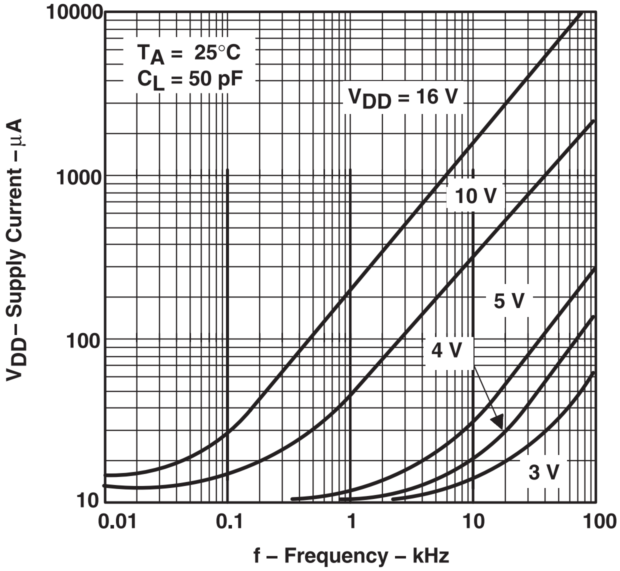


Figure 22.

SUPPLY CURRENT vs SUPPLY VOLTAGE

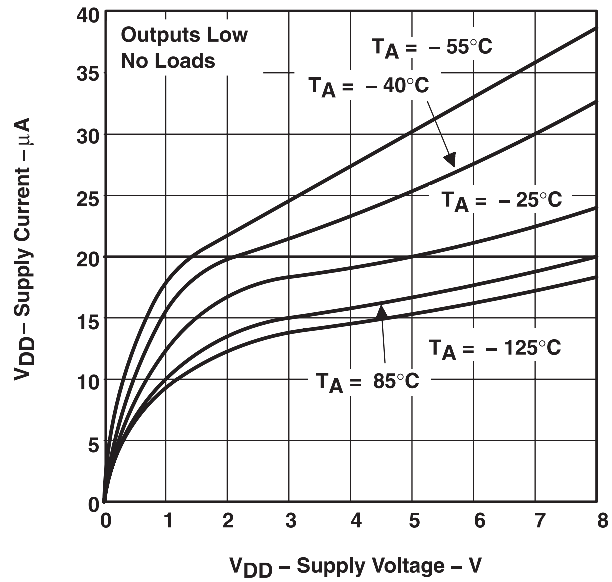


Figure 23.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

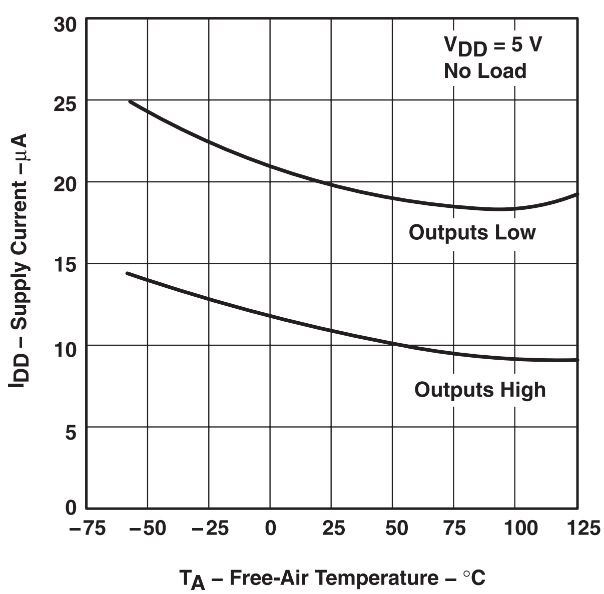


Figure 24.

APPLICATION INFORMATION

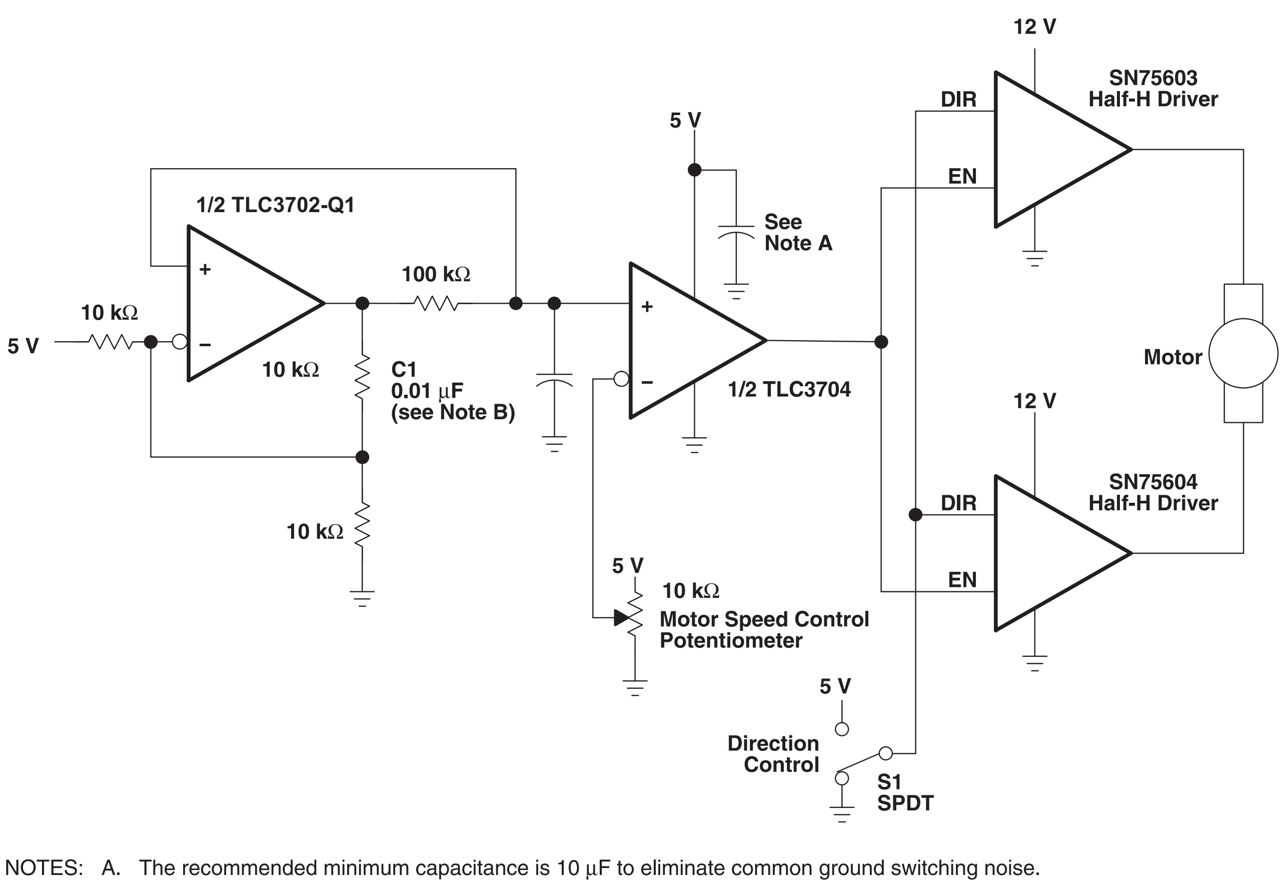
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) that is positioned as close to the device as possible.

The TLC3702-Q1 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

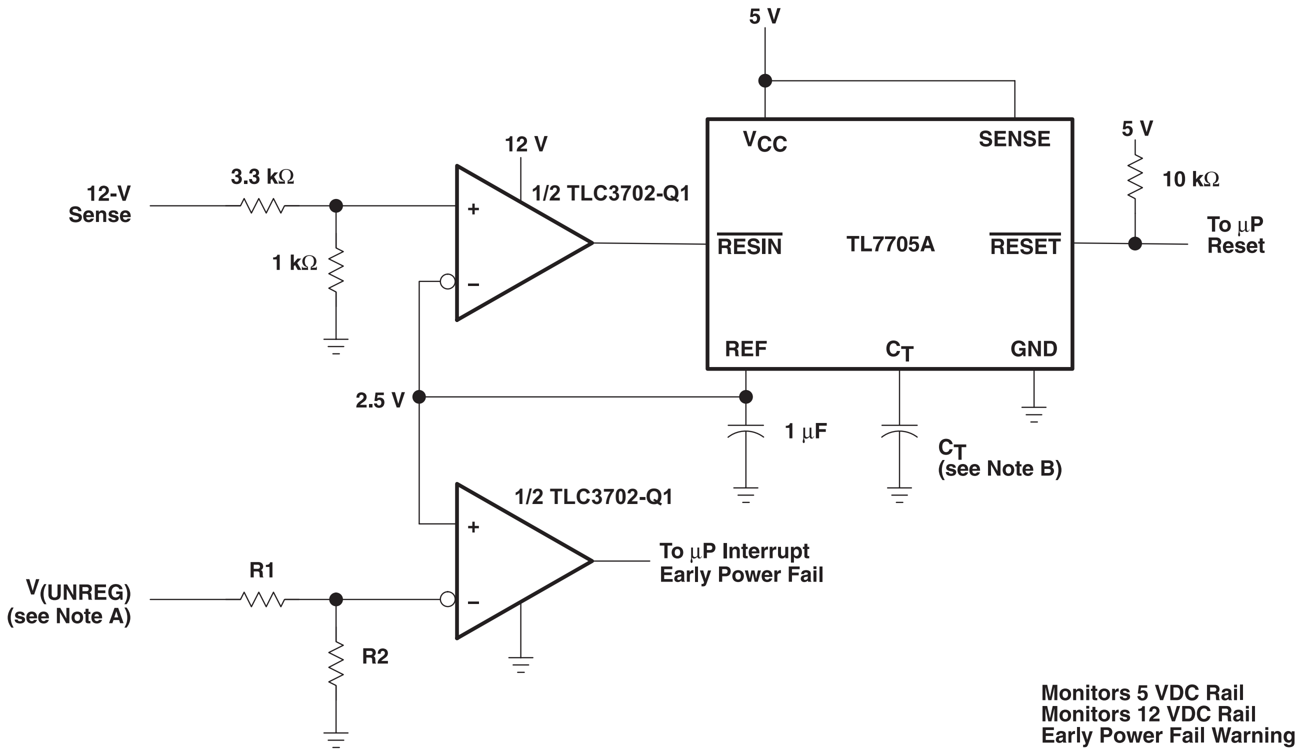
Table 1. Applications

	FIGURE
Pulse-width-modulated motor speed controller	25
Enhanced supply supervisor	26
Two-phase non-overlapping clock generator	27
Micropower switching regulator	28



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

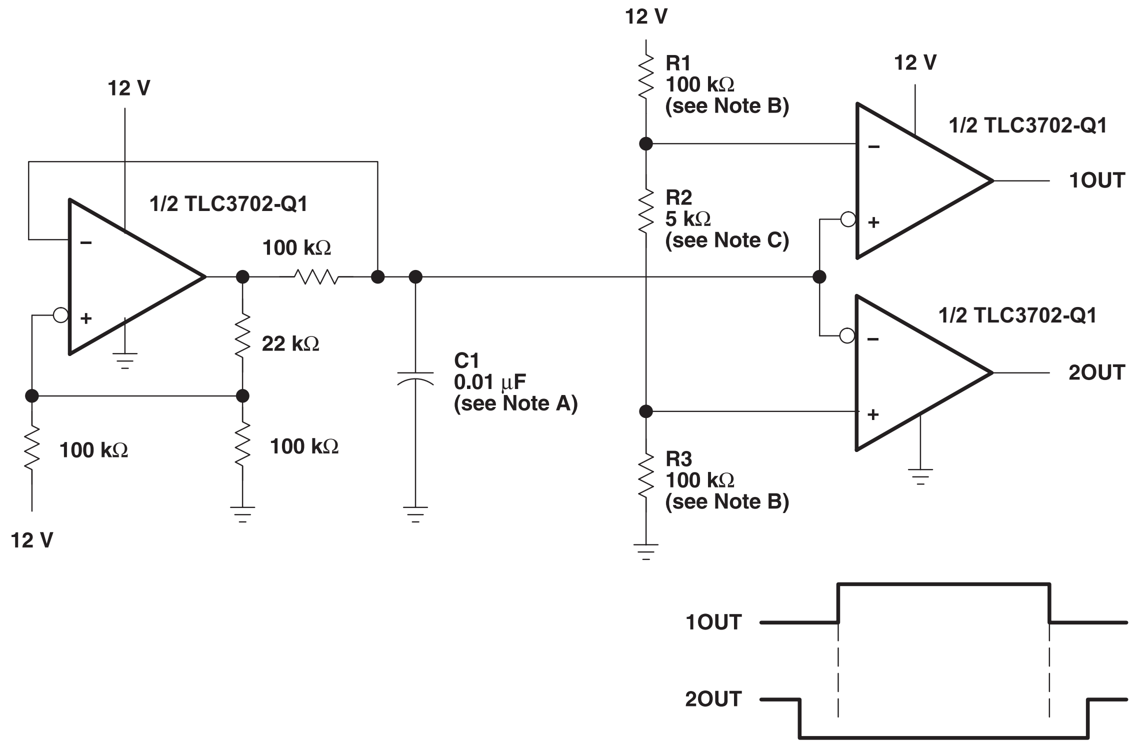
Figure 25. Pulse-Width-Modulated Motor Speed Controller



NOTES: A. $V_{(UNREG)} = 2.5\frac{(R1 + R2)}{R2}$

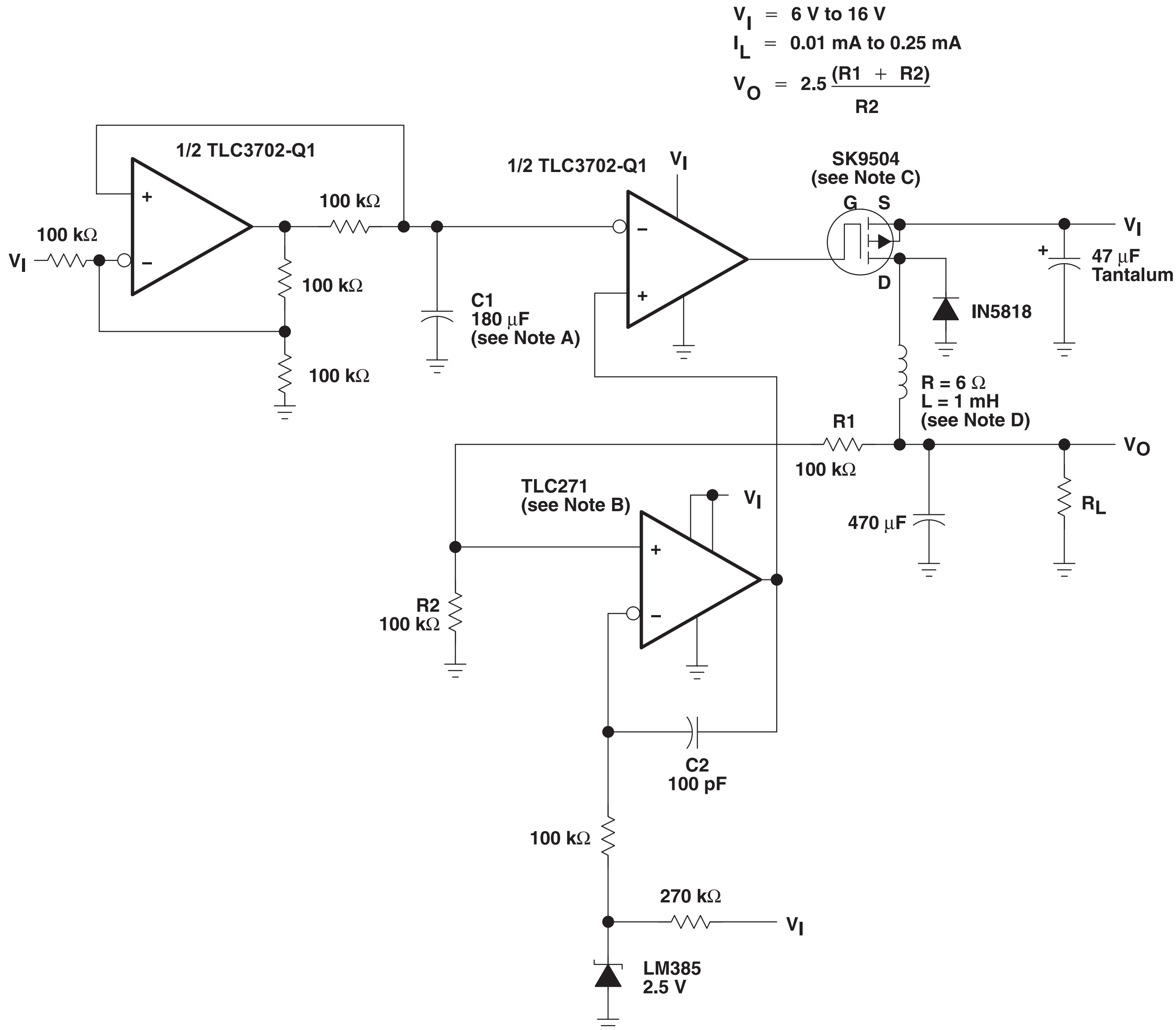
B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor



NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Enhanced Supply Supervisor



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator

REVISION HISTORY

Changes from Revision D (February, 2012) to Revision E	Page
• Changed part numbers from TLC3702 to TLC3702-Q1	1
• Changed units for I_{IB} from dB to pA and nA	3

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC3702QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1	Samples
TLC3702QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1	Samples
TLC3702QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	3702Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TLC3702-Q1 :

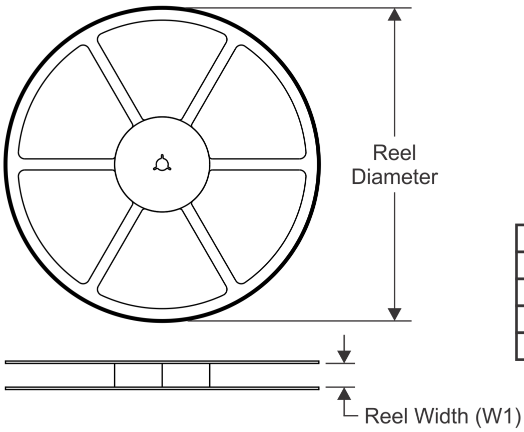
- Catalog: TLC3702
- Enhanced Product: TLC3702-EP
- Military: TLC3702M

NOTE: Qualified Version Definitions:

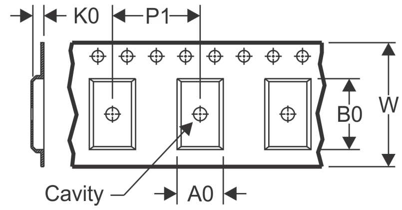
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

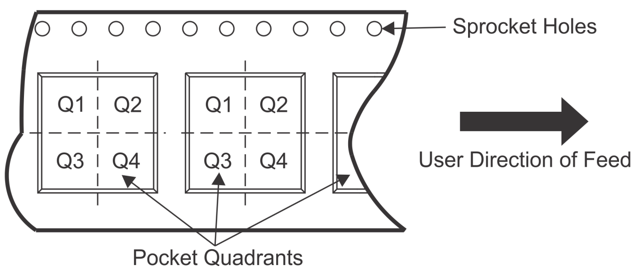


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

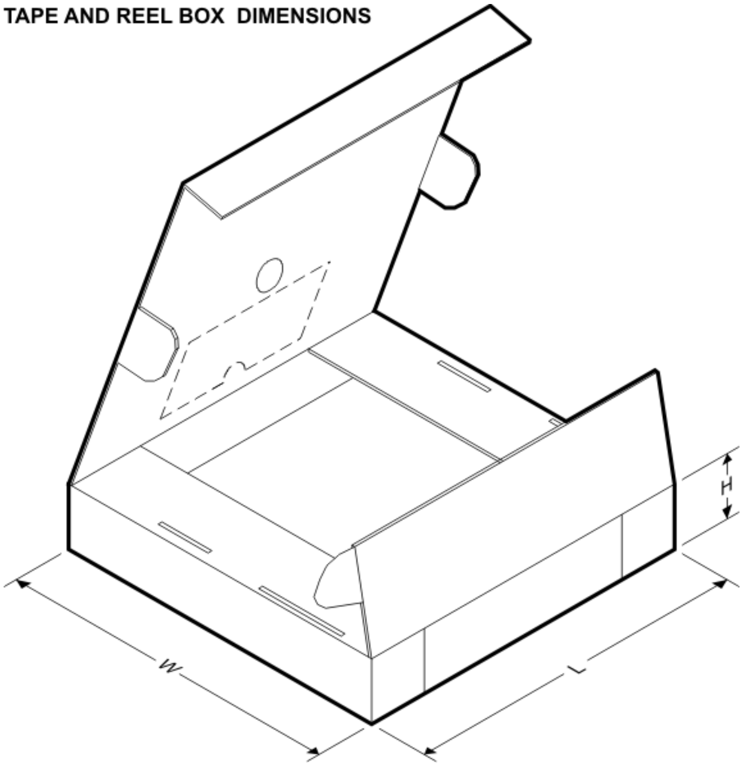
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

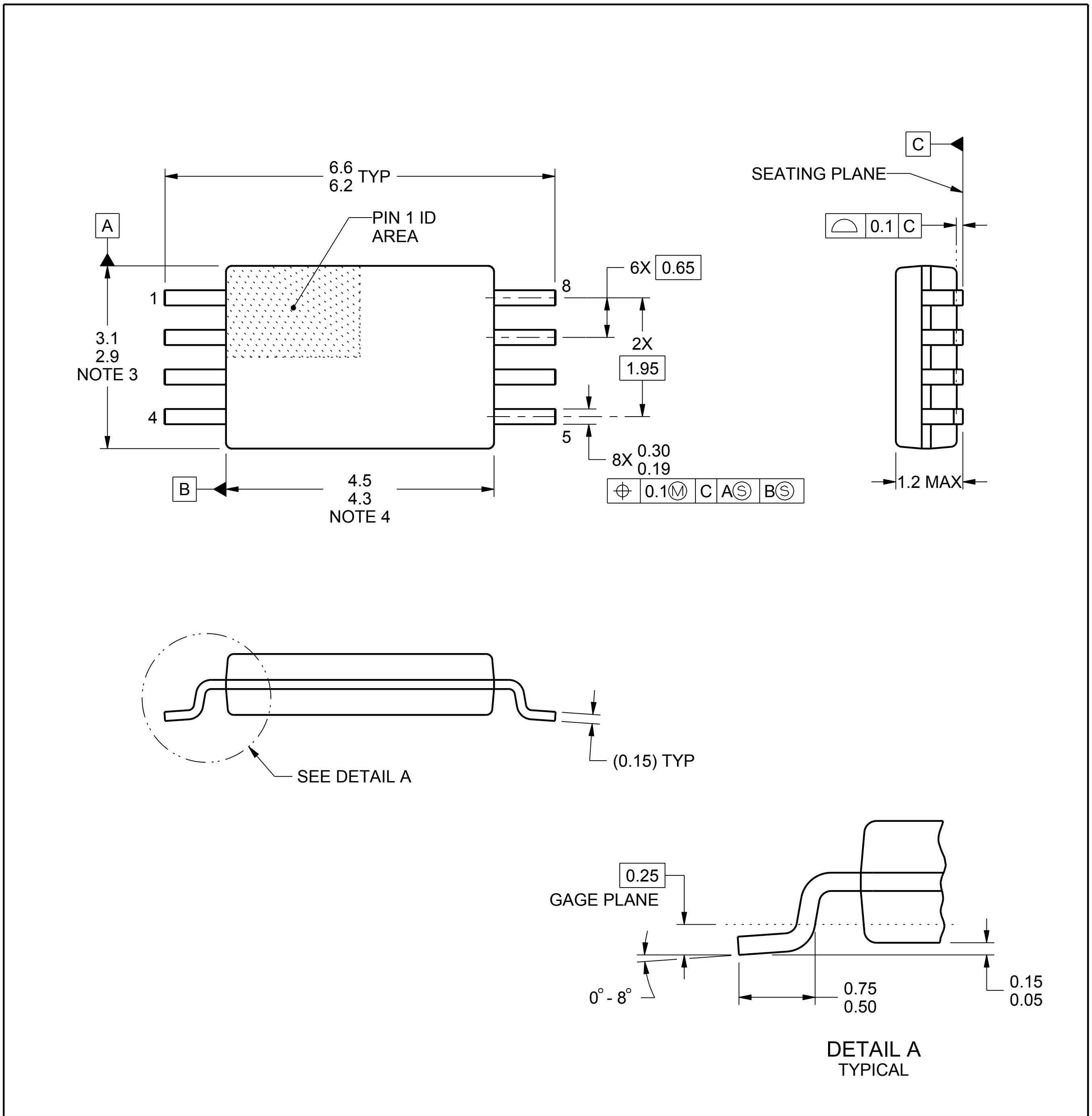
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3702QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3702QPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0



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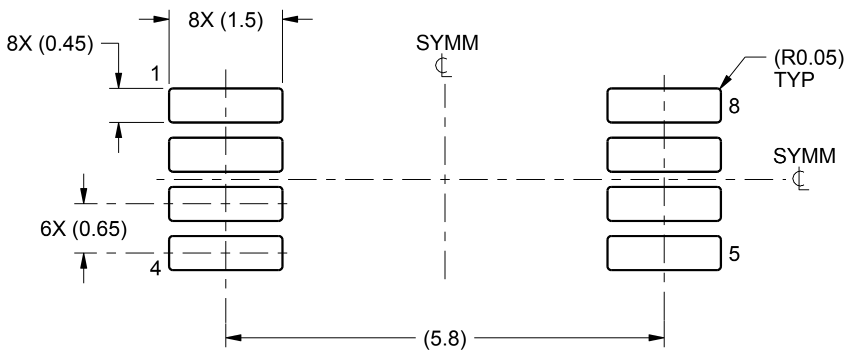
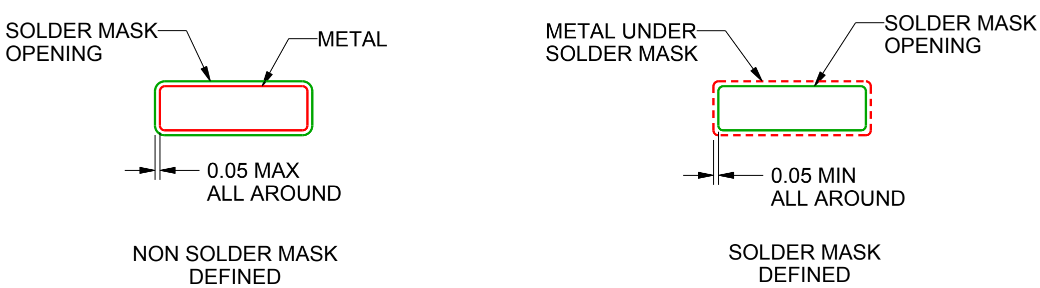
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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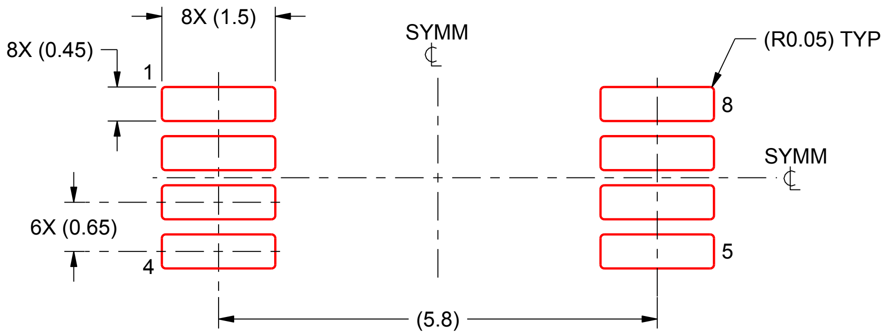
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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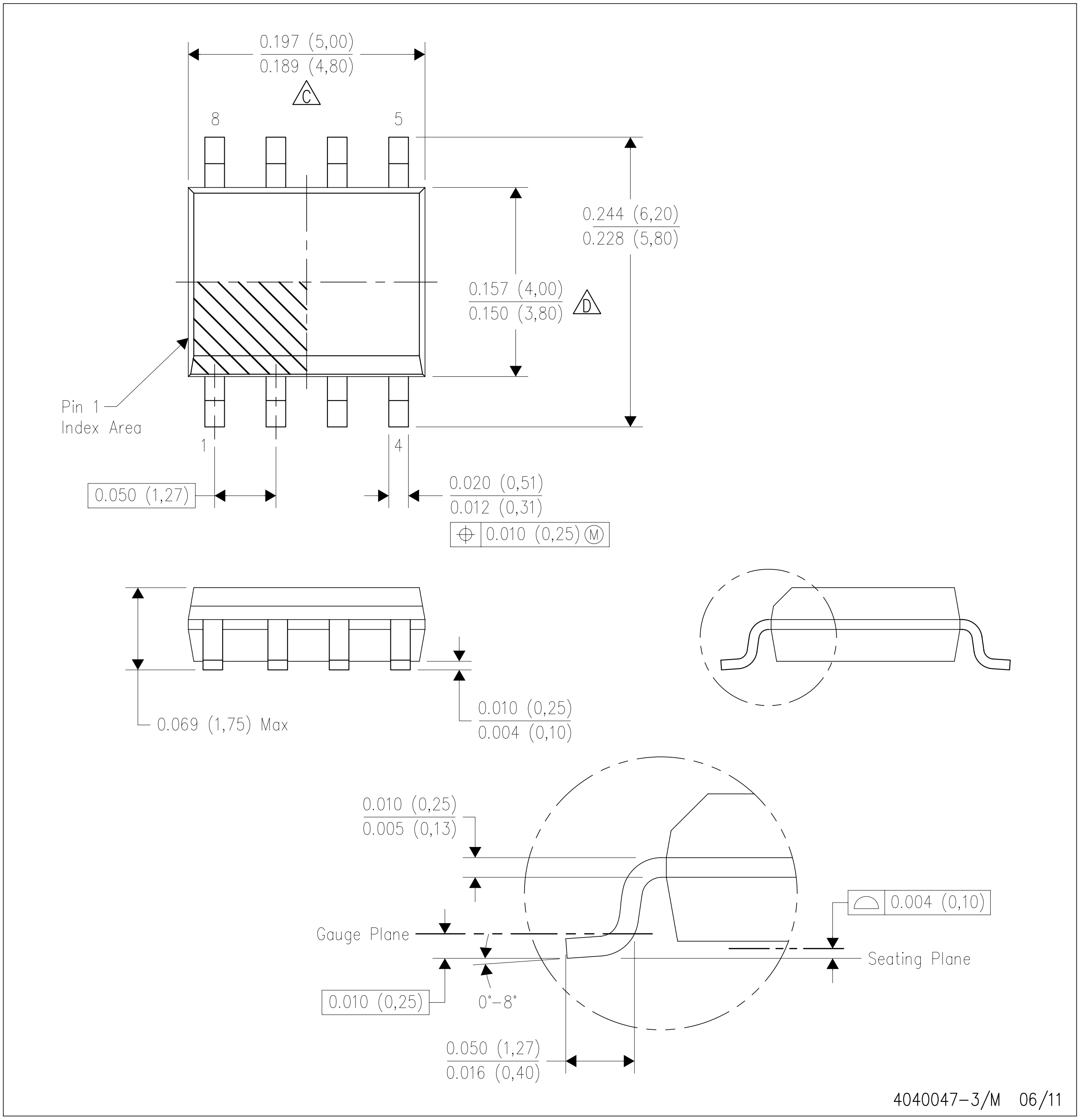
NOTES: (continued)

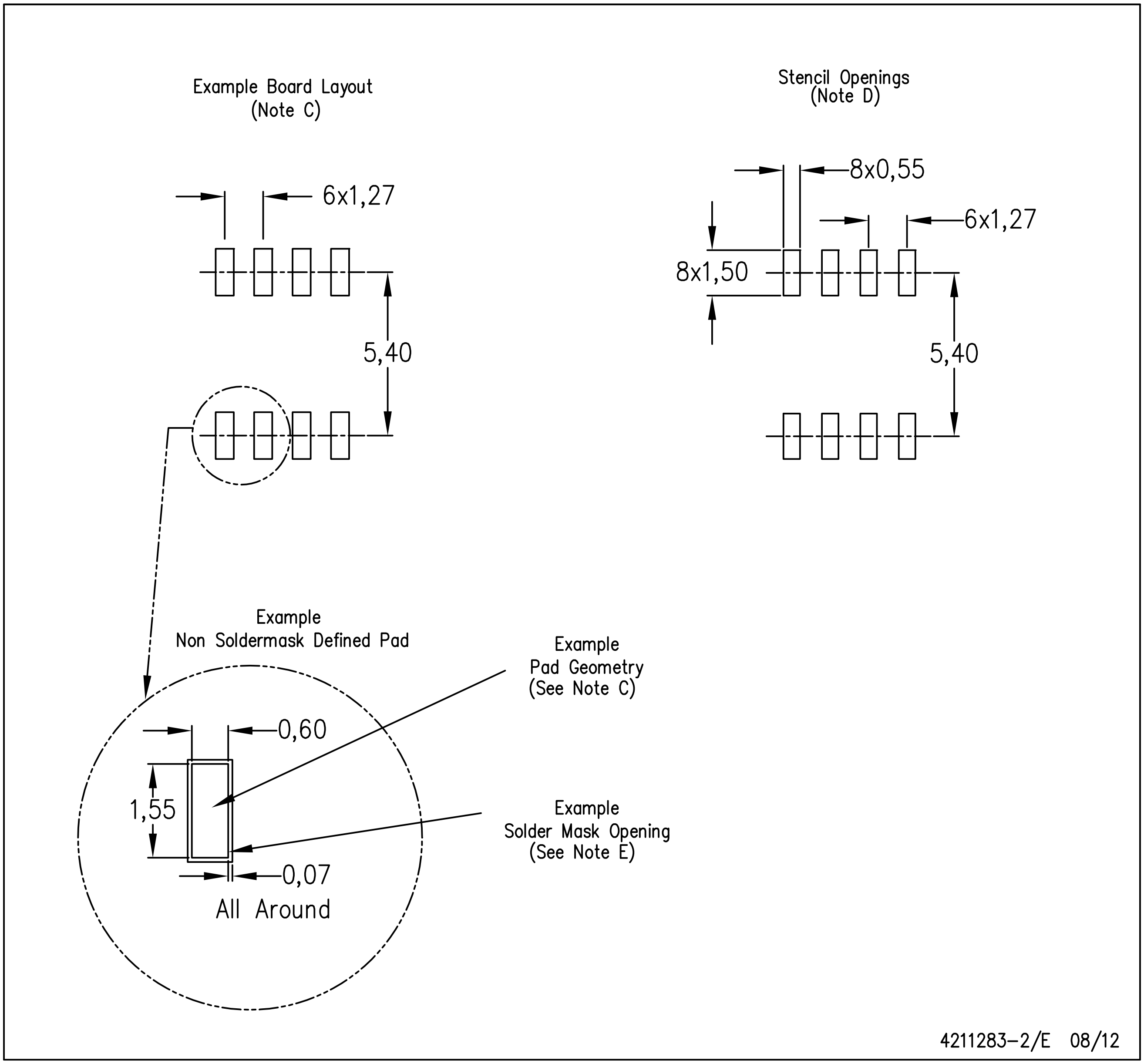
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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