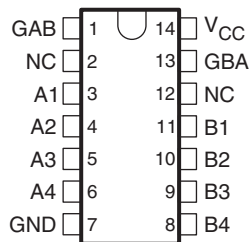# QUADRUPLE BUS TRANSCEIVERS

FEATURES

- **Two-Way Asynchronous Communication Between Data Buses**
- **PNP Inputs Reduce D-C Loading**
- **Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin**

SN54LS243 . . . J OR W PACKAGE
SN74LS243 . . . D, N, OR NS PACKAGE
(TOP VIEW)

GAB	1	14	V_{CC}
NC	2	13	GBA
A1	3	12	NC
A2	4	11	B1
A3	5	10	B2
A4	6	9	B3
GND	7	8	B4

FUNCTION TABLE
(EACH TRANSCEIVER)

INPUTS		SNxxLS243
$\overline{GAB}$	GBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

DESCRIPTION

These four-data-line transceivers are designed for asynchronous two-way communications between data buses. SN74LS243 can be used to drive terminated lines down to 133 Ω.

SN54LS243 is characterized for operation over the full military temperature range of –55°C to 125°C. SN74LS243 is characterized for operation from 0°C to 70°C.

SCHEMATICS OF INPUTS AND OUTPUTS

TYPICAL OF ALL OUTPUTS

V_{CC}
17 kΩ
INPUT

EQUIVALENT OF EACH INPUT

V_{CC}
50 Ω NOM
OUTPUT
GND
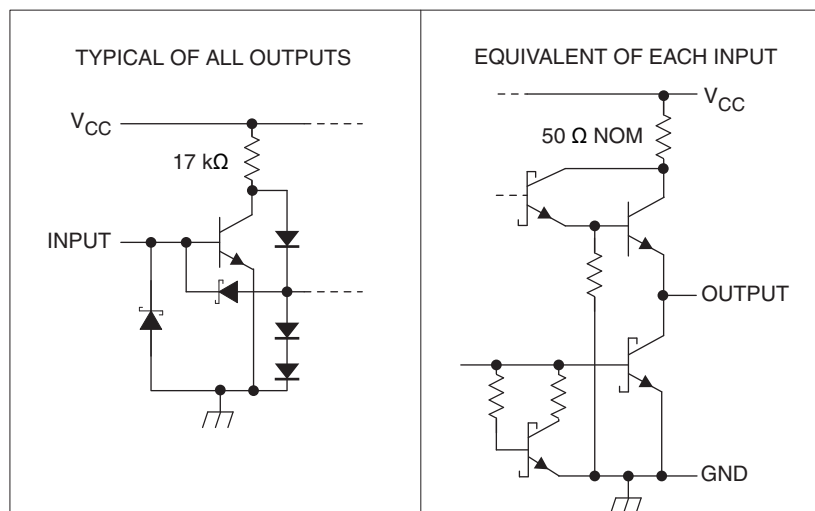
⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC SYMBOL
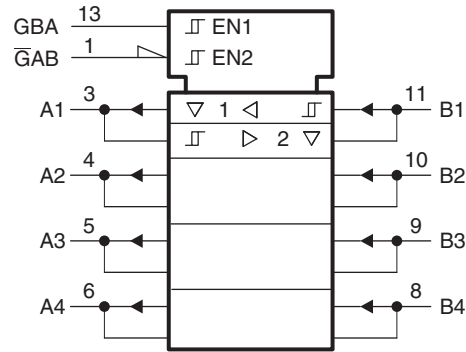
A.   These symbols are in accordance with ANSI/EEE Std. 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)

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Product Folder Link(s): *SN54LS243 SN74LS243*
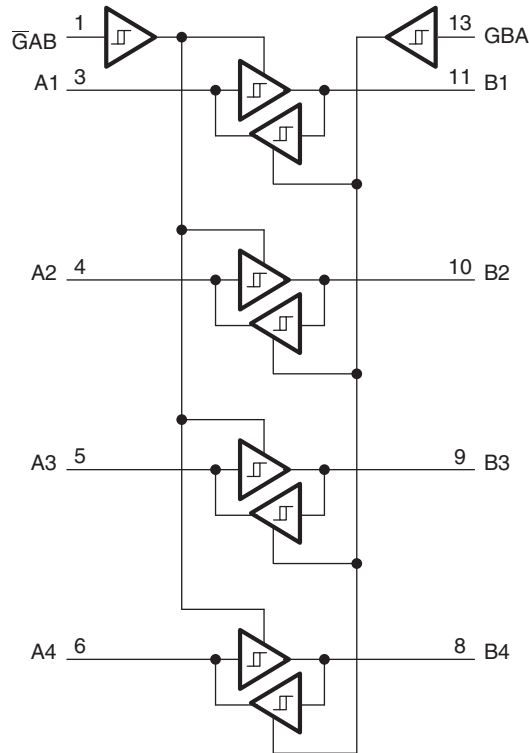
ABSOLUTE MAXIMUM RATINGS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			7	V
V_{IN}	Input voltage			7	V
	OFF-state output voltage			5.5	V
T_A	Operating free-air temperature range	SN54LS243	−55	125	°C
		SN74LS243	0	70	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		SN54LS243			SN74LS243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage[1]	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output voltage			−12			−15	mA
I_{OL}	Low-level output voltage			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

(1) Voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		SN54LS243			SN74LS243			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IK}	A or B	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
Hysteresis (V_{T+} − V_{T-})		V_{CC} = MIN,		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OH} = −3 mA	2.4	3.1		2.4	3.1		V
			V_{IL} = 0.5 V, I_{OH} = MAX	2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	V_O = 2.7 V			40			40	µA
I_{OZL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,	V_O = 0.4 V			−200			−200	µA
I_I	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
	$\overline{GAB}$ or GBA		V_I = 7 V			0.1			0.1	
I_{IH}		V_{CC} = MAX,				20			20	µA
I_{IL}	A inputs	V_{CC} = MAX, V_I = 0.4 V, GAB and GBA at 0 V				−0.2			−0.2	mA
	B inputs	V_{CC} = MAX, V_I = 0.4 V, GAB and GBA at 4.5 V				−0.2			−0.2	
	$\overline{GAB}$ or GBA	V_{CC} = MAX, V_I = 0.4 V,				−0.2			−0.2	
I_{OS}		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Outputs high	V_{CC} = MAX,[3] Outputs open,			22	38		22	38	mA
	Outputs low				29	50		29	50	
	All outputs disabled				32	54		32	54	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under "recommended operating conditions."
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) I_{CC} is measured with transceivers eabled in one direction only, or with all transceivers disabled.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		SN54LS243			SN74LS243			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω,	C_L = 45 pF		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}				20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	R_L = 667 Ω,	C_L = 5 pF		10	20		10	20	ns
t_{PHZ}				15	25		15	25	ns

Product Folder Link(s): SN54LS243 SN74LS243

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
80020022A	OBSOLETE			20		TBD	Call TI	Call TI	-55 to 125		
8002002CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002002CA SNJ54LS243J	Samples
8002002DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002002DA SNJ54LS243W	Samples
SN54LS243J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS243J	Samples
SN74LS243D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS243	Samples
SN74LS243DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS243	Samples
SN74LS243J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN74LS243N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS243N	Samples
SN74LS243N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS243NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS243N	Samples
SNJ54LS243FK	OBSOLETE			20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS243J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002002CA SNJ54LS243J	Samples
SNJ54LS243W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002002DA SNJ54LS243W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS243, SN74LS243 :

• Catalog: SN74LS243

• Military: SN54LS243

NOTE: Qualified Version Definitions:

  • Catalog - TI's standard catalog product

  • Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS243DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS243DR	SOIC	D	14	2500	367.0	367.0	38.0

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R–GDFP–F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.260 (6,60) / 0.235 (5,97)

0.080 (2,03) / 0.045 (1,14)

0.008 (0,20) / 0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48) / 0.015 (0,38)

0.050 (1,27)

0.390 (9,91) / 0.335 (8,51)

0.005 (0,13) MIN
4 Places

0.360 (9,14) / 0.250 (6,35)

0.360 (9,14) / 0.250 (6,35)

4040180–2/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL STD 1835 GDFP1–F14

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N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

$\dfrac{0.344\ (8,75)}{0.337\ (8,55)}$ Ⓒ

14   8

$\dfrac{0.244\ (6,20)}{0.228\ (5,80)}$

$\dfrac{0.157\ (4,00)}{0.150\ (3,80)}$ Ⓓ

1   7

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

$\dfrac{0.010\ (0,25)}{0.004\ (0,10)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

0.004 (0,10)

Gauge Plane

0.010 (0,25)   0°−8°

Seating Plane

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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