



TPA6139A2

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TPA6139A2 DirectPath[™] 25-mW Headphone Amplifier With Programmable-Fixed Gain

Technical

Documents

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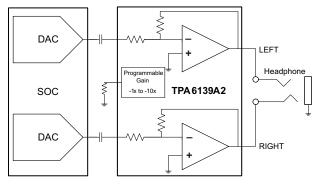
1 Features

- DirectPath[™]
 - Eliminates Pops and Clicks
 - Eliminates Output DC-Blocking Capacitors
 - 3-V to 3.6-V Supply Voltage
- Low Noise and THD
 - SNR > 105 dB at -1x Gain
 - Typical Vn < 15 μVms 20 to 20 kHz at –1x Gain
 - THD+N < 0.003% at 10-k Ω Load and –1x Gain
- 25 mW into 32-Ω Load
- 2-Vrms Output Voltage into 600-Ω Load
- Single-Ended Input and Output
- Programmable Gain Select Reduces Component Count
 - 13x Gain Values
- Active Mute With More Than 80-dB Attenuation
- Short-Circuit and Thermal Protection
- ±8-kV HBM ESD Protected Outputs

2 Applications

- PDP and LCD TVs
- Blu-ray Discs[™], DVD Players
- Mini and Micro Combo Systems
- Soundcards

Functional Block Diagram



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3 Description

Tools &

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The TPA6139A2 is a 25-mW, pop-free stereo headphone driver designed to reduce component count, board space and cost. It is ideal for single-supply electronics where size and cost are critical design parameters.

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The TPA6139A2 device does not require a power supply greater than 3.3 V to generate its 25 mW, nor does it require a split rail power supply.

The TPA6139A2 device was designed using TI's patented DirectPathTM technology, which integrates a charge pump to generate a negative supply rail that provides a clean, pop-free ground biased output. The TPA6139A2 is capable of driving 25 mW into a 32- Ω load and 2 Vrms into a 600- Ω load. DirectPath also allows the removal of the costly output DC-blocking capacitors.

The device has fixed gain single-ended inputs with a gain select pin. Using a single resistor on this pin, the designer can choose from 13 internal programmable gain settings to match the line driver with the CODEC output level. It also reduces the component count and board space.

Headphone outputs have ±8-kV HBM ESD protection enabling a simple ESD protection circuit. The TPA6139A2 has built-in active mute control with more that 80-dB attenuation for pop-free mute ON and OFF control.

The TPA6139A2 device is available in a 14-pin TSSOP and a 16-pin QFN. For a pin-compatible, 2-Vrms line driver see DRV612.

Device Information ⁽¹⁾					
PART NUMBER	PACKAGE	BODY SIZE (NOM)			
TPA6139A2	TSSOP (14)	5.00 mm × 4.40 mm			
1PA0139A2	VQFN (16)	3.00 mm × 3.00 mm			

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

2

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2011) to Revision C

•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
•	Removed Ordering Information table	1
•	Changed 600- Ω Load value to 32- Ω Load in <i>Features</i>	1
•	Changed 5-kΩ Load value to 600-Ω Load in <i>Features</i>	1
•	Changed 2 Vms to 2 Vrms in Description	1
•	Added R _L valuse for the MIN and MAX columns and changed the TYP value from 5 to 32 in the <i>Recommended Operating Conditions</i>	4
•	Changed Line Driver Amplifiers subsection title to DirectPath Headphone Driver	9

Cł	nanges from Original (January 2011) to Revision A	Page
•	Changed "2.5-mW" to "25-mW" in Title line and added revision A - May 2011 pub date to Header infomation	1
•	Changed conditions statement from " $R_{IN} = 10 \text{ k}\Omega$, $R_{fb} = 20 \text{ k}\Omega$ " to "Step = $-2V/V$ " for TYP CHARA, LINE DRIVER section	7



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OUT_R

GAIN

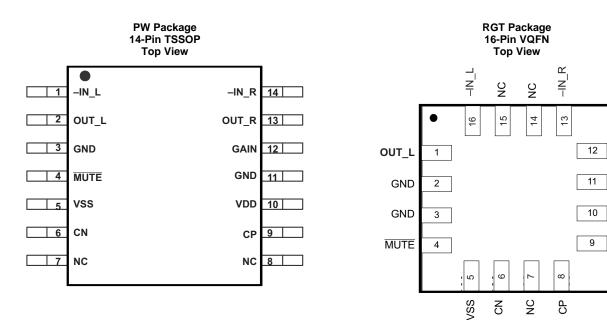
GND

VDD

5 Device Comparison Table

	TPA6132A2	TPA6136A2	TPA6139A2	TPA6141A2
Headphone Channels	Stereo	Stereo	Stereo	Stereo
Output Power (W)	0.025	0.025	0.025	0.025 2.5 to 5.5
Supply Voltage Range	2.3 to 5.5	2.3 to 5.5	3 to 3.6	
PSRR (dB)	100	100	80	105
Pin and Package	16-pin WQFN	16-pin DSBGA	16-pin VQFN, 14-pin TSSOP	16-pin DSBGA

6 Pin Configuration and Functions



Pin Functions

	PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	TSSOP	VQFN	TTPE	DESCRIPTION
CN	6	6	I/O	Charge Pump flying capacitor negative connection
СР	9	8	I/O	Charge Pump flying capacitor positive connection
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See Table 2 for recommended resistor values
GND	3, 11	2, 3, 10	Р	Ground
-IN_L	1	16	I	Negative input, left channel
-IN_R	14	13	I	Negative input, right channel
MUTE	4	4	I	MUTE, active low
NC	7, 8	7. 14, 15	—	No internal connection
OUT_L	2	1	0	Output, left channel
OUT_R	13	12	0	Output, right channel
VDD	10	9	Р	Supply voltage, connect to positive supply
VSS	5	5	0	Change Pump negative supply voltage

(1) I = input, O = output, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
VDD to GND	-0.3	4	V
Input voltage, V _I	VSS – 0.3	VDD + 0.3	V
MUTE to GND	-0.3	VDD + 0.3	V
Maximum operating junction temperature, T _J	-40	150	°C
Lead temperature		260	°C
Storage temperature, T _{stg}	-40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT	
TPA613	9A2 IN PW PACKAC	3E				
Electrostatic		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except 2 and 13	±4000		
V _(ESD)	Electrostatic discharge	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 2 and 13	±8000	V	
	disonarge	Charged-device model (CDM), per JEDE	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾			
TPA613	9A2 IN RGT PACKA	GE		, , , , , , , , , , , , , , , , , , , ,		
		Human-body model (HBM), per	All pins except 1 and 12	±4000		
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 1 and 12	±8000	V	
. ,	uistinarye	Charged-device model (CDM), per JEDE	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾			

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3	3.3	3.6	V
RL	Load resistance		16	32	10000	Ω
VIL	Low-level input voltage	MUTE	38	40	43	%PVDD
VIH	High-level input voltage	MUTE	57	60	66	%PVDD
T _A	Free-air temperature		-40	25	85	°C

7.4 Thermal Information

		TPA6	139A2	
	THERMAL METRIC ⁽¹⁾	PW (TSSOP)	RGT (VQFN)	UNIT
		14 PINS	16 PINS	
R _{0JA}	Junction-to-ambient thermal resistance	130	52	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	49	71	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	26	°C/W
ΨJT	Junction-to-top characterization parameter	3.6	3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62	26	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.



7.5 Electrical Characteristics

VDD = 3.3 V, R_{Load} = 32 Ω , T_A = 25°C, Charge pump: C_{CP} = 1 μ F (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
V _{OS}	Output offset voltage	VDD = 3.3 V, input AC-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V _{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V _{OL}	Low-level output voltage	VDD = 3.3 V			-3.05	V
Vuvp_on	PVDD, under voltage detection				2.8	V
Vuvp_hysteresis	PVDD, under voltage detection, hysteresis			200		mV
Fcp	Charge pump switching frequency			350		kHz
І _{ін}	High-level input current, MUTE	$VDD = 3.3 V, V_{IH} = VDD$			1	μA
I _{IL}	Low-level input current, MUTE	VDD = 3.3 V, V _{IL} = 0 V			1	μA
I (VDD)	Supply current, no load	VDD, $\overline{\text{MUTE}} = 3.3 \text{ V}$		25		mA
	Supply current, MUTED	$VDD = 3.3 V, \overline{MUTE} = GND$		25		mA
Tsd	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C
Po	Output Power, outputs in phase	THD+N = 1%, f = 1 kHz, 32-Ω load		25		mW
M		THD+N = 1%, f = 1 kHz, 32-Ω load		0.9		V _{rms}
Vo	Output Voltage, outputs in phase	THD+N = 1%, f = 1 kHz, 600-Ω load		2	2	
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 32- Ω load, Po = 25 mW, -1x gain	0.	03%		
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 10-kΩ load, Vo = 2 Vrms, $-1x$ gain	0.0	05%		
ΔA_V	Gain matching	Between left and right channels		0.25		dB
Z _O	Output impedance when muted	MUTE = GND			1	Ω
	Input to output attenuation when muted	MUTE = GND		80		dB
SNR	Signal to noise ratio	A-weighted, AES17 filter, 1-Vrms ref 32- Ω load, -1x gain		99		dB
	Signal to noise ratio	A-weighted, AES17 filter, 2-Vrms ref $600-\Omega$ load, -1x gain		105		dB
V _n	Noise voltage	A-weighted, AES17 filter, Gain = $-2x$		12		μV
	Slew rate			4.5		V/µs
Gbw	Unity gain bandwidth			8		MHz
Crosstalk	Channel to channel	f = 1 kHz, Rload = 32 Ω, Po = 25 mW		-85		dB
Vincm_pos	Positive common-mode input voltage			+2		V
Vincm_neg	Negative common-mode input voltage			-2		V
l _{lim}	Output current limit			60		mA

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7.6 Programmable Gain Settings

 V_{DD} = 3.3 V, R_{load} = 32 k Ω , T_A = 25°C, Charge pump:= C_{CP} 1 μ F, C_{IN} = 1 μ F, 1x gain select (unless otherwise noted)⁽¹⁾

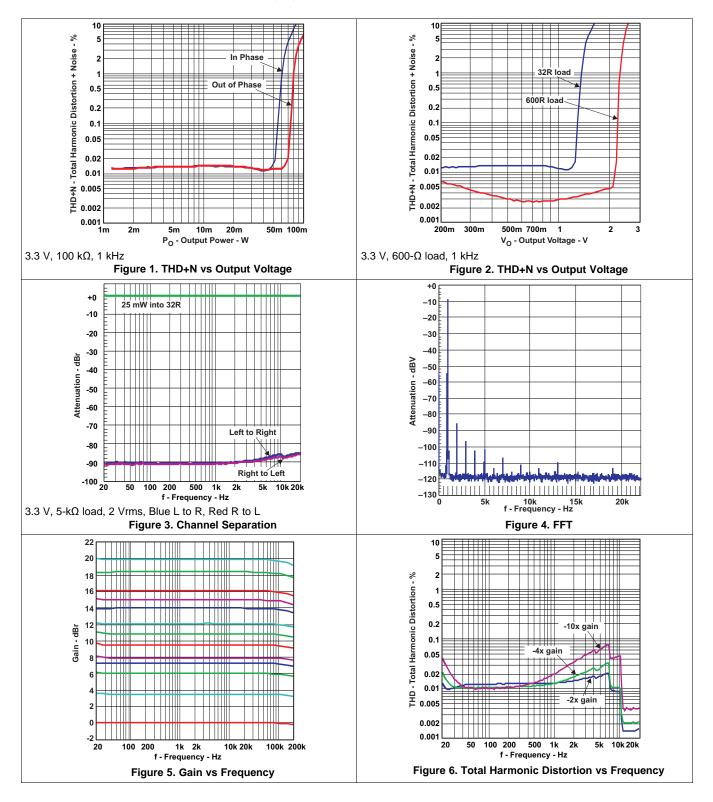
	PARAMETER	TEST CONDITIONS		MIN	TYP I	MAX	UNIT					
R_Tol	Gain programming resistor tolerance				2%							
ΔA _V	Gain matching	Between left and right channels			0.25		dB					
	Gain step tolerance				0.1		dB					
			249k or higher		-2							
			82k0		-1							
			49k2		-1.5							
			35k1		-2.3		1					
Gain steps			27k3		-2.5							
			20k5		-3							
	Gain resistor 2% tolerance	15k4		-3.5		V/V						
			11k5		-4							
			9k09		-5							
			7k50		-5.6							
			6k19		-6.4							
			5k11		-8.3							
			3k90		-10		<u> </u>					
			249k or higher		37		_					
			82k0		55							
			49k2		44							
			35k1		33							
			27k3		31							
			20k5		28							
	Input impedance	Gain resistor 2% tolerance	15k4		24		kΩ					
			11k5		22							
			9k09		18							
			7k50		17							
			6k19		15		I					
			5k11		12							
			3k90		10							

(1) If pin 12, GAIN, is left floating an internal pullup sets the gain to -2x. Gain setting is latched during power up.

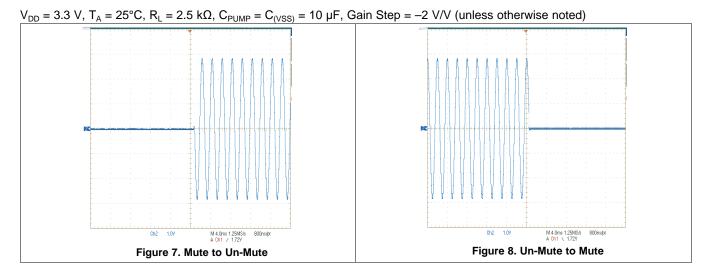


7.7 Typical Characteristics, Line Driver

 $V_{\text{DD}} = 3.3 \text{ V}, \text{ } \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ } \text{R}_{\text{L}} = 2.5 \text{ } \text{k}\Omega, \text{ } \text{C}_{\text{PUMP}} = \text{C}_{(\text{VSS})} = 10 \text{ } \mu\text{F}, \text{ Gain Step} = -2 \text{ } \text{V/V} \text{ (unless otherwise noted)}$



Typical Characteristics, Line Driver (continued)



8 Parameter Measurement Information

All parameters are measured according to the conditions described in the Specifications section.



9 Detailed Description

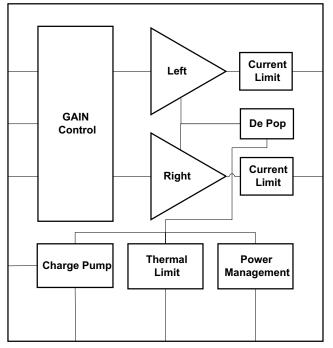
9.1 Overview

The TPA6139A2 is a DirectPath stereo headphone amplifier that requires no output DC-blocking capacitors and is capable of delivering 25 mW into a $32-\Omega$ load. The device has built-in pop suppression circuitry to completely eliminate pop noise during turnon and turnoff. The amplifier outputs have short-circuit protection.

The TPA6139A2 gain is controlled by external resistors Rin and Rfb, see *Gain Setting* for recommended values.

The TPA6139A2 operates from a single 3-V to 3.6-V supply, as it uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 DirectPath Headphone Driver

Single-supply line-driver amplifiers typically require DC-blocking capacitors. The top drawing in Figure 9 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC-blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.



Feature Description (continued)

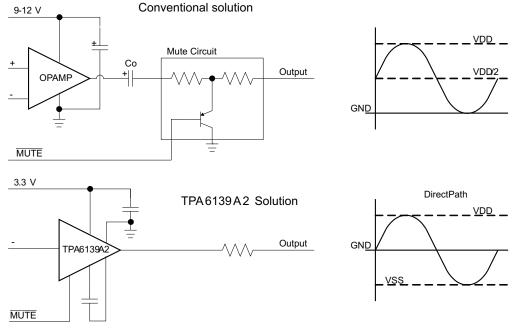


Figure 9. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

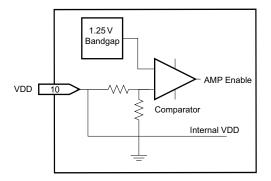
The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output DCblocking capacitors.

The bottom block diagram and waveform of Figure 9 illustrate the ground-referenced line-driver architecture.

9.4 Device Functional Modes

9.4.1 Internal Undervoltage Detection

The TPA6139A2 contains an internal precision band-gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8 V with 200-mV hysteresis.





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Device Functional Modes (continued)

9.4.2 Pop-Free Power Up

Pop-free power up is ensured by keeping the MUTE low during power-supply ramp-up and ramp-down. The pin must be kept low until the input AC-coupling capacitors are fully charged before asserting the MUTE pin high to precharge the AC-coupling; and, pop-less power up is achieved. Figure 10 illustrates the preferred sequence.

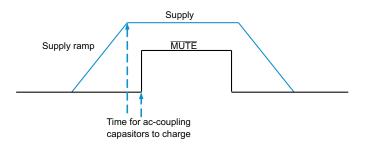


Figure 10. Power-Up Sequence

TEXAS INSTRUMENTS

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA6139A2 device starts its operation by asserting the MUTE pin to logic 1. The device enters in mute mode when pulling the MUTE pin low. The charge pump generates a negative supply voltage. The charge pump flying capacitor connected between CP and CN transfers charge to generate the negative supply voltage. The output voltages are capable of positive and negative voltage swings and are centered close to 0 V, eliminating the need for output capacitors. Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range.

This typical connection diagram highlights the required external components and system level connections for proper operation of the device in popular use case. Any design variation can be supported by TI through schematic and layout reviews. Visit https://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.1.1 Capacitive Load

The TPA6139A2 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.



10.2 Typical Application

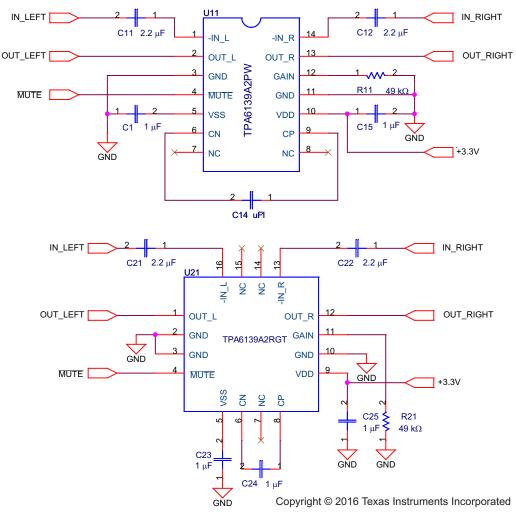


Figure 11. Single-Ended Input and Output, Gain Set to -1.5x

10.2.1 Design Requirements

Table 1 lists the design parameters of this example.

DESIGN PARAMETER	EXAMPLE VALUE				
Input voltage supply range	3 V to 3.6 V				
Current	130 mA				
Load impedance	32 Ω				

10.2.2 Detailed Design Procedure

10.2.2.1 Component Selection

10.2.2.1.1 Charge Pump

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 μ F is typical. Capacitor values that are smaller than 1 μ F cannot be recommended as it limits the negative voltage swing in low impedance loads.

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10.2.2.1.2 Decoupling Capacitors

The TPA6139A2 is a DirectPath amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μ F, placed as close as possible to the device VDD leads works best. Placing this decoupling capacitor close to the TPA6139A2 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10- μ F or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

10.2.2.1.3 Gain Setting

The gain setting is programmed with the GAIN pin individually for line driver and headphone section. Gain setting is latched when the MUTE pin is set high. Table 2 lists the gain settings. The default gain with the gain-set pin left open is -2x.

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE							
No connect	-2x	6	37k							
82k0	-1x	0	55k							
49k2	–1.5x	3.5	44k							
35k1	-2.3x	7.2	33k							
27k3	–2.5x	8	31k							
20k5	–3x	9.5	28k							
15k4	–3.5x	10.9	24k							
11k5	-4x	12	22k							
9k09	–5x	14	18k							
7k50	-5.6x	15	17k							
6k19	-6.4x	16.1	15k							
5k11	-8.3x	18.4	12k							
3k90	-10x	20	10k							

Table 2. Gai	n Settings
--------------	------------

10.2.2.1.4 Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA6139A2. These capacitors block the DC portion of the audio source and allow the TPA6139A2 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 2. Then the frequency or capacitance can be determined when one of the two values is given, as shown in Equation 1.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \text{ or } C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}}$$

(1)

For a fixed cutoff frequency of 2 Hz, the size of the input capacitance is shown Table 3 with the capacitors rounded up to the nearest E6 values. For 20-Hz cutoff, simply divide the capacitor values with 10; for example, for 1x gain, 150 nF is needed.

	• •			
Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2-Hz CUTOFF
249k	-2x	6	37k	2.2 μF
82k0	-1x	0	55k	1.5 µF
49k2	-1.5x	3.5	44k	2.2 μF
35k1	-2.3x	7.2	33k	3.3 µF
27k3	-2.5x	8	31k	3.3 µF

Table 3. Input Capacitor	r for Different	Gain and Cutoff
--------------------------	-----------------	-----------------

Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2-Hz CUTOFF
20k5	-3x	9.5	28k	3.3 µF
15k4	-3.5x	10.9	24k	3.3 µF
11k5	-4x	12	22k	4.7 µF
9k09	–5x	14	18k	4.7 μF
7k50	-5.6x	15	17k	4.7 μF
6k19	-6.4x	16.1	15k	6.8 µF
5k11	-8.3x	18.4	12k	6.8 µF
3k90	-10x	20	10k	10 µF

Table 3. Input Capacitor for Different Gain and Cutoff (continued)

10.2.3 Application Curves

The characteristics of this design are shown in *Typical Characteristics, Line Driver*.

Table 4. Table of Graphs

	FIGURE
THD+N vs Output Voltage	Figure 2
Total Harmonic Distortion vs Frequency	Figure 6
Mute to Un-Mute	Figure 7
Un-Mute to mute	Figure 8

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply from 3 V to 3.6 V. Therefore, the output voltage range of power supply should be within this range and well regulated. TI recommends placing decoupling capacitors in every voltage source pin. Place these decoupling capacitors as close as possible to the TPA6139A2.

12 Layout

12.1 Layout Guidelines

A proposed layout for the TPA6139A2 can be seen in the TPA6139A2EVM User's Guide (SLOU308), and the Gerber files can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/TPA6139A2evm.html. To access this information, open the TPA6139A2 product folder and look in the Tools and Software folder.

TI recommends routing the ground traces as a star ground to minimize hum interference. VDD, VSS decoupling capacitors, and the charge pump capacitors should be connected with short traces.

The TPA6139A2 stereo headphone amplifier is pin-compatible with the DRV612. A single PCB layout can therefore be used with stuffing options for different board configurations.

TPA6139A2

SLOS700C – JANUARY 2011 – REVISED APRIL 2016



www.ti.com

12.2 Layout Example

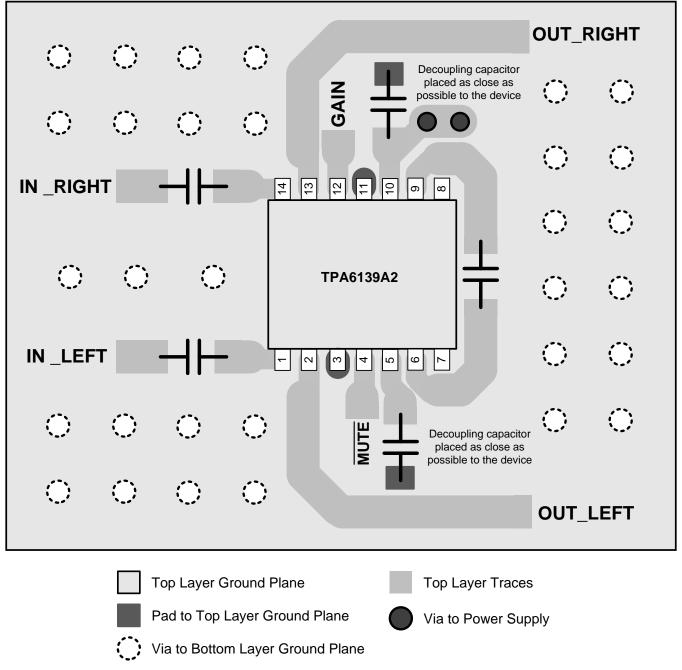
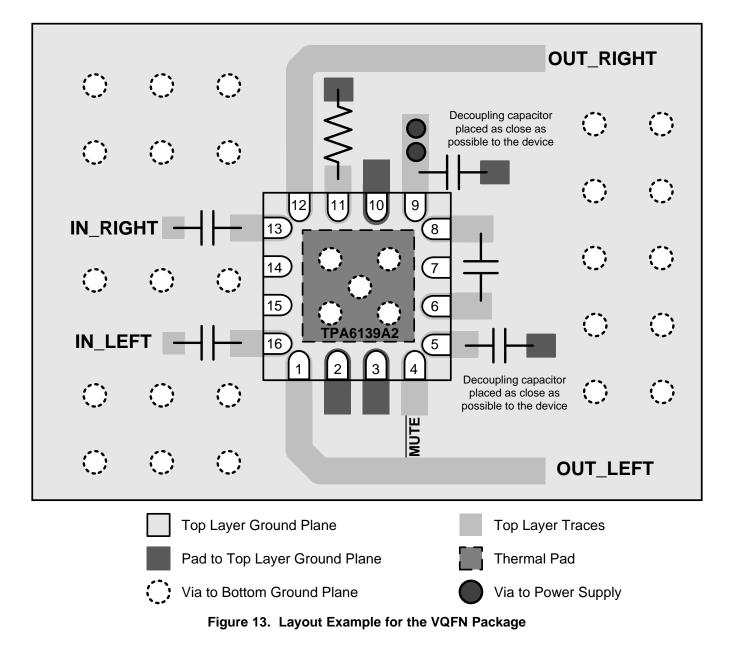


Figure 12. Layout Example for the TSSOP Package



Layout Example (continued)



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13 Device and Documentation Support

13.1 Device Support

For device support, see the following: Gerber – http://focus.ti.com/docs/toolsw/folders/print/TPA6139A2evm.html

13.2 Documentation Support

For related documentation, see the following: TPA6139A2EVM User's Guide (SLOU308)

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

DirectPath, E2E are trademarks of Texas Instruments. Blu-ray Discs is a trademark of Blu-ray Disc Association. All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



24-Jul-2016

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6139A2PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139	Samples
TPA6139A2PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139	Samples
TPA6139A2RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139	Samples
TPA6139A2RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



24-Jul-2016

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6139A2PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPA6139A2RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

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PACKAGE MATERIALS INFORMATION

1-Nov-2016



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6139A2PWR	TSSOP	PW	14	2000	367.0	367.0	38.0
TPA6139A2RGTR	QFN	RGT	16	3000	336.6	336.6	28.6

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA



- Quad Flatpack, No-leads (QFN) package configuration. C. D.
- The package thermal pad must be soldered to the board for thermal and mechanical performance. E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.



RGT (S-PVQFN-N16)

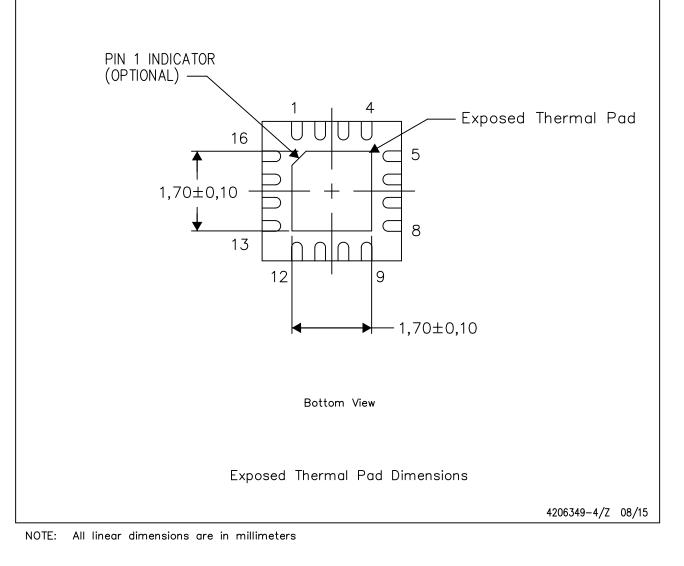
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

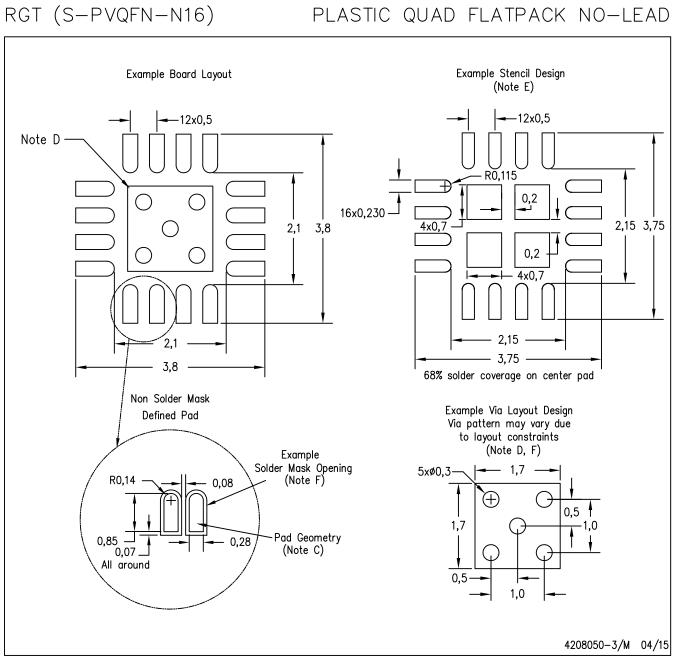
This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.







- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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