Resistor-Programmable Temperature Switch in SOT Package

Check for Samples: TMP708

FEATURES

- **Threshold Accuracy:**
  - **±0.5°C Typical**
  - **±3°C Maximum (+60°C to +100°C)**
- **Temperature Threshold Set By 1% External Resistor**
- **Low Quiescent Current: 40 µA Typical**
- **Open-Drain, Active-Low Output Stage**
- **Pin-Selectable 10°C or 30°C Hysteresis**
- **Reset Operation Specified at V_{CC} = 0.8 V**
- **Supply Range: 2.7 V to 5.5 V**
- **Package: 5-Pin SOT23**

APPLICATIONS

- **Computers (Laptops and Desktops)**
- **Servers**
- **Industrial and Medical Equipment**
- **Storage Area Networks**
- **Automotive**

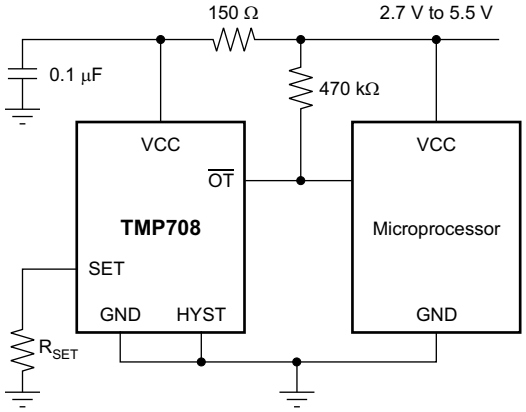
DESCRIPTION

The TMP708 is a fully-integrated, resistor-programmable temperature switch with a temperature threshold that is set by just one external resistor within its entire operating range. The TMP708 provides an open-drain, active-low output and has a 2.7 V to 5.5 V supply voltage range.

The temperature threshold accuracy is typically ±0.5°C with a maximum of ±3°C (+60°C to +100°C). The quiescent current consumption is typically 40 µA. Hysteresis is pin-selectable to 10°C or 30°C.

The TMP708 is available in a 5-pin SOT23 package.

TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
TMP708	SOT23-5	DBV	SBI	TMP708AIDBVR
				TMP708AIDBVT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		TMP708	UNIT
Supply voltage range (VCC)		–0.3 to 6	V
Input voltage range (SET and HYST)		–0.3 to (V_{CC} + 0.3)	V
Output voltage range ($\overline{OT}$)		–0.3 to 6	V
Input current		20	mA
Output current		20	mA
Operating temperature, T_A		–40 to +125	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

THERMAL INFORMATION

THERMAL METRIC(1)		TMP708 DBV (SOT23) 5 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	217.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	86.3	
θ_{JB}	Junction-to-board thermal resistance	44.6	
ψ_{JT}	Junction-to-top characterization parameter	4.4	
ψ_{JB}	Junction-to-board characterization parameter	43.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

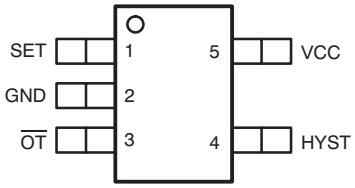
ELECTRICAL CHARACTERISTICS

At T_A = 0°C to +125°C and V_{CC} = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{CC}	Supply voltage range		2.7		5.5	V
I_{CC}	Supply current	V_{CC} = 5 V		40	55	µA
		V_{CC} = 2.7 V		40	55	µA
TEMPERATURE						
T_E	Temperature error	T_A = +60°C to +100°C		±0.5	±3	°C
T_A	Operating temperature range		–40		+125	°C
DIGITAL INPUT (HYST)						
V_{IH}	High-level input voltage		0.7 × V_{CC}			V
V_{IL}	Low-level input voltage				0.3 × V_{CC}	V
I_{lkg_in}	Input leakage current			1		µA
C_{IN}	Input capacitance			10		pF
ANALOG INPUT (SET)						
V_{IN}	Input voltage range		0		V_{CC}	V
DIGITAL OPEN-DRAIN OUTPUT ($\overline{OT}$)						
$I_{(OT\_SINK)}$	Output sink current	V_{OT} = 0.3 V	5	12		mA
$I_{lkg(OT)}$	Output leakage current	V_{OT} = V_{CC}		1		µA

PIN CONFIGURATION

DBV PACKAGE
SOT23-5
(TOP VIEW)



PIN DESCRIPTIONS

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
GND	2	Power	Analog	Device ground
HYST	4	Input	Digital	Hysteresis selection. For 10°C, HYST = VCC; for 30°C, HYST = GND.
$\overline{OT}$	3	Output	Digital	Open-drain, active low output
SET	1	Input	Analog	Temperature set point. Connect an external 1% resistor between SET and GND.
VCC	5	Power	Analog	Power-supply voltage (2.7 V to 5.5 V)

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 2.7 V to 5.5 V, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE

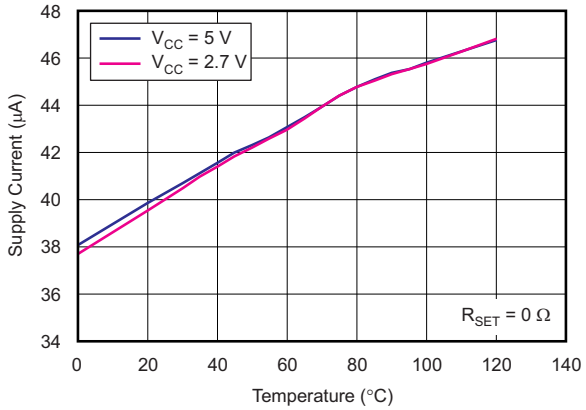


Figure 1.

R_{SET} vs TRIP TEMPERATURE

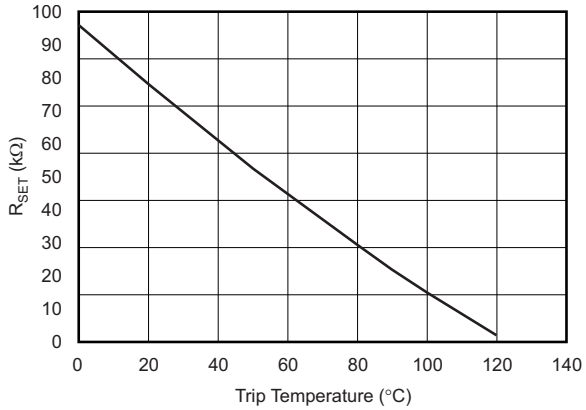


Figure 2.

HYSTERESIS vs TRIP TEMPERATURE

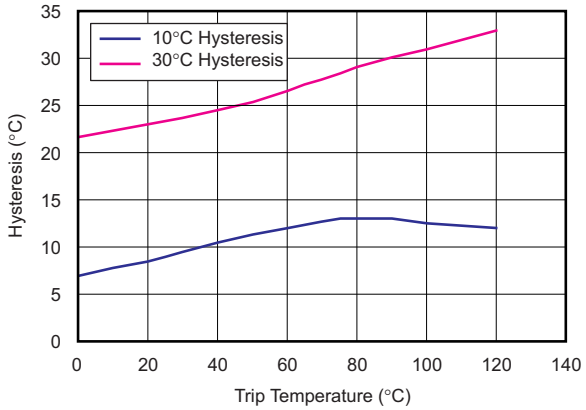


Figure 3.

TEMPERATURE ERROR vs TRIP TEMPERATURE

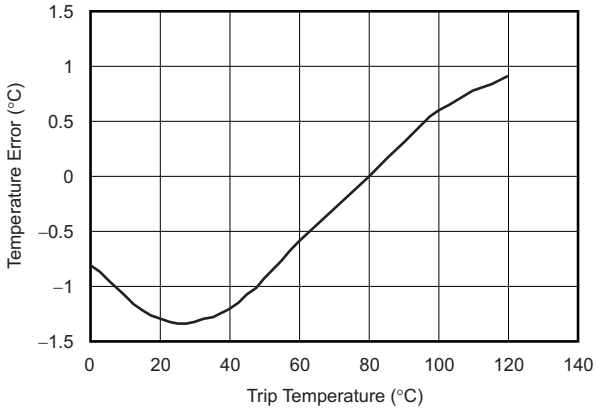


Figure 4.

THEORY OF OPERATION

DEVICE DESCRIPTION

The TMP708 is a fully-integrated, resistor-programmable temperature switch that incorporates two temperature-dependent voltage references and one comparator. One voltage reference exhibits a positive temperature coefficient (tempco), and the other voltage reference exhibits a negative tempco. The temperature at which both voltage references are equal determines the temperature trip point.

The TMP708 temperature threshold is programmable from 0°C to +125°C and is set by an external 1% resistor from the SET pin to the GND pin. The TMP708 has an open-drain, active-low output structure that can easily interface with a microprocessor.

HYSTERESIS INPUT

The HYST pin is a digital input that allows the input hysteresis to be set at either 10°C (when HYST = VCC) or 30°C (when HYST = GND). The hysteresis function keeps the $\overline{OT}$ pin from oscillating when the temperature is near the threshold. Thus, the HYST pin should always be connected to either VCC or GND. Other input voltages on this pin may cause abnormal supply currents and/or function.

CIRCUIT DETAILS

Figure 5 shows the comparator, the NFET open-drain device connected to the $\overline{OT}$ pin, the positive tempco reference using the external R_{SET} resistor, the negative tempco reference, and the hysteresis control. The voltage of the positive tempco reference is controlled by external resistor R_{SET}.

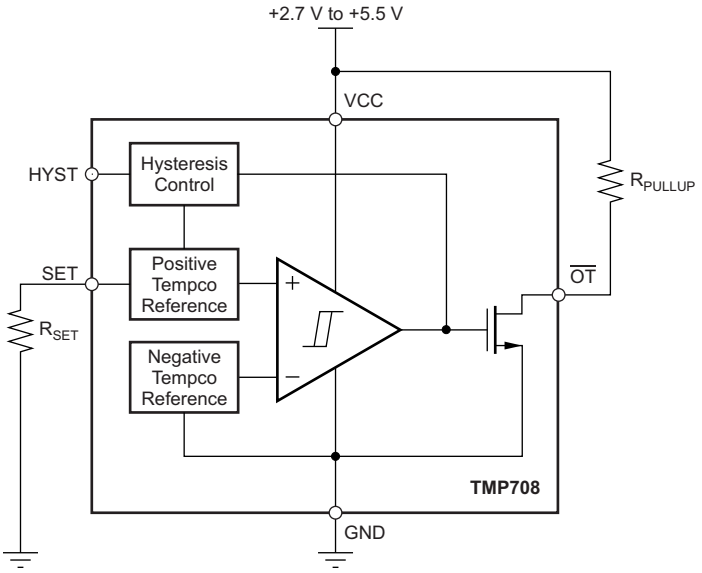


Figure 5. Circuit Details

The TMP708 reaches the temperature trip point when the voltage from the positive tempco reference is greater than the voltage from the negative tempco reference. This situation causes the output of the comparator to switch from logic 0 to logic 1. The comparator output drives the gate of the NFET open-drain device and pulls the voltage on the $\overline{OT}$ pin from logic 1 to logic 0 under these conditions (output *trips*). Furthermore, the logic 1 output from the comparator causes the hysteresis control to increase the voltage of the positive tempco reference by an amount set by the logic setting on the HYST pin (10°C for logic 1 on the HYST pin; 30°C for logic 0 on the HYST pin). Increasing the voltage of the positive tempco reference after the TMP708 *trips* stops the TMP708 from *untripping* (voltage on the $\overline{OT}$ pin changing from logic 0 to logic 1) until the local temperature has been reduced by the amount set by the HYST pin. After the local temperature has been reduced and the voltage from the positive tempco reference is less than the voltage from the negative tempco reference, the output of the comparator switches from logic 1 to logic 0. This condition causes the voltage on the $\overline{OT}$ pin to change from logic 0 to logic 1 (device *untrips*).

APPLICATION INFORMATION

SET-POINT RESISTOR (R_{SET})

The temperature threshold is set by connecting R_{SET} from the SET pin to GND. The value of R_{SET} can be determined using either Figure 2 or from Equation 1:

$$R_{SET}\ (k\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

Where T = temperature threshold in degree Celsius. (1)

THERMAL CONSIDERATIONS

The TMP708 quiescent current is typically 40 µA. The device dissipates negligible power when the output drives a high-impedance load. Thus, the die temperature is the same as the package temperature. In order to maintain accurate temperature monitoring, a good thermal contact should be provided between the TMP708 package and the device being monitored. The rise in die temperature as a result of self-heating is given by the following equation:

$$\Delta T_J = P_{DISS} \times \theta_{JA}$$

Where:

P_{DISS} = power dissipated by the device.

θ_{JA} = package thermal resistance. Typical thermal resistance for SOT-23 package is 217.9°C/W. (2)

To limit the effects of self-heating, keep the output current at a minimum level.

POWER-SUPPLY FILTERING

Any significant noise on the VCC pin may result in a trip-point error. This noise can be minimized by low-pass filtering the device supply (V_{CC}) using a 150-Ω resistor and a 0.1-µF capacitor.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A	Page
• Updated threshold accuracy feature bullet	1
• Updated threshold accuracy text in second paragraph of *Description* section	1
• Updated temperature error parameter in the Electrical Characteristics	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMP708AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBI	Samples
TMP708AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

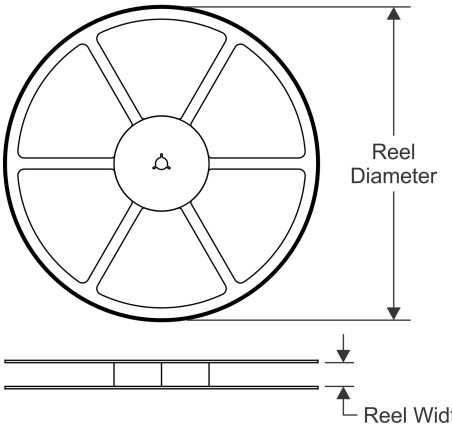
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

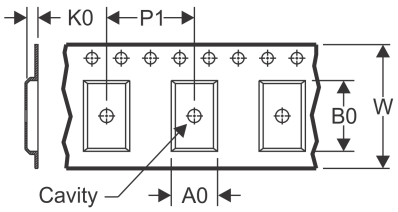
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

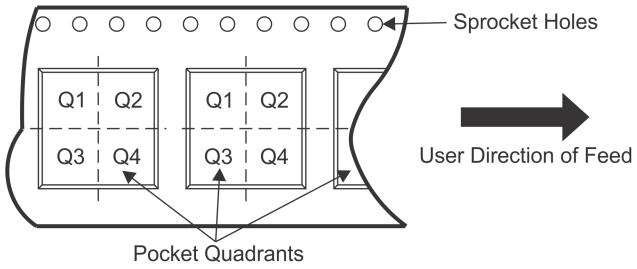


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

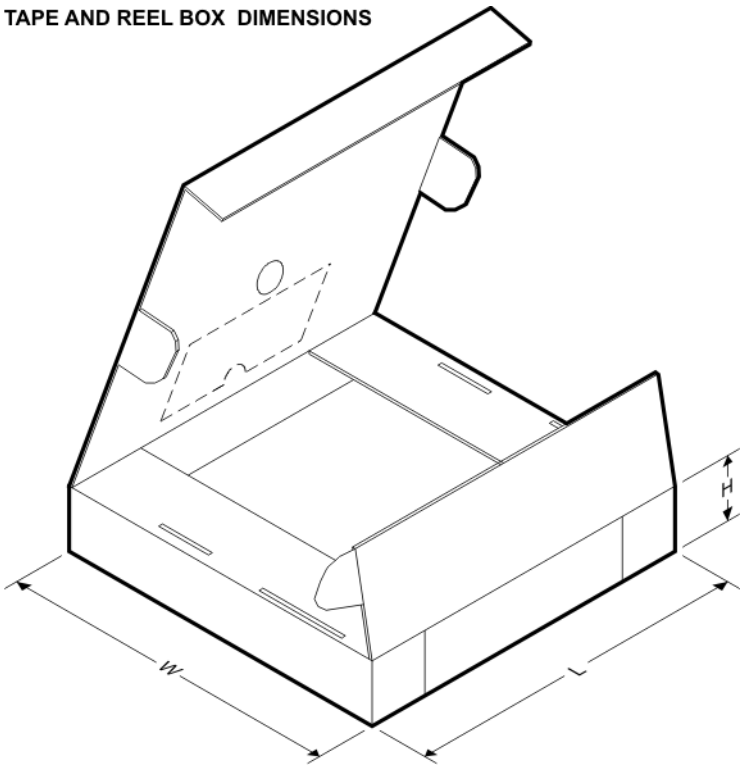
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP708AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TMP708AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

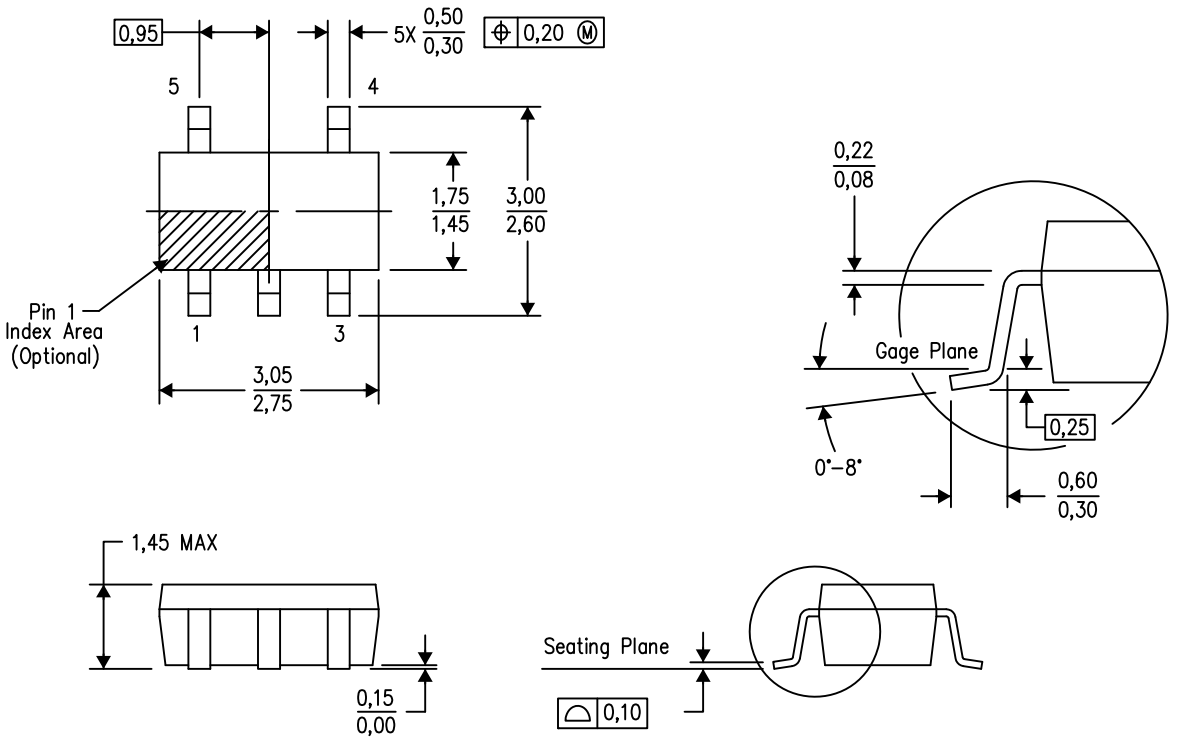
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP708AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TMP708AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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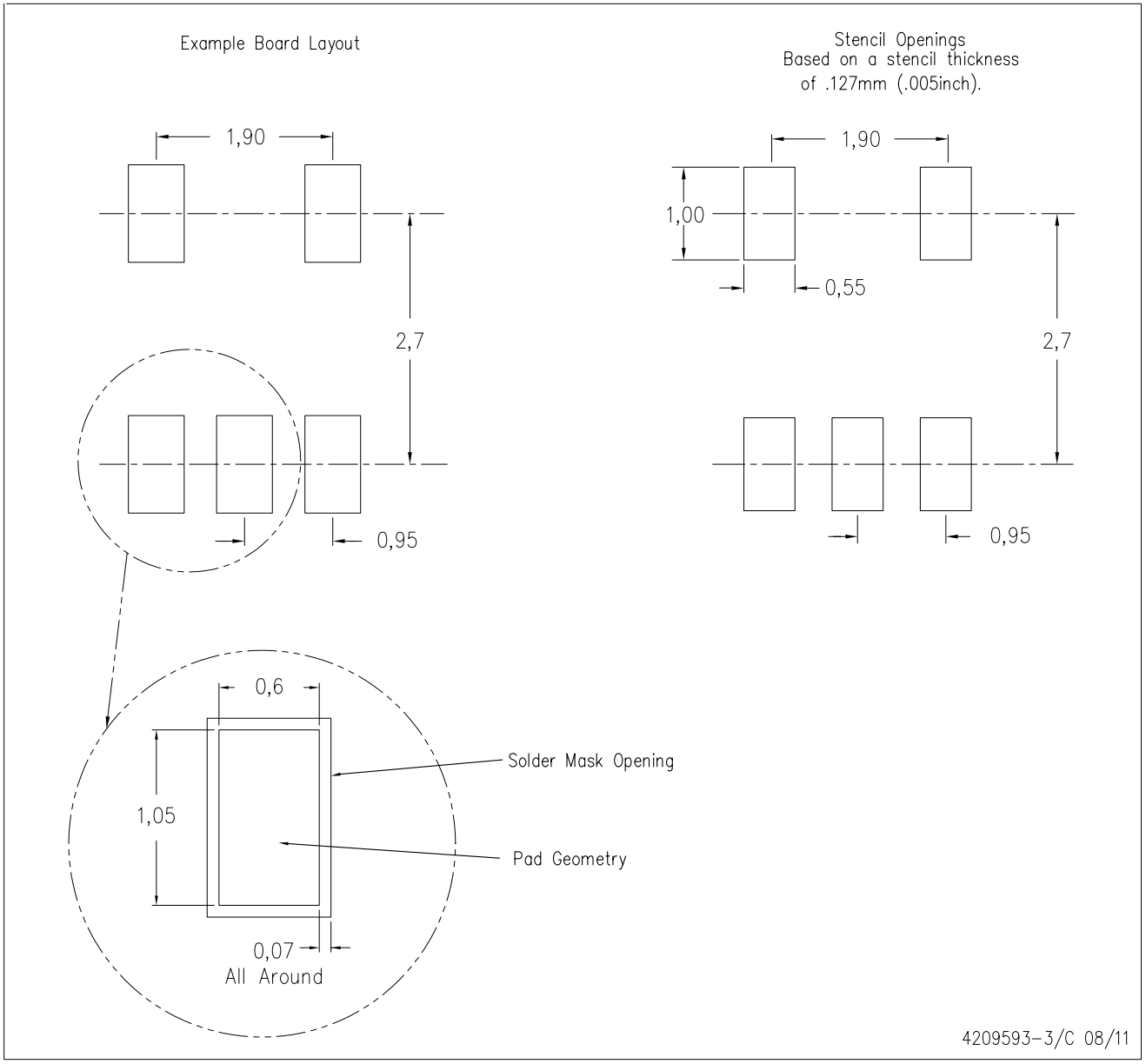
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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