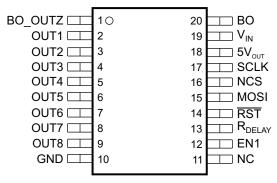
FEATURES

- Eight Low-Side Drivers With Internal Clamp for Inductive Loads and Current Limiting for Self Protection
 - Seven Outputs Rated at 150 mA and Controlled Through Serial Interface
 - One Output Rated at 150 mA and Controlled Through Serial Interface and Dedicated Enable Pin
- 5-V ± 5% Regulated Power Supply With 200-mA Load Capability at V_{IN} Max of 18 V
- Internal Voltage Supervisory for Regulated Output
- Serial Communications for Control of Eight Low-Side Drivers
- Enable/Disable Input for OUT1
- 5-V or 3.3-V I/O Tolerant for Interface to Microcontroller
- Programmable Power-On Reset Delay Before RST Asserted High, Once 5 V Is Within Specified Range (6 ms Typ)
- Programmable Deglitch Timer Before RST Asserted Low (40 μs Typ)
- Programmable Brown-Out Feature
- Thermal Shutoff for Self Protection

APPLICATIONS

- Electrical Applicances
 - Air Conditioning Units
 - Ranges
 - Dishwashers
 - Refrigerators
 - Microwaves
 - Washing Machines
- General-Purpose Interface Circuit Allowing Microcontroller Interface to Relays, Electric Motors, LEDs, and Buzzers

PWP PACKAGE (TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The power supply provides regulated 5-V output to power the system microcontroller and drive eight low-side switches. The brown-out detection output (BO_OUTZ) warns the system if there is a temporary drop in the supply voltage, so the system can prevent potentially hazardous situations.

A serial communications interface controls the eight low-side outputs; each output has an internal snubber circuit to absorb the inductive load at turn OFF. Alternatively, the system can use a fly-back diode to V_{IN} to help recirculate the energy in an inductive load at turn OFF.

ORDERING INFORMATION(1)

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	PowerPAD™ – PWP	Reel of 2000	TPL9202PWPR	PL202
-40°C to 125°C	PowerPAD*** - PWP	Tube of 70	TPL9202PWP	PL202

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Tex

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

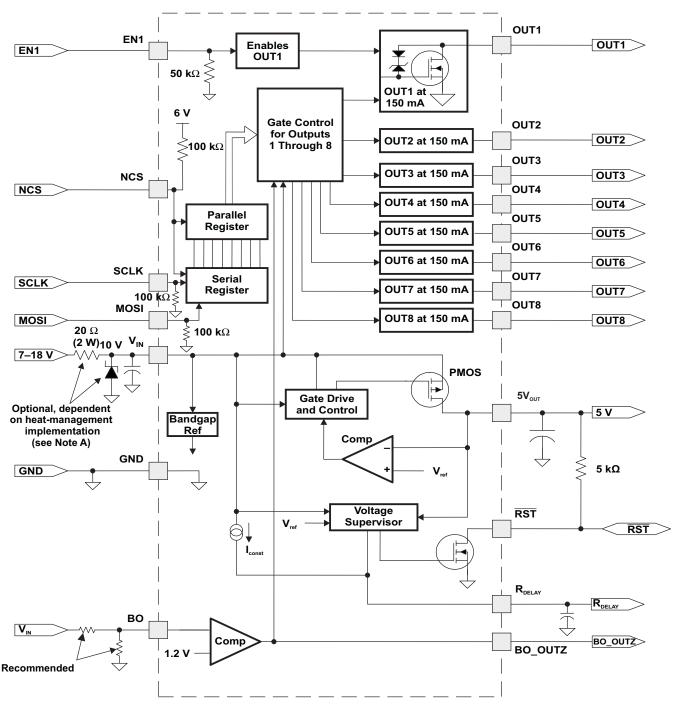


PINOUT CONFIGURATION

NO.	NAME	I/O	DESCRIPTION
1	BO_OUTZ	0	Brown-out indicator
2	OUT1	0	Low-side output 1
3	OUT2	0	Low-side output 2
4	OUT3	0	Low-side output 3
5	OUT4	0	Low-side output 4
6	OUT5	0	Low-side output 5
7	OUT6	0	Low-side output 6
8	OUT7	0	Low-side output 7
9	OUT8	0	Low-side output 8
10	GND	ļ	Ground
11	NC		No connection
12	EN1	1	Enable/disable for OUT1
13	R _{DELAY}	0	Power-up reset delay
14 ⁽¹⁾	RST	I/O	Power-on reset output (open drain)
15	MOSI	ļ	Serial data input
16	NCS	ļ	Chip select
17	SCLK	ļ	Serial clock for data synchronization
18	5V _{OUT}	0	Regulated output
19	V _{IN}	Ī	Unregulated input voltage source
20	ВО	I	Brown-out input threshold setting

⁽¹⁾ Terminal 14 can be used as an input or an output.

FUNCTIONAL BLOCK DIAGRAM



A. The resistor and Zener diode are required if there is insufficient thermal-management allocation.

TPL9202 8-CHANNEL RELAY DRIVER WITH INTEGRATED 5-V LDO AND BROWN-OUT DETECTION

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DETAILED DESCRIPTION

The 5-V regulator is powered from V_{IN} , and the regulated output is within 5 V \pm 5% over the operating conditions. The open-drain power-on reset (RST) pin remains low until the regulator exceeds the set threshold, and the timer value set by the capacitor on the reset delay (R_{DELAY}) pin expires. If both of these conditions are satisfied, \overline{RST} is asserted high. This signifies to the microcontroller that serial communications can be initiated to the TPL9202.

The serial communications is an 8-bit format, with data transfer synchronized using a serial clock from the microcontroller. A single register controls all the outputs (one bit per output). The default value is zero (OFF). If an output requires pulse width modulation (PWM) function, the register must be updated at a rate faster than the desired PWM frequency. OUT1 can be controlled by serial input from the microcontroller or with the dedicated enable (EN1) pin. If EN1 is pulled low or left open, the serial input through the shift register controls OUT1. If EN1 is pulled high, OUT1 always is turned on, and the serial input for OUT1 is ignored.

The brown-out (BO) input is a resistor divided from the input supply and is used to determine if the supply voltage drops to undesired levels. If the input drops below the programmed value, BO_OUTZ is pulled low, and all outputs are disabled. Once the input supply line returns to the minimum desired level, the outputs are enabled to the previous programmed states.

If \overline{RST} is asserted, all outputs are turned OFF internally, and the input register is reset to all zeroes. The microcontroller must write to the register to turn the outputs ON again.

Submit Documentation Feedback

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Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
V	Unregulated input voltage ^{(2) (3)}	V _{IN}		24	V
V _{I(unreg)}	Offiegulated input voltage VVV	ВО		24	V
V	Logic input voltage ⁽²⁾ (3)	EN1, MOSI, SCLK, and NCS		7	V
V _{I(logic)}	Logic input voltage () ()	RST and R _{DELAY}		7	V
Vo	Low-side output voltage	OUT1-OUT8		16.5	V
I _{LIMIT}	Output current limit (4)	OUTn = ON and shorted to V _{IN} with low impedance		350	mA
θ_{JA}	Thermal impedance, junction to ambient ⁽⁵⁾			33	°C/W
θ_{JC}	Thermal impedance, junction to top of package (5)			20	°C/W
$\theta_{\sf JP}$	Thermal impedance, junction to thermal pad (5)			1.4	°C/W
P _D	Continuous power dissipation (6)			3.7	W
ESD	Electrostatic discharge ⁽⁷⁾			2	kV
T _A	Operating ambient temperature range		-40	125	°C
T _{stg}	Storage temperature range		-65	125	°C
T _{lead}	Lead temperature	Soldering, 10 s		260	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values are with respect to GND.

Absolute negative voltage on these pins must not go below -0.5 V.

The thermal data is based on using 1-oz copper trace with JEDEC 51-5 test board for PWP.

The data is based on ambient temperature of 25°C maximum. The Human Body Model is a 100-pF capacitor discharged through a 1.5-k Ω resistor into each pin.

Dissipation Ratings

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 125°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING
PWP	3787 mW	30.3 mW/°C	757 mW

Recommended Operating Conditions

			MIN	MAX	UNIT
V _{I(unreg)} Unregulated input voltage		V _{IN}	7	18	\/
V _{I(unreg)}	Unregulated input voltage	BO (as seen by external resistor network)	0	18	V
V _{I(logic)}	Logic input voltage	EN1, RST, and R _{DELAY} , MOSI, SCLK, and NCS	0	5.25	V
T _A	Operating ambient temperature		-40	125	°C

Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 ms.

TPL9202 8-CHANNEL RELAY DRIVER WITH INTEGRATED 5-V LDO AND BROWN-OUT DETECTION



SLIS124D-JUNE 2006-REVISED FEBRUARY 2008

Electrical Characteristics

 $T_A = -40$ °C to 125°C, $V_{IN} = 7$ V to 18 V (unless otherwise noted)

i	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Supply Volt	age and Current		·			
V _{IN} ⁽²⁾	Input voltage		7		18	V
	lanut augalu augrant	Enable = low, OUT1-OUT8 = Off			3	A
I _{IN}	Input supply current	Enable = high, OUT1-OUT8 = On			5	mA
Logic Input	s (MOSI, NCS, SCLK, and EN1)				
V_{IL}	Logic input low level	I _{IL} = 100 μA			8.0	V
V_{IH}	Logic input high level	$I_{IL} = 100 \mu A$	2.4			V
Reset (RST))					
V_{OL}	Low-level logic output	I _{OL} = 1.6 mA			0.4	V
V _{OH} ⁽³⁾	High-level logic output	5-k Ω pullup to V _{CC}	V _{CC} - 0.8			V
V_{H}	Disabling reset threshold	5-V regulator ramps up		4.25	4.5	V
V_L	Enabling reset threshold	5-V regulator ramps down	3.3	3.75		V
V_{HYS}	Threshold hysteresis		0.12	0.5		V
Reset Delay	(R _{DELAY})					
I _{OUT}	Output current		18	28	48	μΑ
t _{DW}	Reset delay timer	C = 47 nF	3	6		ms
t_{UP}	Reset capacitor to low level	C = 47 nF		45		μs
Output (OU	T1–OUT8)					
V_{OL}	Output ON	I _{OUTn} = 150 mA		0.4	0.7	V
I _{OH}	Output leakage	$V_{OH} = Max \text{ of } 16.5 \text{ V}$			2	μΑ
Regulator C	Output (5V _{OUT})					
5V _{OUT}	Output supply	$I_{5\text{VOUT}}$ = 5 mA to 200 mA, V_{IN} = 7 V to 18 V, $C_{5\text{VOUT}}$ = 1 μF	4.75	5	5.25	٧
I _{5Vout}	Limit output short circuit current	5V _{OUT} = 0 V	200			mA
Brown-Out	(BO) Input		·			
BOV _{thes}	Threshold for brown-out detection	V _{IN} reduced until BO_OUTZ goes low		1.3		V
Brown-Out	Detection Output (BO_OUTZ)					
V _{OL}	Logic level output	I _{OL} = 100 μA			0.4	V
V _{OH} ⁽³⁾	Logic level output	Pullup to V _{CC}	V _{CC} - 0.8			V
Thermal Sh	utdown					
T _{SD}	Thermal shutdown			150		°C
T _{HYS}	Hysteresis			20		°C

 ⁽¹⁾ All typical values are at T_A = 25°C.
 (2) There are external high-frequency noise-suppression capacitors and filter capacitors on V_{IN}.
 (3) V_{CC} is the pullup resistor voltage.

TPL9202 8-CHANNEL RELAY DRIVER WITH INTEGRATED 5-V LDO AND BROWN-OUT DETECTION

SLIS124D-JUNE 2006-REVISED FEBRUARY 2008

Output Control Register

MSB LSB

IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0	0	0	0	0	0	0	0

INn = 0 = Output OFF INn = 1 = Output ON

To operate the output in PWM mode, the output control register must be updated at a rate twice the desired PWM frequency of the output. Maximum PWM frequency is 5 kHz. The register is updated every $100 \, \mu s$.

ENABLE TRUTH TABLE

EN1	SERIAL INPUT FOR OUT1	OUT1
Open	Н	On
Open	L	Off
L	Н	On
L	L	Off
Н	Н	On
Н	L	On



Serial Communications Interface

The serial communications are an 8-bit format, with data transfer synchronized using a serial clock from the microcontroller (see Figure 1). A single register controls all the outputs. The signal gives the instruction to control the output of TPL9202.

The NCS signal enables the SCLK and MOSI data when it is low. After NCS is set to low for T1, synchronization clock and data begin to transmit and, after the 8-bit data has been transmitted, NCS is set high again to disable SCLK and MOSI and to transfer the serial data to the control register. SCLK must be held low when NCS is high.

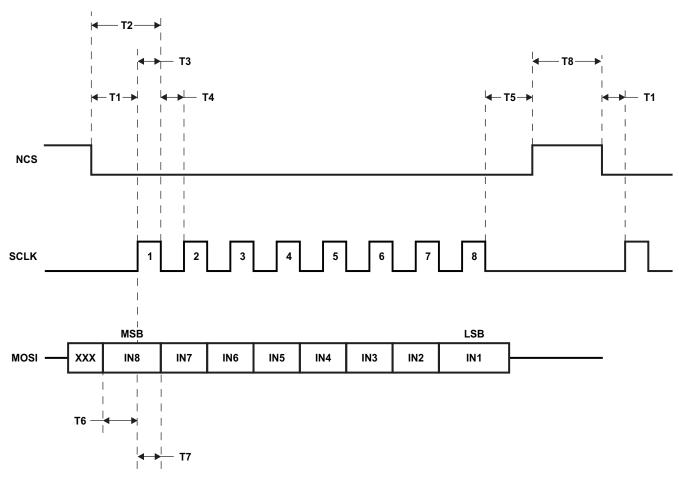


Figure 1. Serial Communications

TPL9202 8-CHANNEL RELAY DRIVER WITH INTEGRATED 5-V LDO AND BROWN-OUT DETECTION

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Timing Requirements

 $T_A = -40^{\circ}C$ to 125°C, $V_{IN} = 7$ V to 18 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SPI}	SPI frequency		4		MHz
T1	Delay time, NCS falling edge to SCLK rising edge	10			ns
T2	Delay time, NCS falling edge to SCLK falling edge	80			ns
Т3	Pulse duration, SCLK high	60			ns
T4	Pulse duration, SCLK low	60			ns
T5	Delay time, last SCLK falling edge to NCS rising edge	80			ns
T6	Setup time, MOSI valid before SCLK edge	10			ns
T7	Hold time, MOSI valid after SCLK edge	10			ns
T8	Time between two words for transmitting	170			ns

Reset Delay (R_{DELAY})

The R_{DELAY} output provides a constant current source to charge an external capacitor to approximately 6.5 V. The external capacitor is selected to provide a delay time, based on the current equation for a capacitor, $I = C(\Delta v/\Delta t)$ and a $28-\mu A$ typical output current.

Therefore, the user should select a 47-nF capacitor to provide a 6-ms delay at 3.55 V.

 $I = C(\Delta v/\Delta t)$ $28 \mu A = C \times (3.55 \text{ V/6 ms})$ C = 47 nF



APPLICATION INFORMATION

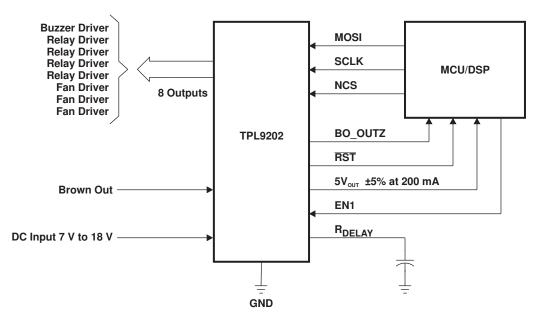


Figure 2. Typical Application

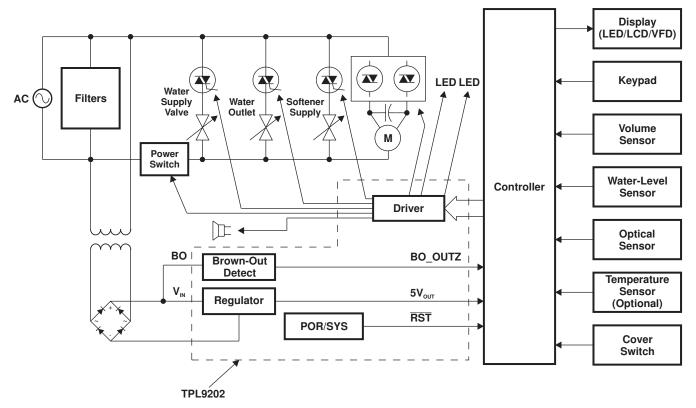


Figure 3. Washing-Machine Application

PCB Layout

To maximize the efficiency of this package for application on a single layer or multilayer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following information is to be used as a guideline only.

For further information, see the PowerPAD concept implementation document.

Application Using a Multilayer PCB

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane (see Figure 4 and Figure 5).

The efficiency of this method depends on several factors: die area, number of thermal vias, thickness of copper, etc. (see the *PowerPAD™ Thermally Enhanced Package Technical Brief*, literature number SLMA002).

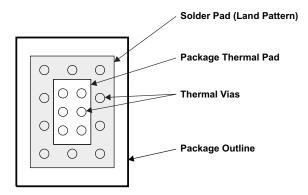


Figure 4. Package and PCB Land Configuration for a Multilayer PCB

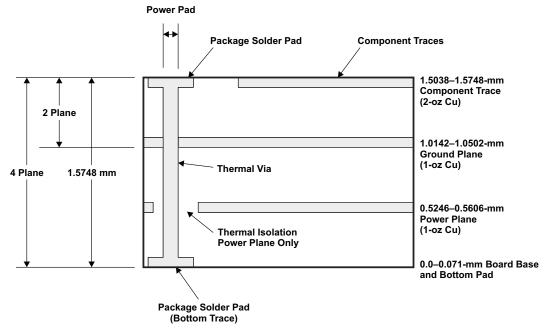


Figure 5. Multilayer Board (Side View)

Application Using a Single-Layer PCB

In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by a low thermal-impedance attachment method (solder paste or thermal conductive epoxy). With either method, it is advisable to use as many copper traces as possible to dissipate the heat.



CAUTION:

If the attachment method is not implemented correctly, the functionality of the product cannot be ensured. Power-dissipation capability is adversely affected if the device is incorrectly mounted on the circuit board.

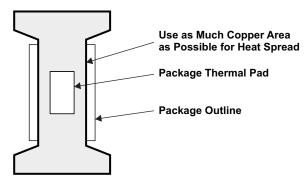


Figure 6. Layout Recommendations for a Single-Layer PCB



Recommended Board Layout

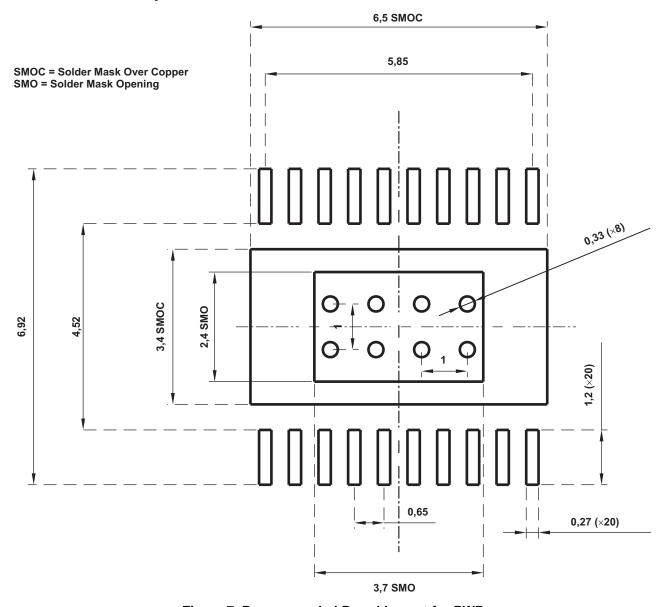


Figure 7. Recommended Board Layout for PWP





11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
TPL9202PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL202	Samples
TPL9202PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL202	Samples
TPL9202PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL202	Samples
TPL9202PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL202	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.





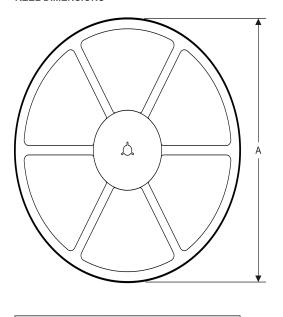
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PACKAGE MATERIALS INFORMATION

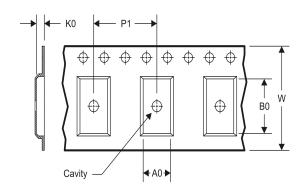
www.ti.com 14-Jul-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL9202PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

www.ti.com 14-Jul-2012

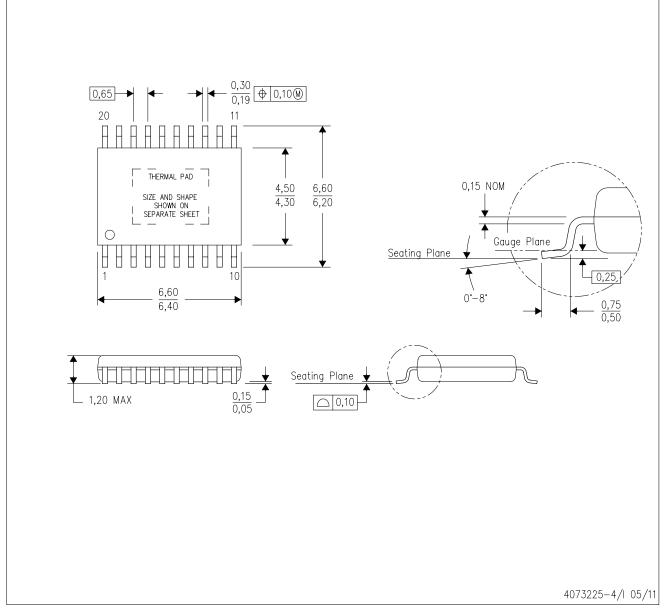


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL9202PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com http://www.ti.com.

 E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

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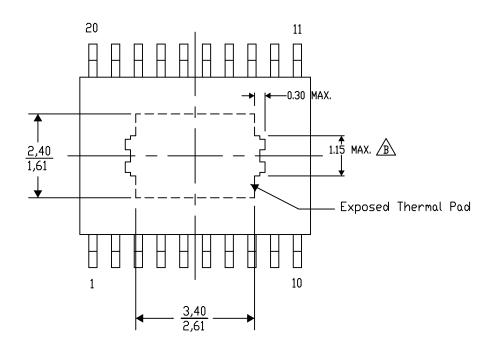
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPADTM package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

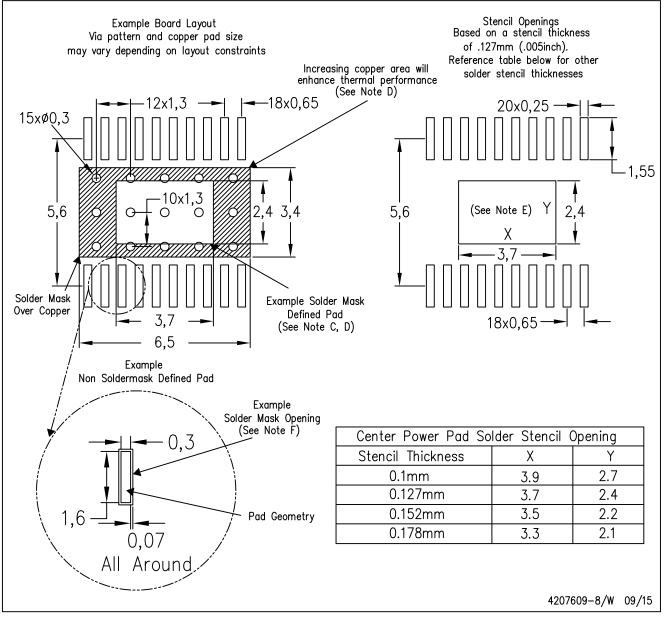
<u>/A</u> Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments



PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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