TLV7211, TLV7211A
CMOS COMPARATORS
WITH RAIL-TO-RAIL INPUT AND PUSH-PULL OUTPUT

SLCS149B – AUGUST 2006 – REVISED JANUARY 2007

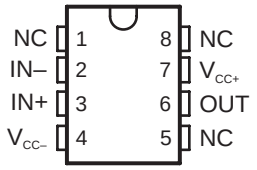
FEATURES

- **Parameters Specified at 2.7-V, 5-V, and 15-V Supplies**
- **Supply Current 7 μA (Typ) at 5 V**
- **Response Time 4 μs (Typ) at 5 V**
- **Push-Pull Output**
- **Input Common-Mode Range Beyond V_{CC-} and V_{CC+}**
- **Low Input Current**

APPLICATIONS

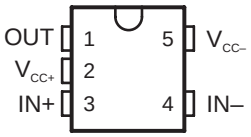
- **Battery-Powered Products**
- **Notebooks and PDAs**
- **Mobile Communications**
- **Alarm and Security Circuits**
- **Direct Sensor Interface**
- **Replaces Amplifiers Used as Comparators With Better Performance and Lower Current**

D PACKAGE
(TOP VIEW)

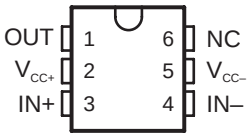


NC – No internal connection

DBV PACKAGE
(TOP VIEW)



DCK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TLV7211 and TLV7211A are micropower CMOS comparators available in the space-saving SOT-23-5 package. This makes the comparators ideal for space- and weight-critical designs. The TLV7211A features an input offset voltage of 5 mV, and the TLV7211 features an input offset voltage of 15 mV.

The main benefits of the SOT-23-5 package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the TLV7211 or TLV7211A a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

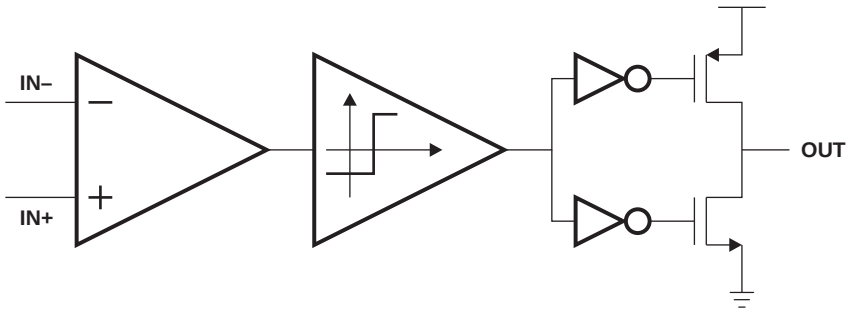
The SOT-23-5 package's small size allows it to fit into tight spaces on PC boards.

ORDERING INFORMATION

T_A	V_{OS} (MAX)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	5 mV	SOIC – D	Reel of 2500	TLV7211AIDR	7211AI
			Tube of 75	TLV7211AID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211AIDBVR	YBN_
		SOT (SC-70) – DCK	Reel of 3000	TLV7211AIDCKR	Y8_
			Reel of 250	TLV7211AIDCKT	
	15 mV	SOIC – D	Reel of 2500	TLV7211IDR	TY7211
			Tube of 75	TLV7211ID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211IDBVR	YBK_
		SOT (SC-70) – DCK	Reel of 3000	TLV7211IDCKR	Y7_
			Reel of 250	TLV7211IDCKT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage(2)			16	V
V_{ID}	Differential input voltage(3)			±Supply voltage	V
V_I	Input voltage range (any input)		V_{CC-} – 0.3	V_{CC+} + 0.3	V
V_O	Output voltage range		V_{CC-} – 0.3	V_{CC+} + 0.3	V
I_{CC}	Supply current			40	mA
I_I	Input current			±5	mA
I_O	Output current			±30	mA
θ_{JA}	Package thermal impedance(4)(5)	D package		97	°C/W
		DBV package		206	
		DCK package		259	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

ESD Protection

	TYP	UNIT
Human-Body Model	2000	V

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	2.7	15	V
T_J	Operating virtual junction temperature	–40	85	°C

2.7-V Electrical Characteristics

V_{CC+} = 2.7 V, V_{CC-} = GND, $V_{CM} = V_O = V_{CC+}/2$, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		1			1		µV/°C
	Input offset voltage average drift (1)		25°C		3.3			3.3		µV/month
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio	0 ≤ V_{CM} ≤ 2.7 V	25°C		75			75		dB
PSRR	Power-supply rejection ratio	2.7 V ≤ V_{CC+} ≤ 15 V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55 dB	25°C	2.9	3		2.9	3		V
			–40°C to 85°C	2.7			2.7			
		CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 2.5 mA	25°C	2.4	2.5		2.4	2.5		V
			–40°C to 85°C	2.3			2.3			
V_{OL}	Low-level output voltage	I_{load} = 2.5 mA	25°C		0.2	0.3		0.2	0.3	V
			–40°C to 85°C			0.4			0.4	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	12		7	12	µA
			–40°C to 85°C			14			14	
		V_{OUT} = High-Idle	25°C		5	10		5	10	
			–40°C to 85°C			12			12	

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.

5-V Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, $V_{CM} = V_O = V_{CC+}/2$, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		1			1		µV/°C
	Input offset voltage average drift (1)		25°C		3.3			3.3		µV/month
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio		25°C		75			75		dB
PSRR	Power-supply rejection ratio	5 V ≤ V_{CC+} ≤ 10 V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55 dB	25°C	5.2	5.3		5.2	5.3		V
			–40°C to 85°C	5			5			
		CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 5 mA	25°C	4.6	4.8		4.6	4.8		V
			–40°C to 85°C	4.45			4.45			
V_{OL}	Low-level output voltage	I_{load} = 5 mA	25°C		0.2	0.4		0.2	0.4	V
			–40°C to 85°C			0.55			0.55	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	14		7	14	µA
			–40°C to 85°C			18			18	
		V_{OUT} = High-Idle	25°C		5	10		5	10	
			–40°C to 85°C			13			13	
I_{OH}	Short-circuit output current	I_{source}	25°C	30			30			mA
I_{OL}	Short-circuit output current	I_{sink}, V_O < 12 V (2)	25°C	45			45			mA

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.
(2) Do not short circuit the output to V+ if V+ is >12 V.

15-V Electrical Characteristics

V_{CC+} = 15 V, V_{CC-} = GND, $V_{CM} = V_O = V_{CC+}/2$, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		4			4		µV/°C
	Input offset voltage average drift(1)		25°C		4			4		µV/month
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio		25°C		82			82		dB
PSRR	Power-supply rejection ratio	5 V ≤ V_{CC+} ≤ 10 V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55 dB	25°C	15.2	15.3		15.2	15.3		V
			–40°C to 85°C	15			15			
		CMRR > 55 dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 5 mA	25°C	14.6	14.8		14.6	14.8		V
			–40°C to 85°C	14.45			14.45			
V_{OL}	Low-level output voltage	I_{load} = 5 mA	25°C		0.2	0.4		0.2	0.4	V
			–40°C to 85°C			0.55			0.55	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	14		7	14	µA
			–40°C to 85°C			18			18	
		V_{OUT} = High-Idle	25°C		5	12		5	12	
			–40°C to 85°C			14			14	
I_{OH}	Short-circuit output current	I_{source}	25°C	30			30			mA
I_{OL}	Short-circuit output current	I_{sink}, V_O < 12 V(2)	25°C	45			45			mA

(1) Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst-case input conditions and includes the first 30 days of drift.
(2) Do not short circuit the output to V+ if V+ is >12 V.

Switching Characteristics

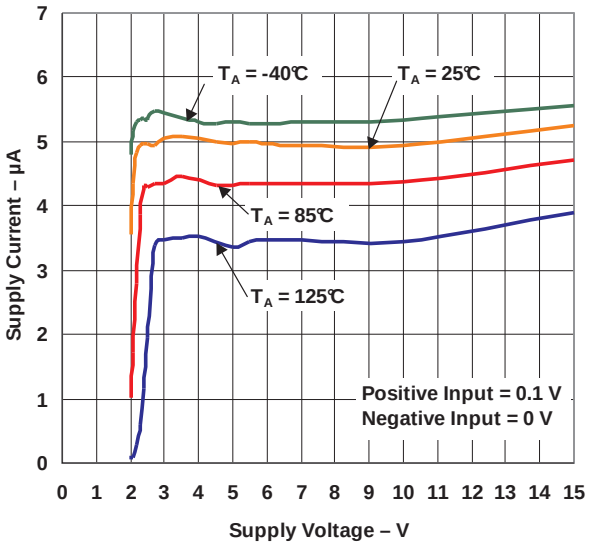
T_J = 25°C, V_{CC+} = 5 V, V_{CC-} = GND, V_{CM} = V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	UNIT
t_{rise}	Rise time	f = 10 kHz, C_L = 50 pF(1), Overdrive = 10 mV		0.3	µs
t_{fall}	Fall time	f = 10 kHz, C_L = 50 pF(1), Overdrive = 10 mV		0.3	µs
t_{PHL}	Propagation delay time, high to low(2)	f = 10 kHz, C_L = 50 pF(1)	10 mV	10	µs
			100 mV	4	
		V_{CC+} = 2.7 V, f = 10 kHz, C_L = 50 pF(1)	10 mV	10	
			100 mV	4	
t_{PLH}	Propagation delay time, low to high(2)	f = 10 kHz, C_L = 50 pF(1)	10 mV	6	µs
			100 mV	4	
		V_{CC+} = 2.7 V, f = 10 kHz, C_L = 50 pF(1)	10 mV	7	
			100 mV	4	

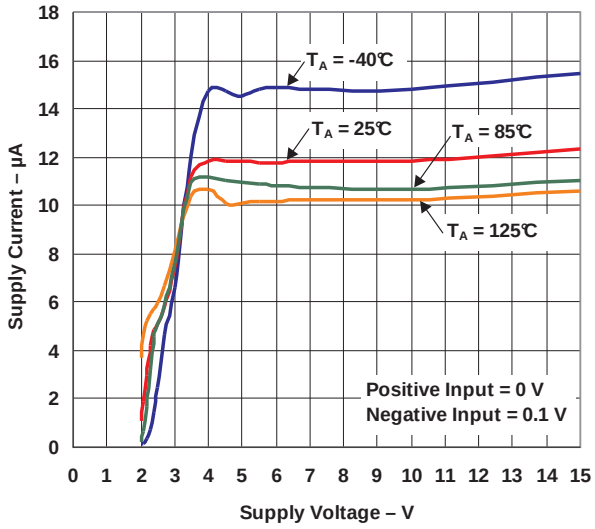
(1) C_L includes probe and jig capacitance.
(2) Input step voltage for propagation delay measurement is 2 V.

TYPICAL CHARACTERISTICS

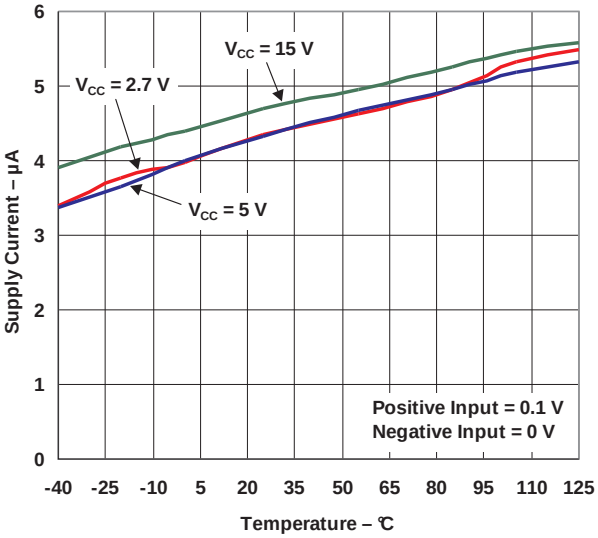
SUPPLY CURRENT vs SUPPLY VOLTAGE (SOURCING)



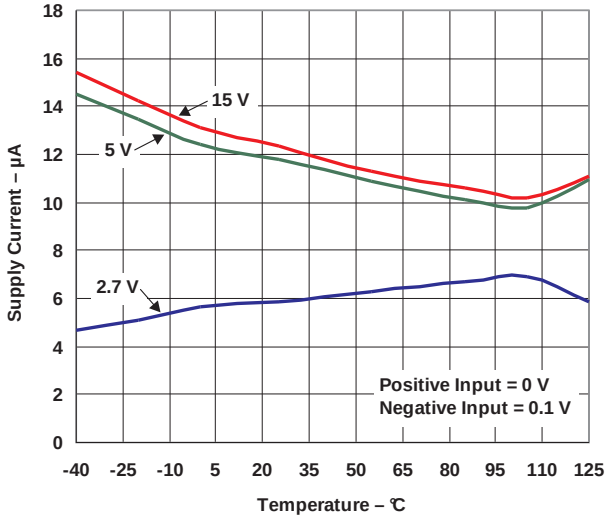
SUPPLY CURRENT vs SUPPLY VOLTAGE (SINKING)



SUPPLY CURRENT vs TEMPERATURE (SOURCING)

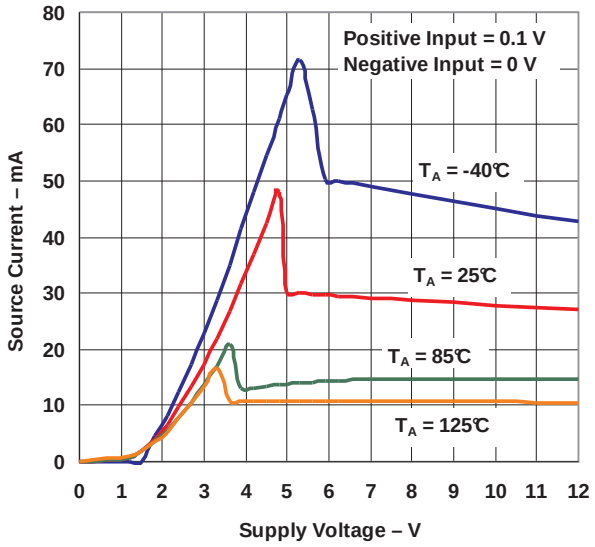


SUPPLY CURRENT vs TEMPERATURE (SINKING)

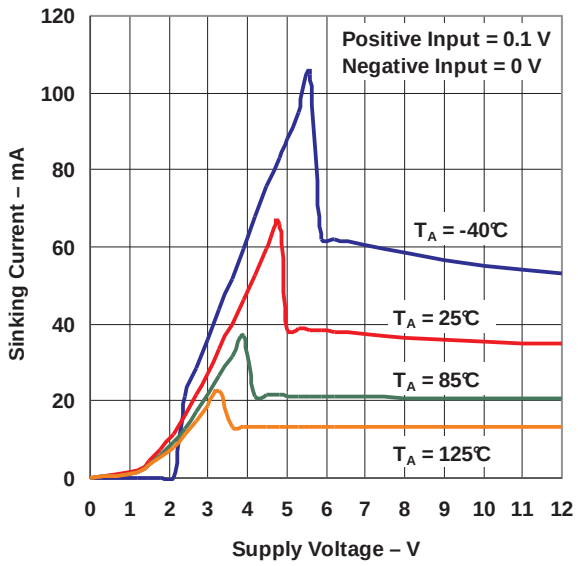


TYPICAL CHARACTERISTICS (continued)

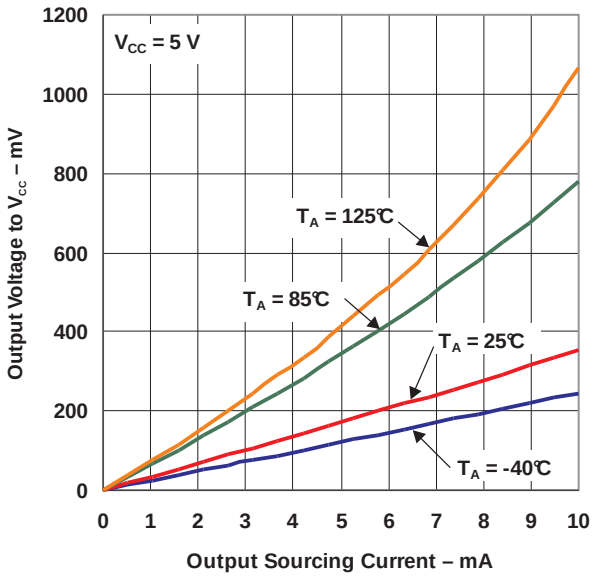
OUTPUT SOURCING CURRENT vs SUPPLY VOLTAGE



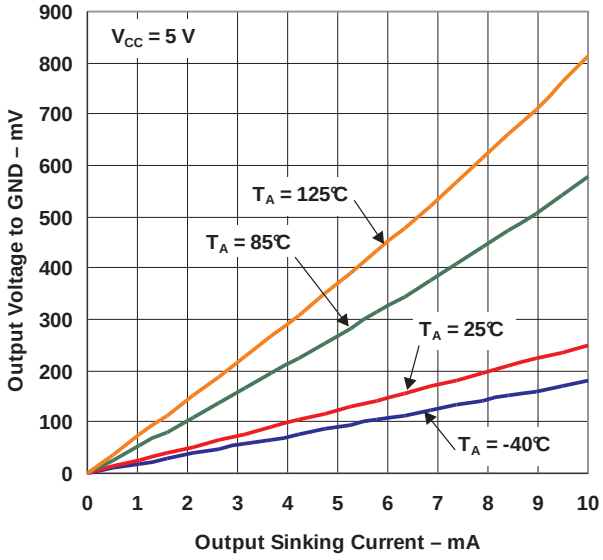
OUTPUT SINKING CURRENT vs SUPPLY VOLTAGE



OUTPUT VOLTAGE vs OUTPUT SOURCING CURRENT

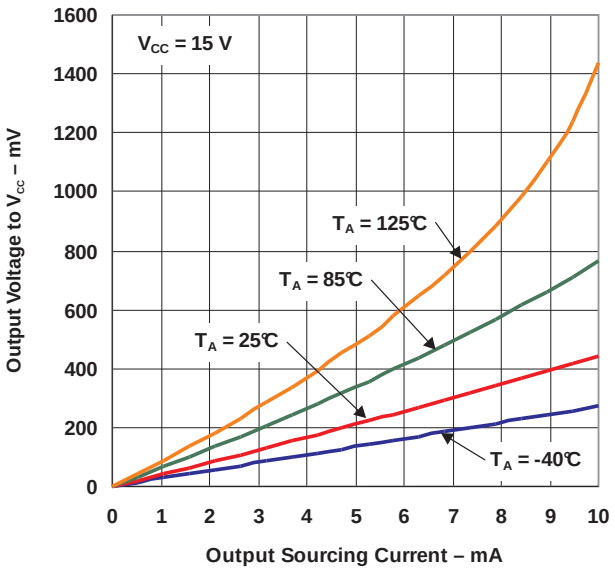


OUTPUT VOLTAGE vs OUTPUT SINKING CURRENT

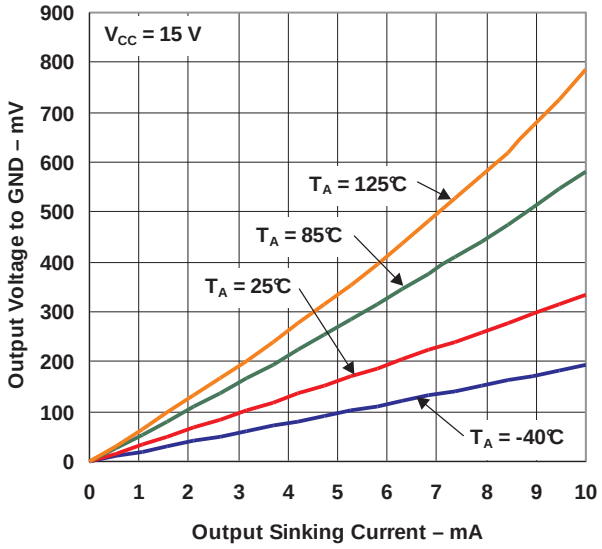


TYPICAL CHARACTERISTICS (continued)

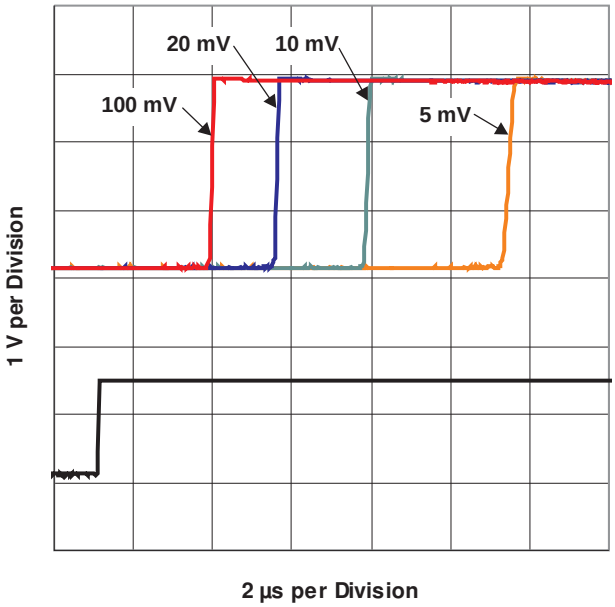
OUTPUT VOLTAGE vs OUTPUT SOURCING CURRENT



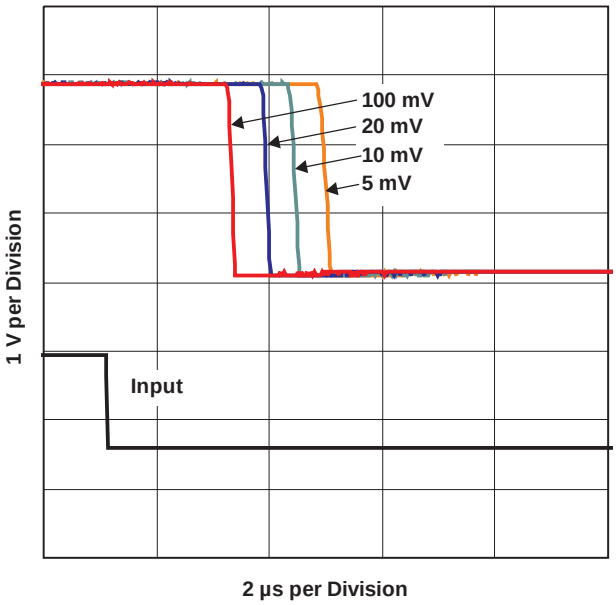
OUTPUT VOLTAGE vs OUTPUT SINKING CURRENT



Response Time (t_{PLH}) for Various Input Overdrives (V_{CC} = 2.7 V)

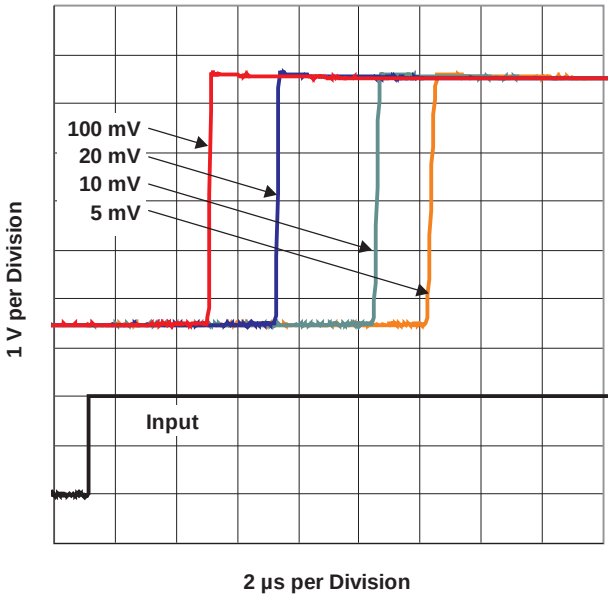


Response Time (t_{PHL}) for Various Input Overdrives (V_{CC} = 2.7 V)

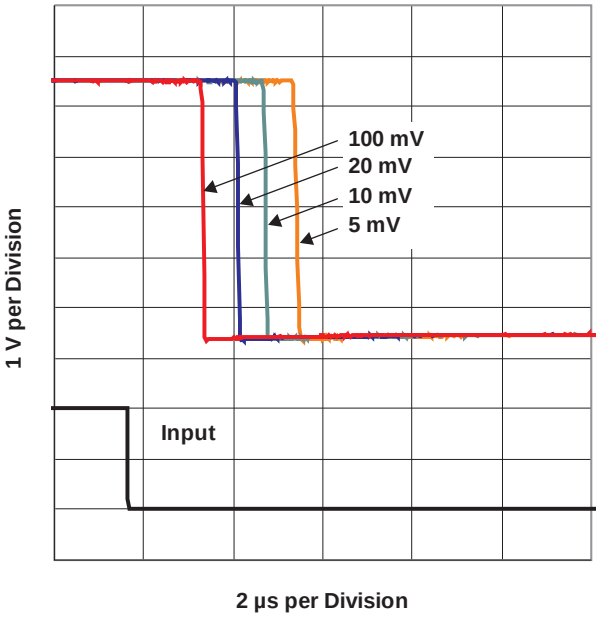


TYPICAL CHARACTERISTICS (continued)

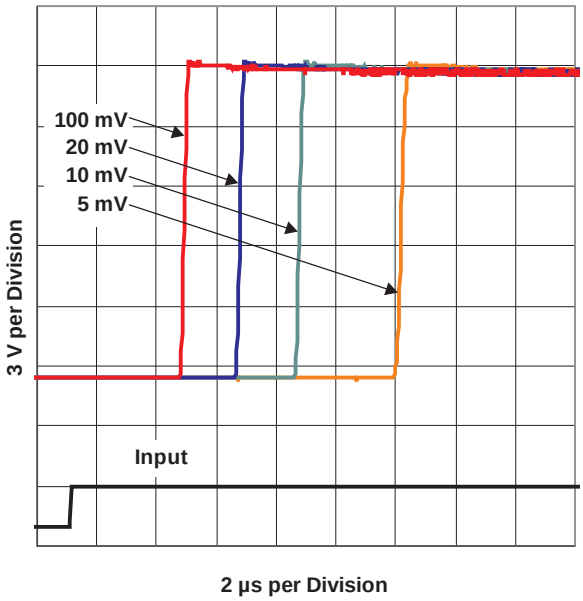
Response Time (t_{PLH}) for Various Input Overdrives (V_{CC} = 5 V)



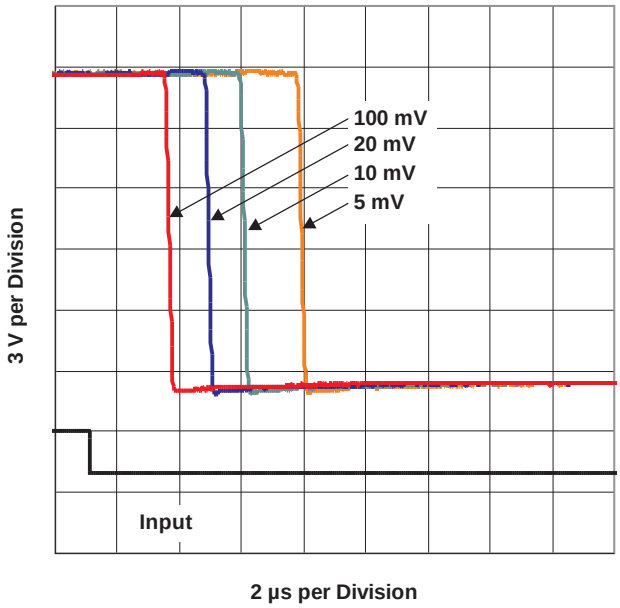
Response Time (t_{PHL}) for Various Input Overdrives (V_{CC} = 5 V)



Response Time (t_{PLH}) for Various Input Overdrives (V_{CC} = 15 V)



Response Time (t_{PHL}) for Various Input Overdrives (V_{CC} = 15 V)



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7211AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI	Samples
TLV7211AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YBNM	Samples
TLV7211AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y8A	Samples
TLV7211AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y8A	Samples
TLV7211AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI	Samples
TLV7211ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211	Samples
TLV7211IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YBKM	Samples
TLV7211IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y7A	Samples
TLV7211IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y7A	Samples
TLV7211IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

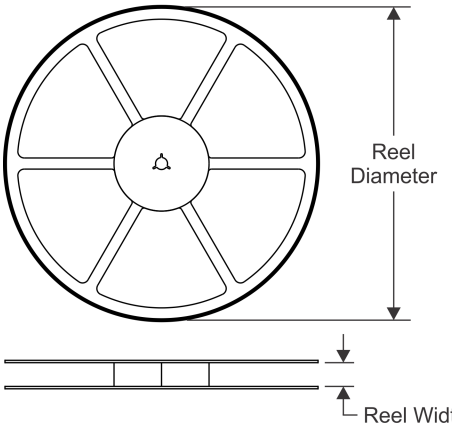
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

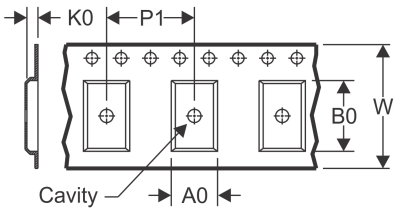
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

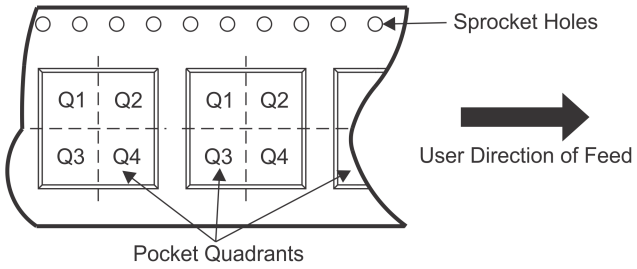


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

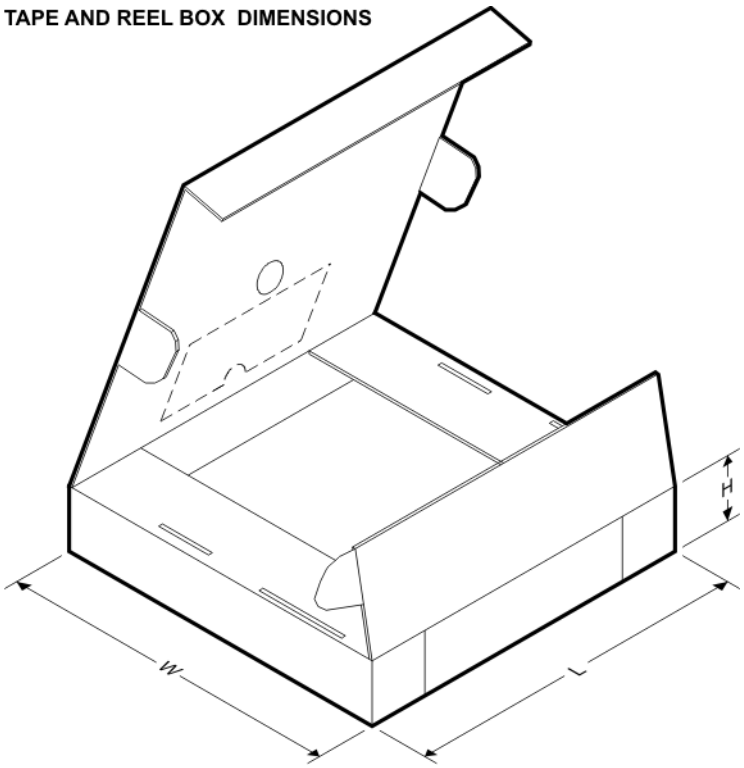
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7211AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7211AIDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TLV7211AIDCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TLV7211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV7211IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV7211IDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TLV7211IDCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TLV7211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

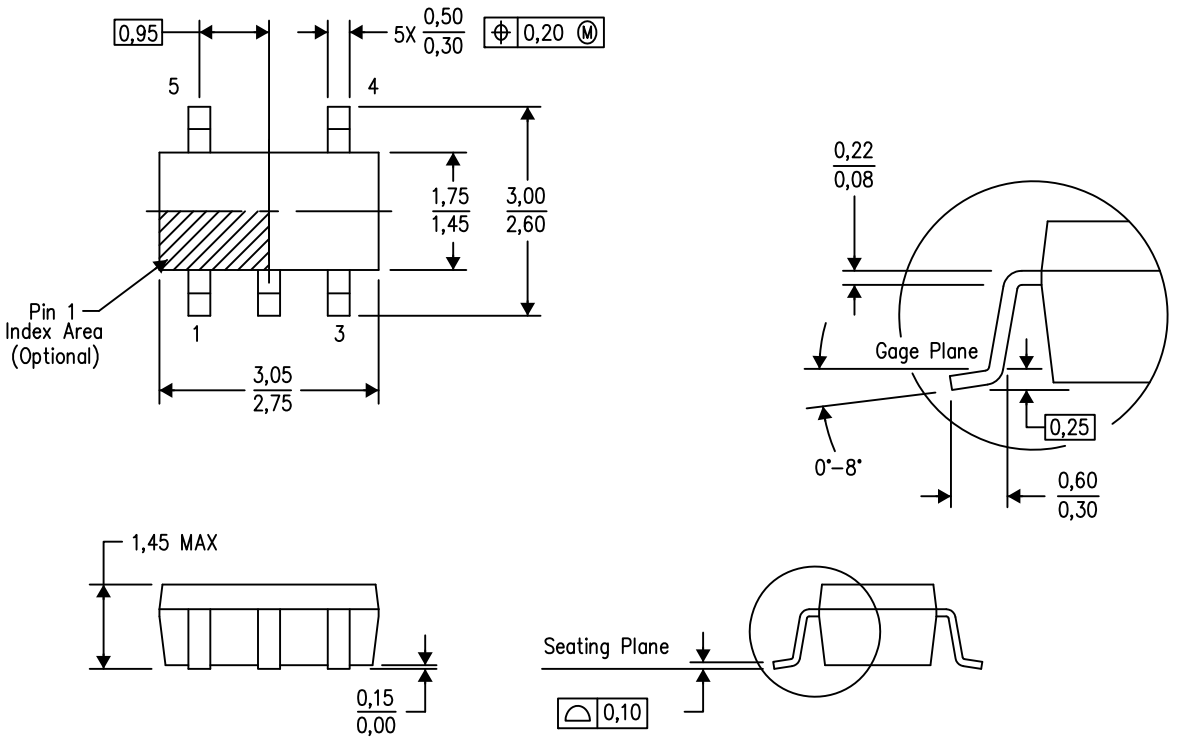
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7211AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211AIDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TLV7211AIDCKT	SC70	DCK	6	250	202.0	201.0	28.0
TLV7211AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV7211IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211IDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TLV7211IDCKT	SC70	DCK	6	250	202.0	201.0	28.0
TLV7211IDR	SOIC	D	8	2500	340.5	338.1	20.6

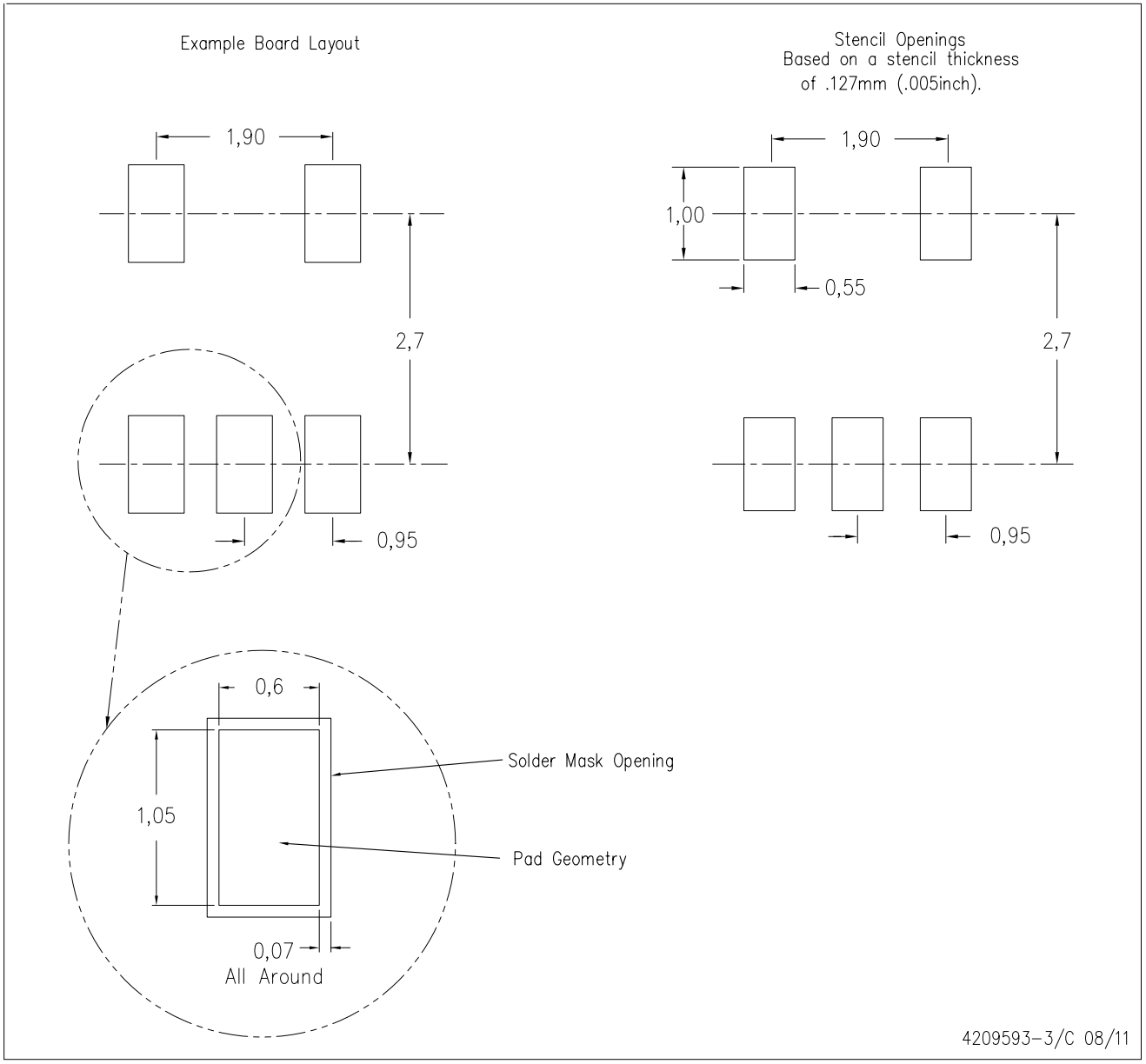
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

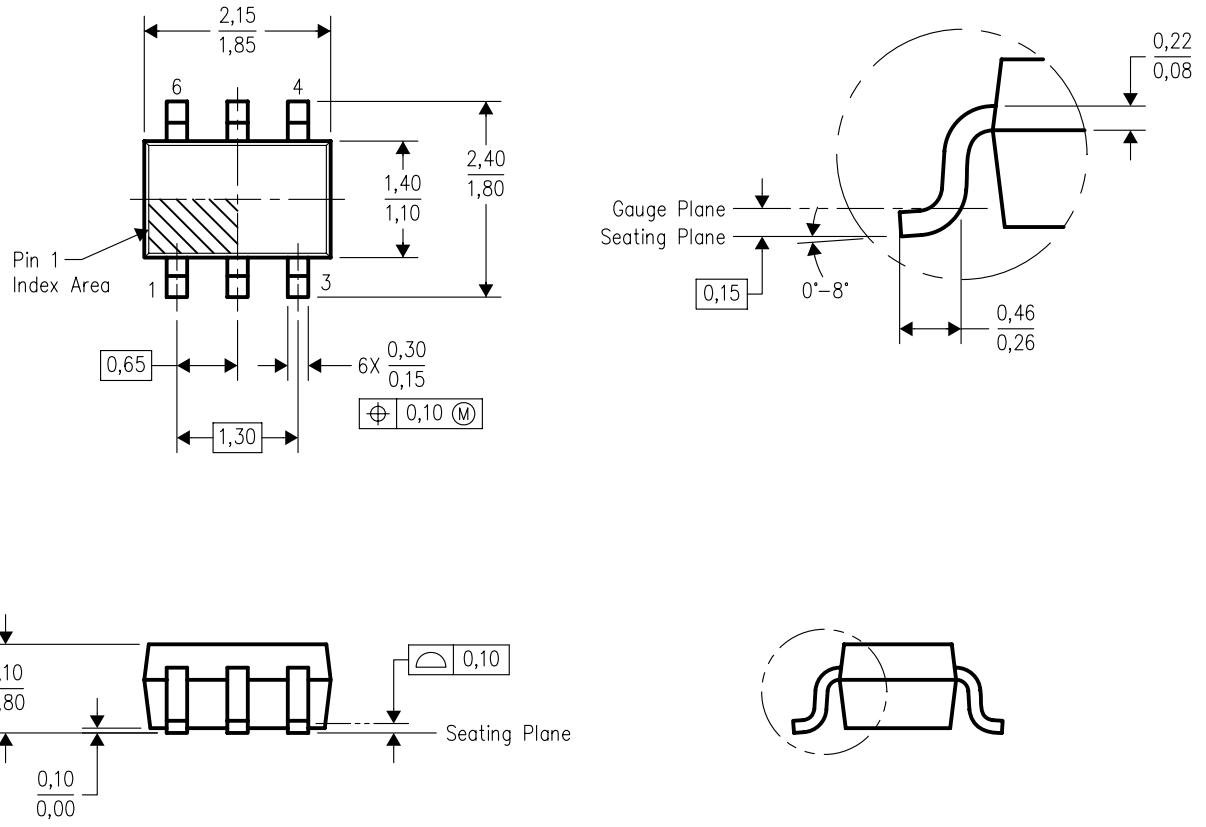
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

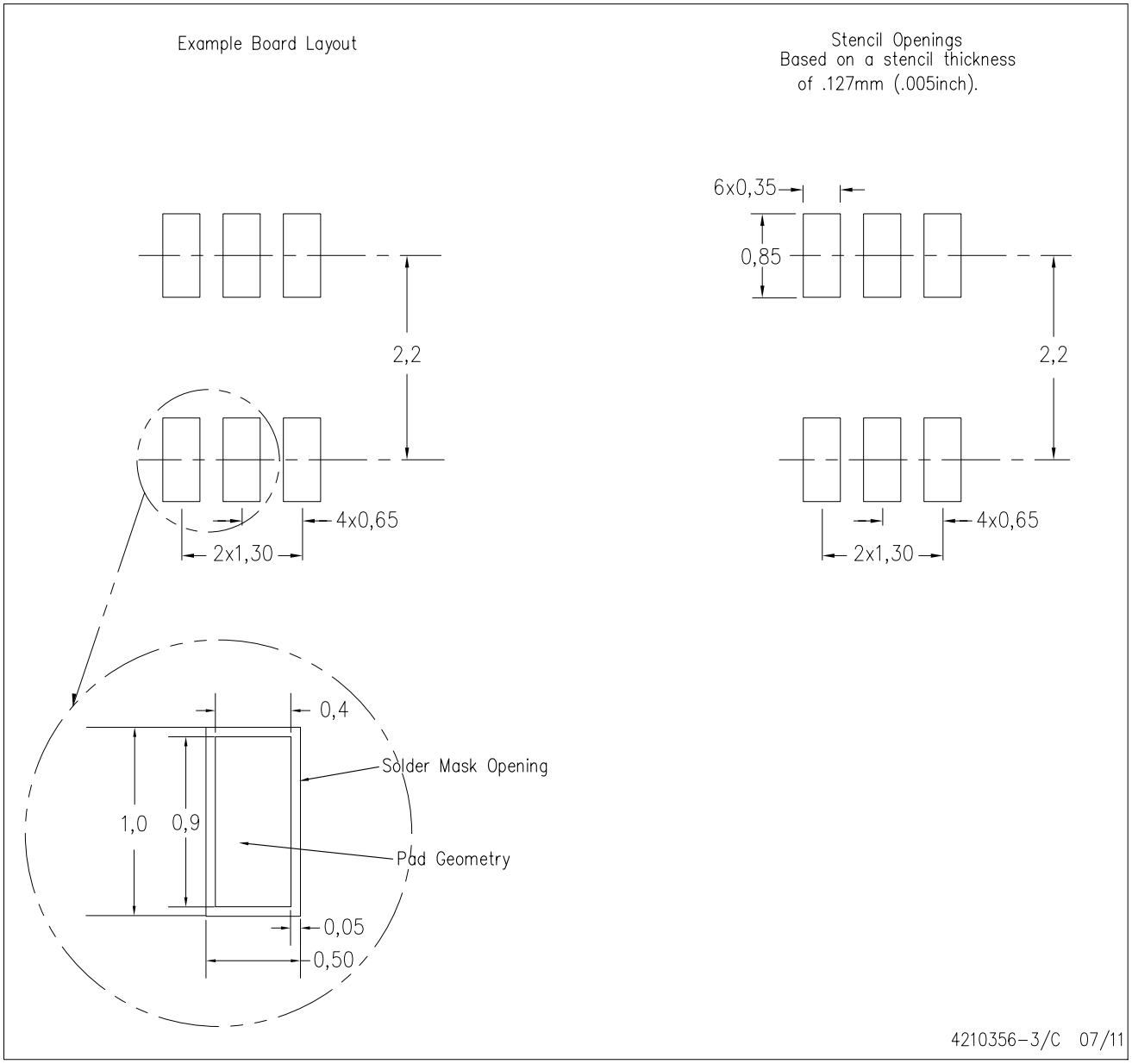
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

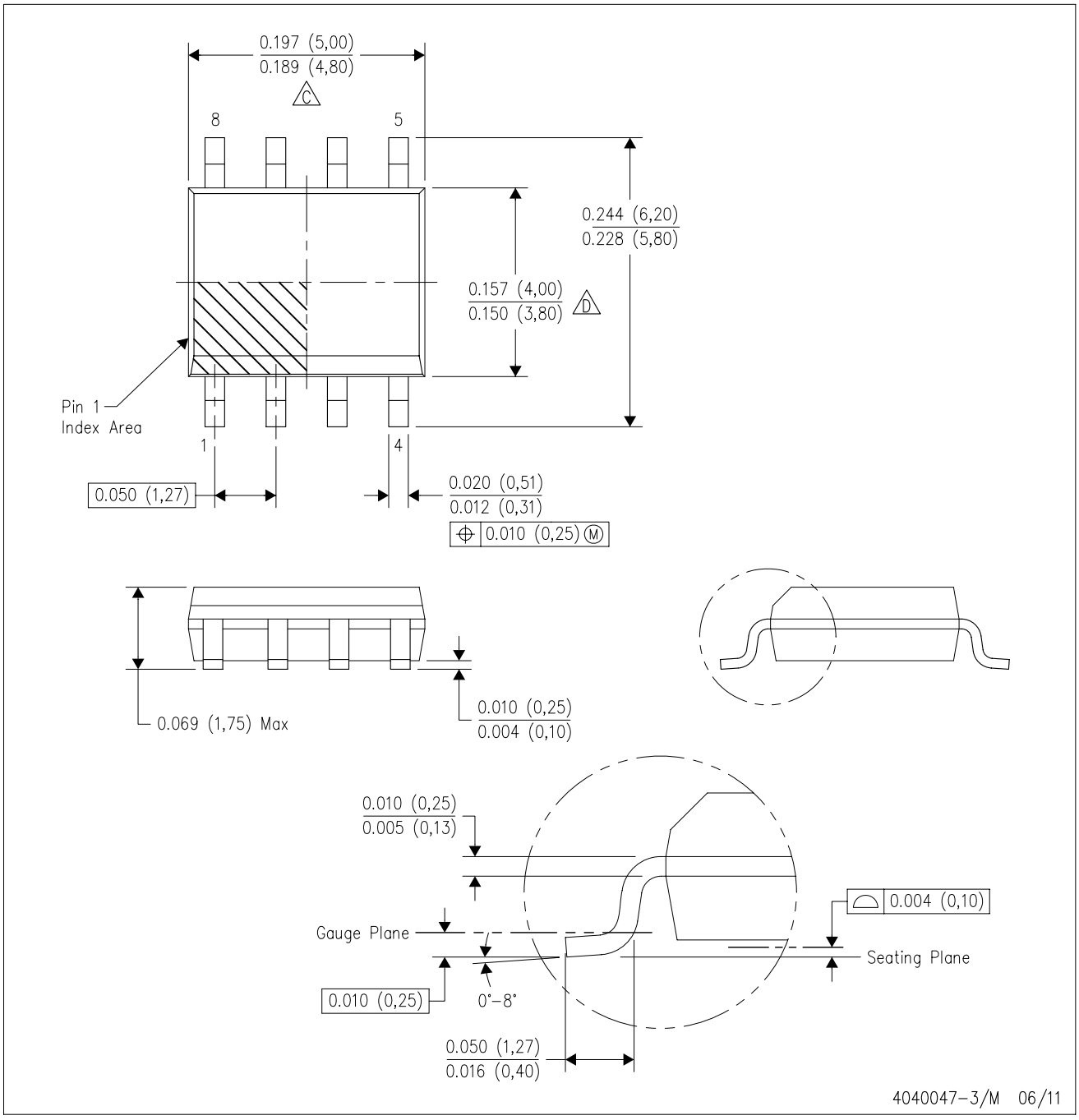
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



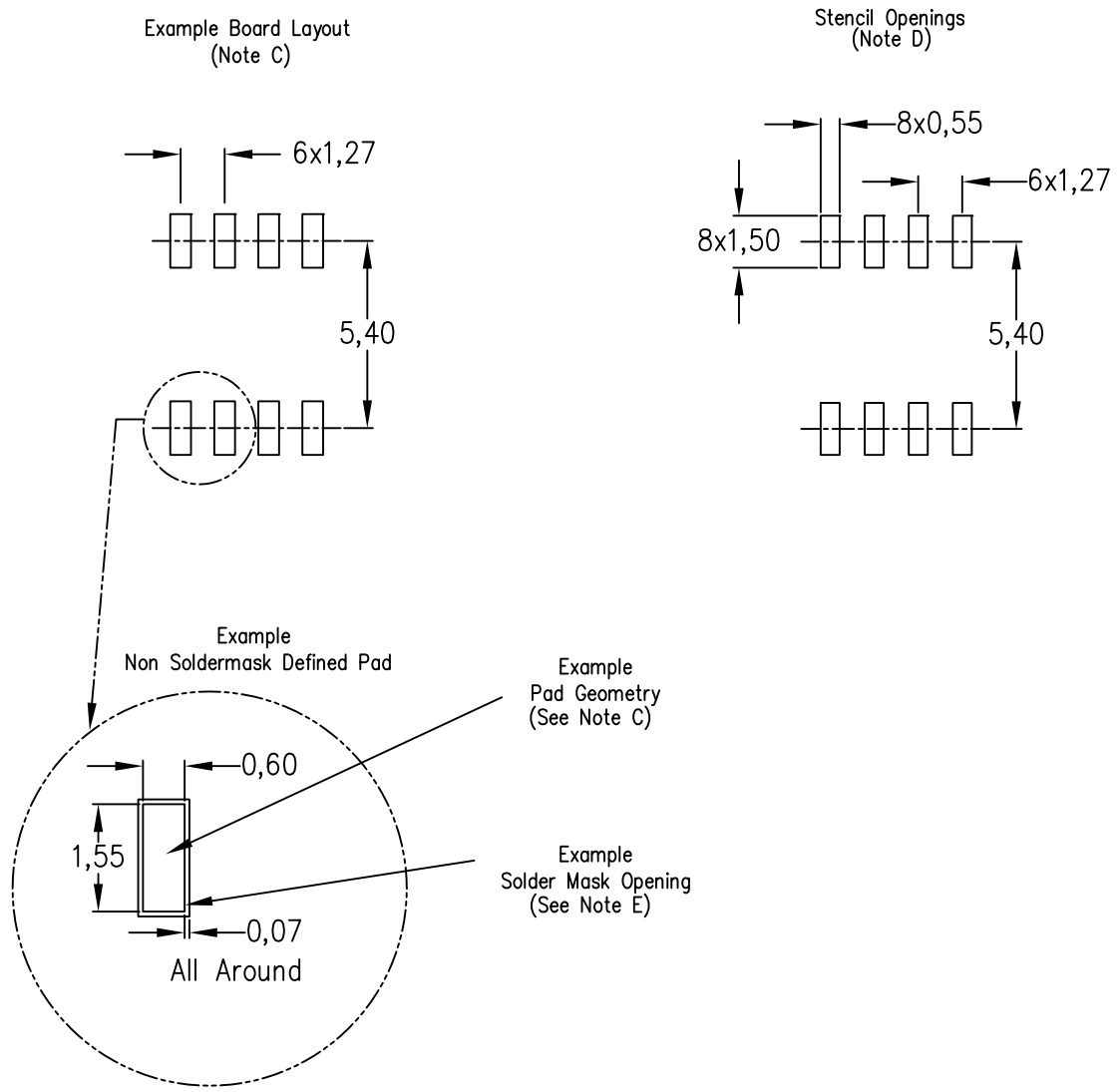
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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