Dual output AMOLED Display Power Supply

Check for Samples: TPS65138, TPS65138A

FEATURES

- **2.9V to 4.5V Input Voltage Range**
- **0.8% Output Voltage Accuracy V_{POS}**
- **Excellent Line Transient Regulation**
- **300mA Output Current**
- **Fixed 4.62V Positive Output Voltage**
- **Digitally Programmable V_{NEG}**
  - **TPS65138: -2.2V to -6.2V**
  - **TPS65138A: -2.2V to -5.2V**
- **-4.9V Default Value for V_{NEG}**
- **Short Circuit Protection**
- **Thermal Hhutdown**
- **3-mm × 3-mm QFN Package**

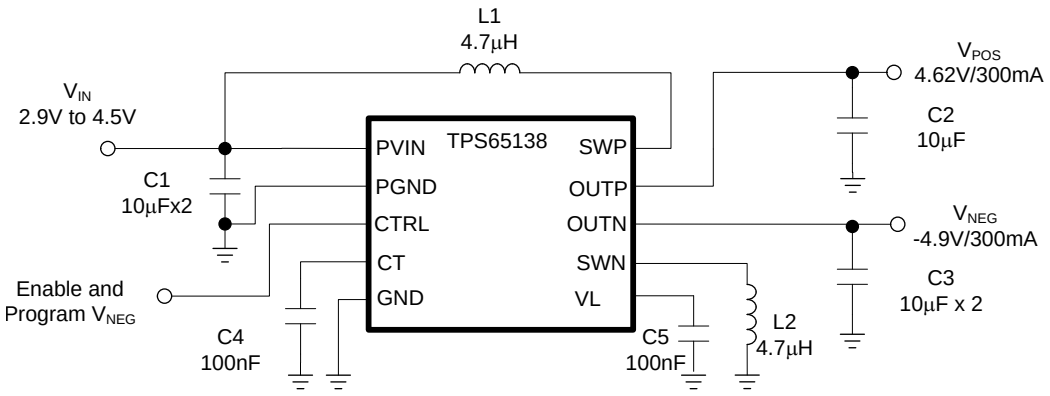
APPLICATIONS

- **Active Matrix OLED**

DESCRIPTION

The TPS65138 is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring positive and negative supply rails. The device integrates boost converter and inverting buck boost converter designed suitable for battery operated products. The digital control pin (CTRL) allows programming the negative output voltage in digital steps. The TPS65138 uses a novel technology enabling excellent line and load regulation. This is required to avoid disturbance of the AMOLED display by the input voltage disturbances occurring during transmit periods in mobile phones.

TYPICAL APPLICATION SCHEMATIC



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	V_{NEG} PROGRAMMING RANGE	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to +85°	-2.2V ~ -6.2V	10-Pin 3x3 QFN	TPS65138DRCR	PUCC
	-2.2V ~ -5.2V		TPS65138ADRCR	PXJI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	PVIN, SWP, OUTP, CTRL, VL		5.5	V
	OUTN		–6.5	
	SWN	–6.5	4.8	
	CT		3.6	
ESD rating	HBM		±2	kV
	MM		±200	V
	CDM		±500	V
Operating junction temperature range, T_J		–40	50	°C
Operating ambient temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND pin

THERMAL INFORMATION(1)

THERMAL METRIC		DRC	UNITS
		10-PINS	
θ_{JA}	Junction-to-ambient thermal resistance	54.7	°C/W
θ_{JB}	Junction-to-board thermal resistance	16.9	
ψ_{JT}	Junction-to-top characterization parameter	4.2	
ψ_{JB}	Junction-to-board characterization parameter	19.5	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9	3.7	4.5	V
T_A	Operating ambient temperature	–40	25	95	°C
T_J	Operating junction temperature	–40	85	125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, CTRL = V_{IN}, V_{POS} = 4.62V, V_{NEG} = –4.9V, T_A = –40°C to 95°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current and Thermal Protection						
V_{IN}	Input voltage range		2.9		4.5	V
I_Q	Operating quiescent current into V_{IN}	V_{POS} and V_{NEG} have no load (1)		13		mA
I_{SD}	Shutdown current into V_{IN}	CTRL = GND		0.1		µA
V_L	Output of internal regulator			5		V
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling			2.1	V
		V_{IN} rising			2.4	V
	Thermal shutdown			145		°C
	Thermal shutdown hysteresis			10		°C
Output V_{POS}						
V_{POS}	Positive output voltage			4.62		V
	Positive output voltage regulation	T_A = –40°C to 85°C	–0.8%		0.8%	
$r_{DS(on)}$	SWP MOSFET on-resistance	I_{SWP} = 200mA		200		mΩ
	SWN MOSFET rectifier on-resistance	I_{SWP} = 200mA		250		mΩ
f_{SWP}	SWP Switching frequency	I_{POS} = 0mA		1.6		MHz
I_{SWP}	SWP switch current limit	Inductor valley current	0.8	1		A
$V_{P(SCP)}$	Short circuit threshold in operation	V_{POS} falling		3.7		V
$t_{P(SCP)}$	Short circuit detection time in operation			8		ms
	Short circuit detection time in operation			3		ms
I_{LKG}	Leakage current into V_{POS}	CTRL = GND		2	5	µA
	Line regulation	I_{POS} = 400mA		0		%/V
	Load regulation			0		%/A

(1) With Inductor DFE252012C 4.7µH from TOKO

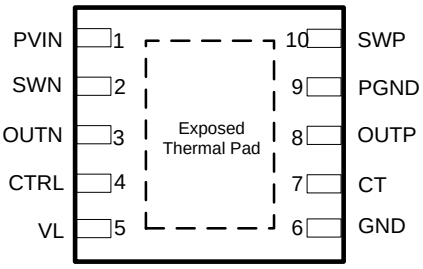
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.7V, CTRL = V_{IN}, V_{POS} = 4.62V, V_{NEG} = –4.9V, T_A = –40°C to 95°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output V_{NEG}						
V_{NEG}	Negative output voltage default			–.94		V
	Negative output voltage range	TPS65138	–2.2		–6.2	V
		TPS65138A	–2.2		–5.2	V
	Negative output voltage regulation	TPS65138, -6.2 ≤ V_{NEG} ≤ -4.2	–1%		1%	
		TPS65138A, -5.2 ≤ V_{NEG} ≤ -4.2	–1%		1%	
		-4.2 ≤ V_{NEG} ≤ -2.2	–1.5%		1.5%	
$r_{DS(on)}$	SWN MOSFET on-resistance	I_{SWN} = 200 mA		200		mΩ
	SWN MOSFET rectifier on-resistance	I_{SWN} = 200 mA		300		mΩ
f_{SWN}	SWN Switching frequency	I_{NEG} = 100 mA		1.6		MHz
	SWN switch current limit	V_{IN} = 2.9 V	1.8	2.2		A
$V_{N(SCP)}$	Short circuit threshold in operation			–1		V
	Short circuit threshold in start-up		0.15	0.28	0.42	V
$t_{N(SCP)}$	Short circuit detection time in start-up			8		V
	Short circuit detection time in operation			3		ms
I_{LKG}	Leakage current out of V_{NEG}	CTRL = GND		2	5	µA
$R_{N(PD)}$	V_{NEG} Pull down resistor before start up	I_{NEG} = 1 mA		270		Ω
	Line regulation			0		%/V
	Load regulation			0		%/A
CTRL Interface						
V_H	Logic high-level voltage		1.2			V
V_L	Logic low-level voltage				0.4	V
R	Pull down resistor		150	400	860	KΩ
t_{INIT}	Initialization time			300	400	µs
t_{OFF}	Shutdown time period		30		80	µs
t_{HIGH}	Pulse high level time period		2	10	25	µs
t_{LOW}	Pulse low level time period		2	10	25	µs
t_{STORE}	Data storage and accept time period		30		80	µs
R_T	C_T pin output impedance		150	325	500	kΩ

PINOUT

(TOP VIEW)



PIN FUNCTIONS

NUMBER	NAME	TYPE(1)	DESCRIPTION
1	PVIN	I	Input supply for the negative buck boost converter generating V_{NEG}
2,	SWN	I	Switch pin of the negative buck boost converter
3	OUTN	O	Output of the negative buck boost converter
4	CTRL	O	Combined enable and V_{NEG} program pin.
5	VL	O	Output of internal regulator
6	GND	G	Analog ground
7	CT	O	Sets the settling time for the voltage on V_{NEG} when programmed to a new value.
8	OUTP	O	Output of the boost converter
9	PGND	G	Power ground of the boost converter
10	SWP	I	Switch pin of the boost converter
	Exposed thermal pad	G	Connect this pad to analog GND.

(1) G = Ground, I = Input, O = Output

FUNCTIONAL BLOCK DIAGRAM

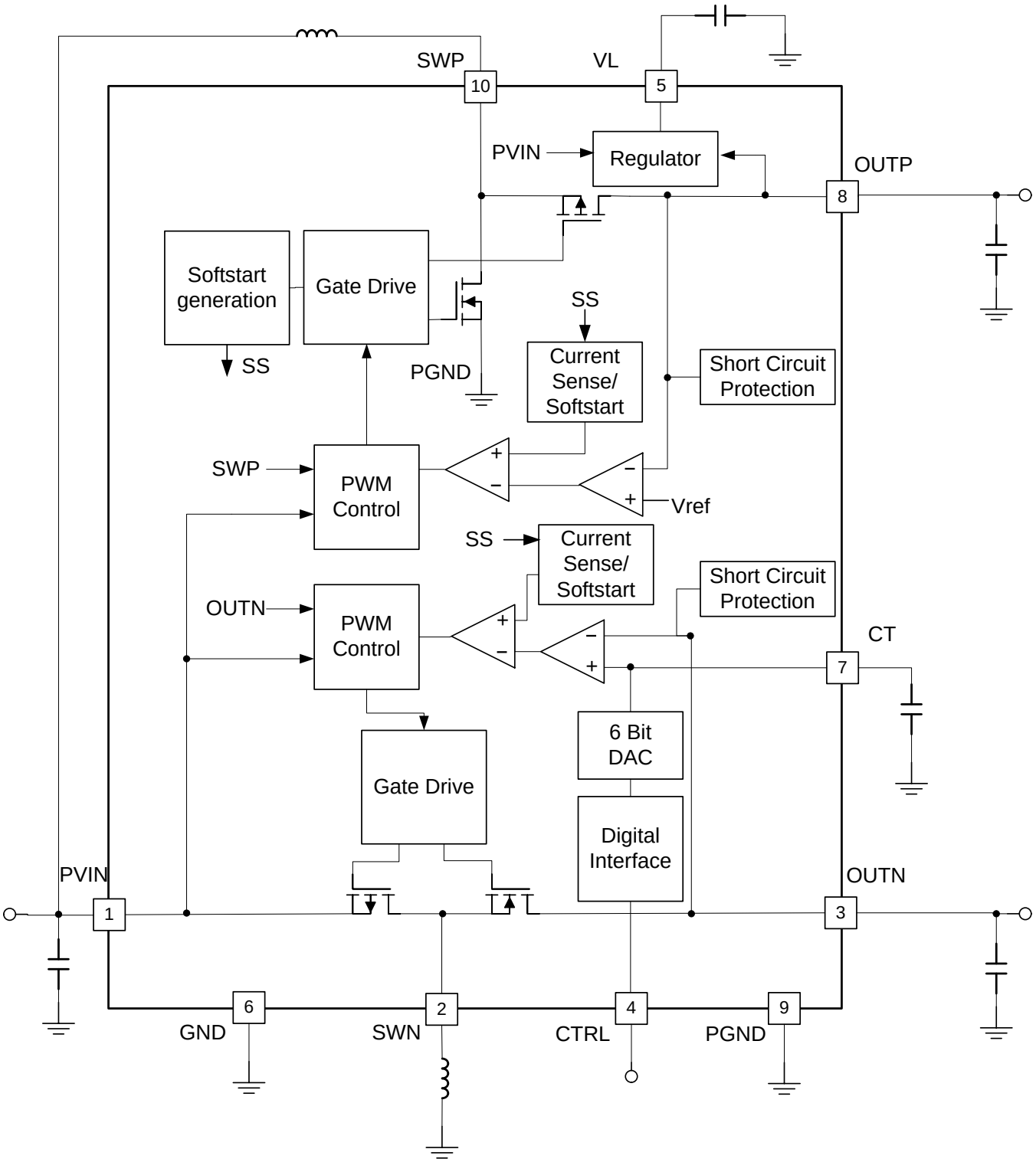


Table 1. TABLE OF GRAPHS

TITLE	TEST CONDITIONS	FIGURE
Efficiency versus Output current (Output current is from V_{POS} to V_{NEG}.)	V_{POS} 4.62 V, V_{NEG} -4.9 V	Figure 1
Start-up		Figure 2
Switch pins and output waveforms	I_{OUT} 100 mA, Boost and BuckBoost	Figure 3
	I_{OUT} 300 mA, Boost and BuckBoost	Figure 4
	I_{OUT} 300 mA, Boost	Figure 5
	I_{OUT} 300 mA, BuckBoost	Figure 6

TYPICAL CHARACTERISTICS

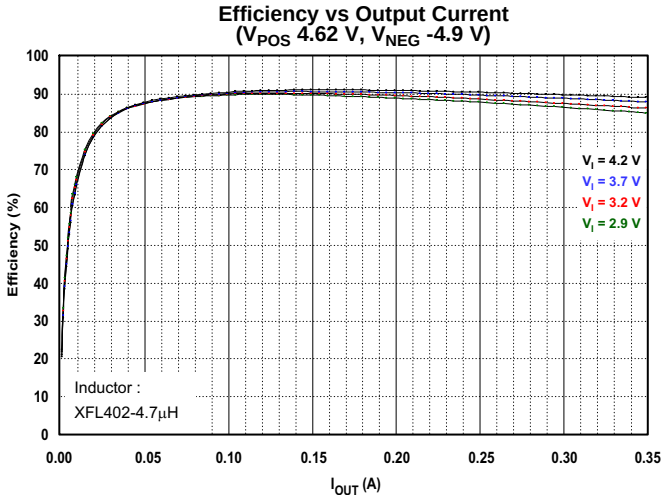


Figure 1.

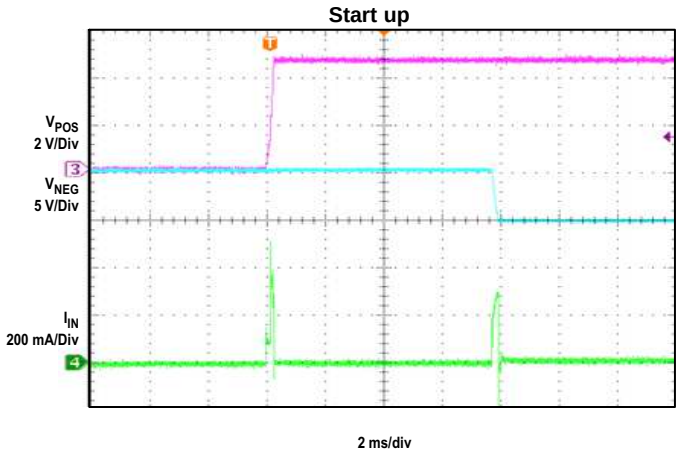


Figure 2.

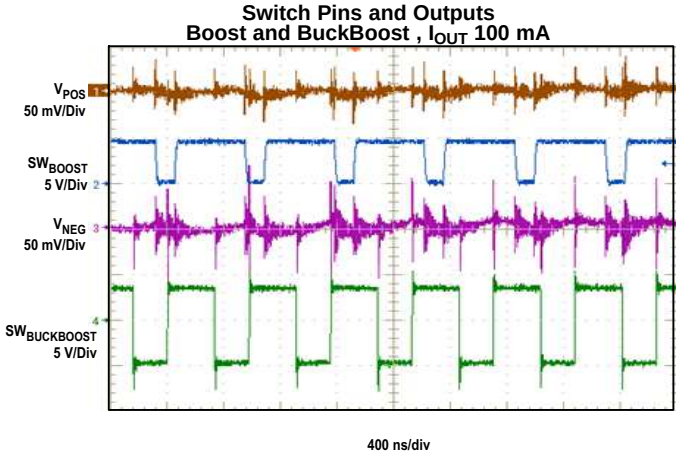


Figure 3.

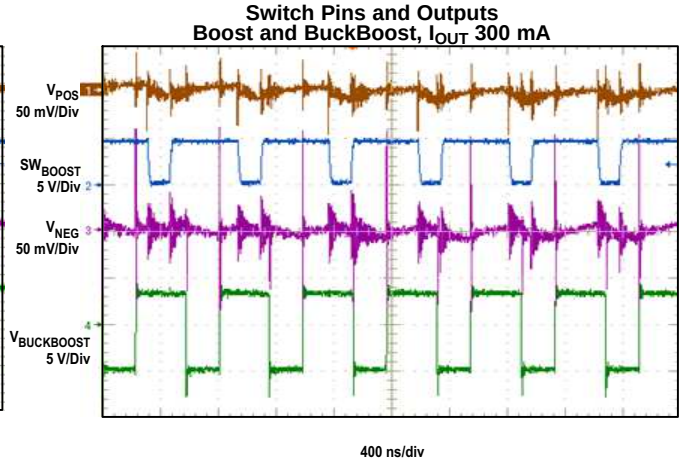


Figure 4.

TYPICAL CHARACTERISTICS (continued)

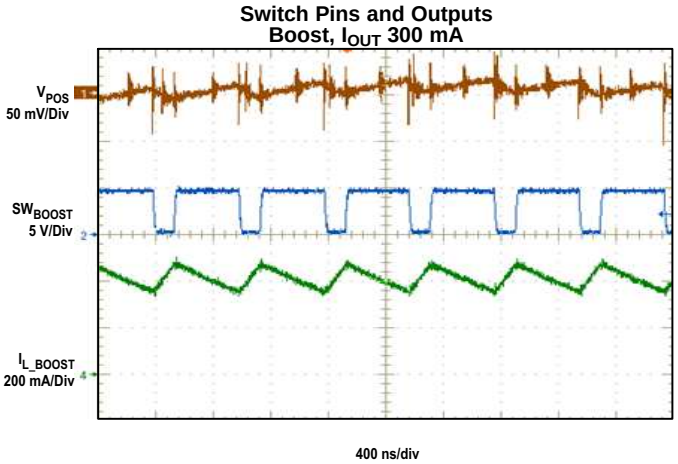


Figure 5.

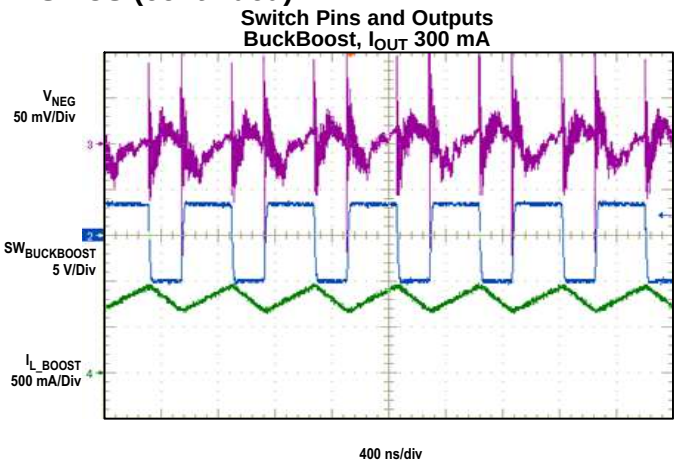


Figure 6.

APPLICATION INFORMATION

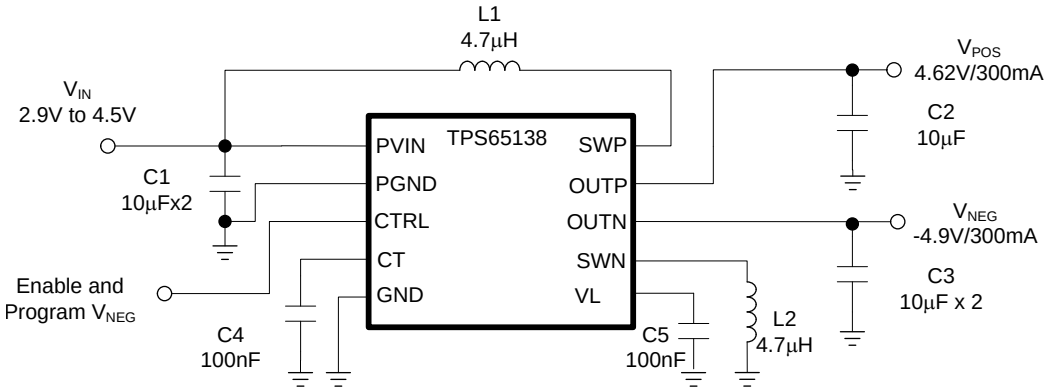


Figure 7. Application for Typical Characteristics

Table 2. Bill of Materials for Typical Characteristics

	Value	Part Number	Manufacturer
C1	10 µF, X7R	GRM21BR70J106KE76	Murata
C2A, C2B, C3A, C3B	4.7 µF, X7R	GRM21BR71A475KA73	Murata
C4, C5	100 nF, X7R	GRM21BR71E104KA01	Murata
L1, L2	4.7 µH	XFL4020-472M	Coil Craft

DETAIL DESCRIPTION

The TPS65138 consists of a boost converter and an inverting buck boost converter. The positive output is fixed at 4.62V. Negative output is programmable by a digital interface, and TPS65138 has the range of -2.2V to approximately -6.2V and TPS65138A has the range of -2.2V to approximately -5.2V. Both TPS65138 and TPS65138A have -4.9V of the default negative output. The transition time of the negative output is adjustable by the CT pin capacitor.

SOFT START and START-UP SEQUENCE

The device has soft start to limit in rush current. When the device is enabled by CTRL pin going HIGH, the boost converter starts with reduced switch current limit. 8 ms after CTRL HIGH, Buck boost converter starts with the default value. V_{NEG} default is –4.9 V. The typical start-up sequence is shown in Figure 8.

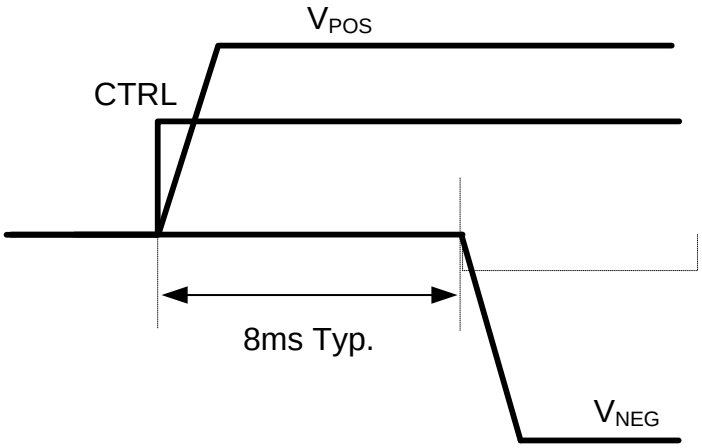


Figure 8. Start-up Sequence

SHORT CIRCUIT PROTECTION

The device is protected against short circuits of the outputs to ground and short circuit of the outputs each other. During normal operation, an error condition is detected if V_{POS} falls below 3.7 V for more than 3 ms or V_{NEG} is above -1 V for more than 3 ms. In either case, the device goes into shutdown and this state is latched. Input and outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

During start up, an error condition is detected in the following cases:

- V_{POS} is not in regulation 8ms after CTRL goes HIGH.
- V_{NEG} is higher than threshold level of 8ms after CTRL goes HIGH.
- V_{NEG} is not in regulation 16ms after CTRL goes HIGH.

For these cases, the device goes into shutdown and this state is latched. Input and outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is to enable and disable the device the other is the output voltage programming of the device. If the digital interface is not required the CTRL pin can be used as a standard enable pin for the device and the device will come up with its default value on V_{NEG} of -4.9V. When CTRL is pulled high, the device is enabled. The device is shut down with CTRL low.

DIGITAL INTERFACE (CTRL PIN)

The digital interface allows programming the negative output voltage V_{NEG} in digital steps. If the digital output voltage setting is not required then the CTRL pin can also be used as a standard enable pin. The digital output voltage programming of V_{NEG} is implemented by a simple digital interface with the timing shown in Figure 9.

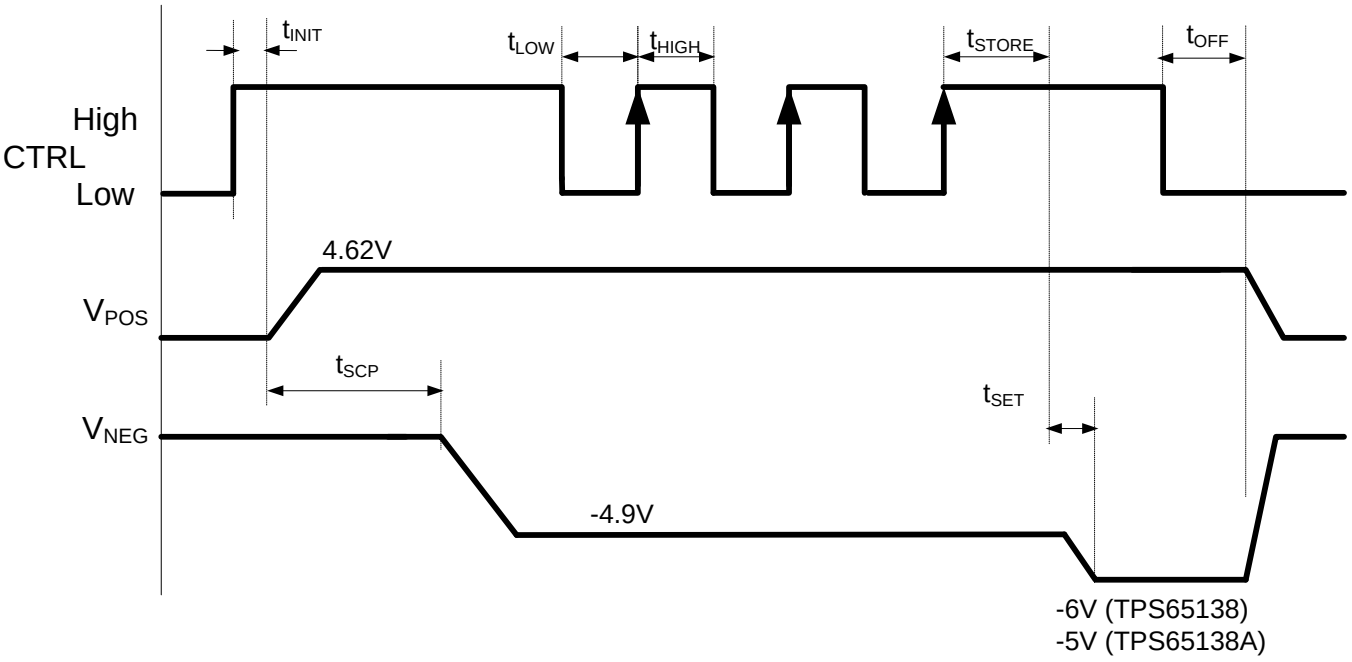


Figure 9. Digital Interface Using CTRL

Once CTRL is pulled high the device will come up with its default voltage of -4.9V. The device has a 6 bit DAC implemented with the corresponding output voltages as given in Table 3 and Table 4. The interface counts now the rising edges applied to CTRL pin once the device is enabled. For the timing table shown in Table 3 and Table 4, V_{NEG} is programmed to -6V in TPS65138 and -5V in TPS65138A, since 3 rising edges are detected. Other output voltages are programmed according to Table 3 and Table 4.

Table 3. TPS65138 Programming Table for V_{NEG}

Bit / rising edges	V_{NEG}	DAC Value	Bit / rising edges	V_{NEG}	DAC Value
0/ no pulse	-4.9V	000000	21	-4.2V	010101
1	-6.2V	000001	22	-4.1V	010110
2	-6.1V	000010	23	-4.0V	010111
3	-6.0V	000011	24	-3.9V	011000
4	-5.9V	000100	25	-3.8V	011001
5	-5.8V	000101	26	-3.7V	011010
6	-5.7V	000110	27	-3.6V	011011
7	-5.6V	000111	28	-3.5V	011100
8	-5.5V	001000	29	-3.4V	011101
9	-5.4V	001001	30	-3.3V	011110
10	-5.3V	001010	31	-3.2V	011111
11	-5.2V	001011	32	-3.1V	100000
12	-5.1V	001100	33	-3.0V	100001
13	-5.0V	001101	34	-2.9V	100010
14	-4.9V	001110	35	-2.8V	100011
15	-4.8V	001111	36	-2.7V	100100
16	-4.7V	010000	37	-2.6V	100101
17	-4.6V	010001	38	-2.5V	100110
18	-4.5V	010010	39	-2.4V	100111
19	-4.4V	010011	40	-2.3V	101000
20	-4.3V	010100	41	-2.2V	101001

Table 4. TPS65138A Programming Table for V_{NEG}

Bit / rising edges	V_{NEG}	DAC Value	Bit / rising edges	V_{NEG}	DAC Value
0/ no pulse	-4.9V	000000	16	-3.7V	010000
1	-5.2V	000001	17	-3.6V	010001
2	-5.1V	000010	18	-3.5V	010010
3	-5.0V	000011	19	-3.4V	010011
4	-4.9V	000100	20	-3.3V	010100
5	-4.8V	000101	21	-3.2V	010101
6	-4.7V	000110	22	-3.1V	010110
7	-4.6V	000111	23	-3.0V	010111
8	-4.5V	001000	24	-2.9V	011000
9	-4.4V	001001	25	-2.8V	011001
10	-4.3V	001010	26	-2.7V	011010
11	-4.2V	001011	27	-2.6V	011011
12	-4.1V	001100	28	-2.5V	011100
13	-4.0V	001101	29	-2.4V	011101
14	-3.9V	001110	30	-2.3V	011110
15	-3.8V	001111	31	-2.2V	011111

SETTING TRANSITION TIME t_{set} for V_{NEG}

The device allows setting the transition time t_{set} using an external capacitor connected to pin CT. The transition time is the time period required to move V_{NEG} from one voltage level to the next programmed voltage level. The capacitor connected to pin CT does not influence on the soft start time t_{ss} of V_{NEG} default value. When the CT pin is left open then the shortest possible transition time is programmed. When connecting a capacitor to the CT pin then the transition time is given by the R-C time constant. This is given by the output impedance of the CT pin typically 325 kΩ and the external capacitance. Within one τ the output voltage of V_{NEG} has reached 70% of its programmed value. An example is given when using 100nF for C_T.

$$\tau \approx t_{set\ 70\%} = 325k\Omega \times C_T = 325k\Omega \times 100nF = 32.5ms \quad (1)$$

The V_{NEG} programmed voltage is almost in nominal value after 3 τ.

PCB LAYOUT DESIGN GUIDELINES

Figure 10 and Figure 11 show the example of PCB layout design.

1. Place the input capacitor on PVIN and the output capacitor on OUTN as close as possible to device. Use short and wide traces to connect the input capacitor on PVIN and the output capacitor on OUTN.
2. Place the output capacitor on OUTP as close as possible to device. Use short and wide traces to connect the output capacitor on OUTP.
3. Connect the ground of CT capacitor with GND, pin 6, directly.
4. Connect input ground and output ground on the same board layer, not through via hole.

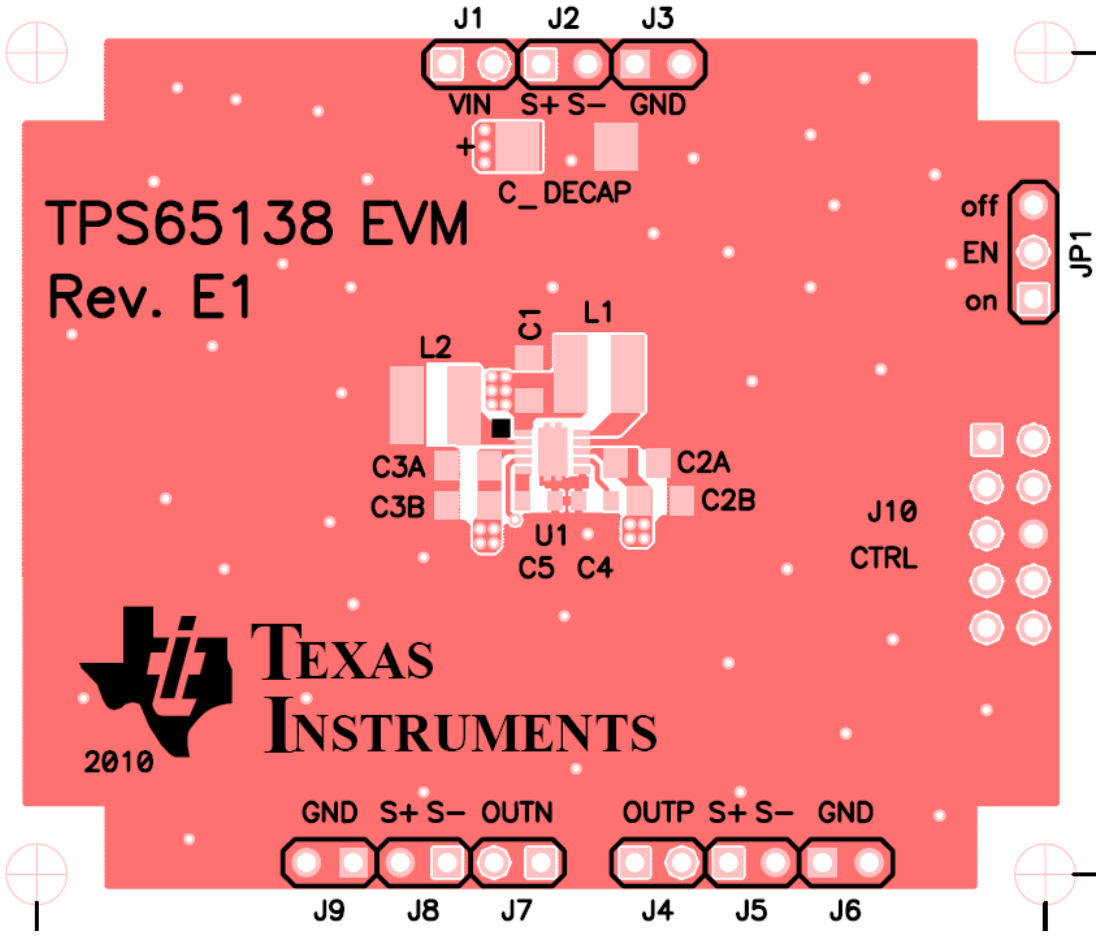


Figure 10. Example of Board Layout. Top Layer

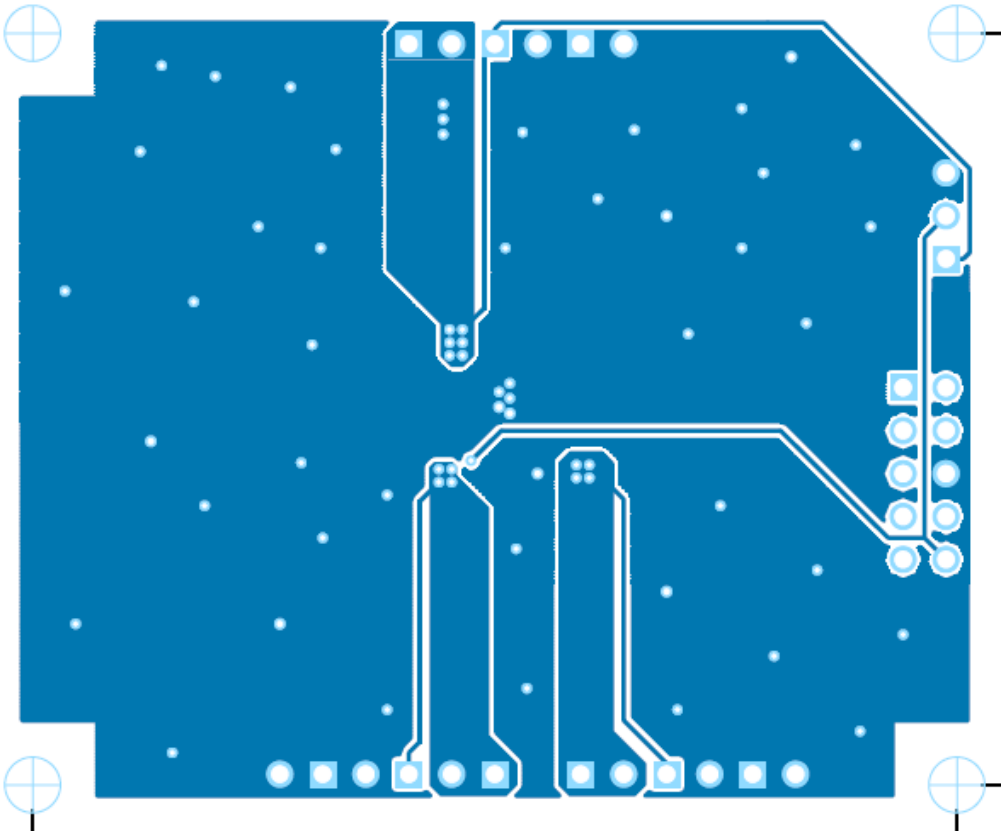


Figure 11. Example of Board Layout. Bottom Layer

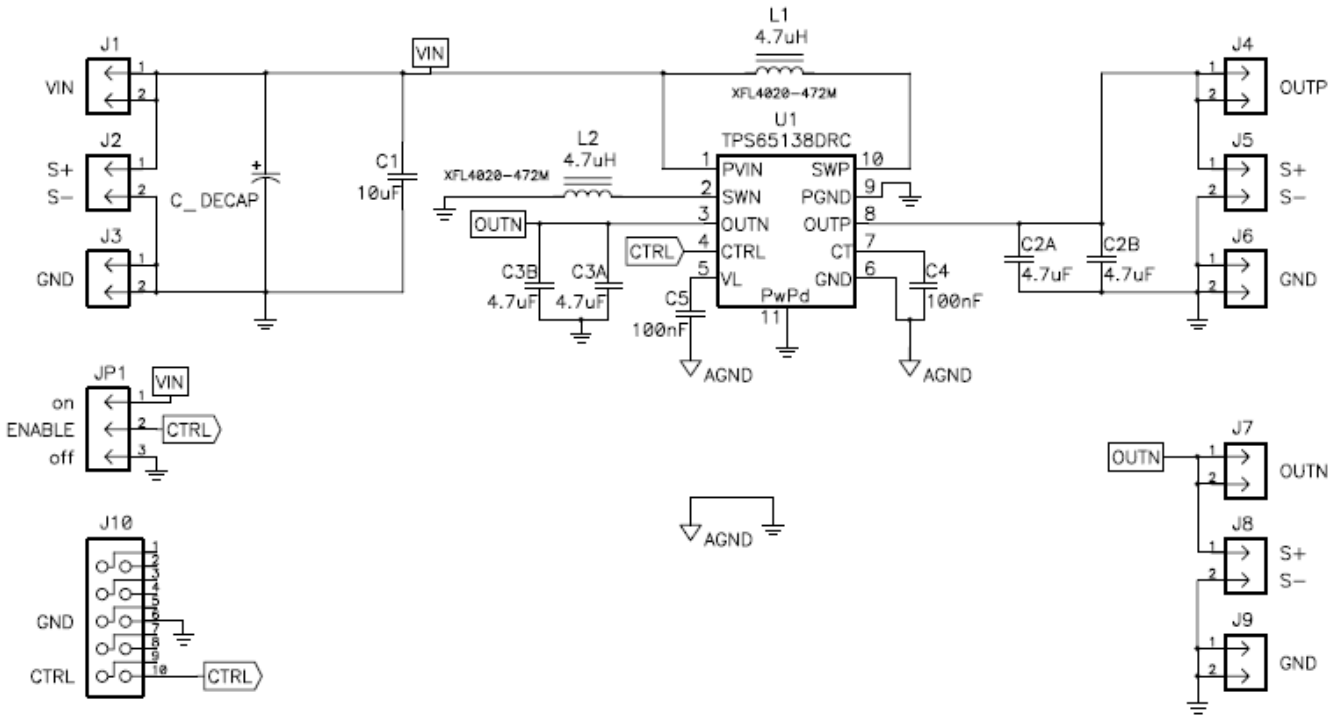


Figure 12. Schematic of Board Layout Example

REVISION HISTORY

Changes from Original (April 2011) to Revision A **Page**

- Changed the TYPICAL CHARACTERISTICS. Deleted Figure 2, Figure 3, Figure 9 through Figure 12 7

Changes from Revision A (May 2011) to Revision B **Page**

- Added Feature TPS65138A: -2.2V to -5.2V 1
- Added V_{NEG} Negative output voltage range for TPS65138A, -2.2V to -5.2V 4
- Added V_{NEG} programming range of TPS65138A, -2.2V to -5.2V to the Detailed Decsription 9
- Changed Figure 9 10

Changes from Revision B (April 2012) to Revision C **Page**

- Changed the device From: Product Preview To: Production 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65138ADRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PXJI	Samples
TPS65138DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PUCC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

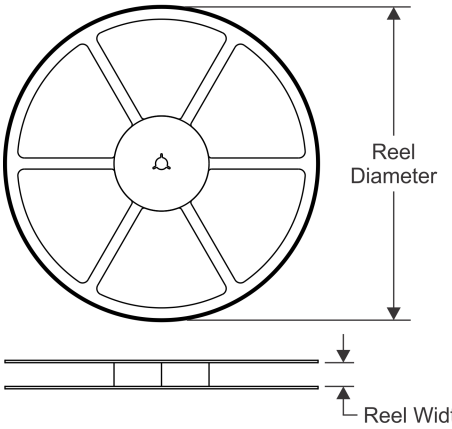
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

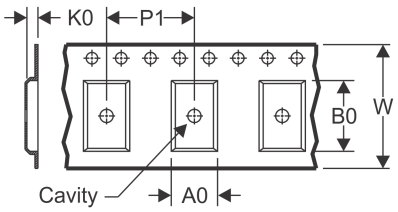
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

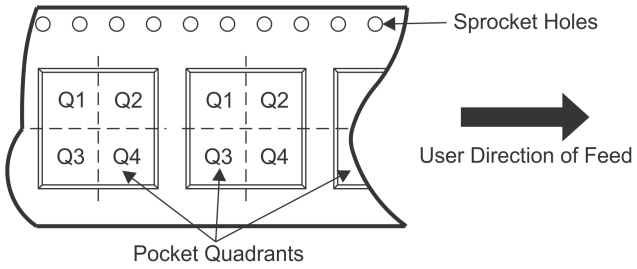


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

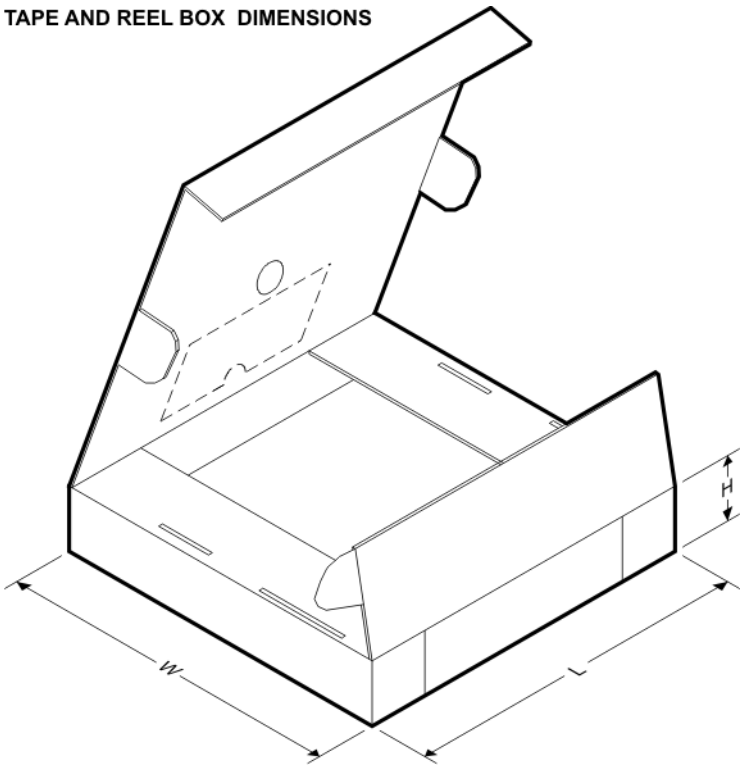
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65138ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65138DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

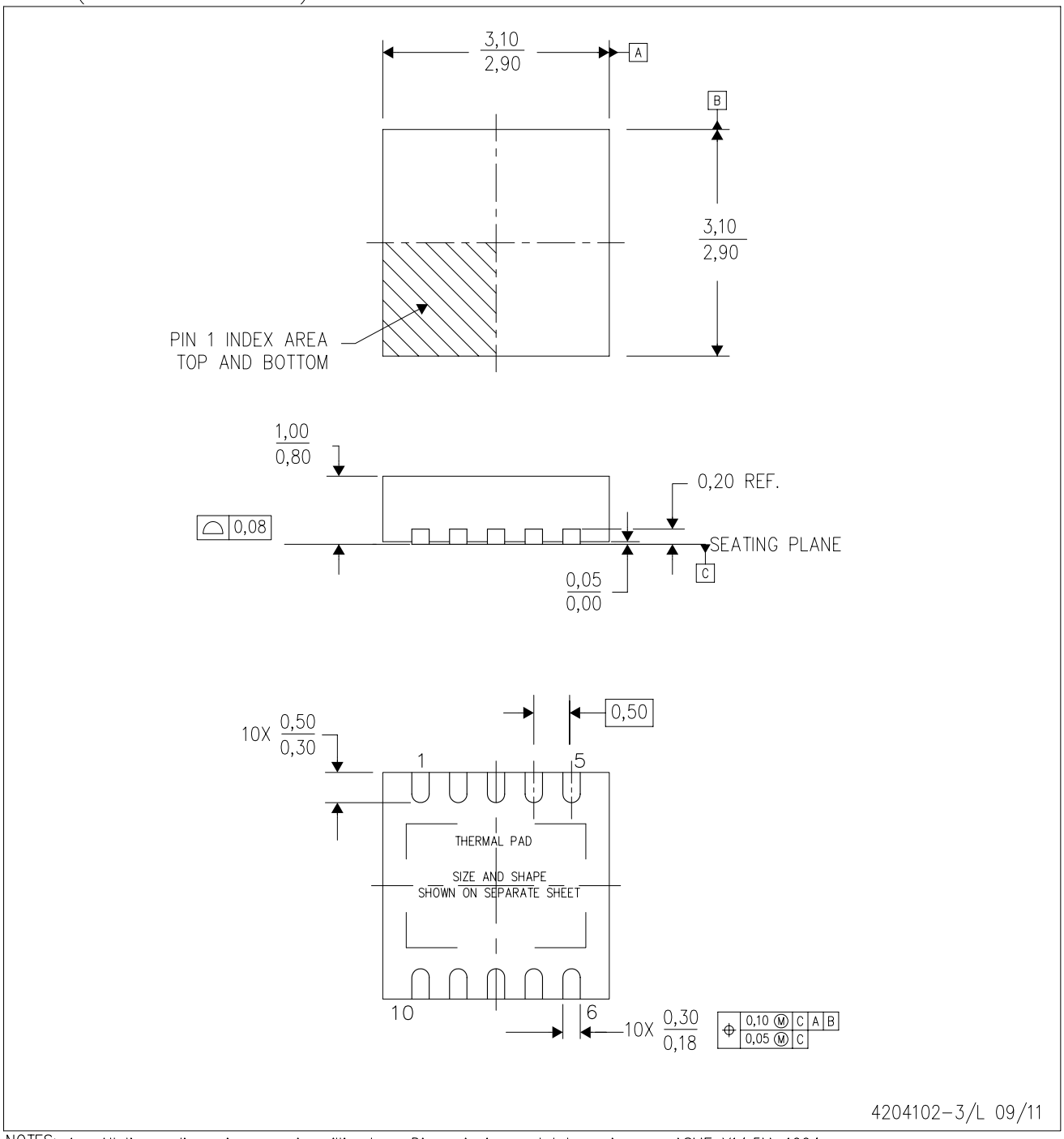
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65138ADRCR	VSON	DRC	10	3000	552.0	367.0	36.0
TPS65138DRCR	VSON	DRC	10	3000	552.0	367.0	36.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

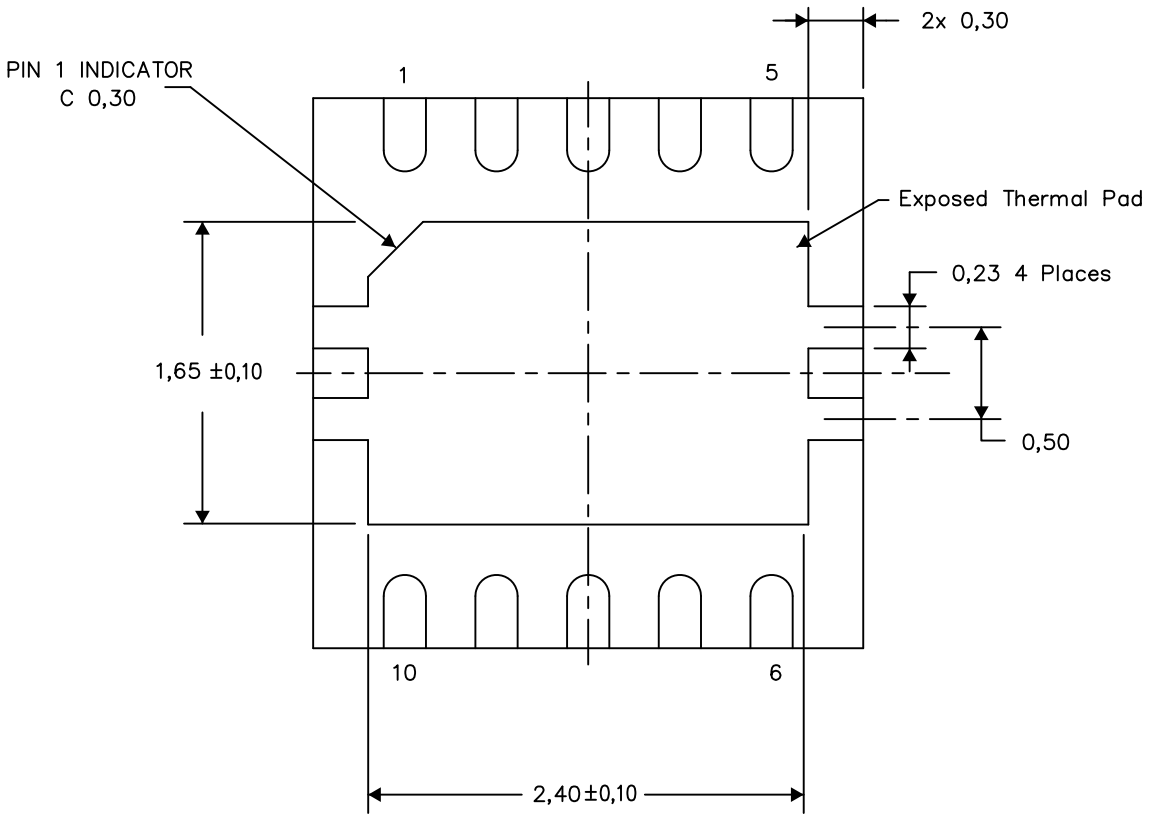
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



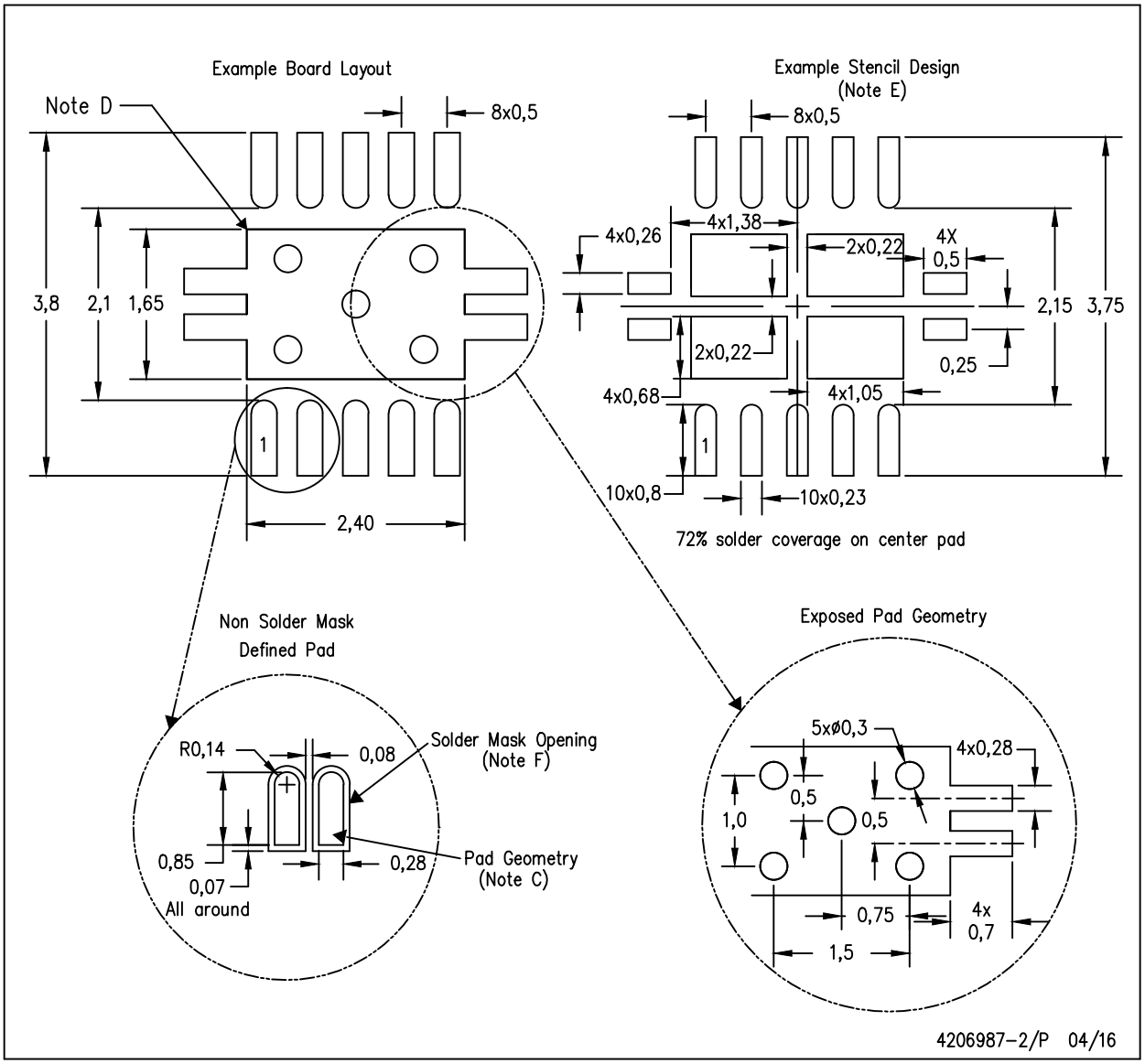
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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