500-mA, HIGH-EFFICIENCY MicroSiP™ STEP-DOWN CONVERTER (PROFILE <1mm)

Check for Samples: TPS82690, TPS82695, TPS82697

FEATURES

- **Total Solution Size <6.7 mm²**
- **95% Efficiency at 4MHz Operation**
- **24µA Quiescent Current**
- **High Duty-Cycle Operation**
- ***Best in Class* Load and Line Transient**
- **±2% Total DC Voltage Accuracy**
- **Automatic PFM/PWM Mode Switching**
- **Low Ripple Light-Load PFM Mode**
- **Excellent AC Load Regulation**
- **Internal Soft Start, 130-µs Start-Up Time**
- **Integrated Active Power-Down Sequencing (Optional)**
- **Current Overload and Thermal Shutdown Protection**
- **Sub 1-mm Profile Solution**

APPLICATIONS

- **LDO Replacement**
- **Cell Phones, Smart-Phones**
- **PoL Applications**

DESCRIPTION

The TPS8269xSIP device is a complete 500mA, DC/DC step-down power supply intended for low-power applications. Included in the package are the switching regulator, inductor and input/output capacitors. No additional components are required to finish the design.

The TPS8269xSIP is based on a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. The MicroSIP™ DC/DC converter operates at a regulated 4-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 24µA (typ) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

The TPS8269xSIP is packaged in a compact (2.3mm x 2.9mm) and low profile (1.0mm) BGA package suitable for automated assembly by standard surface mount equipment.

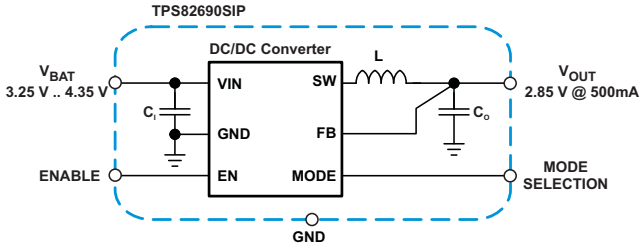

Figure 1. Typical Application

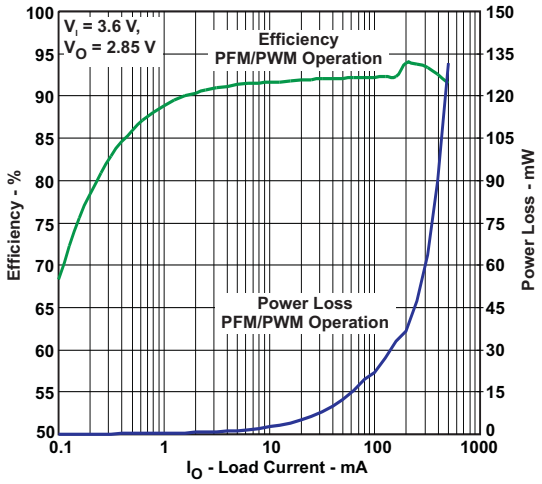

Figure 2. Efficiency vs. Load Current

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	DEVICE SPECIFIC FEATURE	ORDERING(3)	PACKAGE MARKING
-40°C to 85°C	TPS82695	2.5V		TPS82695SIP	UF
	TPS82690(4)	2.85V		TPS82690SIP	RC
	TPS82696(4)	2.9V		TPS82696SIP	
	TPS82697(4)	2.8V		TPS82697SIP	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Internal tap points are available to facilitate output voltages in 25mV increments.
(3) The SIP package is available in tape and reel. Add a R suffix (e.g. TPS82690SIPR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS82690SIPT) to order quantities of 250 parts.
(4) Product preview. Contact TI factory for more information

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_I	Voltage at VIN(2)(3)	–0.3 V to 6 V
	Voltage at VOUT(3)	–0.3 V to 3.6 V
	Voltage at EN, MODE (3)	–0.3 V to V_I + 0.3 V
I_O	Peak output current	500 mA
	Power dissipation	Internally limited
T_A	Operating temperature range(4)	–40°C to 85°C
T_{INT} (max)	Maximum internal operating temperature	125°C
T_{stg}	Storage temperature range	–55°C to 125°C
ESD rating (5)	Human body model	2 kV
	Charge device model	1 kV
	Machine model	200 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.35V input voltage for extended periods may affect device reliability. See *input capacitor selection* section for more details.
(3) All voltage values are with respect to network ground terminal.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating temperature ($T_{INT(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum internal temperature of 105°C.
(5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS82690/95/97 SIP (8-Pins)	UNITS
θ_{JA}	Junction-to-ambient (top) thermal resistance	125	°C/W
	Junction-to-ambient (bottom) thermal resistance	70	
θ_{JCtop}	Junction-to-case (top) thermal resistance	–	
θ_{JB}	Junction-to-board thermal resistance	–	
ψ_{JT}	Junction-to-top characterization parameter	–	
ψ_{JB}	Junction-to-board characterization parameter	–	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	–	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.3		4.35[1]	V
I_O	Output current range	0		500	mA
	Additional output capacitance (PFM/PWM operation)[2]		0	5	µF
	Additional output capacitance (PWM operation)[2]		0	8	µF
T_A	Ambient temperature	–40		+85	°C
T_J	Operating junction temperature	–40		+125	°C

(1) Operation above 4.35V input voltage for extended periods may affect device reliability. See *input capacitor selection* section for more details.
(2) In certain applications larger capacitor values can be tolerable, see *output capacitor selection* section for more details.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_I = 2.3V to 4.35V, V_O = 2.5V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 2.5V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

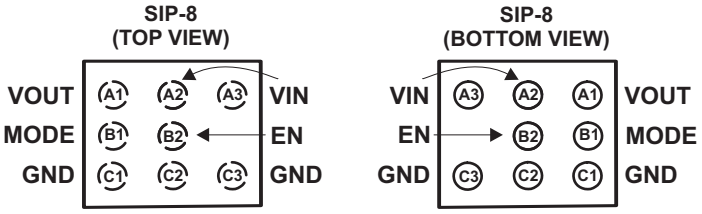
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS82690	I_O = 0mA. Device not switching		24	50	µA
			I_O = 0mA, PWM mode		4.5		mA
I_{SD}	Shutdown current	TPS8269X	EN = GND		0.5	5	µA
UVLO	Undervoltage lockout threshold	TPS82690 TPS82695 TPS82697			2.05	2.1	V
		TPS82696			2.1	2.15	V
PROTECTION							
	Thermal shutdown	TPS8269X			140		°C
	Thermal shutdown hysteresis				10		°C
I_{LIM}	Peak input current limit	TPS8269X			750		mA
I_{SC}	Input current limit under short-circuit conditions	TPS8269X	V_O shorted to ground		15		mA
ENABLE, MODE							
V_{IH}	High-level input voltage	TPS8269X		1.0			V
V_{IL}	Low-level input voltage					0.4	V
	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS8269X	I_O = 0mA. PWM operation. T_A = 25°C	3.6	4	4.4	MHz

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_I = 2.3V to 4.35V, V_O = 2.5V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 2.5V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
$V_{(OUT)}$	Regulated DC output voltage	TPS82690 TPS82697	3.25V ≤ V_I ≤ 4.35V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.25V ≤ V_I ≤ 4.35V, 0mA ≤ I_O ≤ 500 mA Additional output capacitor, C_O= 4.7µF 6.3V 0402 (muRata GRM155R60J475M) PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.25V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.05×V_{NOM}	V
			3.25V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS82695	3.0V ≤ V_I ≤ 4.35V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.0V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.97×V_{NOM}	V_{NOM}	1.05×V_{NOM}	V
			3.0V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS82696	3.25V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.97×V_{NOM}	V_{NOM}	1.05×V_{NOM}	V
			3.25V ≤ V_I ≤ 4.35V, 0mA ≤ I_O ≤ 500 mA Additional output capacitor, C_O= 4.7µF 6.3V 0402 (muRata GRM155R60J475M) PFM/PWM operation	0.97×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.25V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.97×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
	Line regulation	TPS8269X	V_I = V_O + 0.5V (min 3.25V) to 5.5V, I_O = 200 mA		0.18		%/V
	Load regulation		I_O = 0mA to 500 mA. PWM operation		–0.0002		%/mA
	Feedback input resistance	TPS8269X			480		kΩ
rDS(on)	Input-to-output On-resistance	TPS8269X	V_I = 3.25 V. Device not switching		390		mΩ
ΔV_O	Power-save mode ripple voltage	TPS8269X	I_O = 1mA		70		mV_{PP}
			I_O = 1mA Additional output capacitor, C_O= 4.7µF 6.3V 0402 (muRata GRM155R60J475M)		35		mV_{PP}
	Start-up time	TPS82690 TPS82696 TPS82697	I_O = 0mA, Time from active EN to V_O		130		µs
			Time from active EN to full load current operation permitted		350		µs
r_{DIS}	Discharge resistor for power-down sequence	TPS8269X			100	150	Ω

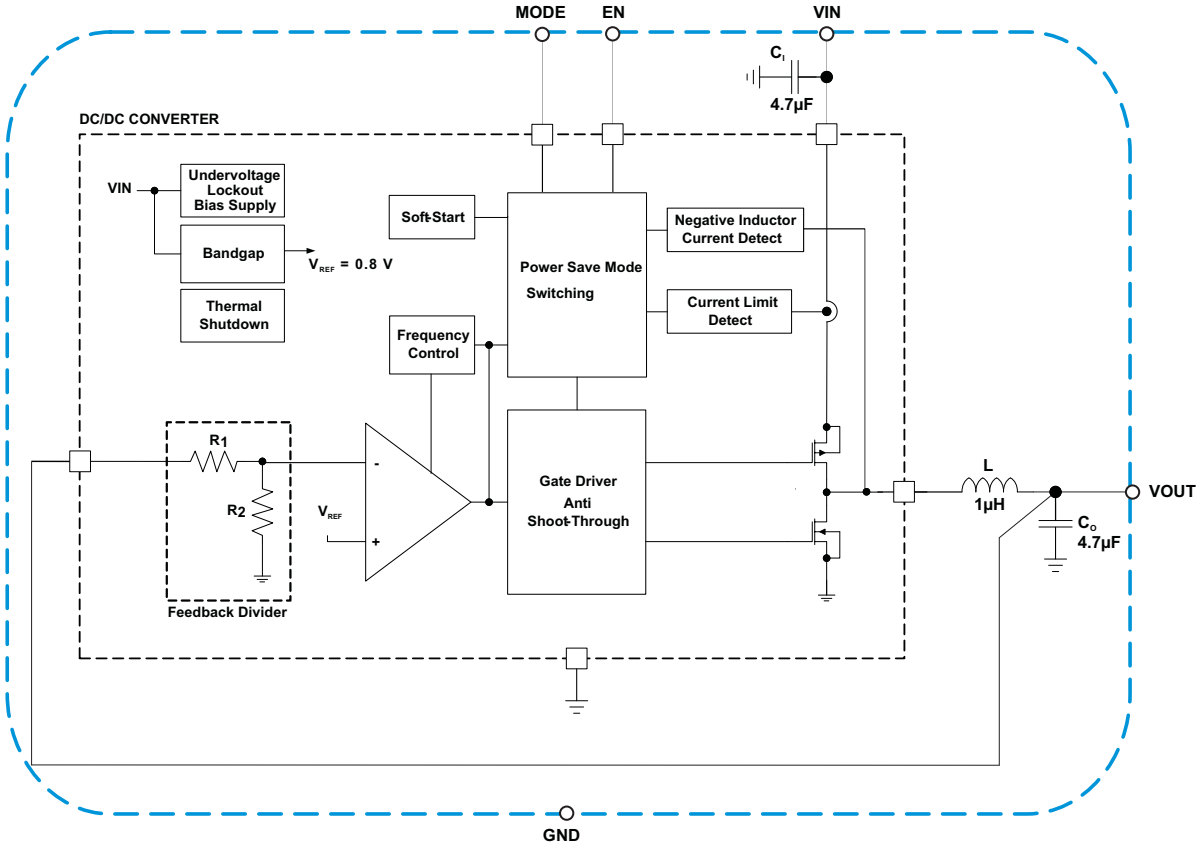
PIN ASSIGNMENTS



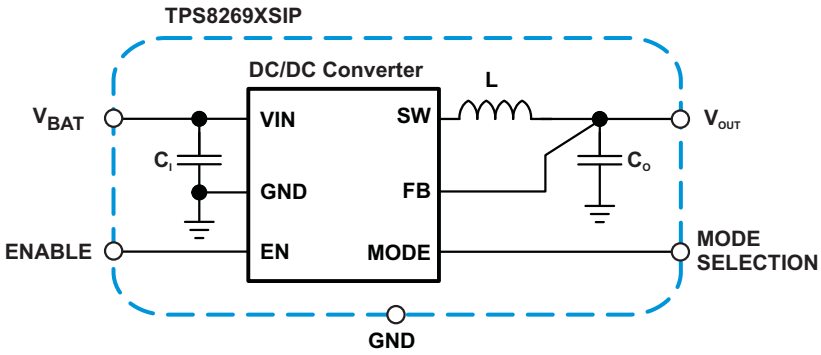
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Power output pin. Apply output load between this pin and GND.
VIN	A2, A3	I	The VIN pins supply current to the TPS8269xSIP's internal regulator.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the converter into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
MODE	B1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated. MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C1, C2, C3	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4
		vs Load current	5, 6
		vs Input voltage	7
	Peak-to-peak output ripple voltage	vs Load current	8, 9
V_O	DC output voltage	vs Load current	10, 11, 120
	Combined line/load transient response		13, 14
	Load transient response		15, 16, 17, 18
	AC load transient response		19, 20, 21, 22, 23, 24, 25
	PFM/PWM boundaries	vs Input voltage	26
I_Q	Quiescent current	vs Input voltage	27
f_s	PWM switching frequency	vs Input voltage	28
	PFM switching frequency	vs Load current	29
	Start-up		30, 31
PSRR	Power supply rejection ratio	vs. Frequency	32

TYPICAL CHARACTERISTICS (continued)

TPS82695
EFFICIENCY
vs
LOAD CURRENT

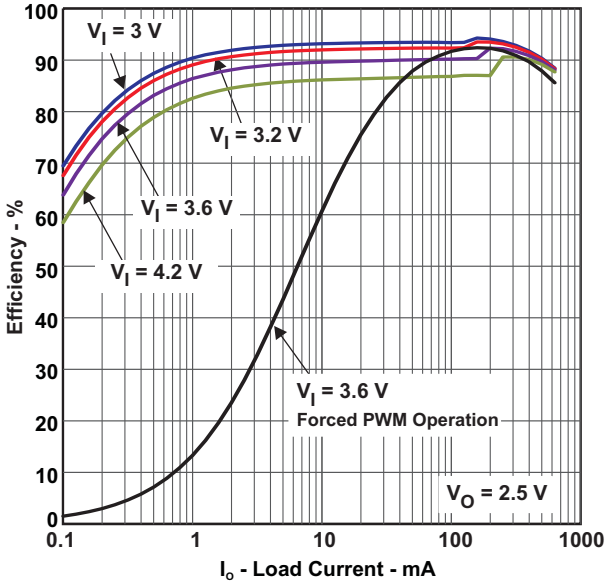


Figure 3.

TPS82695
EFFICIENCY
vs
LOAD CURRENT

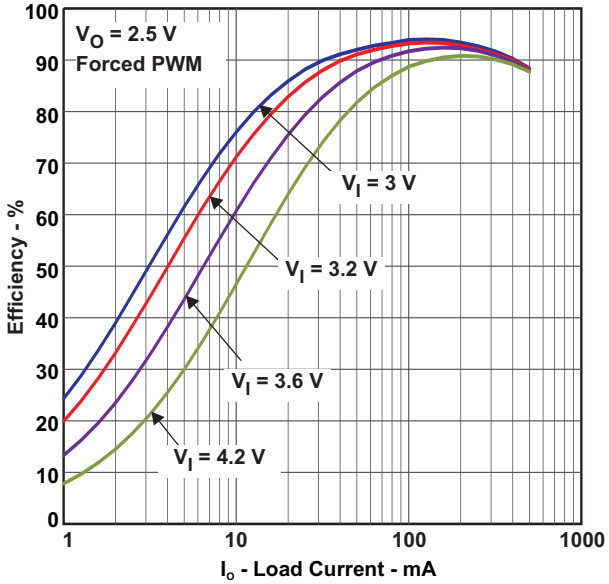


Figure 4.

EFFICIENCY
vs
LOAD CURRENT

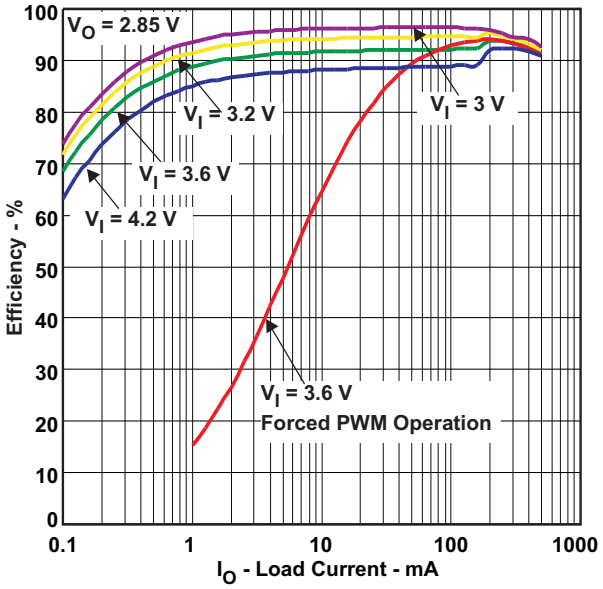


Figure 5.

EFFICIENCY
vs
LOAD CURRENT

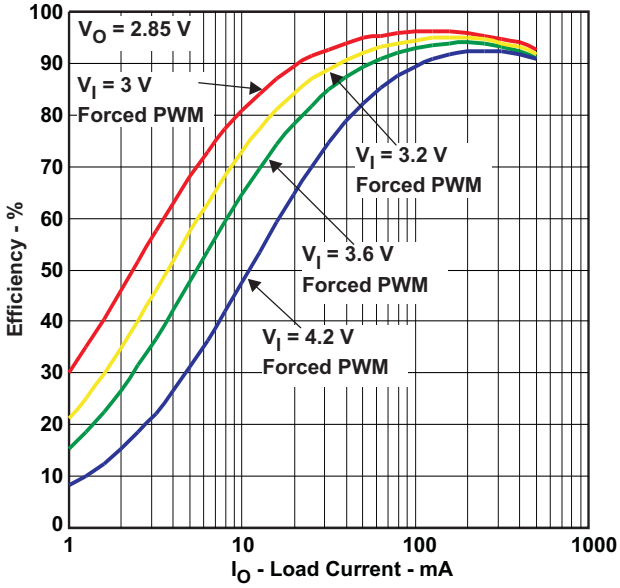


Figure 6.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs INPUT VOLTAGE

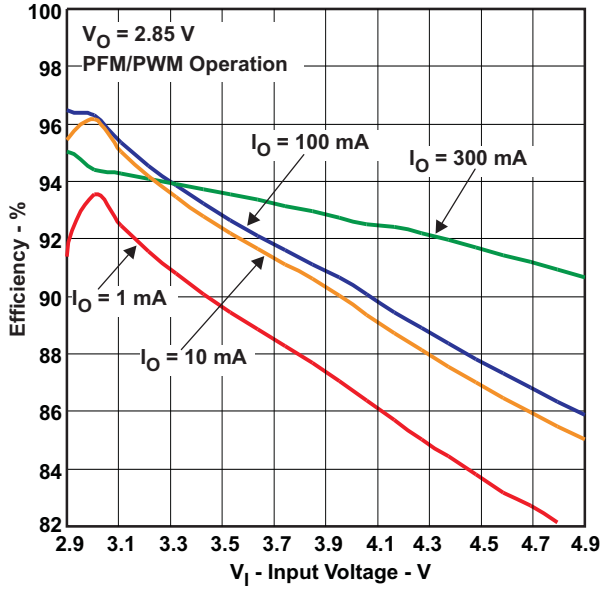


Figure 7.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

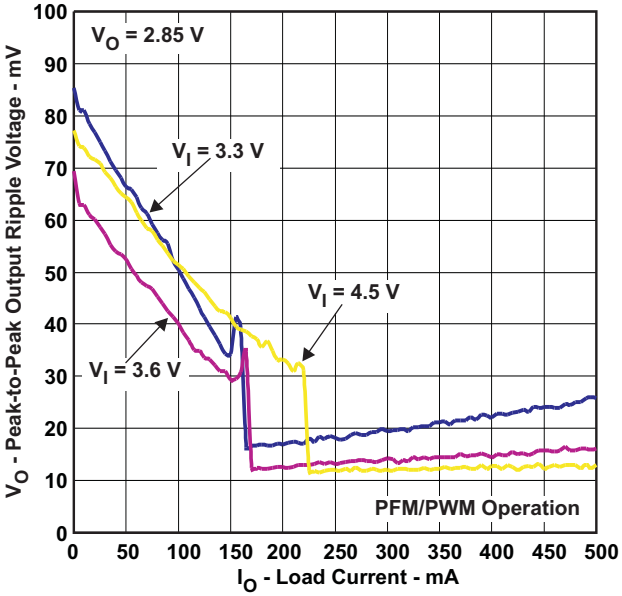


Figure 8.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

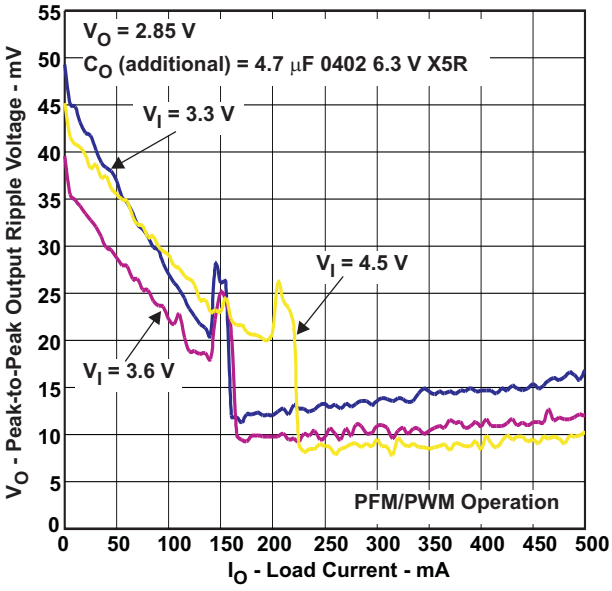


Figure 9.

DC OUTPUT VOLTAGE vs LOAD CURRENT

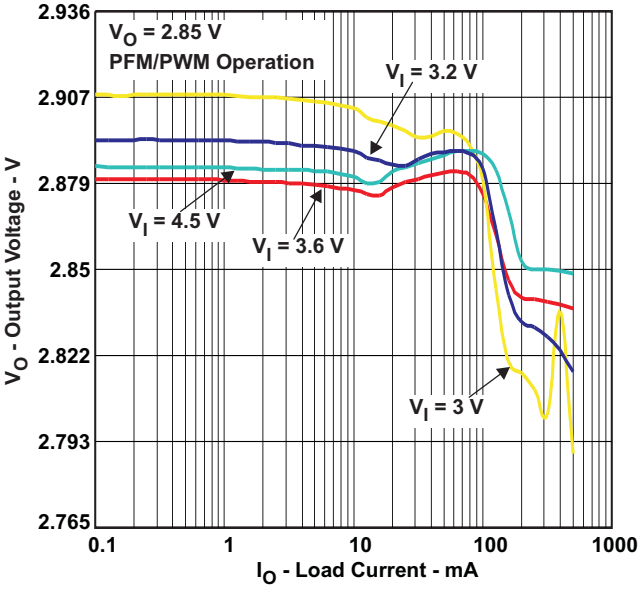


Figure 10.

TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE vs LOAD CURRENT

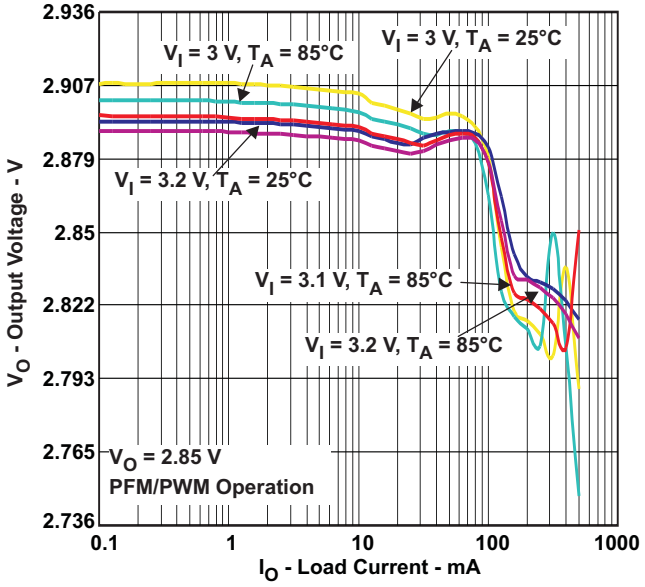


Figure 11.

DC OUTPUT VOLTAGE vs LOAD CURRENT

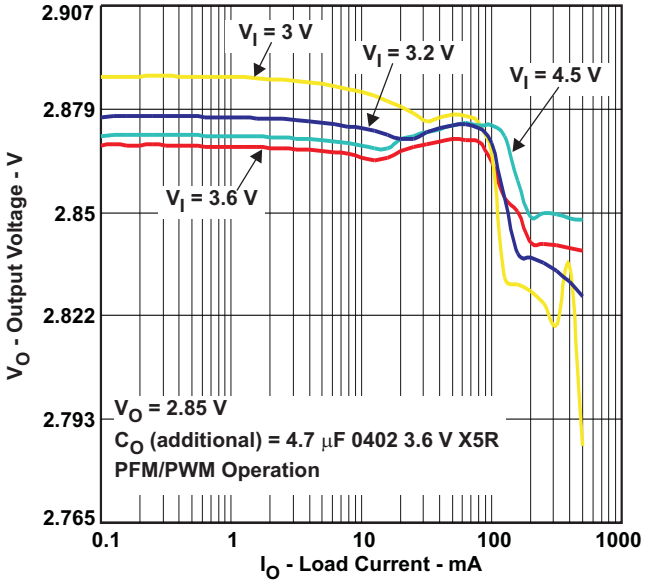


Figure 12.

COMBINED LINE/LOAD TRANSIENT RESPONSE

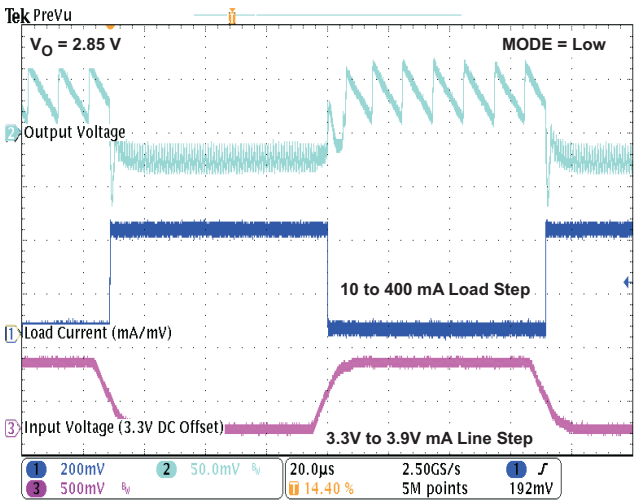


Figure 13.

COMBINED LINE/LOAD TRANSIENT RESPONSE

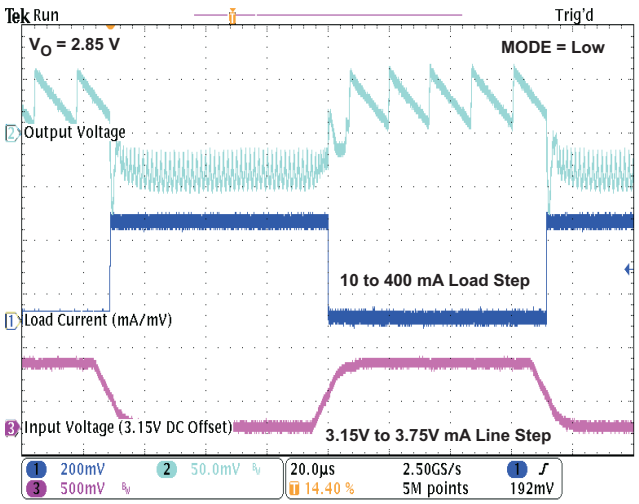


Figure 14.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

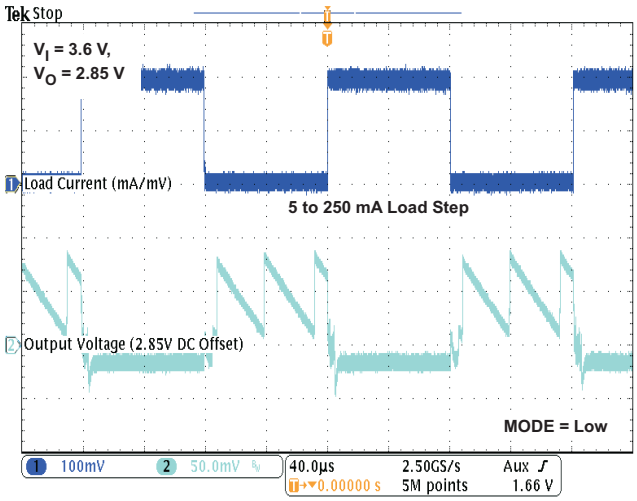


Figure 15.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

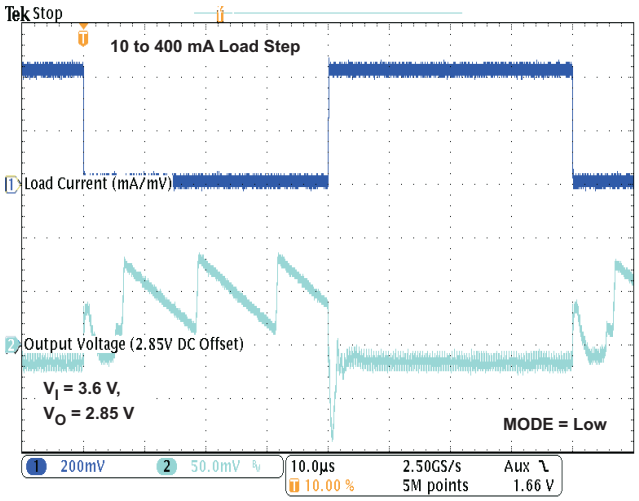


Figure 16.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

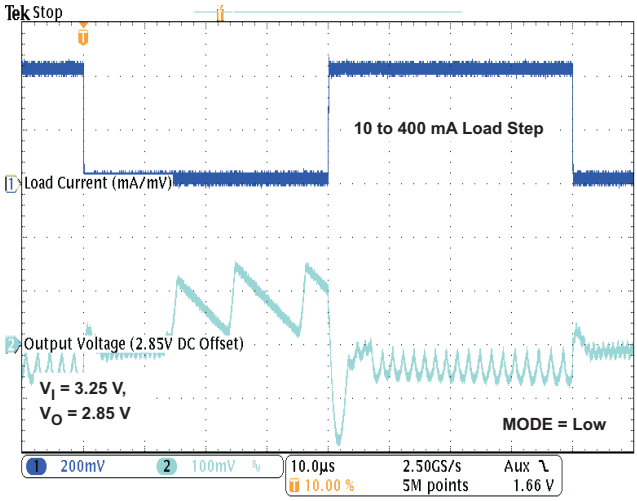


Figure 17.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

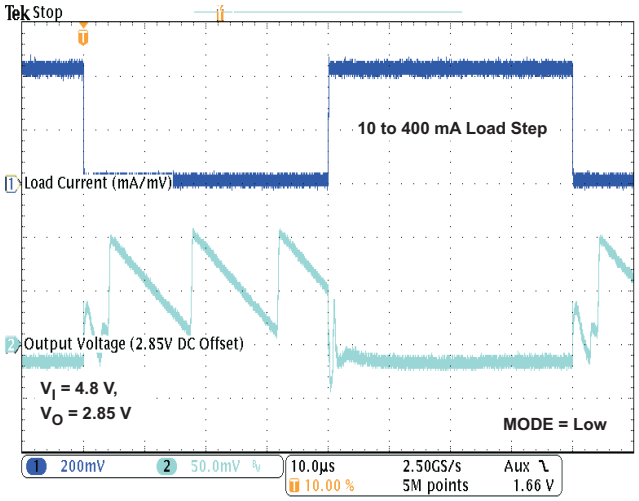


Figure 18.

TYPICAL CHARACTERISTICS (continued)

AC LOAD TRANSIENT RESPONSE

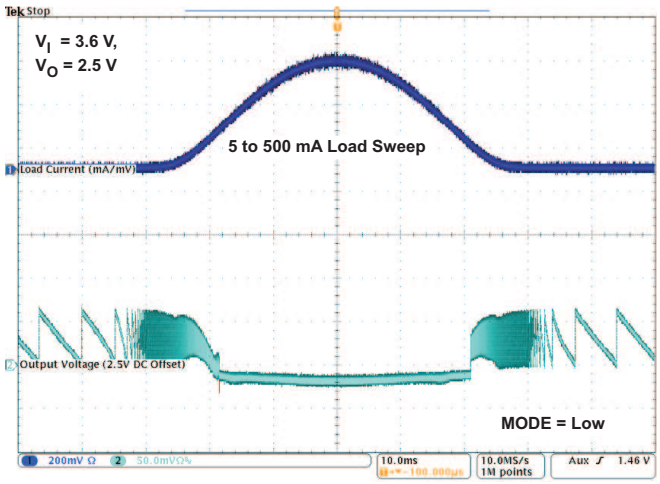


Figure 19.

AC LOAD TRANSIENT RESPONSE

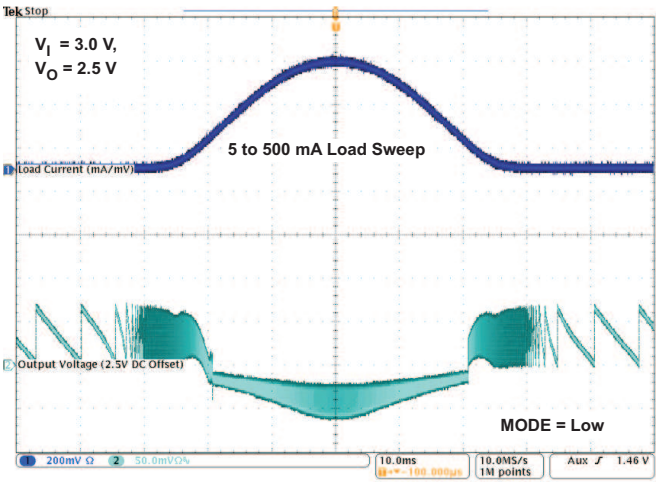


Figure 20.

AC LOAD TRANSIENT RESPONSE

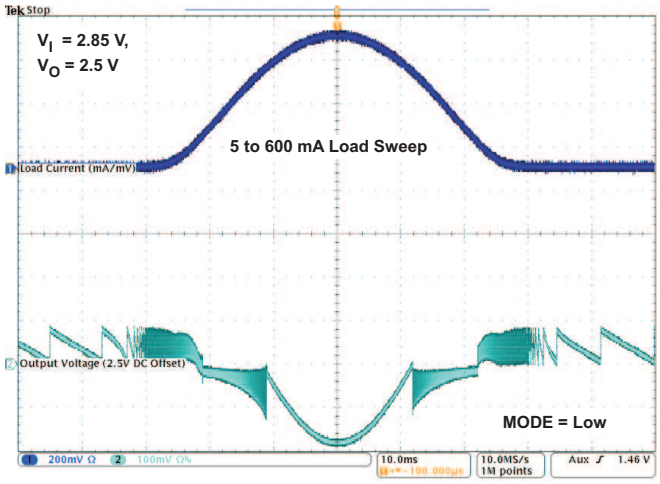


Figure 21.

AC LOAD TRANSIENT RESPONSE

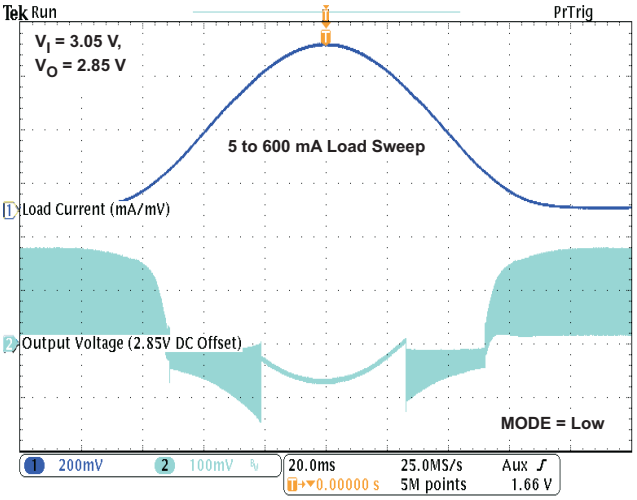


Figure 22.

TYPICAL CHARACTERISTICS (continued)

AC LOAD TRANSIENT RESPONSE

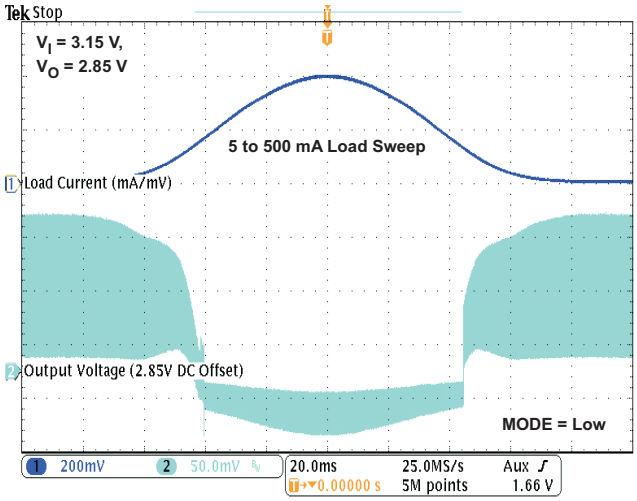


Figure 23.

AC LOAD TRANSIENT RESPONSE

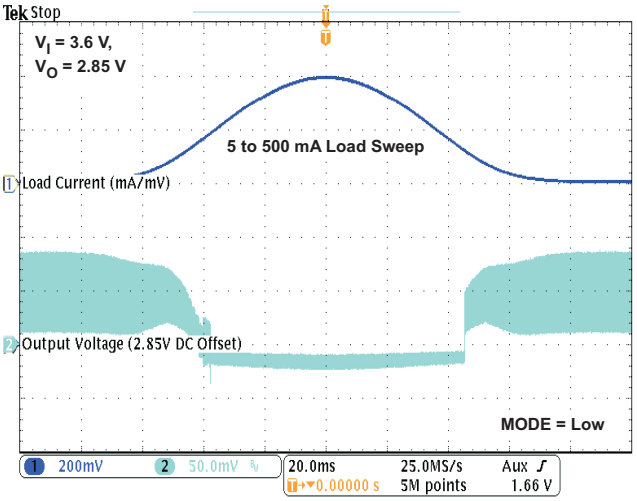


Figure 24.

AC LOAD TRANSIENT RESPONSE

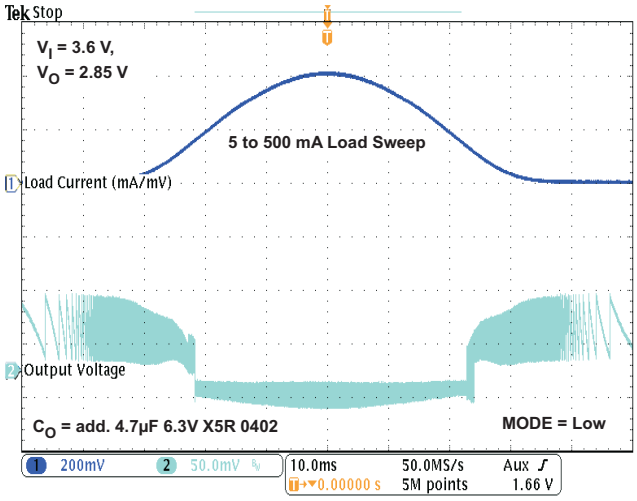


Figure 25.

PFM/PWM BOUNDARIES

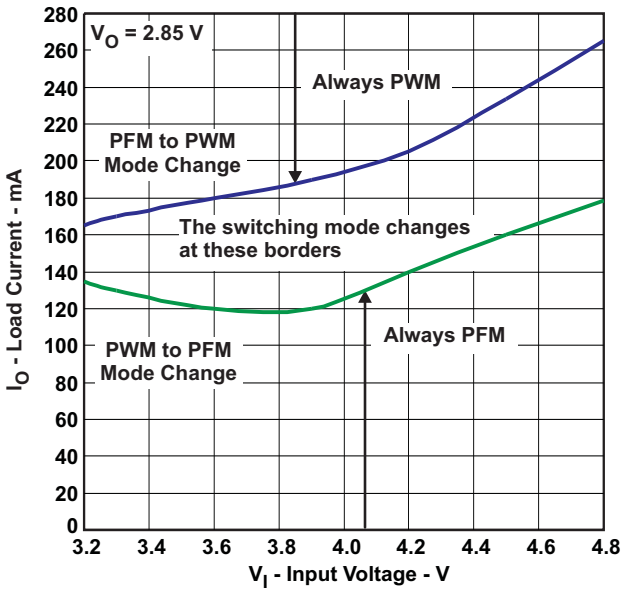


Figure 26.

TYPICAL CHARACTERISTICS (continued)

QUIESCENT CURRENT vs INPUT VOLTAGE

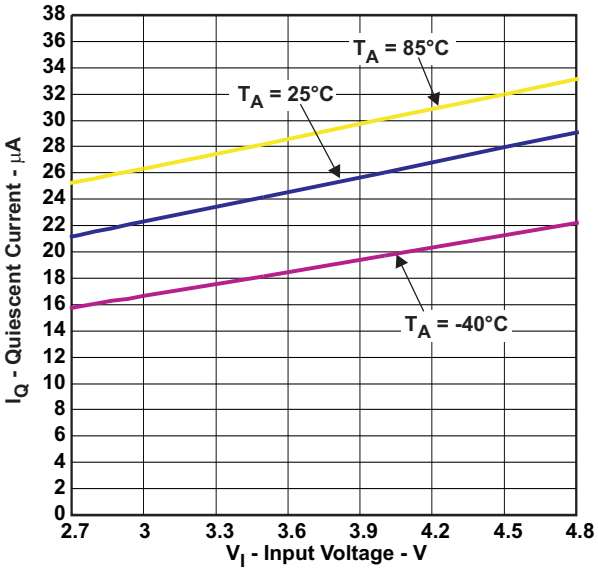


Figure 27.

PWM SWITCHING FREQUENCY vs INPUT VOLTAGE

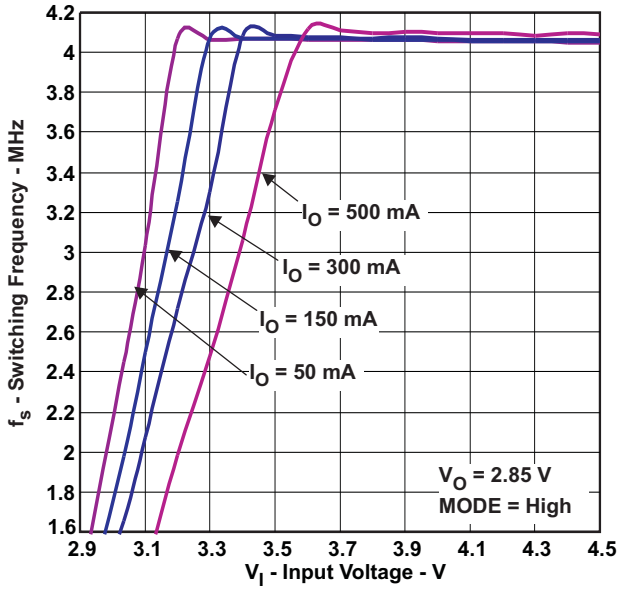


Figure 28.

PFM SWITCHING FREQUENCY vs LOAD CURRENT

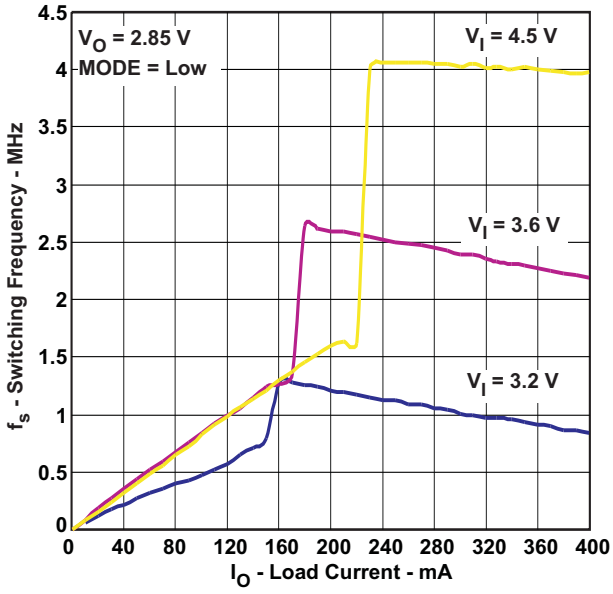


Figure 29.

START-UP

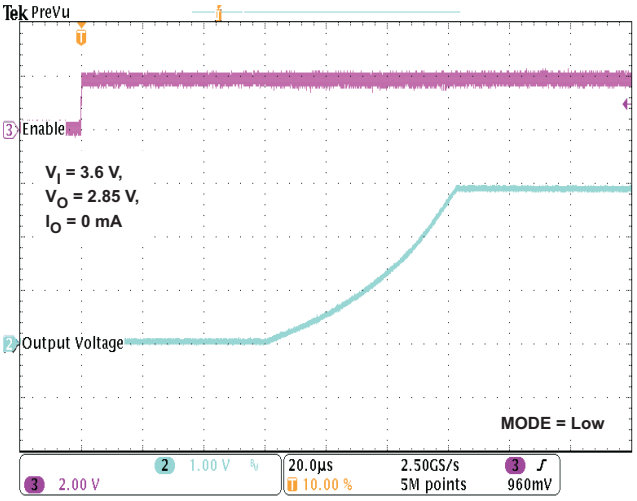


Figure 30.

TYPICAL CHARACTERISTICS (continued)

START-UP

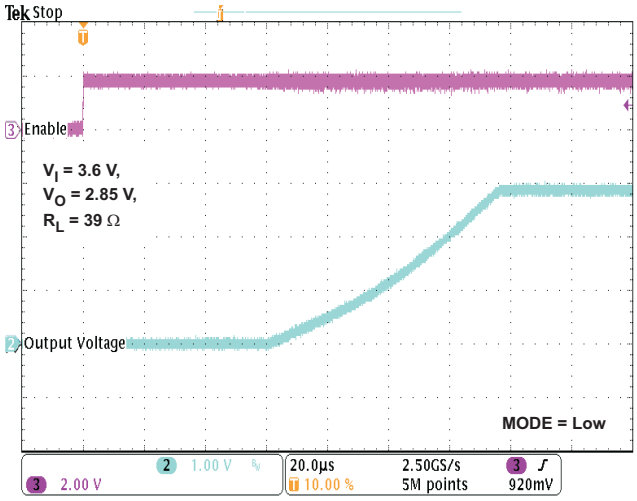


Figure 31.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

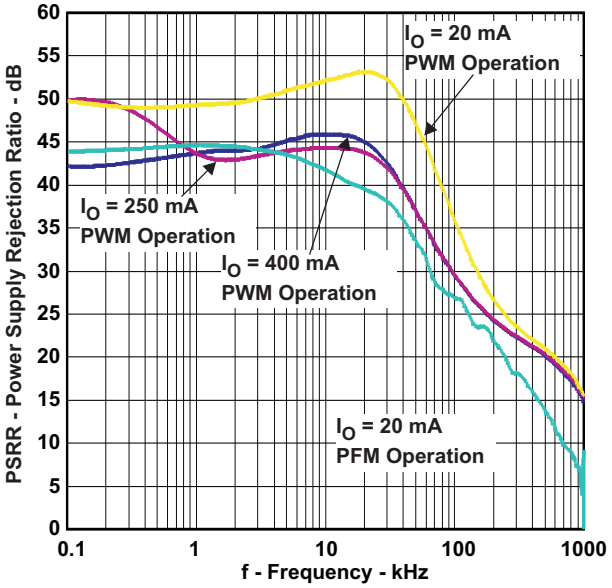


Figure 32.

DETAILED DESCRIPTION

OPERATION

The TPS8269xSIP is a standalone synchronous step-down converter operating at a regulated 4-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents (up to 500mA output current). At light load currents, the TPS8269xSIP's converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response. One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 24µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

The TPS8269xSIP integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages.

POWER-SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically. During power-save mode the converter operates in discontinuous current (DCM) with a minimum of one pulse, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the output voltage is within its regulation limits again.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 1.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

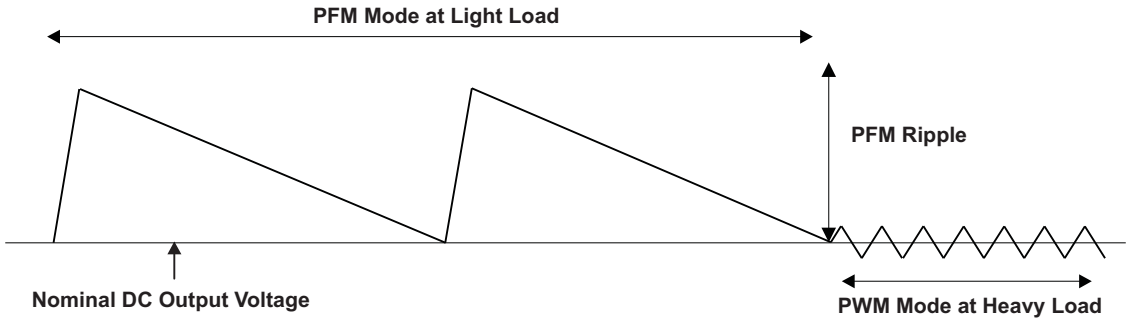


Figure 33. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

LOW DROPOUT, 100% DUTY CYCLE OPERATION

The device starts to enter 100% duty cycle mode once input and output voltage come close together. In order to maintain the output voltage, the DC/DC converter's high-side MOSFET is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side switch is constantly turned on, thereby providing a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

SOFT START

The TPS8269xSIP has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the MicroSiP™ converter.

The soft-start system progressively increases the switching on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for c.a. 100µs after enable. Should the output voltage not have reached its target value by that time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

If the output voltage has raised above 0.5V (approximately), the converter increases the input current limit thereby enabling the power supply to come-up properly. The start-up time mainly depends on the capacitance present at the output node and load current.

ENABLE

The TPS8269xSIP device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown. In this mode, all internal circuits are turned off and V_{IN} current reduces to the device leakage current, typically a few hundred nanoamps.

The TPS8269xSIP device can actively discharge the output capacitor when it turns off (refer to Ordering Information Table). The integrated discharge resistor has a typical resistance of 100 Ω. The required time to ramp-down the output voltage depends on the load current and the capacitance present at the output node.

APPLICATION INFORMATION

INPUT CAPACITOR SELECTION

Because of the pulsating input current nature of the buck converter, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.

For most applications, the input capacitor that is integrated into the TPS8269x should be sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

The TPS8269x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

OUTPUT CAPACITOR SELECTION

The advanced, fast-response, voltage mode, control scheme of the TPS8269x allows the use of a tiny ceramic output capacitor (C_O). For most applications, the output capacitor integrated in the TPS8269x is sufficient.

At nominal load current, the device operates in PWM mode; the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor ESL and the ripple current that flows through the output capacitor impedance. At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions.

The TPS8269x is designed as a Point-Of-Load (POL) regulator, to operate stand-alone without requiring any additional capacitance. Adding a 4.7µF ceramic output capacitor (X7R or X5R dielectric) generally works from a converter stability point of view, helps to minimize the output ripple voltage in PFM mode and improves the converter's transient response under when input and output voltage are close together.

For best operation (i.e. optimum efficiency over the entire load current range, proper PFM/PWM auto transition), the TPS8269xSIP requires a minimum output ripple voltage in PFM mode. The typical output voltage ripple is ca. 1% of the nominal output voltage V_O. The PFM pulses are time controlled resulting in a PFM output voltage ripple and PFM frequency that depends (first order) on the capacitance seen at the MicroSiP™ DC/DC converter's output.

In applications requiring additional output bypass capacitors located close to the load, care should be taken to ensure proper operation. If the converter exhibits marginal stability or erratic switching frequency, experiment with additional low value series resistance (e.g. 50 to 100mΩ) in the output path to find a remedy.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PWB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter small and large signal behavior must be checked over the input voltage range, load current range and temperature range.

The easiest sanity test is to evaluate, directly at the converter’s output, the following aspects:

- PFM/PWM efficiency
- PFM/PWM and forced PWM load transient response

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin.

LAYOUT CONSIDERATION

In making the pad size for the SiP LGA balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 34 shows the appropriate diameters for a MicroSiP™ layout.

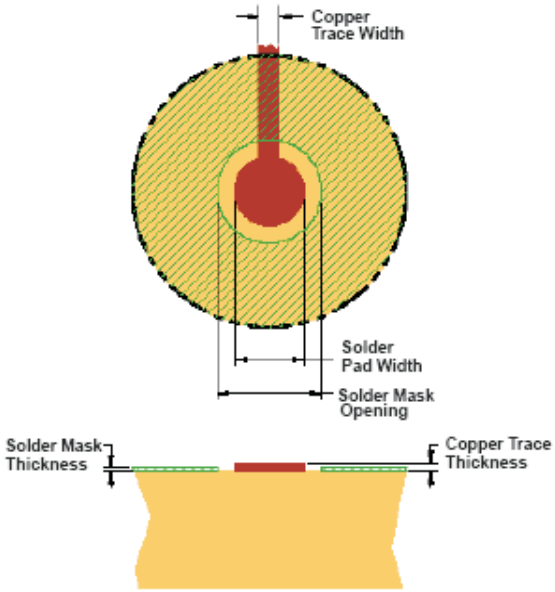


Figure 34. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS(1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

SURFACE MOUNT INFORMATION

The TPS8269x MicroSiP™ DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum thereby to allow the MicroSiP™ device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

THERMAL INFORMATION

The die temperature of the TPS8269x must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the TPS8269x.

To estimate the junction temperature, approximate the power dissipation within the TPS8269x by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking a power measurement if you have an actual TPS8269x device and TPS8269xEVM evaluation module. Then calculate the internal temperature rise of the TPS8269x above the surface of the printed circuit board by multiplying the TPS8269x power dissipation by the thermal resistance.

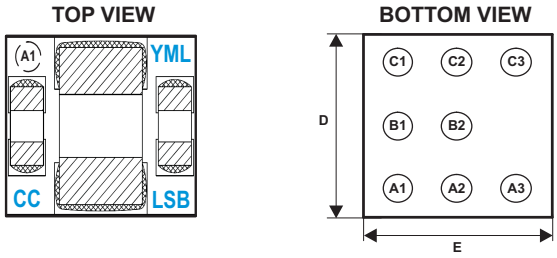
The actual thermal resistance of the TPS8269x to the printed circuit board depends on the layout of the circuit board, but the thermal resistance given in the Thermal Information Table can be used as a guide.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

PACKAGE SUMMARY

SIP PACKAGE



Code:

- CC — Customer Code (device/voltage specific)
- YML — Y: Year, M: Month, L: Lot trace code
- LSB — L: Lot trace code, S: Site code, B: Board locator

MicroSiP™ DC/DC MODULE PACKAGE DIMENSIONS

The TPS8269x device is available in an 8-bump ball grid array (BGA) package. The package dimensions are:

- D = 2.30 ±0.05 mm
- E = 2.90 ±0.05 mm

Note: Page numbers of current version may differ from previous versions.

Changes from Original (June 2011) to Revision A **Page**

- Deleted Product Preview status from TPS82695 device in Ordering Information table. 2

Changes from Revision A (October 2011) to Revision B **Page**

- Added device number TPS82697 1
- Added Efficiency vs Load Current Graphs. Figure 3 and Figure 4 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82690SIPR	PREVIEW	uSiP	SIP	8		TBD	Call TI	Call TI	-40 to 85	RC TXI690	
TPS82690SIPT	PREVIEW	uSiP	SIP	8		TBD	Call TI	Call TI	-40 to 85		
TPS82695SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	UF TXI695	Samples
TPS82695SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	UF TXI695	Samples
TPS826970SIPR	PREVIEW	uSiP	SIP	8	3000	TBD	Call TI	Call TI	-40 to 85		
TPS826970SIPT	PREVIEW	uSiP	SIP	8	250	TBD	Call TI	Call TI	-40 to 85		
TPS82697SIPR	ACTIVE	uSiP	SIP	8	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	C2 TXI697	Samples
TPS82697SIPT	ACTIVE	uSiP	SIP	8	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 85	C2 TXI697	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

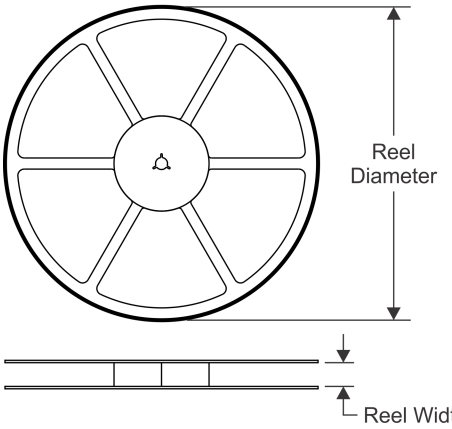
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

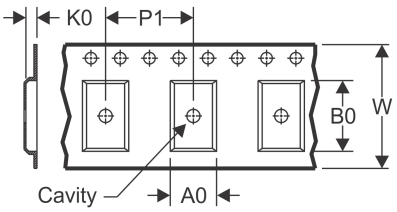
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

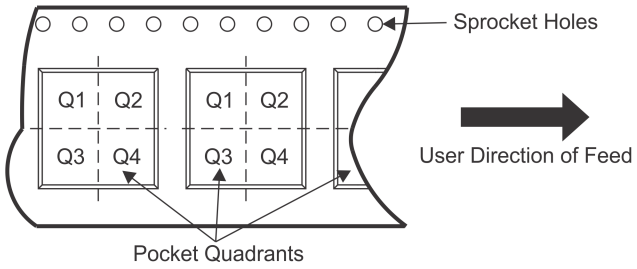


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

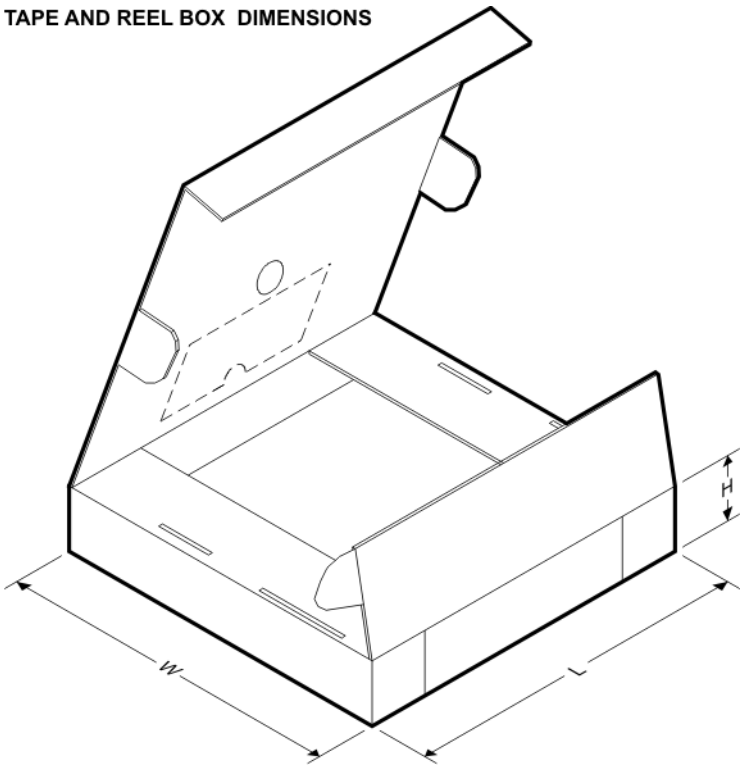
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82695SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82697SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

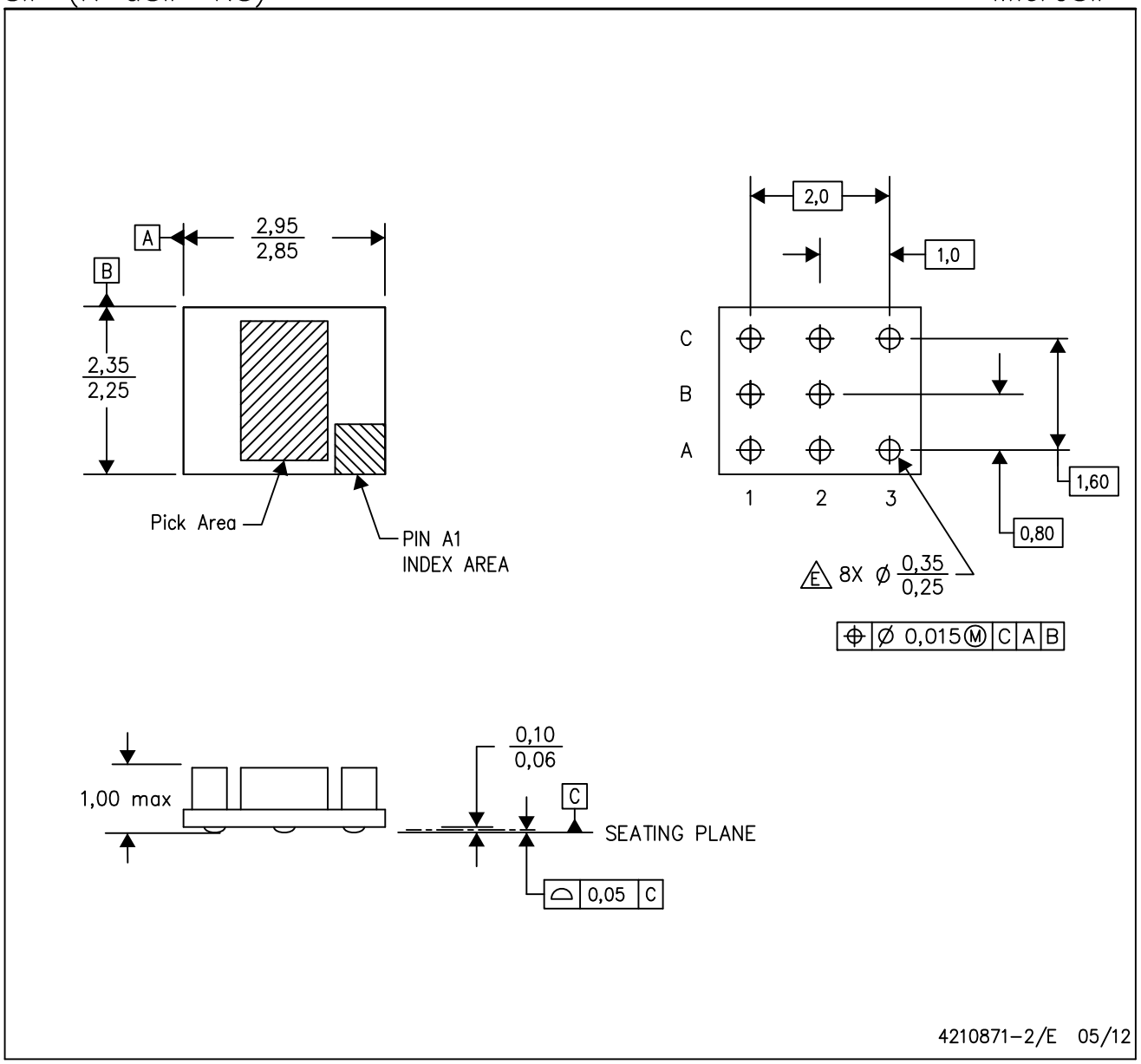
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82695SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82697SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0

SIP (R–uSiP–N8) MicroSiP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicroSiP™ package configuration – Micro System in Package.
D. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
E. This package contains Pb–free balls.

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