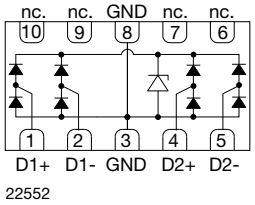
4-Line BUS-Port ESD Protection - Flow Through Design



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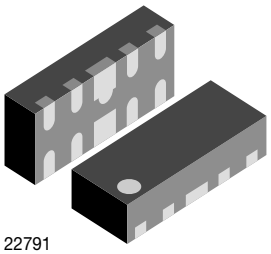
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FEATURES

- Compact LLP2510-10M package
- Low package height < 0.6 mm
- 4-line ESD-protection
- Low leakage current I_R < 0.1 µA
- Low capacitance between I/O lines: 0.3 pF
- Ideal for high speed data line like
  - HDMI, DisplayPort, eSATA
  - USB, 1394/firewire
  - Thunderbolt
- ESD-protection acc. IEC 61000-4-2
  ± 15 kV contact discharge
  ± 15 kV air discharge
- Soldering can be checked by standard vision inspection. No X-ray necessary
- e3 - Sn
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e3

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

MARKING (example only)

20720

Dot = pin 1 marking
YY = type code (see table below)
XX = date code

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS54GD-FBL	VBUS54GD-FBL-G3-08	3000	30 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS54GD-FBL	LLP2510-10M	4G	3.9 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VBUS54GD-FBL

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	I_{PPM}	3	A
Peak pulse power	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	P_{PP}	45	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 15	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 15	
Operating temperature	Junction temperature	T_J	-40 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

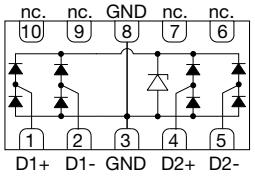
ELECTRICAL CHARACTERISTICS VBUS54GD-FBL (pin 1, 2, 4 or 5 to pin 3) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	4	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V
Reverse voltage	at I_R = 0.1 µA	V_R	5.5	-	-	V
Reverse current	at V_{RWM} = 5.5 V	I_R	-	0.02	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6.9	7.5	8.7	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C	-	9.1	11	V
	at I_{PP} = I_{PPM} = 3 A	V_C	-	12	15	V
Forward clamping voltage	at I_{PP} = 1 A	V_F	-	2.1	2.4	V
	at I_{PP} = 3 A	V_F	-	3.5	4.5	V
Clamping voltage	Transmission line pulse (TLP), t_p = 100 ns I_{TLP} = 8 A	V_{C-TLP}	-	15	-	V
	Transmission line pulse (TLP), t_p = 100 ns I_{TLP} = 16 A	V_{C-TLP}	-	21	-	V
Dynamic resistance	Transmission line pulse (TLP), t_p = 100 ns	R_{DYN}	-	0.76	-	Ω
Capacitance	at V_R = 0 V; f = 1 MHz	C_D	-	0.6	0.75	pF
	at V_R = 3.3 V; f = 1 MHz		-	0.65	0.75	pF
Capacitance between I/O lines	at V_R = 3.3 V; f = 1 MHz	C_{DD}	-	0.3	0.4	pF

APPLICATION NOTE

The **VBUS54GD-FBL** is a four-line ESD-protection device with the characteristic of a Z-diode with a high ESD-immunity and a very low capacitance which makes it usable for high frequency applications like USB2.0, USB3.0 or HDMI.
With the **VBUS54GD-FBL** four high speed data lines can be protected against transient voltage signals like ESD (Electro Static Discharge). Connected to the data line (pin 1, 2 and pin 4, 5) and to ground (pin 3 and 8) negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5.5 V working range. The clamping behaviour of the **VBUS54GD-FBL** is bidirectional but asymmetrical (**BiAs**) and so it offers the best protection for applications running up to 5.5 V.

Pin configuration:

- Pin 3 and 8 are internally shorted and have to be connected to ground
- Pin 1, 2 and 4, 5 are the inputs for the data lines D_{1+} and D_{1-} and D_{2+} and D_{2-}
- Pin 6, 7 and 9, 10 are not connected internally



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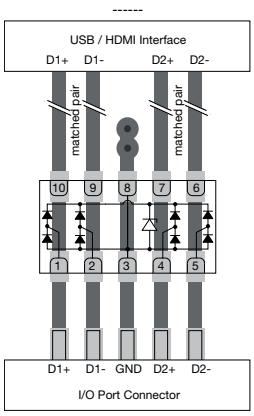

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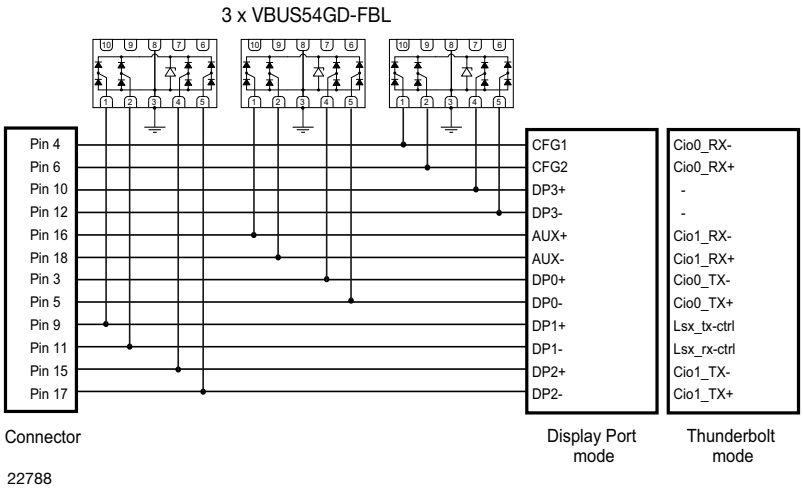
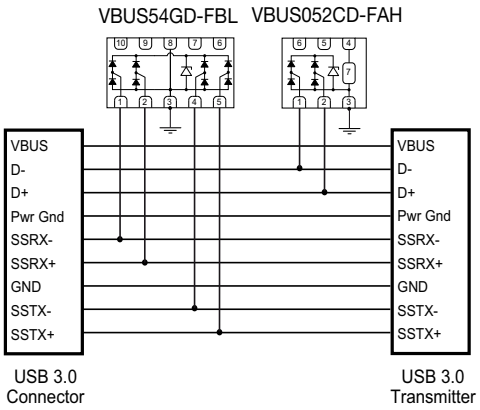
FLOW THROUGH DESIGN

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB2.0) or 1.65 Gbit/s (HDMI).
At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. 50 Ω) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD-protection devices - have to be connected with minimal changes in these trace dimensions and distances.
With the package in the so called “Flow Through Design” this is possible. The lines are running straight along the PCB while the **VBUS54GD-FBL** is placed on top without any via or loops.

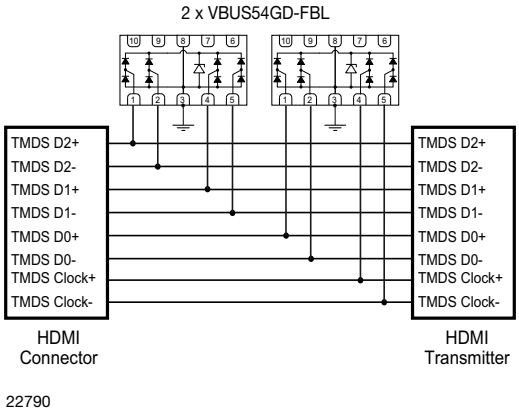
CONNECTION DIAGRAM EXAMPLE FOR THUNDERBOLT DATA PORT



CONNECTION DIAGRAM EXAMPLE FOR USB 3.0 DATA PORT



CONNECTION DIAGRAM EXAMPLE FOR HDMI DATA PORT



TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

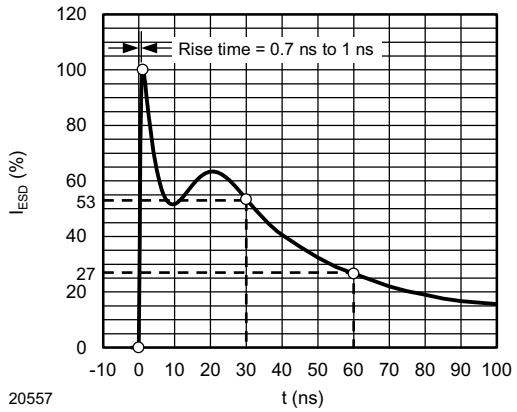


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

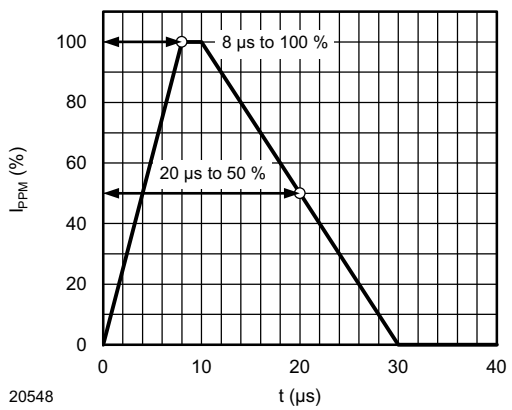


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

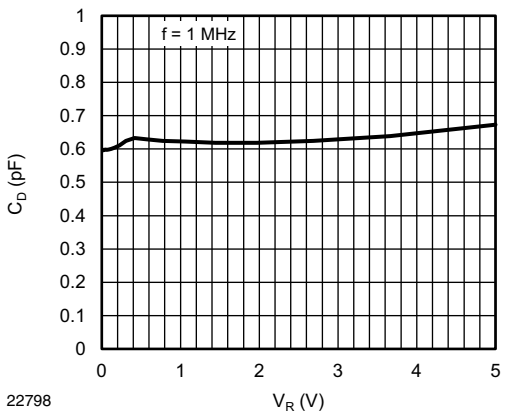


Fig. 3 - Typical Capacitance vs. Reverse Voltage

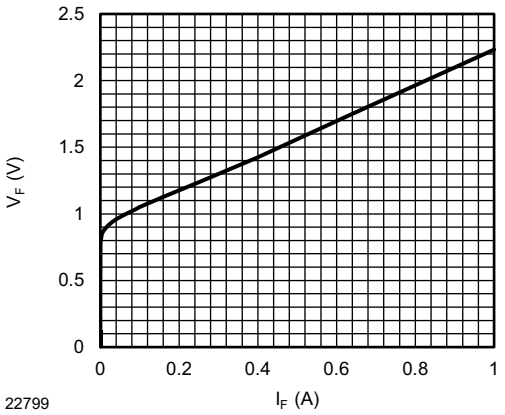


Fig. 4 - Typical Forward Voltage vs. Forward Current

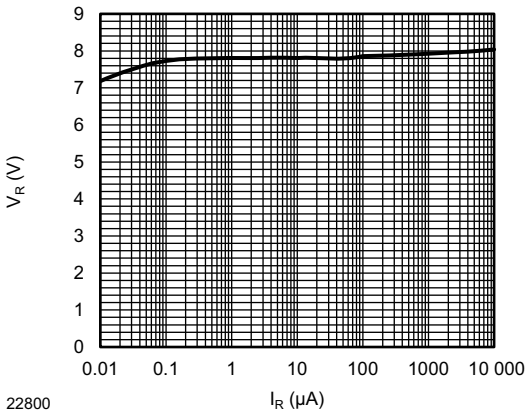


Fig. 5 - Typical Reverse Voltage vs. Reverse Current

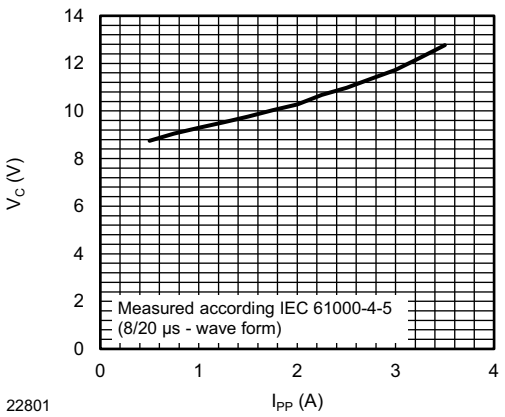


Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current

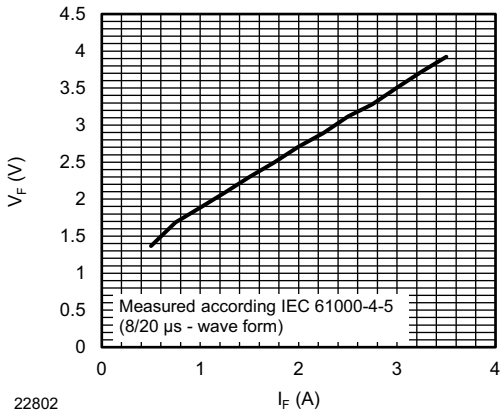


Fig. 7 - Typical Peak Forward Voltage vs. Forward Current

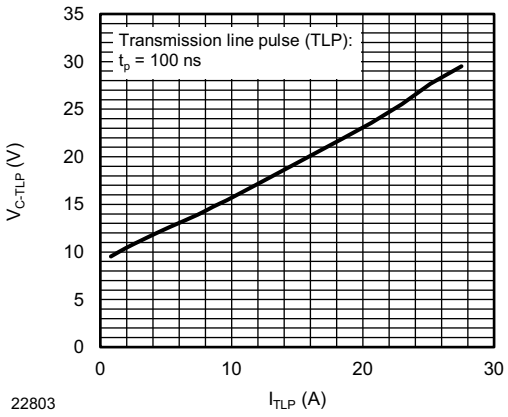
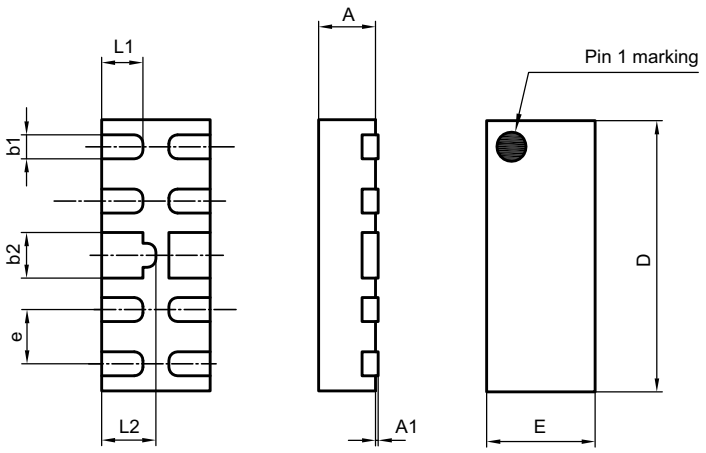


Fig. 8 - Typical Clamping Voltage vs. Peak Pulse Current

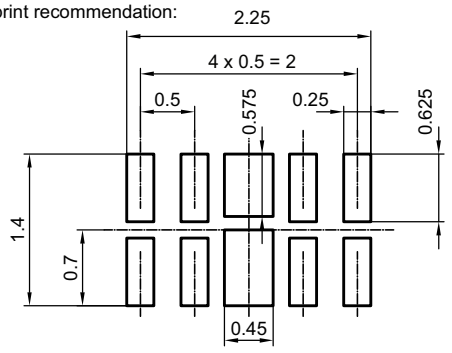
PACKAGE DIMENSIONS in millimeters: **LLP2510-10M**

Package = Chip Dimensions in mm



	Millimeters		
	Min.	Nom.	Max.
A	0.455	-	0.555
A1	0.00	-	0.05
b1	0.19	-	0.25
b2	0.39	-	0.45
D	2.45	-	2.55
E	0.95	-	1.05
e	-	0.50	-
L1	0.35	-	0.41
L2	0.48	-	0.54

foot print recommendation:



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Created - Date: 27. July 2015

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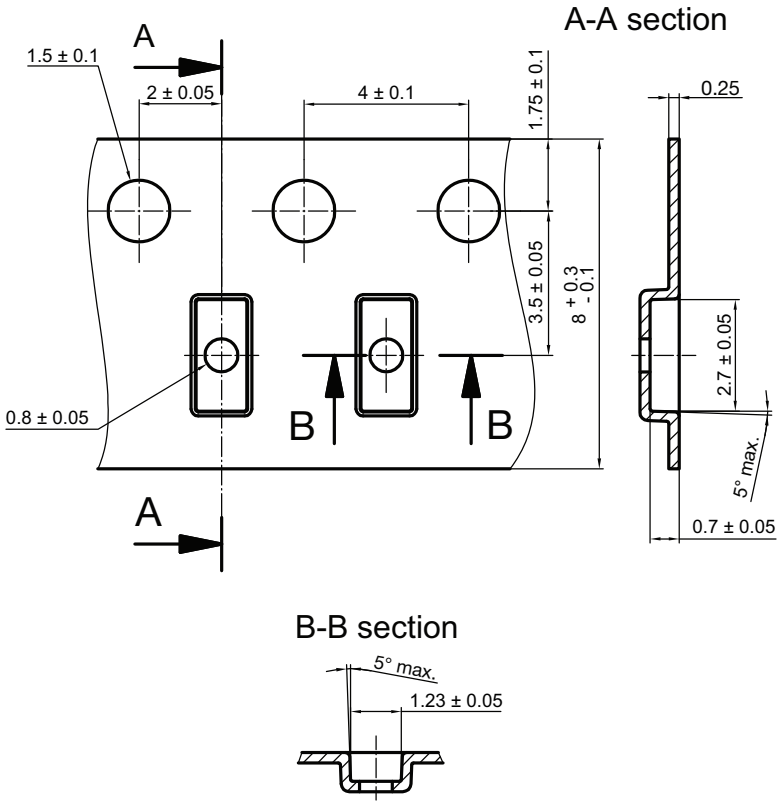
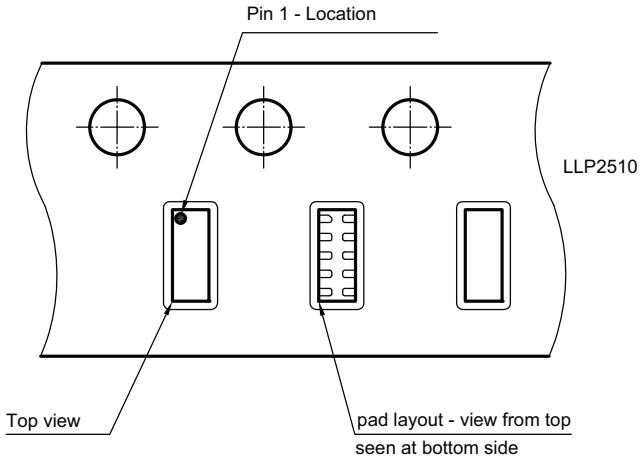
CARRIER TAPE in millimeters **LLP2510**



Cummulative tolerances of 10 sprocket holes is ± 0.2 mm

Document no. S8-V-3906.04-0028 (4)
Created - Date: 08. Jul. 2011

ORIENTATION IN CARRIER TAPE LLP2510



Document no. S8-V-3906.04-0029 (4)
Created - Date: 07. Jul. 2011

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