


Power MOSFET, 190 A


SOT-227

FEATURES

- Fully isolated package
- Very low on-resistance
- Fully avalanche rated
- Dynamic dV/dt rating
- Low drain to case capacitance
- Low internal inductance
- Optimized for SMPS applications
- Easy to use and parallel
- Industry standard outline
- Designed and qualified for industrial level
- UL approved file E78996 
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY	
V_{DSS}	100 V
I_D DC	190 A
$R_{DS(on)}$	0.0065 Ω
Type	Modules - MOSFET
Package	SOT-227

DESCRIPTION

High current density power MOSFETs are paralleled into a compact, high power module providing the best combination of switching, ruggedized device design, very low on-resistance and cost effectiveness.

The isolated SOT-227 package is preferred for all commercial-industrial applications at power dissipation levels to approximately higher than 500 W. The low thermal resistance and easy connection to the SOT-227 package contribute to its universal acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at V_{GS} 10 V	I_D	$T_C = 40\text{ }^\circ\text{C}$	190	A
		$T_C = 100\text{ }^\circ\text{C}$	130	
Pulsed drain current	I_{DM}		720	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	568	W
Linear derating factor			2.7	W/ $^\circ\text{C}$
Gate to source voltage	V_{GS}		± 20	V
Single pulse avalanche energy	E_{AS} ⁽²⁾		700	mJ
Avalanche current	I_{AR} ⁽¹⁾		180	A
Repetitive avalanche energy	E_{AR} ⁽¹⁾		48	mJ
Peak diode recovery dV/dt	dV/dt ⁽³⁾		5.7	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		-55 to +150	$^\circ\text{C}$
Insulation withstand voltage (AC-RMS)	V_{ISO}		2.5	kV
Mounting torque		M4 screw	1.3	Nm

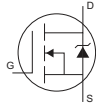
Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature.
- (2) Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 43\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 180\text{ A}$.
- (3) $I_{SD} \leq 180\text{ A}$, $dI/dt \leq 83\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150\text{ }^\circ\text{C}$.



THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T_J, T_{Stg}		- 55	-	150	°C
Junction to case	R_{thJC}		-	-	0.22	°C/W
Case to heatsink	R_{thCS}	Flat, greased surface	-	0.05	-	
Weight			-	30	-	g
Mounting torque		Torque to terminal	-	-	1.1 (9.7)	Nm (lbf.in)
		Torque to heatsink	-	-	1.3 (11.5)	Nm (lbf.in)
Case style			SOT-227			

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ °C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to $25\text{ °C}, I_D = 1\text{ mA}$	-	0.093	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 180\text{ A}$	-	0.0054	0.0065	Ω
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	3.3	4.35	V
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 180\text{ A}$	93	-	-	S
Drain to source leakage current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	500	
Gate to source forward leakage	I_{GSS}	$V_{GS} = 20\text{ V}$	-	-	200	nA
		$V_{GS} = -20\text{ V}$	-	-	- 200	
Total gate charge	Q_g	$I_D = 180\text{ A}$ $V_{DS} = 80\text{ V}$ $V_{GS} = 10\text{ V}$	-	250	-	nC
Gate to source charge	Q_{gs}		-	40	-	
Gate to drain ("Miller") charge	Q_{gd}		-	110	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$ $I_D = 180\text{ A}$ $R_g = 2.0\text{ }\Omega$ (internal) $R_D = 0.27\text{ }\Omega$	-	45	-	ns
Rise time	t_r		-	351	-	
Turn-off delay time	$t_{d(off)}$		-	181	-	
Fall time	t_f		-	335	-	
Internal source inductance	L_S	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$	-	10 700	-	pF
Output capacitance	C_{oss}		-	2800	-	
Reverse transfer capacitance	C_{rss}		-	1300	-	

SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	190	A
Pulsed source current (body diode)	I_{SM}		-	-	740	
Diode forward voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 180\text{ A}, V_{GS} = 0\text{ V}$	-	1.0	1.3	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ °C}, I_F = 180\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$	-	300	-	ns
Reverse recovery charge	Q_{rr}		-	2.6	-	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

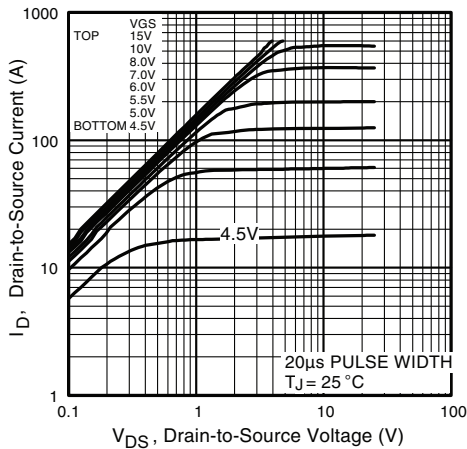


Fig. 1 - Typical Output Characteristics

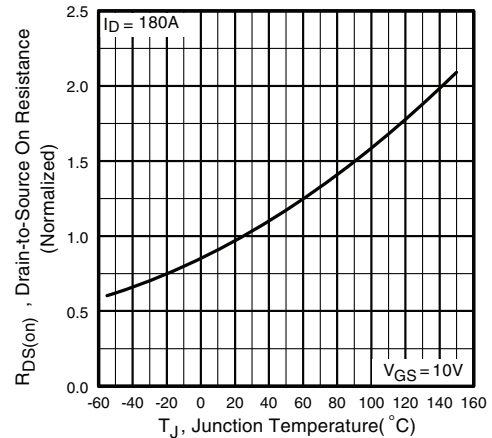


Fig. 4 - Normalized On-Resistance vs. Temperature

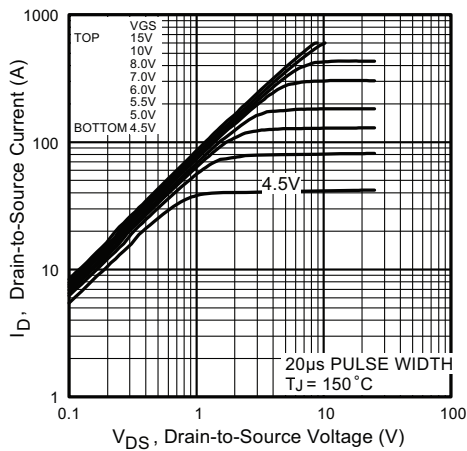


Fig. 2 - Typical Output Characteristics

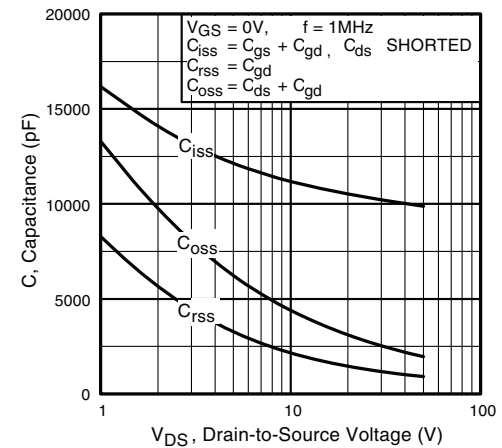


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

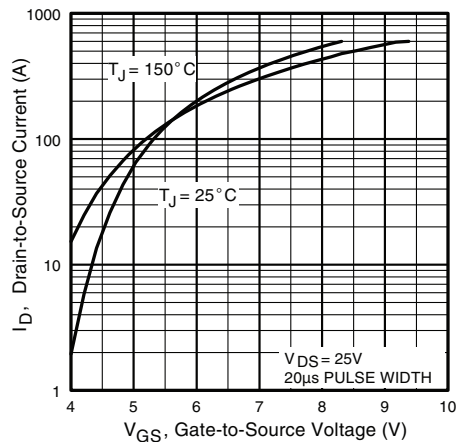


Fig. 3 - Typical Transfer Characteristics

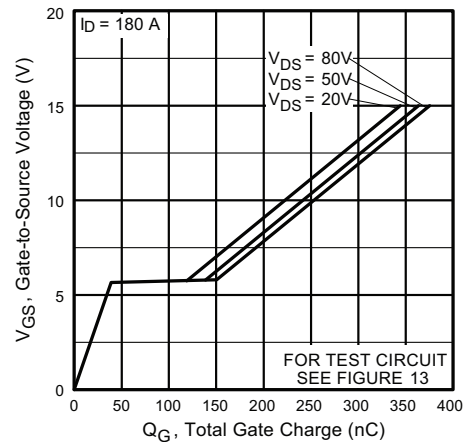


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

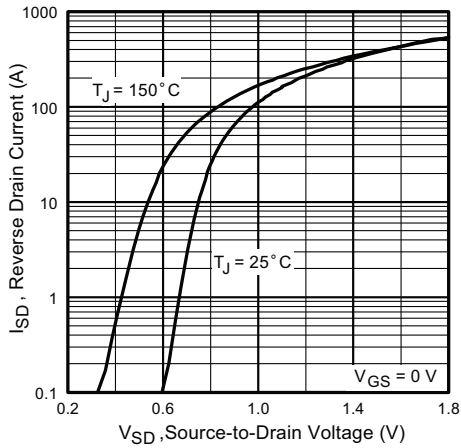


Fig. 7 - Typical Source Drain Diode Forward Voltage

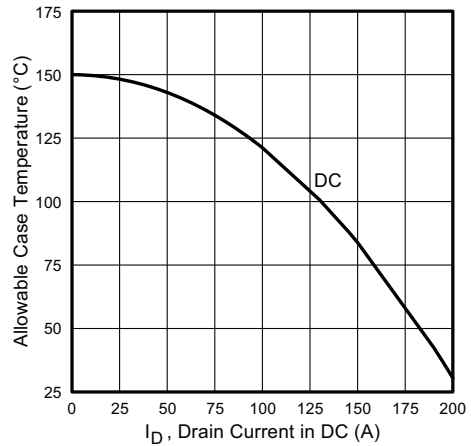


Fig. 9 - Maximum Drain Current vs. Case Temperature

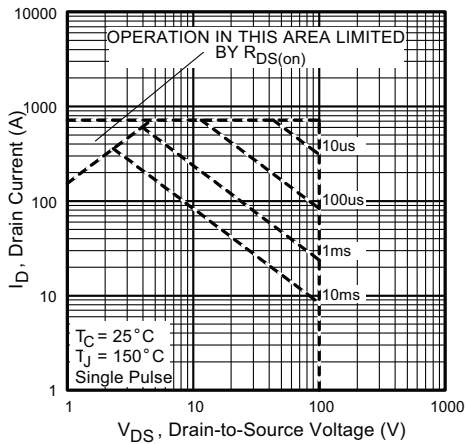


Fig. 8 - Maximum Safe Operating Area

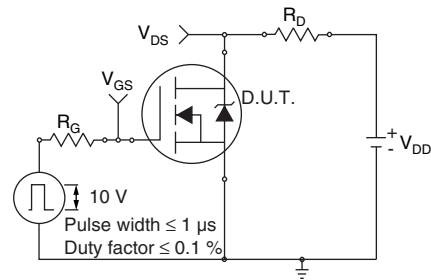


Fig. 10a - Switching Time Test Circuit

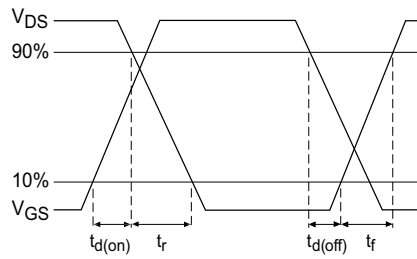


Fig. 10b - Switching Time Waveforms

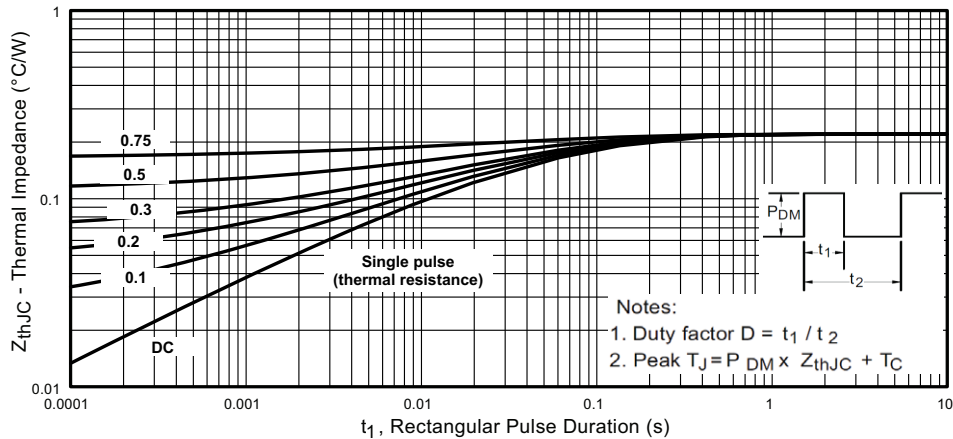


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

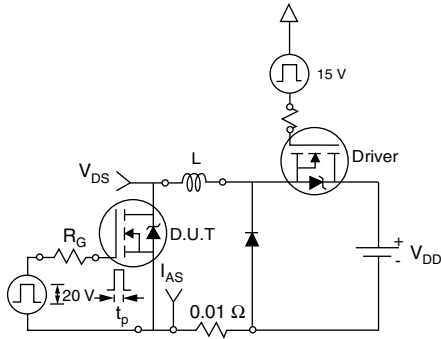


Fig. 12a - Unclamped Inductive Test Circuit

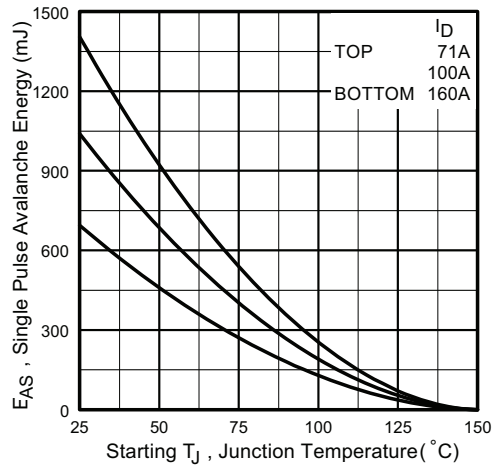


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

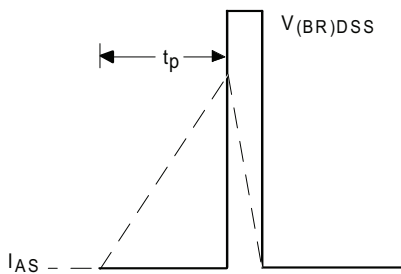


Fig. 12b - Unclamped Inductive Waveforms

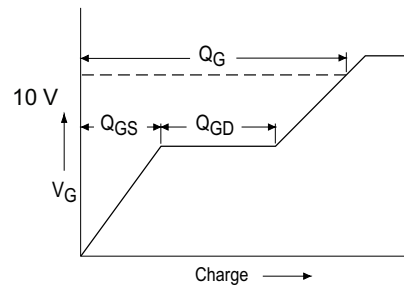


Fig. 13a - Basic Gate Charge Waveform

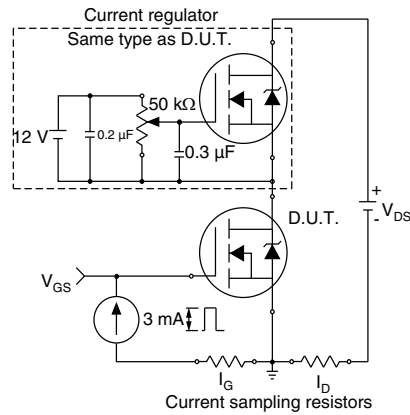


Fig. 13b - Gate Charge Test Circuit

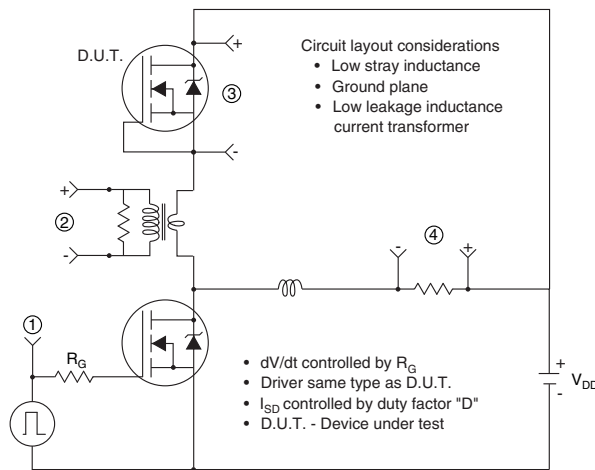
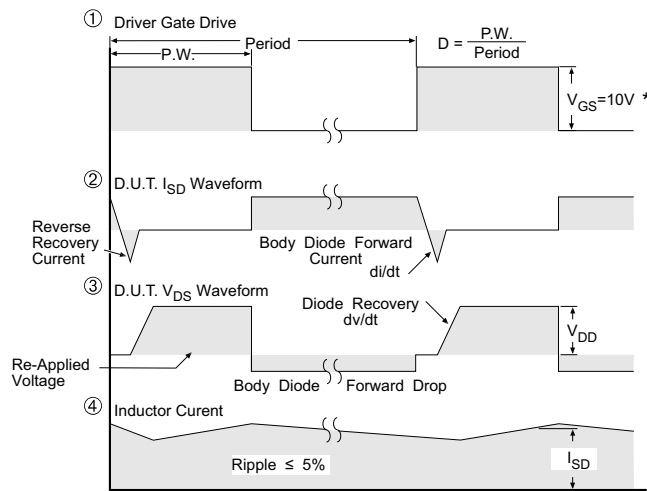


Fig. 13c - Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig. 14 - For N-Channel Power MOSFETs

ORDERING INFORMATION TABLE

Device code	VS-	F	B	190	S	A	10		
	①	②	③	④	⑤	⑥	⑦		
	1	-	Vishay Semiconductors product	2	-	Power MOSFET	3	-	Generation 5 MOSFET
	4	-	Current rating (190 = 190 A)	5	-	Single switch	6	-	Package indicator (SOT-227)
	7	-	Voltage rating (10 = 100 V)						

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch	S	<p>The drawing includes a MOSFET symbol with labels: D (3) for Drain, G (2) for Gate, and S (1-4) for Source. Below it is a 'Lead Assignment' diagram showing a top-down view of the SOT-227 package with leads labeled (S), (D), (S), and (G) corresponding to pins 1, 2, 3, and 4. To the right is a schematic diagram of the MOSFET with pins 3 (D), 2 (G), 4 (S), and 1 (S) connected to a circuit.</p>

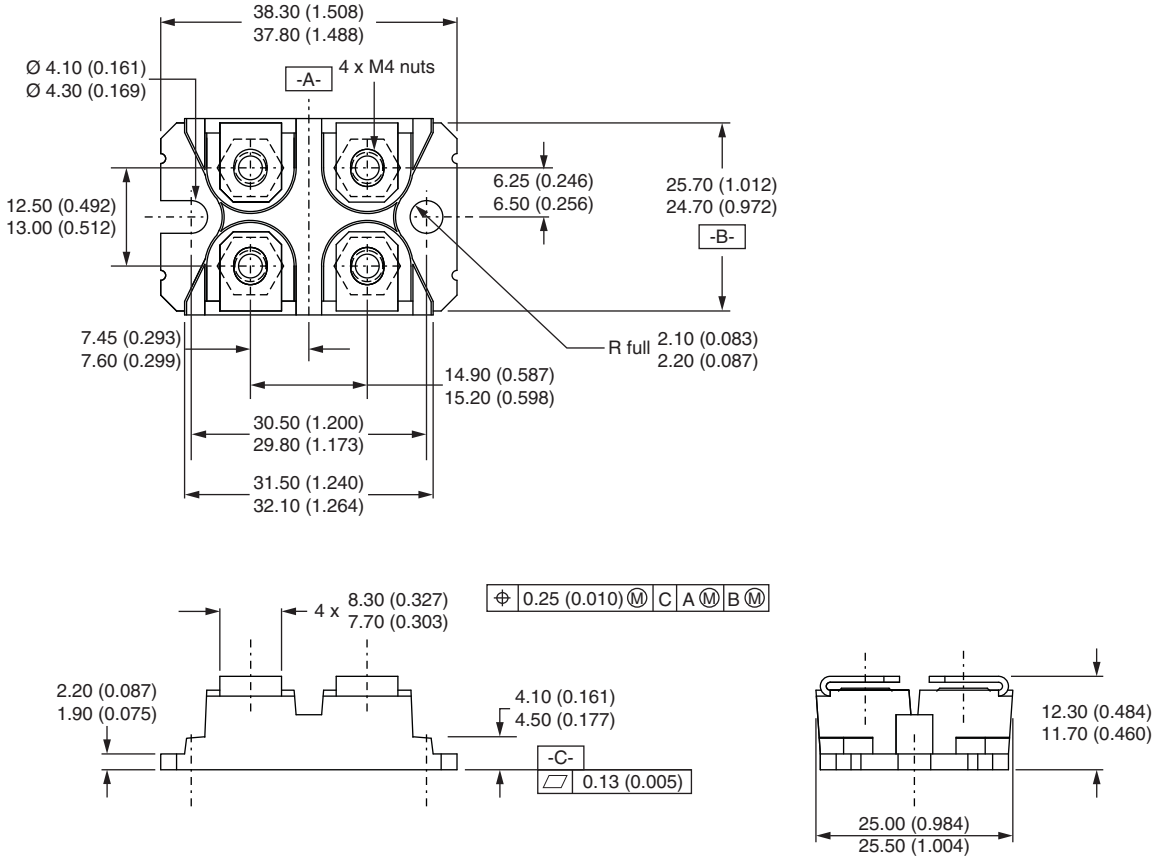
LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95423
Packaging information	www.vishay.com/doc?95425



SOT-227 Generation II

DIMENSIONS in millimeters (inches)



Note

- Controlling dimension: millimeter



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