Triple Skew-Compensating Video Delay Line with Analog and Digital Control

Data Sheet **AD8120**

FEATURES

- Corrects for unshielded twisted pair (UTP) cable skew
- Delay of up to 50 ns per channel
- High speed
  - 200 MHz BW @ V_{OUT} = 1.4 V p-p and 0 ns delay
  - 150 MHz BW @ V_{OUT} = 1.4 V p-p and 50 ns delay
- Excellent channel-to-channel matching
  - 30 mV offset matching RTI
  - 0.8% gain matching
- Low output offset
  - ±30 mV RTI
  - No external circuitry required to correct for offsets
- Independent red, green, and blue delay controls
- Drives 4 double-terminated video loads
- Digital and analog delay control
  - 6-bit SPI bus
  - I²C bus
  - Analog voltage control
- Fixed gain of 2
- Low noise
- High differential input impedance: 500 kΩ
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Keyboard-video-mouse (KVM)
- Digital signage
- RGB video over UTP cable
- Professional video projection and distribution
- HD video
- Security video
- General broadband delay lines

GENERAL DESCRIPTION

The AD8120 is a triple broadband skew-compensating delay line that corrects for time mismatch between video signals incurred by transmission in unshielded twisted pairs of Category 5 and Category 6 type cables. Skew between the individual pairs exists in most types of multipair UTP cables due to the different twist rates that are used for each pair to minimize crosstalk between pairs. For this reason, some pairs are longer than others, and in long cables, the difference in propagation time between two pairs can be well into the tens of nanoseconds.

The AD8120 contains three delay paths that provide broadband delays up to 50 ns, in 0.8 ns increments, using 64 digital control steps or analog control adjustment. The delay technique used in the AD8120 minimizes noise and offset at the outputs.

The bandwidth of the AD8120 ranges from 150 MHz to 200 MHz, depending on the delay setting. This wide bandwidth makes the AD8120 ideal for use in applications that receive high resolution video over UTP cables.

The logic circuitry of the AD8120 provides individual delay controls for each channel. The delay times are set independently using a standard 4-wire SPI bus or a standard I²C bus, or by applying analog control voltages to the V_{CR}, V_{CG}, and V_{CB} pins. Analog control offers a simple solution for systems that do not have digital control available.

The AD8120 is designed to be used with the AD8123 triple UTP equalizer in video over UTP applications, but it can also be used in other applications where similar controllable broadband delays are required.

The AD8120 is available in a 5 mm × 5 mm, 32-lead LFCSP and is rated to operate over the industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

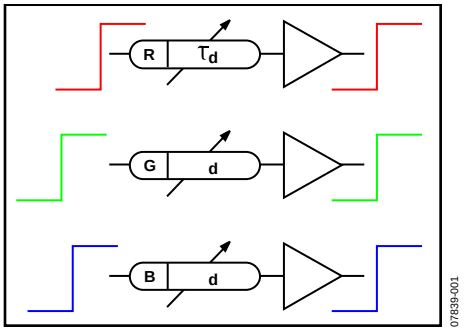

Figure 1.

Rev. A

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Documentation

Data Sheet

- AD8120: Triple Skew-Compensating Video Delay Line with Analog and Digital Control Datasheet

Reference Designs

- CN0275

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- AD8120 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changes to Table 1 4
Added Power Down Section 10
Updated Outline Dimensions 16

7/09—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, 10% to 90% input rise/fall time (t_R/t_F) = 4 ns, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DELAY CHARACTERISTICS					
Total Adjustable Delay Range	Delay Code 63 to Delay Code 0		50		ns
Delay Resolution	Monotonic, 1 LSB		0.8		ns
Propagation Delay	Delay = 0 ns		4.9		ns
Channel-to-Channel Delay Error	All channels at maximum delay		0.4		ns
DYNAMIC PERFORMANCE					
−3 dB Video Signal Bandwidth	V_{OUT} = 1.4 V p-p, delay = 0 ns		200		MHz
	V_{OUT} = 1.4 V p-p, delay = 50 ns		150		MHz
−3 dB Small-Signal Bandwidth	V_{OUT} = 0.2 V p-p, delay = 0 ns		165		MHz
	V_{OUT} = 0.2 V p-p, delay = 50 ns		140		MHz
0.1 dB Video Signal Flatness	V_{OUT} = 1.4 V p-p, delay = 0 ns		27		MHz
	V_{OUT} = 1.4 V p-p, delay = 50 ns		35		MHz
10% to 90% Rise/Fall Time	V_{OUT} = 1.4 V step, delay = 0 ns		2.5/3		ns
	V_{OUT} = 1.4 V step, delay = 50 ns		3/4.2		ns
Settling Time to 1%	V_{OUT} = 1.4 V step, delay = 0 ns		8		ns
	V_{OUT} = 1.4 V step, delay = 50 ns		18		ns
Slew Rate	V_{OUT} = 1.4 V step, delay = 0 ns, rising edge		550		V/µs
	V_{OUT} = 1.4 V step, delay = 0 ns, falling edge		540		V/µs
	V_{OUT} = 1.4 V step, delay = 50 ns, rising edge		510		V/µs
	V_{OUT} = 1.4 V step, delay = 50 ns, falling edge		360		V/µs
Overshoot	V_{OUT} = 1.4 V step, delay = 0 ns		1		%
	V_{OUT} = 1.4 V step, delay = 50 ns		20		%
Gain	0 ns to 50 ns delay	1.95	2.01	2.06	V/V
Channel-to-Channel Gain Matching	Over all codes, among all channels		0.8	3	%
Hostile Crosstalk	Measured on G with R and B driven at 1 MHz, V_{OUT} = 1.4 V p-p, delay = 0 ns		−80		dB
VIDEO INPUT CHARACTERISTICS	R_{IN}, G_{IN}, B_{IN}				
Input Bias Current			0.8	1.5	µA
Input Capacitance			1		pF
Input Resistance			500		kΩ
VIDEO OUTPUT CHARACTERISTICS	R_{OUT}, G_{OUT}, B_{OUT}				
Output Voltage Swing			±3.25		V
Output Current			50		mA
Integrated Output Noise	100 kHz to 160 MHz				
	Delay = 0 ns		1		mV rms
	Delay = 50 ns		4		mV rms
Output Offset Voltage (RTI)	Over all codes	−30	0	+30	mV
Channel-to-Channel Output Offset Voltage Matching (RTI)	Over all codes, among all channels		30		mV
Output Impedance	$\overline{PD}$ high, at 20 MHz		1.5		Ω
ANALOG CONTROL INPUT CHARACTERISTICS					
Input Bias Current	V_{CR}, V_{CG}, V_{CB}		1		µA
Operating Range	V_{CR}, V_{CG}, V_{CB}	0		2	V
Delay Voltage Step Size in Linear Range	ΔV_{CR}, ΔV_{CG}, ΔV_{CB} to move one delay LSB		28		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUT CHARACTERISTICS (SEE BELOW FOR POWER DOWN)	SDO/SDA, SCK/SCL, SDI/A1, $\overline{CS}$/A0, SER_SEL, MODE				
Input Bias Current			2		µA
Input High Voltage		2.6			V
Input Low Voltage				0.6	V
Output High Voltage				4.5	V
Output Low Voltage		0.6			V
POWER DOWN CHARACTERISTICS	$\overline{PD}$				
Input High Voltage		4.0			V
Input Low Voltage				0.6	V
SPI TIMING CHARACTERISTICS					
Clock Frequency	SCK			10	MHz
$\overline{CS}$ Setup Time, t_1	$\overline{CS}$ to SCK	5			ns
Clock Pulse High, t_2	SCK	50			ns
Clock Pulse Low, t_3	SCK	50			ns
Data Setup Time, t_4	SDI to SCK	5			ns
Data Hold Time, t_5	SDI to SCK	5			ns
$\overline{CS}$ Hold Time, t_6	SCK to $\overline{CS}$	5			ns
I^2C TIMING CHARACTERISTICS					
Clock Frequency	SCL			100	kHz
Start Setup Time, t_1	SDA to SCL	10			ns
Clock Pulse High, t_2	SCL	5			µs
Clock Pulse Low, t_3	SCL	5			µs
Data Setup Time, t_4	SDA (input) to SCL	100			ns
Data Hold Time, t_5	SDA (input) to SCL	100			ns
Hold Time, t_6	SCL to SDA	10			ns
POWER SUPPLY					
Positive Supply Range		4.5		5.5	V
Negative Supply Range		−5.5		−4.5	V
Positive Quiescent Current	Delay = 0 ns		44		mA
	Delay = 50 ns		114		mA
	Powered down, $\overline{PD}$ low		4		mA
Negative Quiescent Current	Delay = 0 ns		37		mA
	Delay = 50 ns		108		mA
	Powered down, $\overline{PD}$ low		0.5		mA
Quiescent Current Drift	T_{MIN} to T_{MAX}, delay = 0 ns		0.13		mA/°C
	T_{MIN} to T_{MAX}, delay = 50 ns		0.36		mA/°C
+PSRR	R_L = 150 Ω, delay = 50 ns		56		dB
−PSRR	R_L = 150 Ω, delay = 50 ns		44		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±6 V
Internal Power Dissipation	
32-Lead LFCSP at T_A = 25°C	3.5 W
Input Voltage	V_{S-} − 0.3 V to V_{S+} + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, for a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5 mm × 5 mm, 32-Lead LFCSP	36	2	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8120 package is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is approximately 150°C. Temporarily exceeding this limit may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power dissipation is the voltage between the supply pins (V_{S+} and V_{S-}) times the quiescent current (I_S). Power dissipated due to load drive depends upon the particular application. It is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation by reducing θ_{JA}.

To ensure optimal thermal performance, the exposed paddle must be in an optimized thermal connection with an external plane layer.

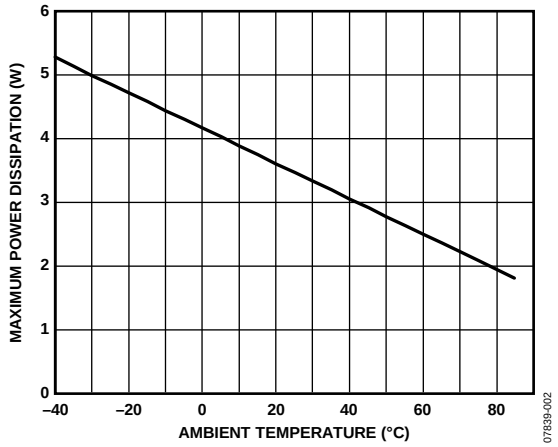


Figure 2. Maximum Power Dissipation vs. Ambient Temperature on a JEDEC Standard 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

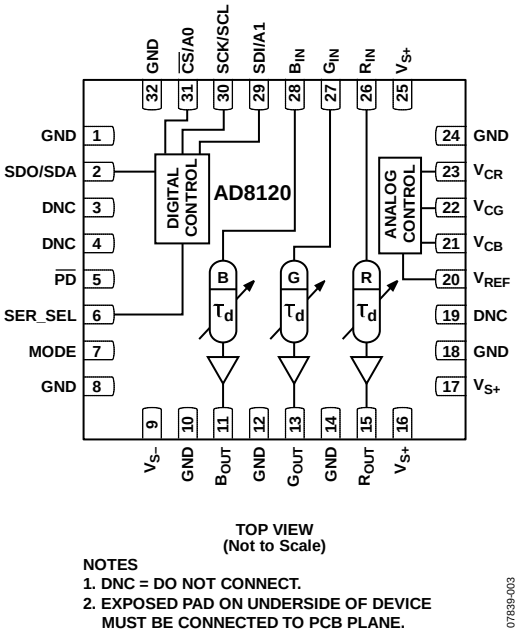


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 10, 12, 14, 18, 24, 32	GND	Ground.
2	SDO/SDA	Serial Data Output for SPI Bus/Bidirectional Serial Data Line for I²C Bus.
3, 4, 19	DNC	Do Not Connect.
5	$\overline{PD}$	Power-Down.
6	SER_SEL	Selection of SPI Serial Bus or I²C Serial Bus (I²C = 0, SPI = 1).
7	MODE	Selection of Analog Control Mode or Digital Control Mode (Digital = 0, Analog = 1).
9	V_{S-}	Negative Power Supply. Connect to −5 V.
11	B_{OUT}	Blue Channel Video Output.
13	G_{OUT}	Green Channel Video Output.
15	R_{OUT}	Red Channel Video Output.
16, 17, 25	V_{S+}	Positive Power Supply. Connect to +5 V.
20	V_{REF}	Internal Reference Bypass. Connect a 0.01 µF capacitor between this pin and GND.
21	V_{CB}	Analog Delay Control Voltage, Blue Channel.
22	V_{CG}	Analog Delay Control Voltage, Green Channel.
23	V_{CR}	Analog Delay Control Voltage, Red Channel.
26	R_{IN}	Red Channel Video Input.
27	G_{IN}	Green Channel Video Input.
28	B_{IN}	Blue Channel Video Input.
29	SDI/A1	Serial Data Input for SPI Bus/I²C Address Bit 1.
30	SCK/SCL	Serial Clock for SPI Bus/Serial Clock for I²C Bus.
31	$\overline{CS}$/A0	Chip Select for SPI Bus/I²C Address Bit 0.
Exposed Pad	EP	Thermal Plane Connection. Connect the exposed pad on the underside of the AD8120 to any PCB plane with voltage between V_{S+} and V_{S-}.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, 10% to 90% input rise/fall time (t_R/t_F) = 4 ns, unless otherwise noted.

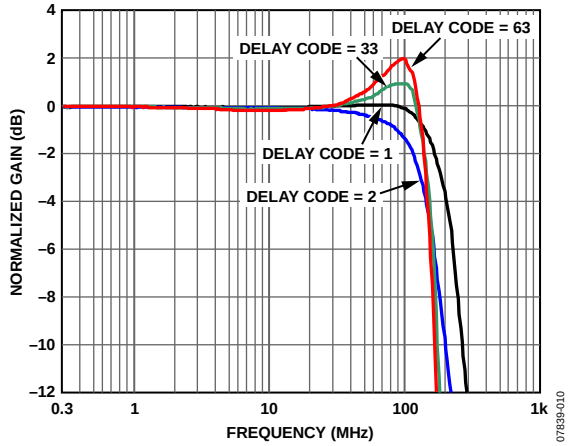


Figure 4. Small-Signal Frequency Response for Various Delay Settings, V_{OUT} = 0.2 V p-p

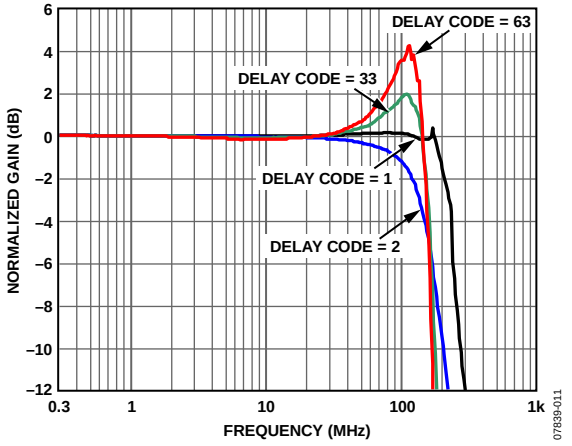


Figure 7. Video Signal Frequency Response for Various Delay Settings, V_{OUT} = 1.4 V p-p

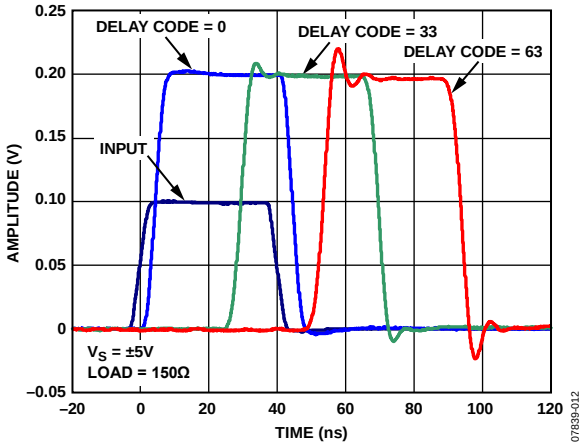


Figure 5. Small-Signal Pulse Response for Various Delay Settings

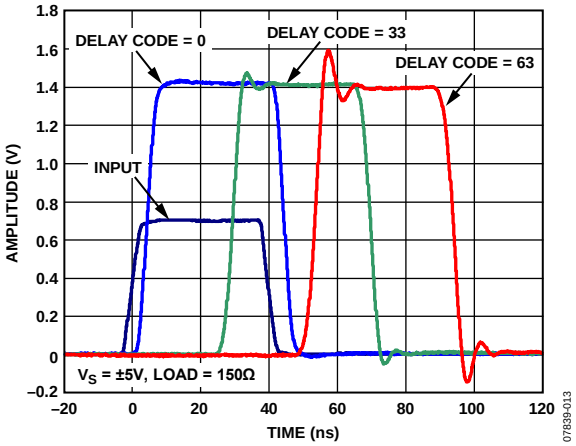


Figure 8. Large-Signal Pulse Response for Various Delay Settings

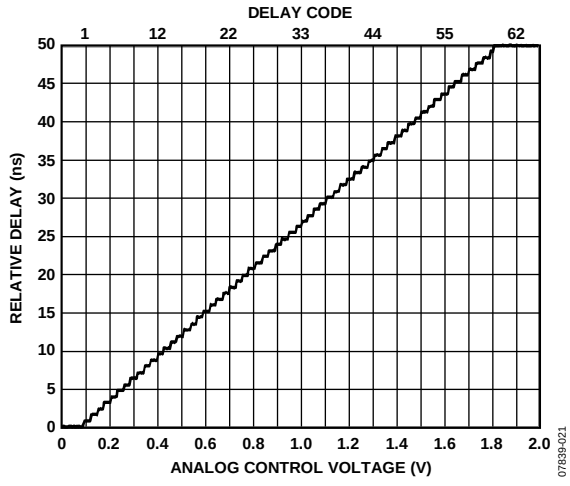


Figure 6. Relative Delay vs. Delay Code and Analog Control Voltage

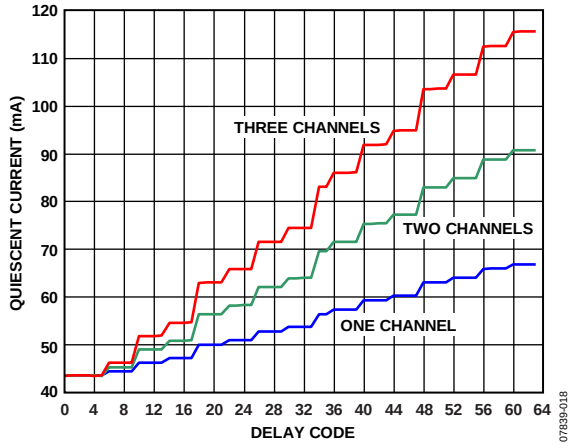


Figure 9. Quiescent Current vs. Delay Code

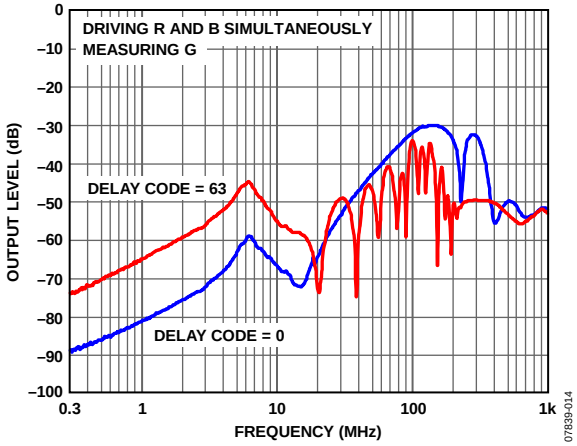


Figure 10. Crosstalk on Green Channel vs. Frequency, V_{OUT} = 1.4 V p-p

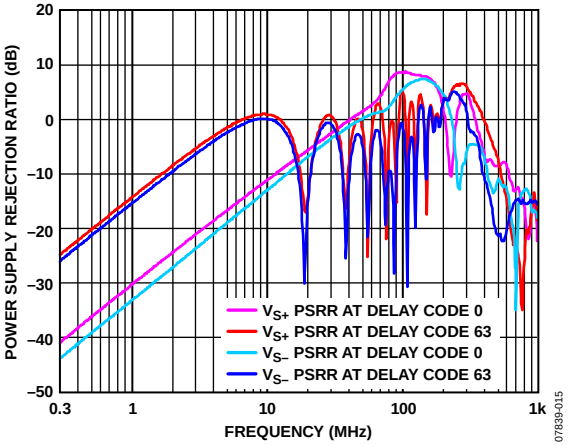


Figure 13. PSRR vs. Frequency

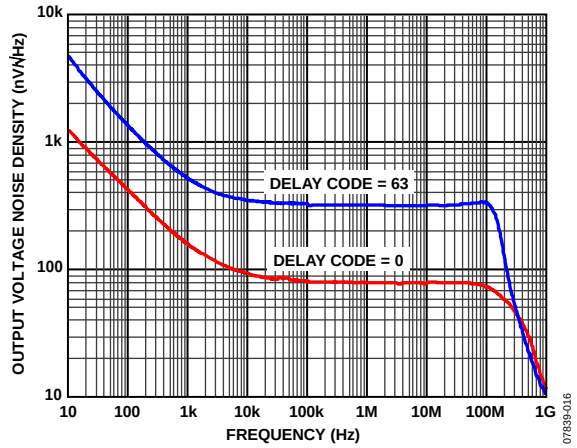


Figure 11. Output Voltage Noise Density vs. Frequency

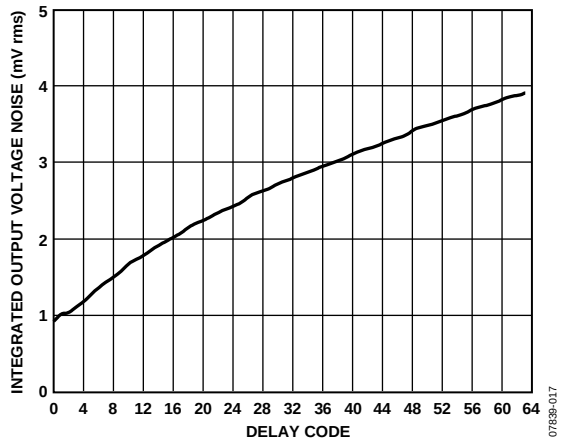


Figure 14. Integrated Output Voltage Noise vs. Delay Code, 100 kHz to 160 MHz

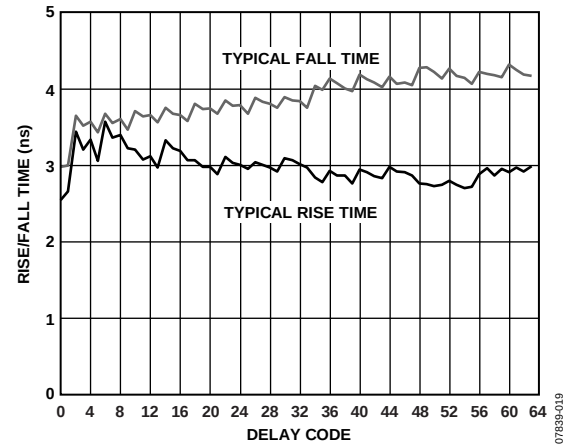


Figure 12. 10% to 90% Rise/Fall Time vs. Delay Code, V_{OUT} = 1.4 V p-p, V_{IN} Rise/Fall = 2 ns

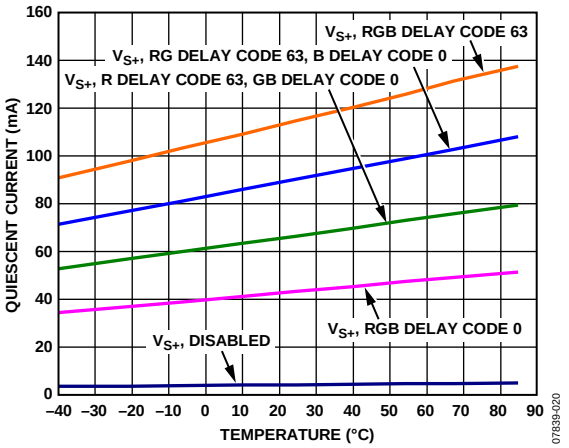


Figure 15. Quiescent Current vs. Temperature

THEORY OF OPERATION

The AD8120 is a triple, digitally controlled analog delay line, optimized for correcting delay skew between individual channels in common wired communication media such as unshielded twisted pair (UTP), shielded twisted pair (STP), and coaxial cables. In these applications, the AD8120 is used to time-align three video signals, usually RGB or YPbPr, that arrive at a receiver at different times due to variations in total delay per channel. Although its primary application is analog video, the AD8120 can be applied in other systems that require variable analog delays up to 50 ns with 0.8 ns resolution.

The three channels consist of cascaded delay sections that are switched in such a way as to provide a total of 50 ns total delay difference between channels with 0.8 ns resolution. A fixed propagation delay is common to all channels, where the associated delay is set to 0. Therefore, the delay setting for a given channel is a measure of the relative delay among the channels, rather than an absolute delay.

There are three options for controlling the delay: serial peripheral interface (SPI) serial bus, I²C serial bus, and analog control voltage. Two pins select the type of control: the MODE pin selects analog or digital control, and the SER_SEL pin selects the SPI or I²C serial bus (see Table 5).

Table 5. Modes of Control

$\overline{PD}$ (Pin 5)	MODE (Pin 7)	SER_SEL (Pin 6)	Control Type
0	X	X	Power-down
1	0	0	I²C control
1	0	1	SPI control
1	1	X	Analog control

In analog control mode, three control voltages, V_{CR}, V_{CG}, and V_{CB}, control the delay of each channel. These voltages are converted internally to digital codes with 0.8 ns steps.

Each AD8120 channel has a fixed overall gain of 2 and can drive up to four double-terminated 75 Ω cables or PCB traces. A power-down feature can shut down the AD8120 for power saving when not in use.

CONTROLLING THE DELAY

The delay time of each of the three channels is controlled in one of three ways. One control option is the application of analog control voltages to the V_{CR}, V_{CG}, and V_{CB} inputs. The other two control options are via the SPI or I²C serial digital bus. The delay is set in discrete amounts with a nominal resolution of 0.8 ns per quantization level (or LSB), even in the analog control mode.

A delay code is assigned to each quantization level, ranging from 0 to 63 in decimal format. The means of control (analog, SPI, or I²C) is selected by applying the appropriate logic levels to the MODE and SER_SEL inputs (see Table 5). All three channels must use the same delay control option in a given application.

It is important to note that in skew correction applications, the metric is the relative delay between channels, not the absolute delay. Each channel of the AD8120 exhibits a constant delay at its zero delay setting, referred to as its propagation delay. This propagation delay is well matched between the channels and is subtracted out when performing skew correction. The delay codes, therefore, ignore the constant propagation delay and refer only to adjustable delay beyond the propagation delay.

Delay can be calculated by multiplying the delay code by 0.8 ns. For example, setting the red delay to 8 ns (delay code = 10), the green delay to 16 ns (delay code = 20), and the blue delay to 28 ns (delay code = 35) produces the following relative delays: green delayed by 8 ns relative to red, blue delayed by 20 ns relative to red, and blue delayed by 12 ns relative to green. If an application requires control of absolute delay, the propagation delay must be added to the delay corresponding to the associated delay code.

SETTING THE DELAY

In most video skew compensation applications, it is best to set the delay of the path with the longest delay to 0, and then to add delay to the other paths to match the longest delay. In this way, the bandwidth of each path is maximized, and the noise of each path is minimized. Figure 16 illustrates a case where a test step is applied simultaneously to each cable input, and the green cable delay is the longest.

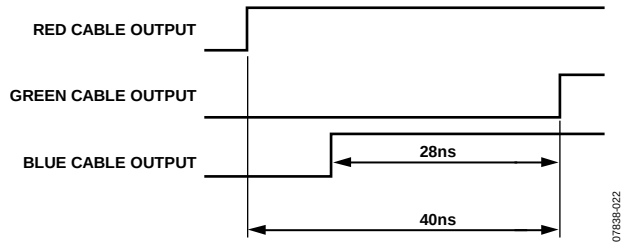


Figure 16. Cable Delay Example

In the example in Figure 16, the AD8120 green delay should be set to 0. The AD8120 red delay is then set to the delay difference between the green and red outputs, or 40 ns. Finally, the AD8120 blue delay is set to the delay difference between the green and blue outputs, or 28 ns. Using the digital delay codes, green delay = 0, red delay = 50, and blue delay = 35.

ANALOG CONTROL

A number of video transmission systems do not have a microcontroller embedded or otherwise available to provide digital control. These systems require analog control. Potentiometer control is one of the most common ways to implement analog control (see Figure 25). To select analog control, set the MODE pin high.

The AD8120 has one analog control input for each channel: V_{CR}, V_{CG}, and V_{CB}. The maximum recommended control voltage range on these inputs is 0 V to 2.0 V, although the actual control range where delay changes take effect is smaller and lies within this larger range. An internal ADC converts the analog control voltages into binary delay codes; therefore, the analog control is discrete with nominally 0.8 ns resolution. Figure 6 illustrates the typical transfer characteristic between control voltage and delay code.

POWER DOWN

The power-down feature is intended to be used to reduce power consumption when a particular device is not in use and does not place the output in a high-Z state when asserted. Note that the input high level for the power-down input is higher than it is for the other digital inputs. Refer to the Specifications in Table 1 for details.

DIGITAL CONTROL

Set the MODE pin low to select digital control (SPI or I^2C). Set the SER_SEL pin high to select SPI mode, or set the SER_SEL pin low to select I^2C mode. Table 6 provides the bit values for reading and writing the red, green, and blue registers.

Table 6. Read/Write Instruction and Color Registers

Operation	R/$\overline{W}$ Bit	C1 Bit	C0 Bit
Write Red	0	0	0
Read Red	1	0	0
Write Green	0	0	1
Read Green	1	0	1
Write Blue	0	1	0
Read Blue	1	1	0

SPI Control

The SPI bus operates in full-duplex mode and consists of four digital lines: SDI, SDO, SCK, and $\overline{CS}$.

Table 7. AD8120 SPI Pin Descriptions

Pin No.	Pin Name	Description
29	SDI	Serial data input, master out slave in (MOSI)
2	SDO	Serial data output, master in slave out (MISO)
30	SCK	Serial clock from master
31	$\overline{CS}$	Chip select; active low

The AD8120 is programmed in SPI mode using a 2-byte sequence (see Table 8). Data is clocked into the SDI pin or clocked out of the SDO pin on the rising edge of the clock, MSB first. The first byte contains the read/write (R/$\overline{W}$) instruction and the color register address (see Table 6). The second byte contains the delay code to write to the part (R/$\overline{W}$ = 0) or the stored delay code to read from the part (R/$\overline{W}$ = 1).

Figure 17 shows how to write Delay Code 42 to the green register. Figure 18 shows how to read Delay Code 21 from the blue register.

Table 8. SPI 2-Byte Sequence

	Byte 1 (R/$\overline{W}$ Bit and Color Register)								Byte 2 (Data)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDI	R/$\overline{W}$	0	0	0	0	0	C1	C0	X	X	D5	D4	D3	D2	D1	D0
SDO	X	X	X	X	X	X	X	X	X	X	D5	D4	D3	D2	D1	D0

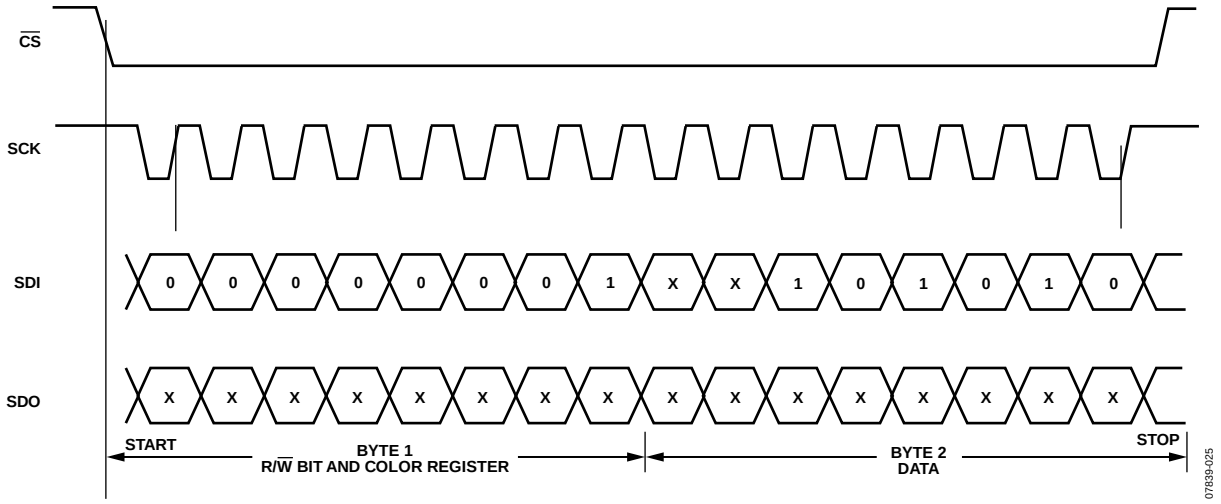


Figure 17. Setting the Green Register to Delay Code 42 Using SPI

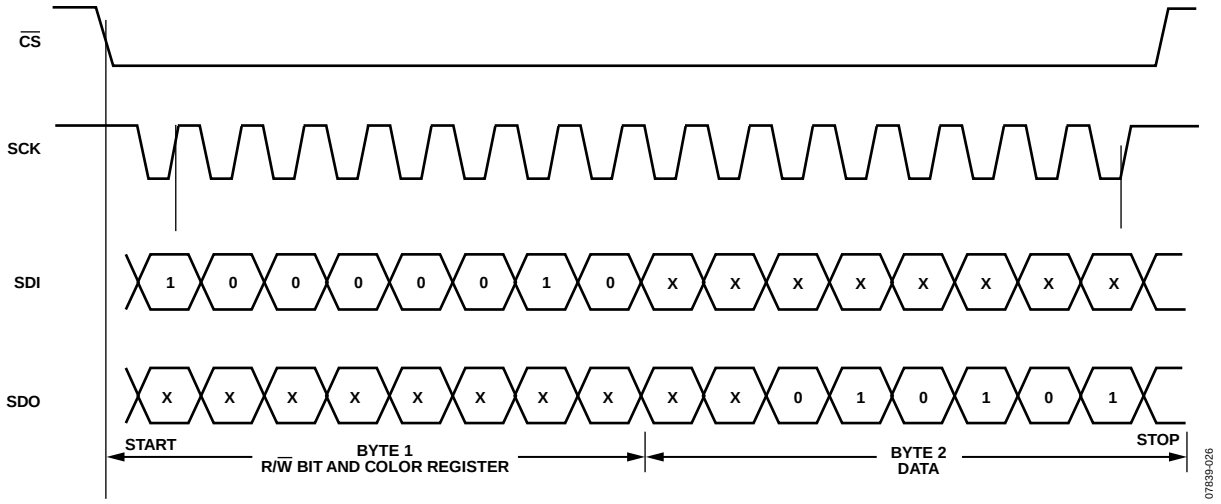


Figure 18. Reading Delay Code 21 from the Blue Register Using SPI

I²C Control

The I²C interface of the AD8120 is a 2-wire interface consisting of a clock input and a bidirectional data line. The AD8120 drives the SDA line either to acknowledge the master (ACK) or to send data during a read operation. The SDA pin for the I²C port is open drain and requires a 10 kΩ pull-up resistor.

Table 9. AD8120 I²C Pin Descriptions

Pin No.	Pin Name	Description
2	SDA	Serial data input/output
30	SCL	Serial clock input
29	A1	I²C Address Bit A1
31	A0	I²C Address Bit A0

The AD8120 address consists of a built-in address of 0x38 and the two address pins, A0 and A1. The two address pins enable up to four AD8120 devices to be used in a system (see Table 10). Both address pins must be terminated (high or low) for the AD8120 I²C interface to operate properly.

Table 10. I²C Addresses

A1 Pin	A0 Pin	I²C Address
0	0	0x38
0	1	0x39
1	0	0x3A
1	1	0x3B

In I²C mode, the AD8120 is programmed with a 3-byte sequence for a write operation (see Figure 19) and a 4-byte sequence for a read operation (see Figure 20). The first byte contains the 7-bit device address and the R/$\overline{W}$ instruction bit. The second byte contains the color register.

In write mode, the third byte contains the delay code. In read mode, the third byte contains the device address, and the fourth byte contains the stored delay code.

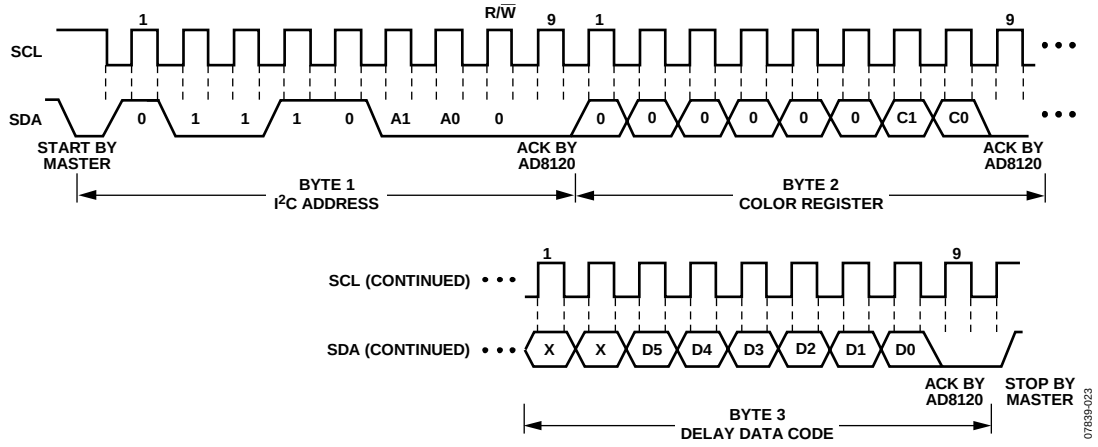


Figure 19. I²C Write Sequence

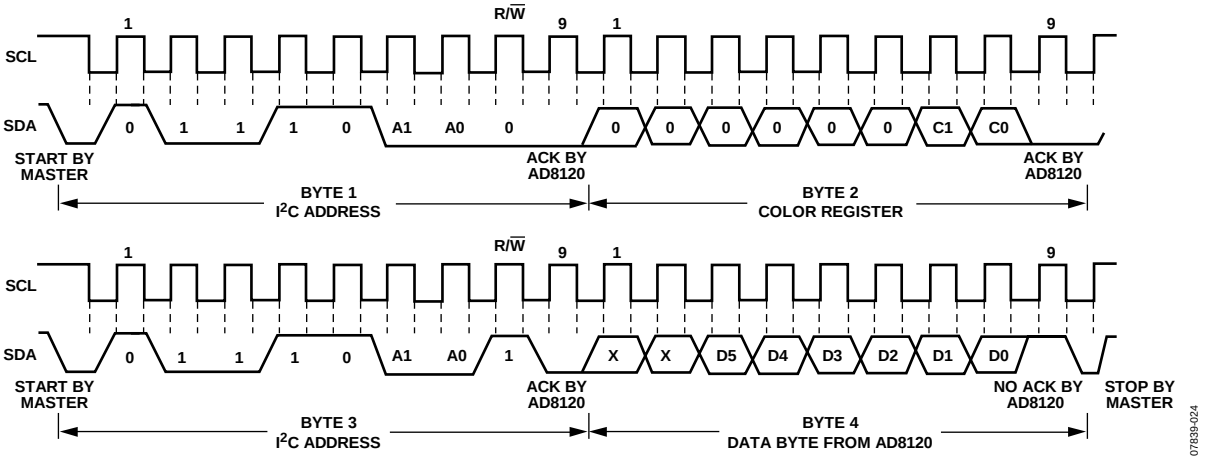


Figure 20. I²C Read Sequence

SPI Timing

Figure 21 shows the SPI 2-byte timing sequence. Table 11 lists the timing parameters for SPI.

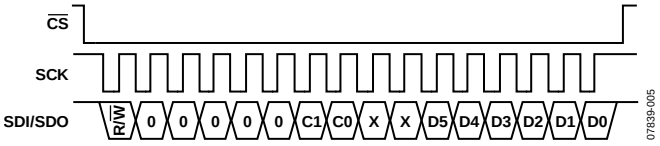


Figure 21. SPI 2-Byte Timing Sequence

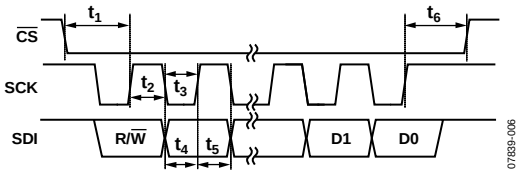


Figure 22. SPI Timing Diagram

Table 11. SPI Timing Parameters

Parameter	Description
t_1	Setup time, $\overline{CS}$ to SCK
t_2	Clock pulse high, SCK
t_3	Clock pulse low, SCK
t_4	Setup time, SDI to SCK
t_5	Hold time, SDI to SCK
t_6	Hold time, SCK to $\overline{CS}$

I^2C Timing

Figure 23 shows the I^2C 3-byte timing sequence. Table 12 lists the timing parameters for I^2C.

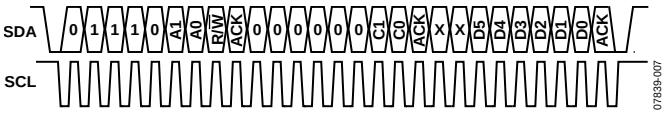


Figure 23. I^2C 3-Byte Timing Sequence

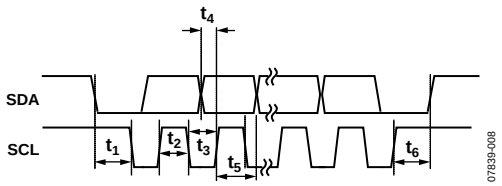


Figure 24. I^2C Timing Diagram

Table 12. I^2C Timing Parameters

Parameter	Description
t_1	Setup time, SDA to SCL
t_2	Clock pulse high, SCL
t_3	Clock pulse low, SCL
t_4	Setup time, SDA (input) to SCL
t_5	Hold time, SDA (input) to SCL
t_6	Hold time, SCL to SDA

APPLICATIONS INFORMATION

Most twisted pair (TP) cables used for video transmission are designed for data communication and typically contain four individual TP channels. Minimization of crosstalk between pairs is of paramount importance in data communication applications. This is accomplished by varying the twist rates (twists per unit length) of each pair. For a given cable length, signals traveling on pairs with relatively high twist rates have longer distances to traverse than signals traveling on pairs with relatively low twist rates. The longer relative distances translate into longer relative delays and, similarly, the shorter relative distances translate into shorter relative delays.

The delay of any TP channel is not flat over frequency, and an equalizer is generally used at the receiver to produce an approximately flat delay vs. frequency characteristic as well as an approximately flat frequency response magnitude over the bandwidth of interest. The term "group delay" is often used in the delay vs. frequency context. When the group delay and the magnitude response have been corrected to the best possible degree at the receiver, the remaining signals are close approximations to those sent at the transmit end of the cable, but with different delays with respect to the signals sent at the transmit end. The signals, therefore, manifest different delays relative to each other.

The relative delay difference between any two equalized signals at the receiver is defined as delay skew, or simply skew, and is measured in units of time. Some bundled coaxial cables also exhibit delay skew between channels; these skew levels are typically much smaller than those encountered among similar length TP channels.

The AD8120 can be used with RGB and YPbPr, as well as other video formats. Typically, three video component signals are transmitted over the TP cables, with each component carried on a pair. For example, with RGB video signals, the red, green, and blue signals are each transmitted over one pair. If these signals are carried over a cable with skew larger than a quarter of a pixel time and are displayed on a video monitor, the three colors will not be properly aligned and the skew will be visible at the vertical edges of objects displayed on the monitor. For fractional pixel time skew levels, a rainbow-like effect appears at the vertical edges of the objects; for skew levels longer than a pixel time, vertical lines are visible on the vertical edges of objects. The vertical lines are due to one color arriving earlier or later than the others. The best way to observe skew is to view an object against a black background.

The AD8120 is a triple adjustable delay line, and its primary application is to realign the received, equalized video components. The pixel time of UXGA video with a refresh rate of 60 Hz is approximately 6.2 ns. In this case, the 0.8 ns delay resolution of the AD8120 represents approximately 13% of a pixel time.

TYPICAL APPLICATION CIRCUIT FOR THE AD8123 AND AD8120

Figure 25 illustrates a complete receiver application circuit using sync-on common mode; this circuit comprises the AD8123 triple equalizer and the AD8120. The circuit receives balanced RGB video signals over TP cable, performs cable equalization and skew correction, and directly drives 75 Ω coaxial cable. The 6 dB voltage gain in the AD8120 compensates for the 6 dB double termination loss incurred driving the coaxial cable. The low-pass filter is optimized for short distances. Refer to the AD8123 data sheet for details regarding the sync encoding and decoding.

The filter between the AD8123 and the AD8120 is a three-pole low-pass filter (LPF) with a cutoff frequency of approximately 148 MHz; the LPF is included to provide high frequency noise reduction. The filter shown in the application circuit performs well for short to medium length cables. Note that the 1 pF capacitance of each AD8120 input is added to each filter capacitor that is connected to each AD8120 input. Thus, for the filter shown, the actual filter capacitance at each AD8120 input is 16 pF.

For longer cables, where much greater high frequency gain is required from the AD8123, it may be desirable to scale the LPF bandwidth back to provide greater noise reduction. This can be done by simply scaling the inductor and capacitor values by the ratio of the existing cutoff frequency of 140 MHz to the desired new cutoff frequency. For example, if a new cutoff frequency of 100 MHz is desired, the inductor and capacitor values are scaled by a factor of (140 MHz/100 MHz) = 1.4. This is summarized in Table 13.

Table 13. Low-Pass Filter Component Selection for 100 MHz Cutoff

Original Value	Scale Factor	New Value	
		Ideal	Standard
5.6 pF	1.4	7.8 pF	7.5 pF
150 nH	1.4	210 nH	220 nH
15 pF + 1 pF[1] = 16 pF	1.4	22.4 pF − 1 pF[1] = 21.4 pF	22 pF

[1] Input capacitance of the AD8120.

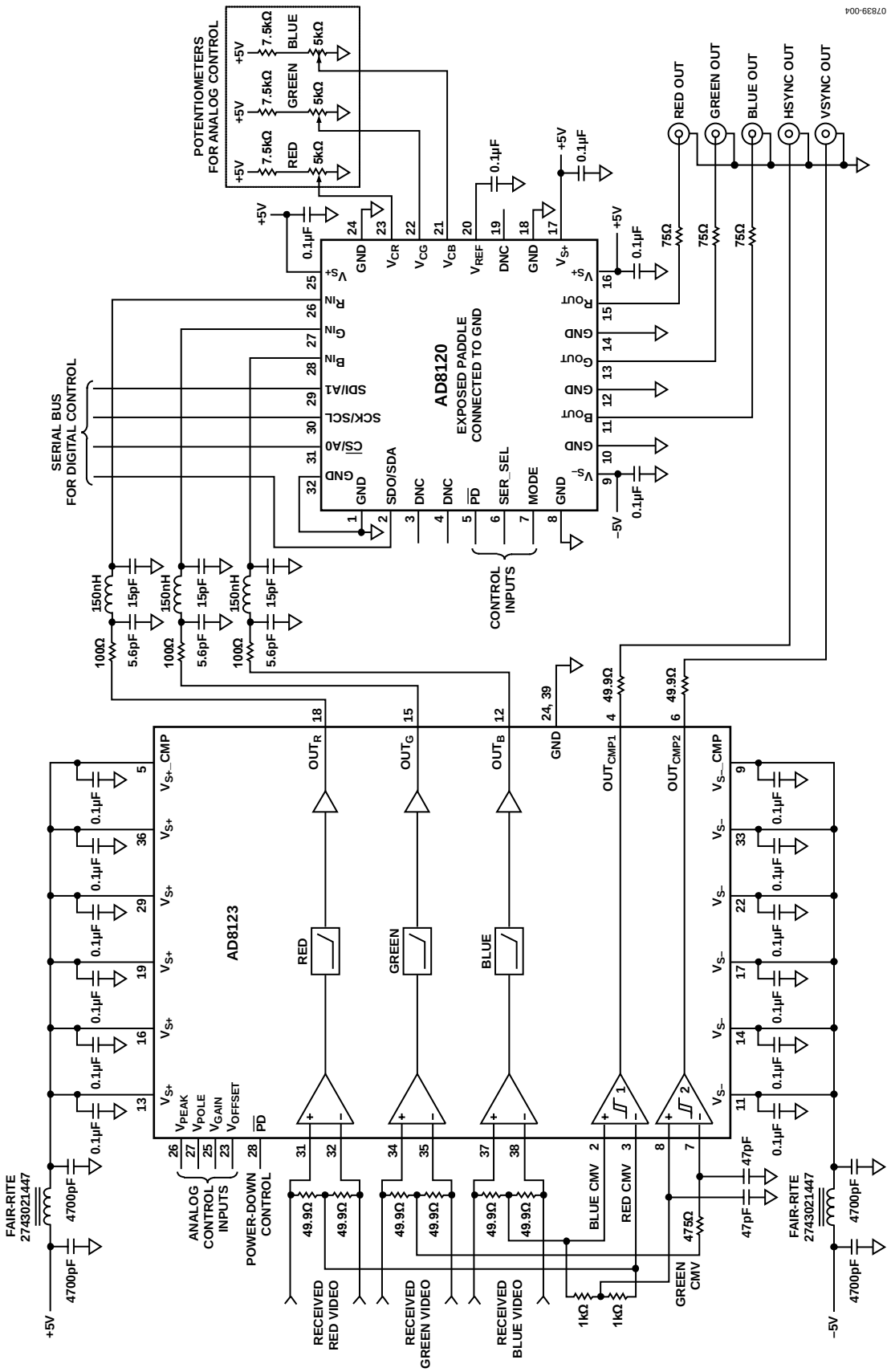
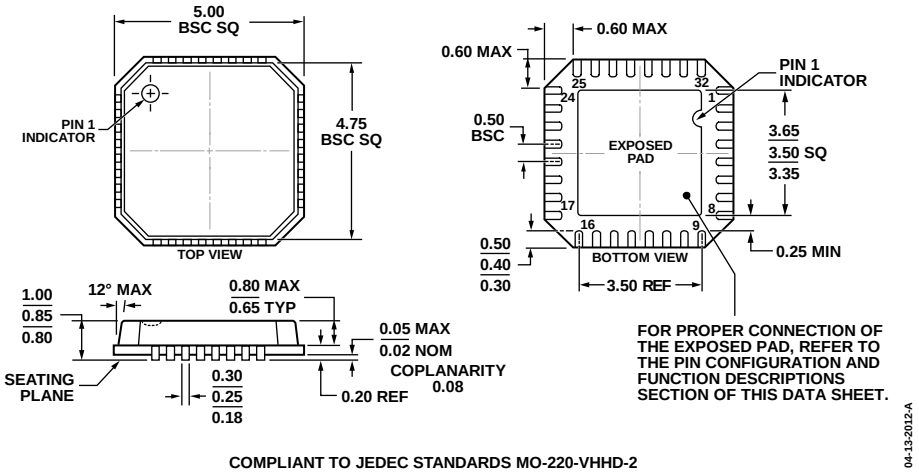


Figure 25. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 26. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8120ACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-4
AD8120ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-4
AD8120ACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-4

[1] Z = RoHS Compliant Part.