ADV7280/ADV7281/ADV7282 Hardware Reference Manual
UG-637

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ADV7280/ADV7281/ADV7282 Functionality and Features

OVERVIEW

This user guide provides a detailed description of the functionality and features of the ADV7280, ADV7280-M, ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M video decoders. Table 1 list the shorthand notations used for these decoders in this user guide.

The ADV7280, ADV7280-M, ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M automatically detect and convert standard composite analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards. These video recorders accept composite video signals (CVBS) as well as S-Video (YC) and YPbPr video signals, supporting a wide range of consumer and automotive video sources. The ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models can also accept pseudo differential and true differential CVBS inputs.

The ADV7282x-T models (ADV7280, ADV7281, and ADV7282) convert the analog video inputs into a YCrCb 4:2:2 component video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard.

The ADV728x-M models (ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M) convert the analog video inputs into an 8-bit YcrCb 4:2:2 video stream, and that is output over an MIPI CSI-2 interface. This MIPI CSI-2 output interface connects to a wide range of video processors and FPGAs.

The AGC and clamp-restore circuitry allow an input video signal peak-to-peak range to 1.0 V at the analog video input pin of the ADV728x. Alternatively, these can be bypassed for manual settings.

AC coupling of the input video signals provides STB protection. On the ADV7281, ADV7281-M, ADV7282, and ADV7282-M models, short-to-battery (STB) diagnostics can be carried out on two input video signals.

The ADV728x is programmed via a two-wire, serial, bidirectional port ($I^2C^®$ compatible). The ADV728x supports a number of functions including 8-bit to 6-bit down dither mode and adaptive contrast enhancement (ACE).

The advanced interlaced-to-progressive (I2P) function allows the ADV7280, ADV7280-M, ADV7282, and ADV7282-M to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. Edge adaptive technology is used to minimize video defects on low angle lines.

The ADV728x is fabricated in a 1.8 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV728x are available in −40°C to +85°C temperature range models. This makes the ADV728x ideal for automotive applications.

See Table 6 for a descriptive list of these video decoder models.

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REVISION HISTORY

5/14—Revision 0: Initial Version

USING THIS HARDWARE REFERENCE GUIDE

GENERIC SHORTHAND NOTATIONS

Table 1. Shorthand Notations

Notation	Description
ADV728x	Refers to the ADV7280, ADV7280-M, ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models
ADV728x-T	Refers to the ADV7280, ADV7281, and ADV7282 models
ADV728x-M	Refers to the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M models

NUMBER NOTATIONS

Table 2. Number Notations

Notation	Description
Bit N	Bits are numbered in little endian format, that is, the least significant bit of a number is referred to as Bit 0.
V[X:Y]	Bit field representation covering Bit X to Bit Y of a value or a field (V).
0xNN	Hexadecimal (Base 16) numbers are preceded by the prefix 0x.
0bNN	Binary (Base 2) numbers are preceded by the prefix 0b.
NN	Decimal (Base 10) are represented using no additional prefixes or suffixes.

REGISTER ACCESS CONVENTIONS

Table 3. Register Access Conventions

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only. A read always returns 0 unless otherwise specified.
W	Memory location is write access only.

ACRONYMS AND ABBREVIATIONS

Table 4. Acronyms and Abbreviations

Acronym/ Abbreviation	Description
AA	Anti-alias
ACE	Adaptive contrast enhancement
ADC	Analog-to-digital converter
AFE	Analog front end
AGC	Automatic gain control
AIN	Analog video input pin
CMR	Common-mode rejection
CVBS	Composite video baseband signal
AVI	Auxiliary video information
DE	Data enable
GPO	General-purpose output
HS	Horizontal synchronization
I2P	Interlaced-to-progressive converter (that is, deinterlacer)
IC	Integrated circuit
I^2C	Inter integrated circuit
LLC	Line locked clock
LSB	Least significant bit
Mbps	Megabits per second
ms	Millisecond
MSB	Most significant bit
MIPI CSI-2	Mobile industry processor interface camera serial interface, version 2
NC	No connect
PLL	Phase-locked loop
Rx	Receiver
SAV	Start of active video
SFL	Color subcarrier frequency lock
SHA	Sample-and-hold
SNR	Signal-to-noise ratio
STB	Short-to-battery
TTL	Transistor-to-transistor level
Tx	Transmitter
VBI	Vertical blanking interval
VS	Vertical synchronization
XTAL	Crystal oscillator

FIELD FUNCTION DESCRIPTIONS

Throughout this reference manual, a series of function tables are provided. The function of a field is described in a table preceded by the bit name, a short function description, the I²C map, the register location within the I²C map, and a detailed description of the field.

The detailed description consists of:

- the values the field can take (for a readable field)
- the values the field can be set to (for a writable field)

Example Field Function Description

This section provides an example of a field function table followed by a description of each part of the table.

DIAG1_SLICE_LEVEL[2:0], User Sub Map, Address 0x5D[4:2]

The DIAG1_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG1 pin.

Table 5. DIAG1_SLICE_LEVEL[2:0] Settings

DIAG1_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

In this example

- The name of the field is **DIAG1_SLICE_LEVEL** and it is three bits long.
- **User Sub Map** indicates which I²C map or sub map the field is located in.
- Address **0x5D** is the I²C location of the field within the I²C Map or Sub Map. The address is stated in a big endian format (MSB first, LSB last).
- The address is followed by a description of the field.
- The first column of the table lists values the field can take or can be set to. These values are in binary format if not preceded by 0x or in hexadecimal format if preceded by 0x.
- The second column of the table describes the operation of the field (such as DIAG1_SLICE_LEVEL) for each value the field can be set to.

VIDEO DECODER MODELS

Table 6 lists the Analog Devices, Inc., video decoders described in this reference manual. Select columns are described in full in the sections that follow.

Table 6. Description of ADV728x Models

Model Number	Generic Shorthand Notation	Video Input Pins	Differential AFE	Output Format	Diagnostic Pins	GPO Pins	Sync Output Pins	ACE	I2P	Package
ADV7280	ADV728x-T	4	No	TTL	No	No	Yes (2)	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7281	ADV728x-T	4	Yes	TTL	Yes (2)	No	No	Yes	No	32-lead LFCSP, 5 mm × 5 mm
ADV7282	ADV728x-T	4	Yes	TTL	Yes (2)	No	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7280-M	ADV728x-M	8	No	MIPI CSI-2	No	Yes (3)	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm
ADV7281-M	ADV728x-M	6	Yes	MIPI CSI-2	Yes (2)	Yes (3)	No	Yes	No	32-lead LFCSP, 5 mm × 5 mm
ADV7281-MA	ADV728x-M	8	Yes	MIPI CSI-2	No	Yes (3)	No	Yes	No	32-lead LFCSP, 5 mm × 5 mm
ADV7282-M	ADV728x-M	6	Yes	MIPI CSI-2	Yes (2)	Yes (3)	No	Yes	Yes	32-lead LFCSP, 5 mm × 5 mm

VIDEO INPUT PINS COLUMN

Indicates how many analog video inputs pins are available on each ADV728x model.

- One analog video input pin is required for single-ended CVBS inputs.
- Two analog video input pins are required for pseudo differential and fully differential CVBS inputs.
- Two analog video input pins are required for S-Video (YC) inputs.
- Three analog video input pins are required for component (YPbPr) inputs.

DIFFERENTIAL AFE COLUMN

Indicates if the ADV728x model has a differential analog front end (AFE). A differential AFE is needed to process pseudo differential and fully differential CVBS inputs.

OUTPUT FORMAT COLUMN

Indicates the digital video output format output from each ADV728x model.

- TTL means that the ADV728x model outputs 8-bit YUV video data over a TTL bus.
- MIPI CSI-2 indicates that the ADV728x model outputs 8-bit YUV video data over a MIPI CSI-2 bus. This MIPI CSI-2 bus consists of one differential data channel (D0P, D0N) and one differential clock channel (CLKP, CLKN).

DIAGNOSTIC PINS COLUMN

Indicates if the ADV728x model has diagnostic pins and, if so, how many. Diagnostic pins are used to monitor analog video input lines for short-to-battery (STB) events.

GPO PINS COLUMN

Indicates if the ADV728x model has general-purpose output (GPO) pins and, if so, how many. GPO pins are outputs from the ADV728x that can be used to control other external devices.

SYNC OUTPUT PINS COLUMN

Indicates if the video decoder has synchronization output pins and, if so, how many. Examples of synchronization output pins include horizontal synchronization (HS), vertical synchronization(VS), and subcarrier frequency lock (SFL).

ACE COLUMN

Indicates if the ADV728x model has the ability to perform the adaptive contrast enhancement (ACE) function.

The ACE function allows dark areas of the video to be brightened up without saturating bright areas. This is useful for automotive applications.

I2P COLUMN

Indicates if the ADV728x model has an in-built interlaced-to-progressive converter (I2P). This is also known as a deinterlacer. The I2P core converts the interlaced video formats of NTSC (480i) or PAL (576i) into progressive standards (480p, 576p).

PACKAGE COLUMN

Indicates the package in which the video decoder is available.

FUNCTIONAL BLOCK DIAGRAMS

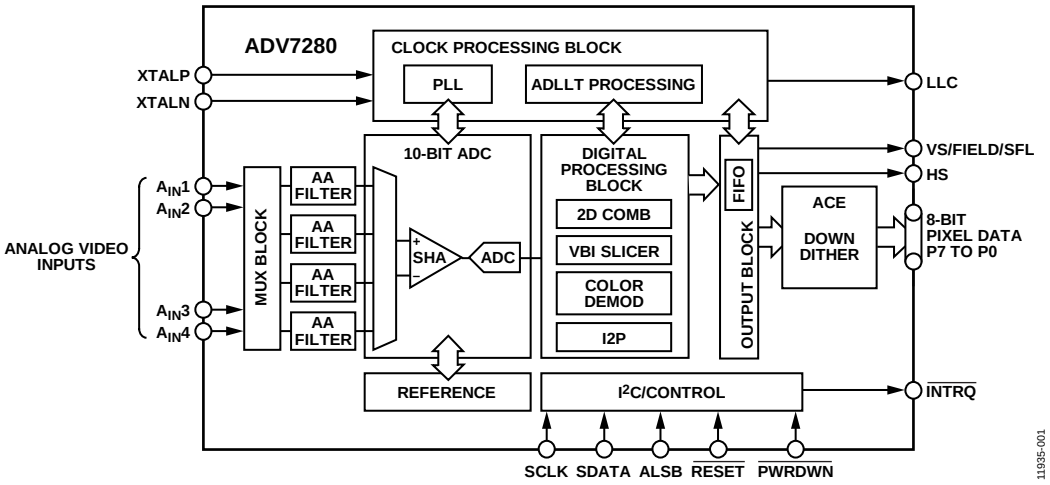

Figure 1. ADV7280 Functional Block Diagram

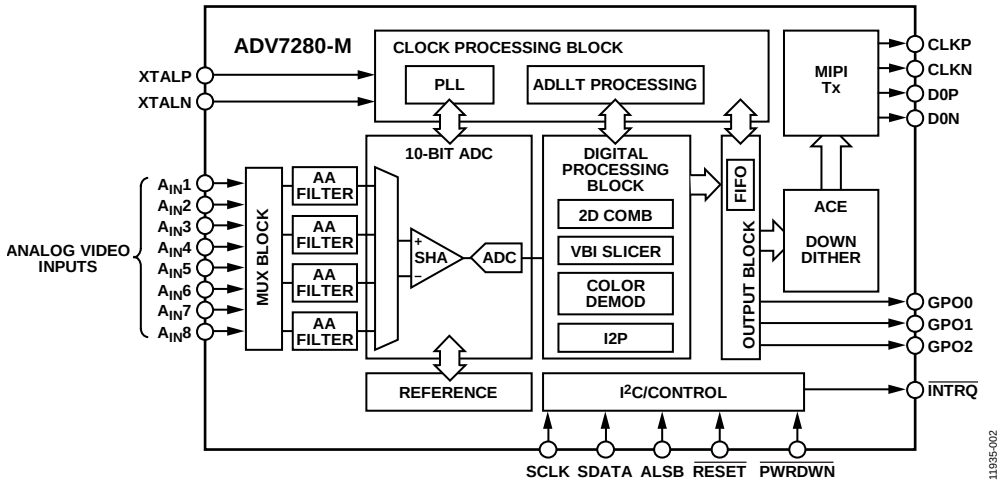

Figure 2. ADV7280-M Functional Block Diagram

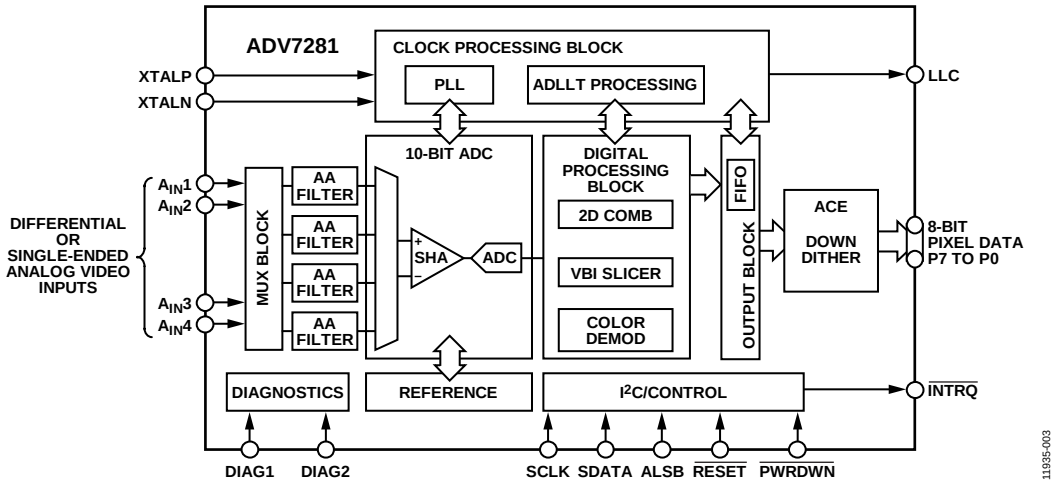

Figure 3. ADV7281 Functional Block Diagram

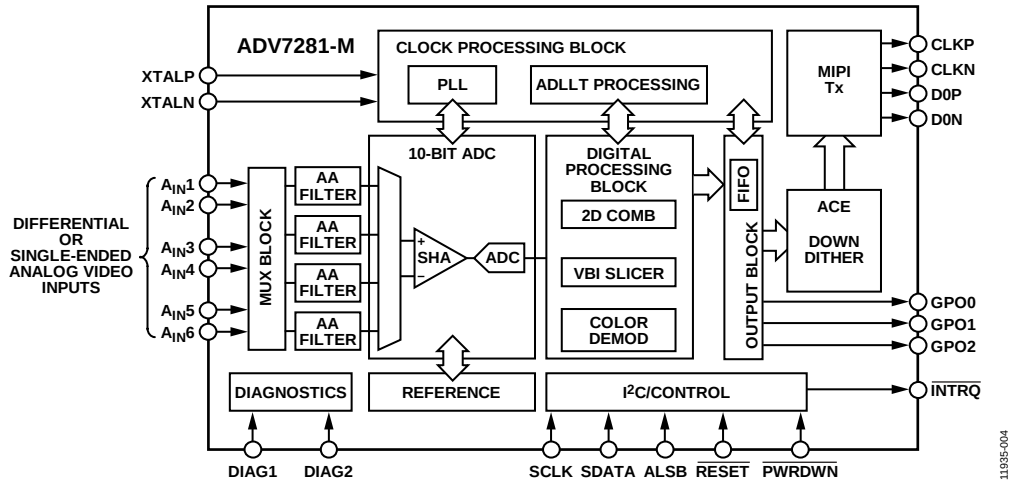

Figure 4. ADV7281-M Functional Block Diagram

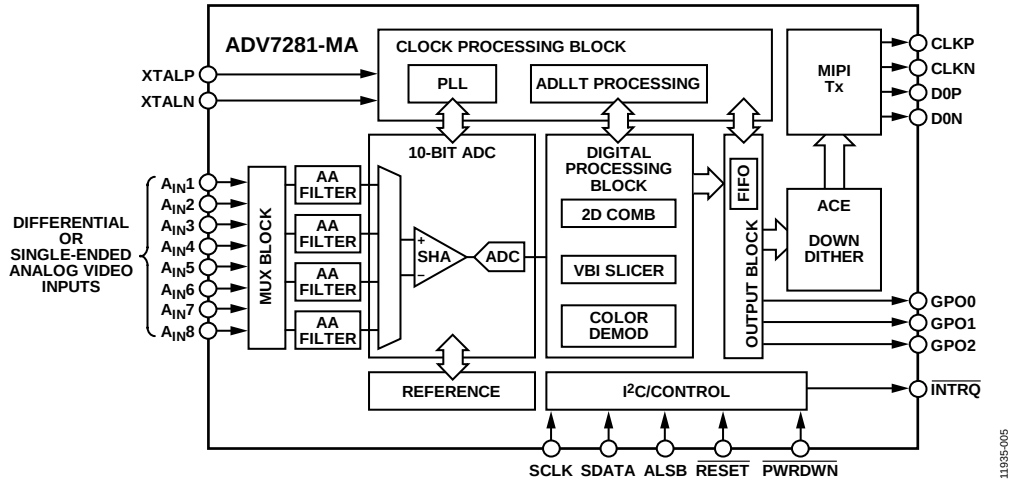

Figure 5. ADV7281-MA Functional Block Diagram

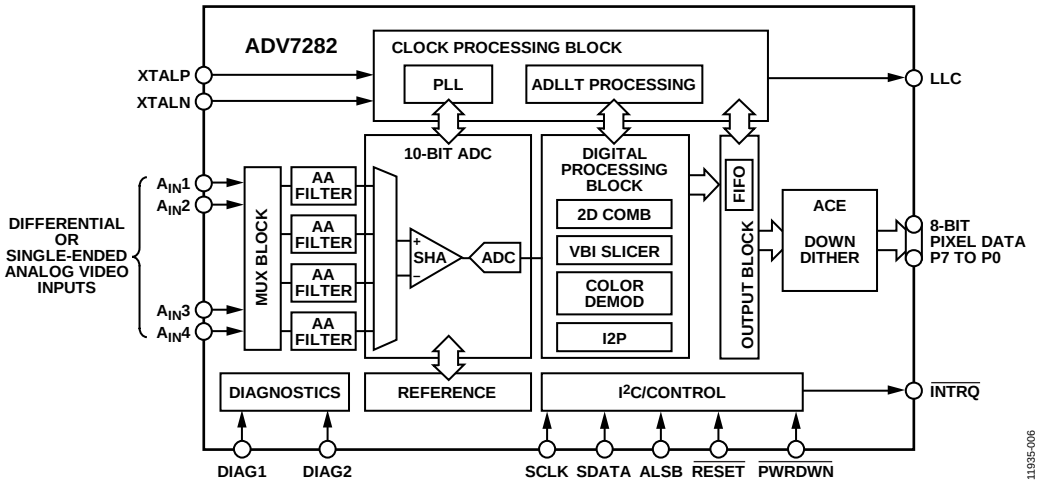

Figure 6. ADV7282 Functional Block Diagram

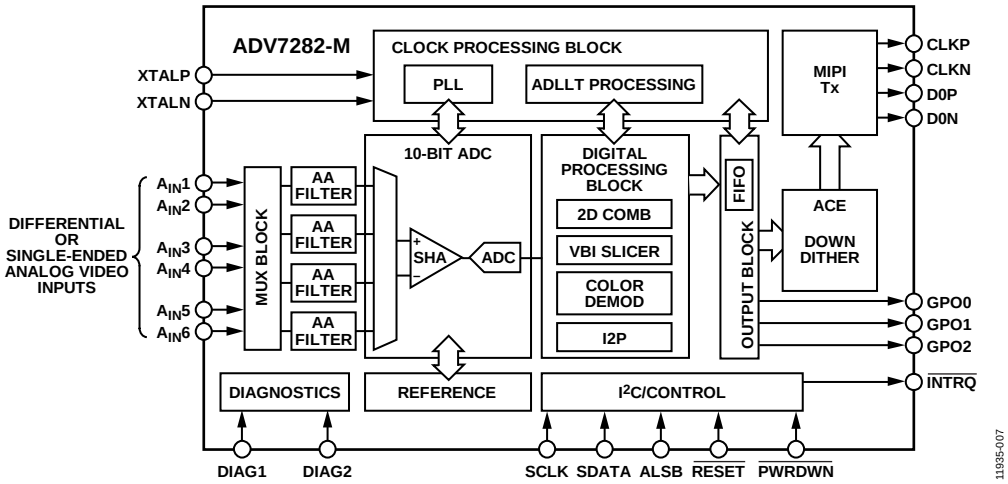

Figure 7. ADV7282-M Functional Block Diagram

GENERAL DESCRIPTION

OVERVIEW OF ANALOG FRONT END

The ADV728x AFE consists of a single high speed, 10-bit analog-to-digital converter (ADC) that digitizes the analog video signal before applying it to the standard definition processor.

The front end also includes a four-channel input mux that enables multiple composite video signals to be applied to the ADV728x. Clamp restore circuitry is positioned in front of the ADC to ensure that the video signal remains within the range of the converter. An external resistor and capacitor circuit is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see the

Input Networks section). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV728x.

Table 7 shows the three ADC clocking rates that are determined by the video input format to be processed—that is, INSEL[4:0]. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPbPr modes.

Table 7. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)	114	4×
YPbPr	172	4×

[1] Based on a 28.63636 MHz crystal between the XTAL and XTAL1 pins.

OVERVIEW OF STANDARD DEFINITION PROCESSOR

The ADV728x is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The ADV7281, ADV7281-M, ADV7281-MA, ADV7282 and ADV7282-M are also capable of receiving pseudo-differential and fully differential CVBS inputs. The video standards supported by the video processor include PAL B/D/I/G/H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV728x can automatically detect the video standard and process it accordingly.

The ADV728x has a five-line, adaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls, such as brightness, contrast, saturation, and hue, are also available with these video decoders.

The ADV728x implements a patented ADLLT™ algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV728x to track and decode poor quality video sources, such as VCRs and noisy sources, from tuner outputs and camcorders. The ADV728x contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

ACE offers improved visual detail using an algorithm to automatically vary contrast levels in order to enhance picture detail. This increases the brightness of dark regions of an image without saturating bright areas of the image.

Down dithering converts the output of the ADV728x from an 8-bit output to a 6-bit output.

The I2P block on the ADV7280, ADV7280-M, ADV7282, and ADV7282-M converts the interlaced video input into a progressive video output. This is done without a need for external memory.

The ADV728x can process a variety of vertical blanking interval (VBI) data services, such as closed captioning (CCAP), widescreen signaling (WSS), and copy generation management systems (CGMS). VBI data is transmitted as ancillary data packets.

The ADV728x is fully Rovi (previously Macrovision) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Rovi signal inputs.

INPUT NETWORKS

An input network (external resistor and capacitor circuit) is required on the $A_{IN}x$ input pins of the ADV728x. The components of the input network depend on the video format selected for the analog input.

SINGLE-ENDED INPUT NETWORK

Figure 8 shows the input network to use on each $A_{IN}x$ input pin of the ADV728x when any of the following video input formats are used:

- Single-ended CVBS
- YC (S-Video)
- YPrPb

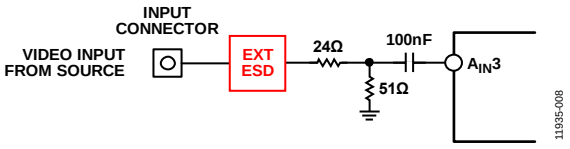

Figure 8. Single-Ended Input Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the ADV728x. This allows an input range to the ADV728x of up to 1.47 V peak-to-peak. Note that amplifiers within the ADC restore the amplitude of the input signal so that signal-to-noise ratio (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the $A_{IN}x$ pin of the ADV728x. The clamping circuitry within the ADV728x restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV728x.

The 100 nF ac coupling capacitor limits the current flow into the ADV728x during short-to-battery (STB) events. Note that the 24 Ω and 51 Ω resistors can be damaged during STB events unless high power resistors are used. To avoid the need for high power resistors, use the differential input network described in the Differential Input Network section.

DIFFERENTIAL INPUT NETWORK

This section applies to the ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models only.

Figure 9 shows the input network to use when pseudo differential or fully differential CVBS video is input on the $A_{IN}x$ input pins.

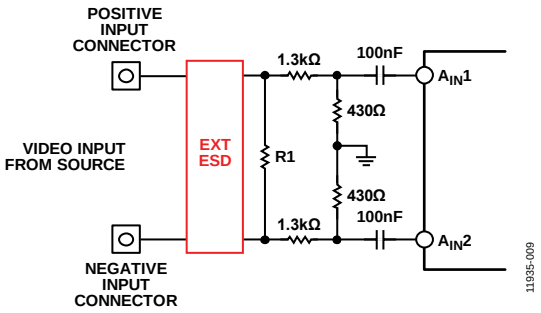

Figure 9. Differential Input Network

Fully differential video transmission involves transmitting two complementary CVBS signals. Pseudo differential video transmission involves transmitting a CVBS signal and a source ground signal.

Differential video transmission has several key advantages over single-ended transmission, including the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

Resistor R1 provides the RF end termination for the differential CVBS input lines. For a pseudo differential CVBS input, R1 should have a value of 75 Ω. For a fully differential CVBS input, R1 should have a value of 150 Ω.

The 1.3 kΩ and 430 Ω resistors create a resistor divider with a gain of 0.25. The resistor divider attenuates the amplitude of the input analog video, but increases the input common-mode range to 4 V peak-to-peak. Note that amplifiers within the ADC restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the $A_{IN}x$ pin. The clamping circuitry within the part restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the part.

The 100 nF ac coupling capacitors limit the current flow into the ADV7281/ADV7281-M/ADV7281-MA/ADV7282/ADV7282-M during STB events. The 1.3 kΩ and 430 Ω resistors are sized in order to withstand STB events.

To achieve optimal performance, the 1.3 kΩ and 430 Ω resistors should be closely matched; that is, all 1.3 kΩ and 430 Ω resistors should have the same resistance tolerance, and this tolerance should be as low as possible.

SHORT-TO-BATTERY (STB) DIAGNOSTICS

Short-to-battery (STB) diagnostic pins are only available on the ADV7281, ADV7281-M, ADV7282, and ADV7282-M models.

The input circuitry of all ADV728x models are protected against STB events by ac coupling capacitors. In single-ended CVBS, YC, and YPbPr modes, the inputs network resistors need to have high power ratings in order to be robust to STB events. However the input network resistors for differential CVBS are sized to reduce the current flow during an STB event, thus low power rated resistors can be used and remain robust to STB events. The R1 resistor is protected because no current or limited current flows through it during an STB event. See the Differential Input Network section.

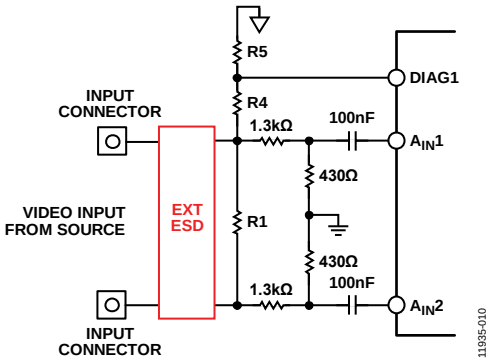

Figure 10. Diagnostic Connections

The ADV7281/ADV7281-M/ADV7282/ADV7282-M senses an STB event via the DIAG1 and DIAG2 pins. The DIAG1 and DIAG2 pins can sense an STB event on either the positive or negative differential input because of the negligible voltage drop across Resistor R1.

Resistors R4 and R5 divide down the voltage at the input connector to protect the DIAGx pin from an STB event. The DIAGx pin circuitry compares this voltage to a programmable reference voltage, known as the diagnostic slice level. When the diagnostic slice level is exceeded, an STB event has occurred.

When the DIAGx pin voltage exceeds the diagnostic slice level voltage, a hardware interrupt is triggered and indicated by the $\overline{\text{INTRQ}}$ pin. A readback register is also provided, which allows the user to determine the DIAGx pin on which the STB event occurred.

Use Equation 1 to find the trigger voltage for a selected diagnostic slice level.

$$V_{STB\_TRIGGER} = \frac{R5+R4}{R5} \times DIAGNOSTIC\_SLICE\_LEVEL \quad (1)$$

where:

$V_{STB\_TRIGGER}$ is the minimum voltage required at the input connector to trigger the STB interrupt on the ADV7282-M.

DIAGNOSTIC_SLICE_LEVEL is the programmable reference voltage.

PROGRAMMING DIAGNOSTIC SLICE LEVELS

DIAG1 Pin

DIAG1_SLICER_PWRDN, User Sub Map, Address 0x5D[6]

This bit powers up or powers down the diagnostic circuitry for the DIAG1 pin.

Table 8. DIAG1_SLICER_PWRDN Function

DIAG1_SLICER_PWRDN	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG1 pin.
1 (default)	Power down the diagnostic circuitry for the DIAG1 pin.

DIAG1_SLICE_LEVEL[2:0], User Sub Map, Address 0x5D[4:2]

The DIAG1_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG1 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG1 pin, an STB interrupt is triggered.

For the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG1 pin must be powered up (see Table 8).

Table 9. DIAG1_SLICE_LEVEL[2:0] Settings

DIAG1_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

DIAG2 Pin

DIAG2_SLICER_PWRDN, User Sub Map, Address 0x5E[6]

This bit powers up or powers down the diagnostic circuitry for the DIAG2 pin.

Table 10. DIAG2_SLICER_PWRDN Function

DIAG2_SLICER_PWRDN	Diagnostic Slice Level
0	Power up the diagnostic circuitry for the DIAG2 pin.
1 (default)	Power down the diagnostic circuitry for the DIAG2 pin.

DIAG2_SLICE_LEVEL[2:0], User Sub Map, Address 0x5E[4:2]

The DIAG2_SLICE_LEVEL[2:0] bits allow the user to set the diagnostic slice level for the DIAG2 pin. When a voltage greater than the diagnostic slice level is seen on the DIAG2 pin, an STB interrupt is triggered.

For the diagnostic slice level to be set correctly, the diagnostic circuitry for the DIAG2 pin must be powered up (see Table 10).

Table 11. DIAG2_SLICE_LEVEL[2:0] Settings

DIAG2_SLICE_LEVEL[2:0]	Diagnostic Slice Level
000	75 mV
001	225 mV
010	375 mV
011 (default)	525 mV
100	675 mV
101	825 mV
110	975 mV
111	1.125 V

ANALOG FRONT END

INPUT CONFIGURATION

The following two steps are key for configuring the ADV728x to correctly decode the input video.

1. Use INSEL[4:0] to configure the routing and format decoding (CVBS, Y/C, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. The standard definition processor block, which decodes the digital data, should be configured to process the CVBS, Y/C, or YPrPb format. This is performed by the INSEL[4:0] selection.

INSEL[4:0], Input Control, Address 0x00[4:0]

The INSEL bits allow the user to select the input format. They also configure the standard definition processor core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format.

INSEL[4:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 12). This allows the user to route the various video signal types to the decoder and select them using INSEL[4:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 12. INSEL[4:0]

INSEL [4:0]	Video Format	Analog Input for ADV7280	Analog Input for ADV7280-M	Analog Input for ADV7281 and ADV7282	Analog Input for ADV7281-M and ADV7282-M	Analog Input for ADV7281-MA
00000	CVBS	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$	CVBS input on $A_{IN}3$	Reserved	CVBS input on $A_{IN}3$	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$	CVBS input on $A_{IN}4$	Reserved	CVBS input on $A_{IN}4$	CVBS input on $A_{IN}4$
00100	CVBS	Reserved	CVBS input on $A_{IN}5$	Reserved	Reserved	CVBS input on $A_{IN}5$
00101	CVBS	Reserved	CVBS input on $A_{IN}6$	Reserved	Reserved	CVBS input on $A_{IN}6$
00110	CVBS	Reserved	CVBS input on $A_{IN}7$	CVBS input on $A_{IN}3$	CVBS input on $A_{IN}5$	CVBS input on $A_{IN}7$
00111	CVBS	Reserved	CVBS input on $A_{IN}8$	CVBS input on $A_{IN}4$	CVBS input on $A_{IN}6$	CVBS input on $A_{IN}8$
01000	Y/C (S-Video)	Y input on $A_{IN}1$, C input on $A_{IN}2$	Y input on $A_{IN}1$, C input on $A_{IN}2$	Y input on $A_{IN}1$, C input on $A_{IN}2$	Y input on $A_{IN}1$, C input on $A_{IN}2$	Y input on $A_{IN}1$, C input on $A_{IN}2$
01001	Y/C (S-Video)	Y input on $A_{IN}3$, C input on $A_{IN}4$	Y input on $A_{IN}3$, C input on $A_{IN}4$	Reserved	Y input on $A_{IN}3$, C input on $A_{IN}4$	Y input on $A_{IN}3$, C input on $A_{IN}4$
01010	Y/C (S-Video)	Reserved	Y input on $A_{IN}5$, C input on $A_{IN}6$	Reserved	Reserved	Y input on $A_{IN}5$, C input on $A_{IN}6$
01011	Y/C (S-Video)	Reserved	Y input on $A_{IN}7$, C input on $A_{IN}8$	Y input on $A_{IN}3$, C input on $A_{IN}4$	Y input on $A_{IN}5$, C input on $A_{IN}6$	Y input on $A_{IN}7$, C input on $A_{IN}8$
01100	YPrPb	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	Reserved[1]	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$
01101	YPrPb	Reserved	Y input on $A_{IN}4$, Pb input on $A_{IN}5$, Pr input on $A_{IN}6$	Reserved[1]	Reserved	Y input on $A_{IN}4$, Pb input on $A_{IN}5$, Pr input on $A_{IN}6$
01110	Differential CVBS	Reserved	Reserved	Positive on $A_{IN}1$, Negative on $A_{IN}2$	Positive on $A_{IN}1$, Negative on $A_{IN}2$	Positive on $A_{IN}1$, Negative on $A_{IN}2$
01111	Differential CVBS	Reserved	Reserved	Reserved	Positive on $A_{IN}3$, Negative on $A_{IN}4$	Positive on $A_{IN}3$, Negative on $A_{IN}4$
10000	Differential CVBS	Reserved	Reserved	Reserved	Reserved	Positive on $A_{IN}5$, Negative on $A_{IN}6$
10001	Differential CVBS	Reserved	Reserved	Positive on $A_{IN}3$, Negative on $A_{IN}4$	Positive on $A_{IN}5$, Negative on $A_{IN}6$	Positive on $A_{IN}7$, Negative on $A_{IN}8$
10010 to 11111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

[1]Note that it is possible for the ADV7281/ADV7282 to receive YPbPr formats; however, a manual muxing scheme is required. In this case luma(Y) is fed in on $A_{IN}1$ or $A_{IN}3$, blue chroma (Pb) is fed in on $A_{IN}4$ and red chroma (Pr) is fed in on $A_{IN}2$. See the Manual Muxing Mode section for more information.

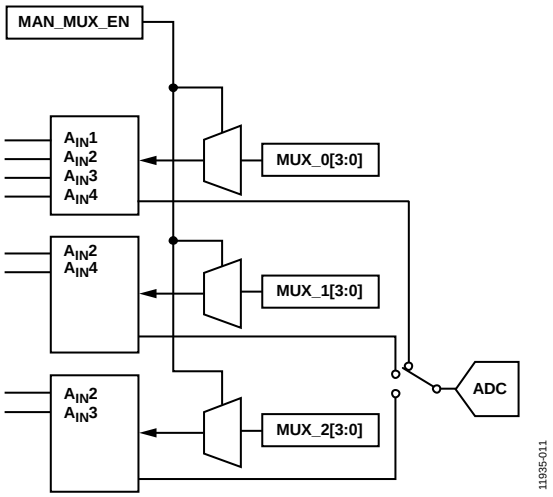

Figure 11. Manual Muxing Scheme for ADV7280

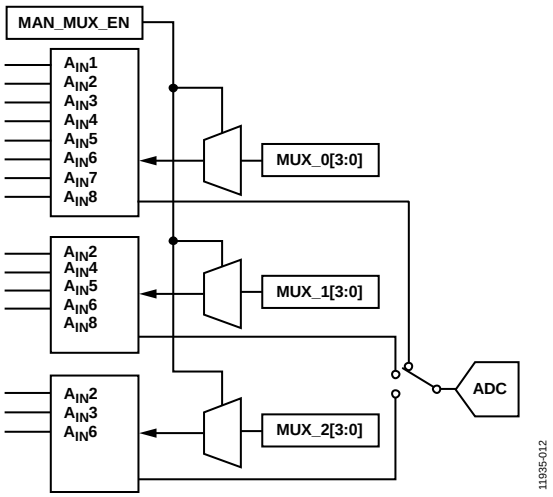

Figure 12. Manual Muxing Scheme for ADV7280-M

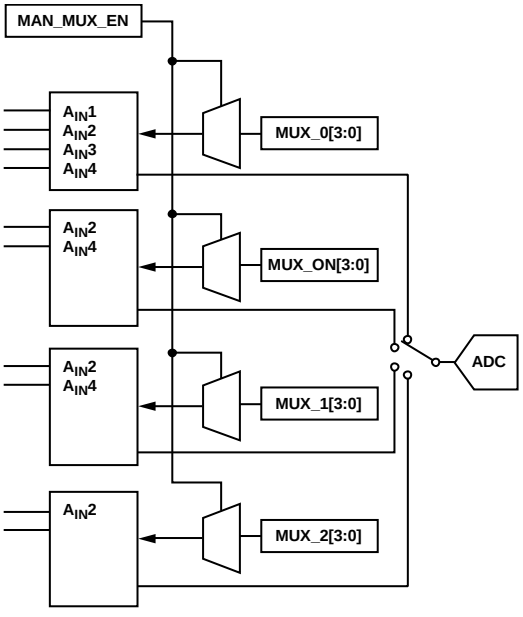

Figure 13. Manual Muxing Scheme for ADV7281 and ADV7282

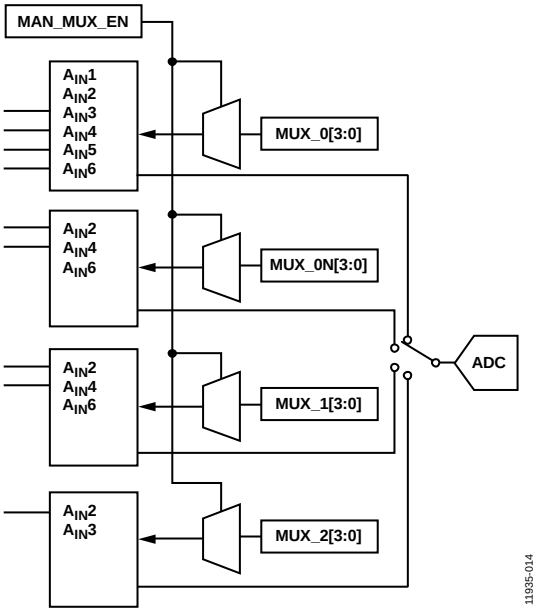

Figure 14. Manual Muxing Scheme for ADV7281-M and ADV7282-M

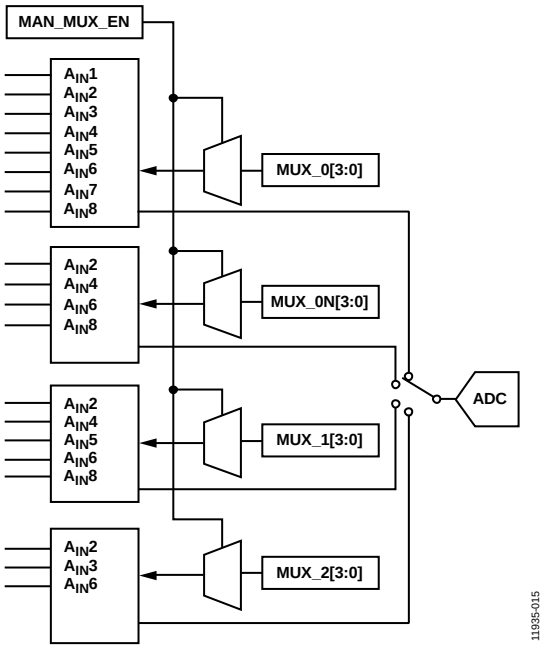

Figure 15. Manual Muxing Scheme for ADV7281-MA

MANUAL MUXING MODE

In manual muxing mode, the user selects the analog input pin (for example, $A_{IN}1$, $A_{IN}2$, and so on) that is to be processed by the ADC of the ADV728x. MAN_MUX_EN (User Map, Register 0xC4, Bit 7) must be set to 1 to enable the following muxing blocks:

- MUX0[3:0], ADC mux configuration, Address 0xC3[3:0]
- MUX0N[3:0], ADC mux configuration, Address 0x60[3:0] (MUX0N[3:0] applies only to the ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models)
- MUX1[3:0], ADC mux configuration, Address 0xC3[7:4]
- MUX2[3:0], ADC mux configuration, Address 0xC4[3:0]

The four mux sections are controlled by the signal buses, MUX0/MUX0N/MUX2/MUX3[2:0].

The tables in this section explain the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX0. For example, in a Y/C input configuration, connect MUX0 to the Y channel and MUX1 to the C channel.

MUX0N is only used to process the negative input for fully differential or pseudo differential CVBS inputs.

When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers should be powered down (see the description of Register 0x3A in the User Map in Table 95).

Note that MUX0N cannot be powered down independently. MUX0N can only be powered down when MUX0, MUX1, and MUX2 are all powered down.

Manual Muxing of the ADV7280

Table 13 shows the settings for manual muxing of the ADV7280.

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7).
- CVBS can only be processed by MUX0.
- Y/C can only be processed by MUX0 and MUX1. MUX0 processes the luma (Y) and MUX1 processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX0(Y), MUX1(Pb), and MUX2(Pr).

Manual Muxing of the ADV7280-M

Table 14 shows the settings for manual muxing of the ADV7280-M.

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7).
- CVBS can only be processed by MUX0.
- Y/C can only be processed by MUX0 and MUX1. MUX0 processes the luma (Y) and MUX1 processes the chroma (C).

Component (YPbPr) signals can only be processed by MUX0(Y), MUX1(Pb), and MUX2(Pr).

Table 13. Manual Mux Settings for ADC of ADV7280

MUX0[3:0]	ADC Connection	MUX1[3:0]	ADC Connected To	MUX2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101 to 1111	No connect	0101 to 1111	No connect	0101 to 1111	No connect

Table 14. Manual Mux Settings for ADC of ADV7280-M

MUX0[3:0]	ADC Connection	MUX1[3:0]	ADC Connection	MUX2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101	$A_{IN}5$	0101	$A_{IN}5$	0101	No connect
0110	$A_{IN}6$	0110	$A_{IN}6$	0110	$A_{IN}6$
0111	$A_{IN}7$	0111	No connect	0111	No connect
1000	$A_{IN}8$	1000	$A_{IN}8$	1000	No connect
1001-1111	No connect	1001-1111	No connect	1001-1111	No connect

Manual Muxing of the ADV7281 and ADV7282

Table 16 shows the settings for manual muxing of the ADV7281 and ADV7282.

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7)
- CVBS can only be processed by MUX0.
- Differential CVBS can only be processed by MUX0 (positive channel) and MUX0N (negative channel).
- Y/C can only be processed by MUX0 and MUX1. MUX0 processes the luma (Y) and MUX1 processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX0(Y), MUX1(Pb), and MUX2(Pr). For example, Y can be fed in on $A_{IN}1$ or $A_{IN}3$ for MUX0. Pb can be fed in on $A_{IN}4$ for MUX1. Pr can be fed in on $A_{IN}2$ for MUX2. Table 15 gives an example of how to program the ADV7281/ADV7282 to accept YPrPb inputs.

Table 15. Register Writes to Program the ADV7281 or ADV7282 to Accept YPbPr Input

Register Map	Register Address	Register Write	Description
User Map (0x40 or 0x42)	0x00	0x0C	Program INSEL for YPbPr input.
	0xC3	0x87	Program manual muxing. Y is fed in on $A_{IN}3$ for MUX0. Pb is fed in on $A_{IN}4$ for MUX1.
	0xC4	0x82	Enable manual muxing. Pr is fed in on $A_{IN}2$ for MUX2.

Table 16. Manual Mux Settings for ADC of ADV7281 and ADV7282

MUX0[3:0]	ADC Connection	MUX0N[3:0]	ADC Connection	MUX1[3:0]	ADC Connection	MUX2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	No connect	0011	No connect	0011	No connect	0011	No connect
0100	No connect	0100	No connect	0100	No connect	0100	No connect
0101	No connect	0101	No connect	0101	No connect	0101	No connect
0110	No connect	0110	No connect	0110	No connect	0110	No connect
0111	$A_{IN}3$	0111	No connect	0111	No connect	0111	No connect
1000	$A_{IN}4$	1000	$A_{IN}4$	1000	$A_{IN}4$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

Manual Muxing of the ADV7281-M and ADV7282-M

Table 17 shows the settings for manual muxing of the ADV7281-M and ADV7282-M.

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7)
- CVBS can only be processed by MUX0.
- Differential CVBS can only be processed by MUX0 (positive channel) and MUX0N (negative channel).
- Y/C can only be processed by MUX0 and MUX1. MUX0 processes the luma (Y) and MUX1 processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX0(Y), MUX1(Pb), and MUX2(Pr).

Table 17. Manual Mux Settings for ADC of ADV7281-M and ADV7282-M

MUX0[3:0]	ADC Connection	MUX0N[3:0]	ADC Connection	MUX1[3:0]	ADC Connection	MUX2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101	No connect	0101	No connect	0101	No connect	0101	No connect
0110	No connect	0110	No connect	0110	No connect	0110	No connect
0111	$A_{IN}5$	0111	No connect	0111	No connect	0111	No connect
1000	$A_{IN}6$	1000	$A_{IN}6$	1000	$A_{IN}6$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

Manual Muxing of the ADV7281-MA

Table 18 shows the settings for manual muxing of theADV7281-MA.

- MAN_MUX_EN must be set to 1 (User Map, Register 0xC4, Bit 7).
- CVBS can only be processed by MUX0.
- Differential CVBS can only be processed by MUX0 (positive channel) and MUX0N (negative channel).
- Y/C can only be processed by MUX0 and MUX1. MUX0 processes the luma (Y) and MUX1 processes the chroma (C).
- Component (YPbPr) signals can only be processed by MUX0(Y), MUX1(Pb), and MUX2(Pr).

Table 18. Manual Mux Settings for ADC of ADV7281-MA

MUX0[3:0]	ADC Connection	MUX0N[3:0]	ADC Connection	MUX1[3:0]	ADC Connection	MUX2[3:0]	ADC Connection
0000	No connect	0000	No connect	0000	No connect	0000	No connect
0001	$A_{IN}1$	0001	No connect	0001	No connect	0001	No connect
0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$	0010	$A_{IN}2$
0011	$A_{IN}3$	0011	No connect	0011	No connect	0011	$A_{IN}3$
0100	$A_{IN}4$	0100	$A_{IN}4$	0100	$A_{IN}4$	0100	No connect
0101	$A_{IN}5$	0101	No connect	0101	$A_{IN}5$	0101	No connect
0110	$A_{IN}6$	0110	$A_{IN}6$	0110	$A_{IN}6$	0110	$A_{IN}6$
0111	$A_{IN}7$	0111	No connect	0111	No connect	0111	No connect
1000	$A_{IN}8$	1000	$A_{IN}8$	1000	$A_{IN}8$	1000	No connect
1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect	1001 to 1111	No connect

ANTIALIASING FILTERS

The ADV728x has optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 16).

The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 17 and Figure 18 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA_FILT_MAN_OVR control.

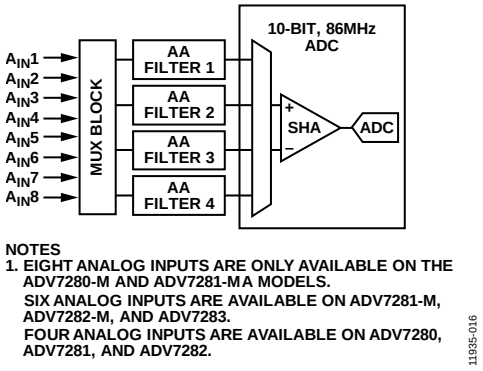

Figure 16. Antialias Filter Configuration

ANTIALIASING FILTER CONFIGURATION

AA_FILT_MAN_OVR, Antialiasing Filter Override, Address 0xF3[4]

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

AA_FILT_EN[3:0], Antialiasing Filter Enable, Address 0xF3[3:0]

These bits allow the user to enable or disable the antialiasing filters on each of the three input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

AA_FILT_EN[0], Antialiasing Filter Enable, Address 0xF3[0]

When AA_FILT_EN[0] is set to 0, AA Filter 1 is disabled.

When AA_FILT_EN[0] is set to 1, AA Filter 1 is enabled.

AA_FILT_EN[1], Antialiasing Filter Enable, Address 0xF3[1]

When AA_FILT_EN[1] is set to 0, AA Filter 2 is disabled.

When AA_FILT_EN[1] is set to 1, AA Filter 2 is enabled.

AA_FILT_EN[2], Antialiasing Filter Enable, Address 0xF3[2]

When AA_FILT_EN[2] is set to 0, AA Filter 3 is disabled.

When AA_FILT_EN[2] is set to 1, AA Filter 3 is enabled.

AA_FILT_EN[3], Antialiasing Filter Enable, Address 0xF3[3]

When AA_FILT_EN[3] is set to 0, AA Filter 4 is disabled.

When AA_FILT_EN[3] is set to 1, AA Filter 4 is enabled.

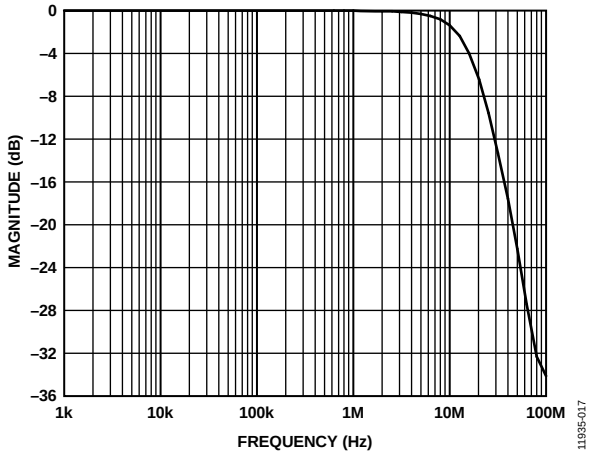

Figure 17. Antialiasing Filter Magnitude Response

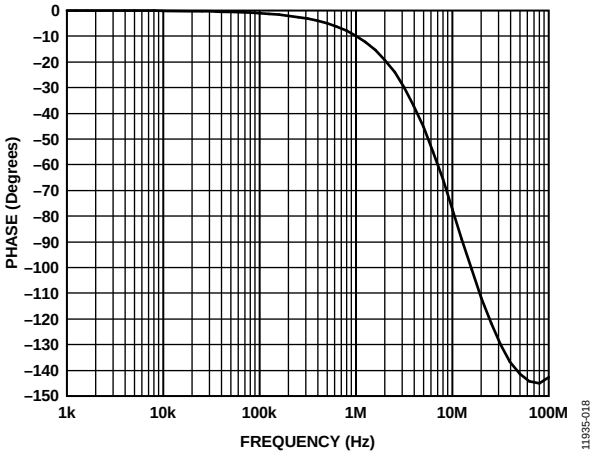

Figure 18. Antialiasing Filter Phase Response

GLOBAL CONTROL REGISTERS

The register control bits listed in this section affect the entire chip.

POWER SAVING MODE AND RESET CONTROL

Power Down

PWRDWN, Address 0x0F[5]

The ADV728x can be placed into a chip-wide, power-down mode by setting the PWRDWN bit or by using the PWRDWN pin. The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I²C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I²C interface is unaffected and remains operational in power-down mode.

When PWRDWN is set to 0, the chip is operational. When PWRDWN is set to 1 (default), the ADV728x is in a chip-wide, power-down mode.

Reset, Chip Reset, Address 0x0F[7]

Setting this bit, which is equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV728x, issues a full chip reset. All I²C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified; they keep their last written value. Those bits are marked as having a reset value of x in the register tables (see Table 95 and Table 97). After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the $\overline{\text{RESET}}$ pin), the part returns to the default for its primary mode of operation. All I²C bits are loaded with their default values, making this bit self-clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I²C writes are performed.

The I²C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented.

When the reset bit is set to 0 (default), operation is normal.

When the reset bit is set to 1, the reset sequence starts.

GLOBAL PIN CONTROL

Drive Strength Selection (I²C)

DR_STR_S[1:0], Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the I²C signal output drivers. This affects the drive strength for the SDA and SCL pins.

Table 19. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

GENERAL-PURPOSE OUTPUT CONTROLS

The ADV7280-M, ADV7281-MADV7281-MA, and ADV7282-M have three general-purpose outputs (GPO).

Three GPOs

These outputs allow the user to control other devices in a system via the I²C port of the device.

GPO_ENABLE, General-Purpose Output Enable, User Sub Map, Address 0x59[4]

When GPO_ENABLE is set to 0 (default), all GPO pins are tristated.

When GPO_ENABLE is set to 1, all GPO pins are in a driven state. The polarity output from each GPO is controlled by GPO[3:0].

GPO[2:0], General-Purpose Outputs, User Sub Map, Address 0x59[2:0]

Individual control of the four GPO ports is achieved using GPO[2:0].

GPO_ENABLE must be set to 1 for the GPO pins to become active.

GPO[0]

When GPO[0] is set to 0 (default), Logic 0 is output from the GPO0 pin.

When GPO[0] is set to 1, Logic 1 is output from the GPO0 pin.

GPO[1]

When GPO[1] is set to 0 (default), Logic 0 is output from the GPO1 pin.

When GPO[1] is set to 1, Logic 1 is output from the GPO1 pin.

GPO[2]

When GPO[2] is set to 0 (default), Logic 0 is output from the GPO2 pin.

When GPO[2] is set to 1, Logic 1 is output from the GPO2 pin.

Table 20. General-Purpose Output Truth Table

GPO_ENABLE	GPO[2:0]	GPO2	GPO1	GPO0
0	XXX[1]	Z[2]	Z[2]	Z[2]
1	000	0	0	0
1	001	0	0	1
1	010	0	1	0
1	011	0	1	1
1	100	1	0	0
1	101	1	0	1
1	110	1	1	0
1	111	1	1	1

[1] X indicates any value.
[2] Z indicates high impedance.

GLOBAL STATUS REGISTER

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV728x. The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the ADV728x.

IDENTIFICATION

IDENT[7:0], Address 0x11[7:0]

This is the register identification of the ADV728x revision. Table 21 describes the various versions of the ADV728x.

Table 21. IDENT CODE

IDENT[7:0]	Description
0x40	Pre-release Silicon
0x41	Pre-release Silicon
0x42	Released Silicon

STATUS 1

Status 1[7:0], Address 0x10[7:0]

This read-only register provides information about the internal status of the ADV728x.

See the CIL[2:0], Count into Lock, Address 0x51[2:0] section and the COL[2:0], Count Out of Lock, Address 0x51[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable, Address 0x51[7] section.

Table 22. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read)
2	FSC_LOCK	f_{SC} locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2

Status 2[7:0], Address 0x12[7:0]

Table 23. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Rovi (previously Macrovision) color striping
1	MVCS T3	Rovi color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV PS DET	Detected Rovi pseudo sync pulses
3	MV AGC DET	Detected Rovi AGC pulses
4	LL NSTD	Line length is nonstandard
5	FSC NSTD	f_{SC} frequency is nonstandard
6	Reserved	
7	Reserved	

STATUS 3

Status 3[7:0], Address 0x13[7:0]

Table 24. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	Reserved	
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved
4	FREE_RUN_ACT	Flags if ADV728x has entered free-run mode (see Free-Run Operation section)
5	STD FLD LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

AUTODETECTION RESULT

AD_RESULT[2:0], Address 0x10[6:4]

The AD_RESULT[2:0] bits report back on the findings from the ADV728x autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure it.

Table 25. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

VIDEO PROCESSOR

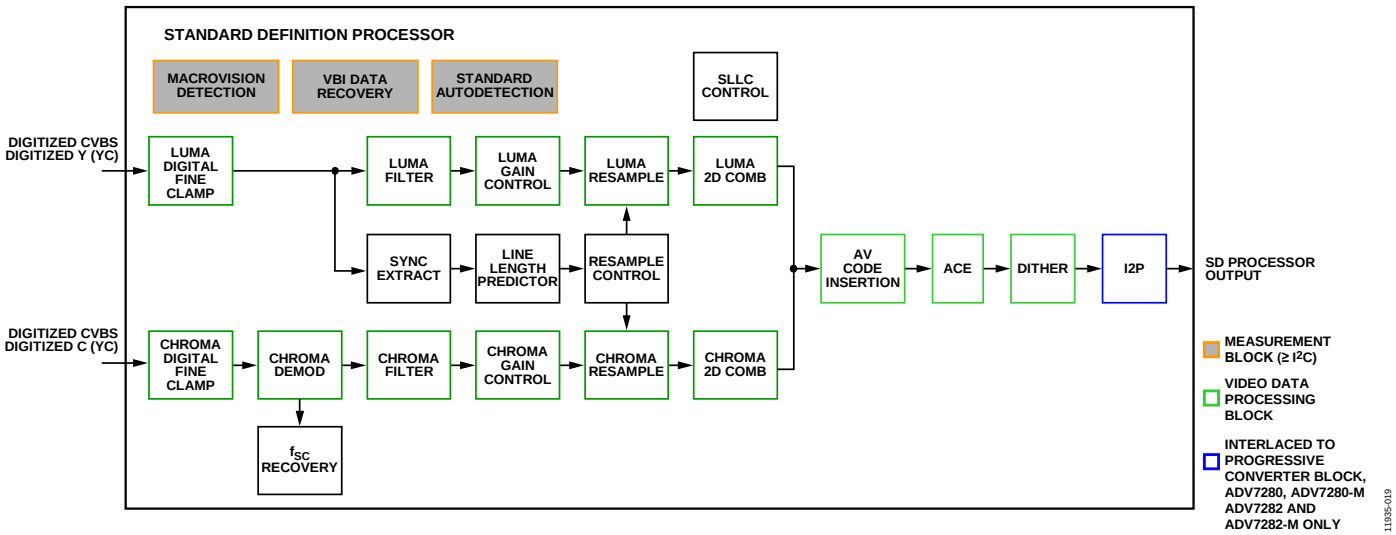

Figure 19. Block Diagram of Video Processor

Figure 19 shows a block diagram of the video processor within the ADV728x. The ADV728x can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input. The output from the video processor is fed into a MIPI CSI-2 Tx block in the ADV728x-M models. In the ADV728x-T models, the output of the video processor is output from the part in an ITU-R BT.656 video stream.

SD LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct for line length errors as well as dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted (as per ITU-R BT.656).

SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier (f_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, super adaptive comb filter provides high quality Y/C separation if the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted (as per ITU-R BT.656).

ACE, I2P, AND DITHER PROCESSING BLOCKS

- Adaptive contrast enhancement (ACE). This block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail. See the Adaptive Contrast Enhancement section.
- Dither. When enabled, this block converts the digital output of the ADV728x from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV728x to communicate with some LCD panels. See the Dither Function section.

- Interlaced-to-progressive converter (I2P). This block is only available in the ADV7280, ADV7280-M, ADV7282, and ADV7282-M models. This block converts interlaced video formats (480i and 576i) into progressive video formats (480p and 576p).

SYNC PROCESSING

The ADV728x extracts syncs embedded in the analog input video signal. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure that the ADV728x outputs 720 active pixels per line.

The sync processing on the ADV728x also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSYNC processor. This block provides extra filtering of the detected VSYNCs to improve vertical lock.
- HSYNC processor. The HSYNC processor is designed to filter incoming HSYNCs that were corrupted by noise, providing much improved performance for video signals with a stable time base, but poor SNR.

VBI DATA RECOVERY

The ADV728x can retrieve the following information from the input video:

- Wide screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed captioning (CCAP)
- Rovi protection presence
- Teletext

The ADV728x is also capable of automatically detecting the incoming video standard with respect to the following:

- Color subcarrier frequency
- Field rate
- Line rate

The ADV728x can configure itself to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits (Address 0x02[7:4]) allow the user to force the digital core into a specific video standard. This is not necessary under normal circumstances. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Autodetection of SD Modes

To guide the autodetect system of the ADV728x, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID_SEL[3:0], Address 0x02[7:4]

Table 26. VID_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

AD_SEC525_EN, SECAM 525 Autodetect Enable, Address 0x07[7]

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection of a SECAM style, FM-modulated color component.

AD_SECAM_EN, SECAM Autodetect Enable, Address 0x07[6]

Setting AD_SECAM_EN to 0 (default) disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 enables the detection of SECAM.

AD_N443_EN, NTSC 4.43 Autodetect Enable, Address 0x07[5]

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

AD_P60_EN, PAL 60 Autodetect Enable, Address 0x07[4]

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

AD_PALN_EN, PAL N Autodetect Enable, Address 0x07[3]

Setting AD_PALN_EN to 0 (default) disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 enables the detection of the PAL N standard.

AD_PALM_EN, PAL M Autodetect Enable, Address 0x07[2]

Setting AD_PALM_EN to 0 (default) disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 enables the detection of PAL M.

AD_NTSC_EN, NTSC Autodetect Enable, Address 0x07[1]

Setting AD_NTSC_EN to 0 (default) disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 enables the detection of standard NTSC.

AD_PAL_EN, PAL B/PAL D/PAL I/PAL G/PAL H Autodetect Enable, Address 0x07[0]

Setting AD_PAL_EN to 0 (default) disables the detection of standard PAL.

Setting AD_PAL_EN to 1 enables the detection of standard PAL.

SFL_INV, Subcarrier Frequency Lock Inversion, Address 0x41[6] (ADV7280 Only)

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. Implemented to solve compatibility issues with video encoders, it solves two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

Second, there was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (genlock telegram) bit directly, whereas the newer ones invert the bit prior to using it. The reason for this is that the inversion compensated for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the ADV717x and ADV73xx encoders, the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For the older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL_INV to 0 (default) makes the part SFL compatible with the ADV717x and ADV73xx video encoders.

Setting SFL_INV to 1 makes the part SFL compatible with the older video encoders.

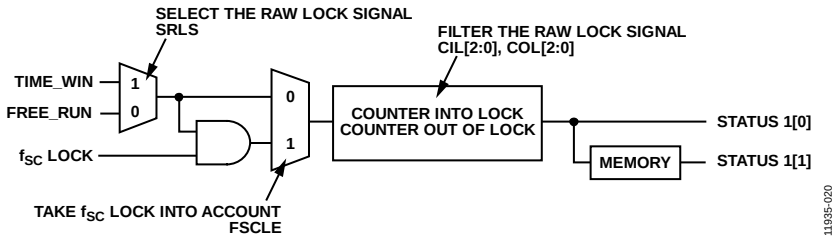

Figure 20. Lock Related Signal Path

Lock Related Controls

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1[7:0], Address 0x10[7:0] section). Figure 20 outlines the signal flow and the controls that are available to influence the way the lock status information is generated.

SRLS, Select Raw Lock Signal, Address 0x51[6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register). See Figure 20.

- The TIME_WIN signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quickly.
- The FREE_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE_RUN signal (to evaluate over several fields).

Setting SRLS to 1 selects the TIME_WIN signal (to evaluate on a line-to-line basis).

FSCLE, f_{SC} Lock Enable, Address 0x51[7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV728x in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is set to 0 (default), the overall lock status is dependent only on horizontal sync lock.

When FSCLE is set to 1, the overall lock status is dependent on horizontal sync lock and f_{SC} lock.

CIL[2:0], Count into Lock, Address 0x51[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Status 1[1:0]. The bit counts the value in lines of video.

Table 27. CIL Function

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COL[2:0], Count Out of Lock, Address 0x51[5:3]

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into the unlocked state and reports this via Status 1[1:0]. It counts the value in lines of video.

Table 28. COL Function

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

COLOR CONTROLS

These registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

CON[7:0], Contrast Adjust, Address 0x08[7:0]

This register allows the user to control contrast adjustment of the picture.

Table 29. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0], SD Saturation Cb Channel, Address 0xE3[7:0]

This register allows the user to control the gain of the Cb channel only, which in turn adjusts the saturation of the picture.

Table 30. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0], SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only, which in turn adjusts the saturation of the picture.

Table 31. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cr channel = −42 dB
0xFF	Gain on Cr channel = +6 dB

SD_OFF_Cb[7:0], SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register (Address 0x0B).

Table 32. SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 mV offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0], SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

Table 33. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 mV offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0], Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 34. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = −30 IRE

HUE[7:0], Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM-modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 35. HUE Function

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0], Default Value Y, Address 0x0C[7:2]

When the ADV728x loses lock on the incoming video signal or when there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF_VAL_AUTO_EN bit is set to 1 and the ADV728x has lost lock to the input video signal, this is the intended mode of operation (automatic mode).
- If the DEF_VAL_EN bit is set to 1, regardless of the lock status of the video decoder, this is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = (DEF_Y[5:0], 0, 0).

For DEF_Y[5:0], 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

DEF_C[7:0], Default Value C, Address 0x0D[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if:

- The DEF_VAL_AUTO_EN bit is set to high and the ADV728x cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV728x for the chroma side is Cr[4:0] = (DEF_C[7:4]) and Cb[4:0] = (DEF_C[3:0]).

For DEF_C[7:0], 0x7C (blue) is the default value for Cr and Cb.

FREE-RUN OPERATION

Free-run mode provides the user with a stable clock and predictable data if the input signal cannot be decoded, for example, if input video is not present.

The ADV728x automatically enters free-run mode if the input signal cannot be decoded. The user can prevent this operation by setting the DEF_VAL_AUTO_EN to 0. When the DEF_VAL_AUTO_EN bit is set to 0, the ADV728x outputs noise if it cannot decode the input video. It is recommended that the user keep DEF_VAL_AUTO_EN set to 1.

The user can force free-run mode by setting the DEF_VAL_EN bit to 1. This can be a useful tool in debugging system level issues.

The VID_SEL[3:0] bits can be used to force the video standard output in free-run mode (see the Video Standard Selection section).

The user can also specify which data is output in free-run mode with the FREE_RUN_PAT_SEL bits. The following test patterns can be set using this function:

- Single color
- Color bars
- Luma ramp
- Boundary box

Single Color Test Pattern

In this mode, the ADV728x device can be set to output the default luma and chroma data stored in DEF_Y and DEF_C (see the Color Controls section).

Color Bars Test Pattern

In this mode, the ADV728x device outputs the 100% color bars pattern.

Luma Ramp Test Pattern

In this mode, the ADV728x device outputs a series of vertical bars. Each vertical bar is progressively brighter than the vertical bar to its left.

Boundary Box Test Pattern

In this mode, the ADV728x device outputs a black screen with a 1-pixel depth white border (see Figure 21).

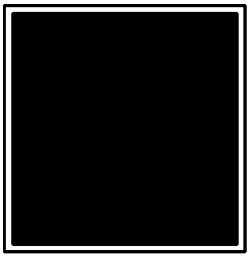

Figure 21. Boundary Box Free-Run Test Pattern

DEF_VAL_AUTO_EN, Default Value Automatic Enable, User Map, Address 0x0C[1]

This bit enables the ADV728x to enter free-run mode if it cannot decode the video signal that has been input.

Table 36. DEF_VAL_AUTO_EN Function

DEF_VAL_AUTO_EN	Description
0	The ADV728x outputs noise if it loses lock with the inputted video signal.
1 (default)	The ADV728x enters free-run mode if it loses lock with the inputted video signal.

DEF_VAL_EN, Default Value Enable, User Map, Address 0x0C[0]

This bit forces free-run mode.

Table 37. DEF_VAL_EN Function

DEF_VAL_EN	Description
0 (default)	Do not force free-run mode (that is, free-run mode dependent on DEF_VAL_AUTO_EN)
1	Force free-run mode

FREE_RUN_PAT_SEL[2:0], Free Run Pattern Select, User Map, Address 0x14[2:0]

This function selects what data is output in free-run mode.

Table 38. FREE_FUN_PAT_SEL Function

FREE_RUN_PAT_SEL	Description
000 (default)	Single color set by DEF_C and DEF_Y controls; see the Color Controls section
001	100% color bars
010	Luma ramp. Note that to display properly, the DEF_C register should be set to 0x88; see the Color Controls section
101	Boundary box

CLAMP OPERATION

The input video is ac-coupled into the ADV728x. This has the advantage of protecting the ADV728x from STB events. However, the dc value of the input video needs to be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV728x in both single-ended and differential modes. This section also shows the different ways in which a user can configure clamp operation behavior.

Single-Ended CVBS Clamp Operation

The ADV728x uses a combination of current sources and a digital processing block for clamping as shown in Figure 22.

The analog processing channel shown is replicated three times inside the IC. While only a single channel is needed for a single-ended CVBS signal, two independent channels are needed for Y/C (SVHS) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections.

- Clamping before the ADC (analog domain): current sources and voltage sources.
- Clamping after the ADC (digital domain): digital processing block.

The primary task of the analog clamping circuits is to ensure that the video signal stays within the valid 1.0 V ADC input window so that the analog-to-digital conversion can take place. The current sources in the AFE correct the dc level of the ac-coupled input video signal before it is fed into the ADC. The digitized data from the ADC is then fed into the video processor. The digital fine clamp block within the video processor corrects for any remaining variation in the dc level. The video processor also sends clamp control signals to the current sources. This feedback loop fine tunes the current clamp operation and compensates for any noise on the input video signal. This maintains the dc level of the video signal during normal operation.

Differential CVBS Clamping Operation

This section applies to the ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models only.

The differential clamping operation works in a similar manner to the single-ended clamping operation (see the Single-Ended CVBS Clamp Operation section). In differential mode, a coarse clamp pulls the positive and negative video input to a common-mode voltage VCML (see Figure 23). The feedback loop between the current clamps and the video processor fine tunes this coarse dc offset and makes the clamping robust to noise on the video input. Note that the current clamps are controlled within a feedback loop between the AFE and the video processor; the coarse clamps are not.

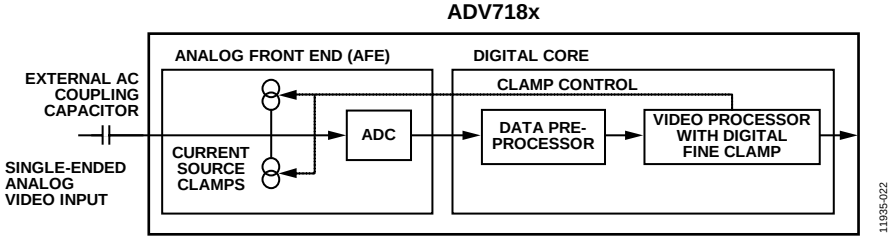

Figure 22. Single-Ended Clamping Overview

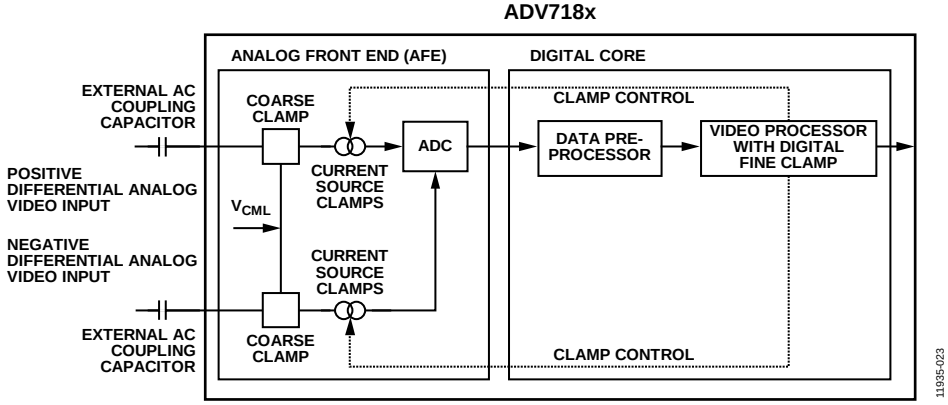

Figure 23. Differential Clamping Overview

Clamp Operation Controls

The following sections describe the I²C signals that can be used to influence the behavior of the clamping block.

CCLEN, Current Clamp Enable, Address 0x14[4]

The current clamp enable bit allows the user to switch off all the current sources in the AFE simultaneously. This may be useful if the incoming analog video signal is clamped externally.

When CCLEN is set to 0, the current sources are switched off.

When CCLEN is set to 1 (default), the current sources are enabled.

DCT[1:0], Digital Clamp Timing, Address 0x15[6:5]

The clamp timing register determines the time constant of the digital fine clamp circuitry. Note that the digital fine clamp reacts quickly because it immediately corrects any residual dc level error for the active line. The time constant from the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 39. DCT Function

DCT[1:0]	Description
00 (default)	Slow (TC = 1 sec)
01	Medium (TC = 0.5 sec)
10	Fast (TC = 0.1 sec)
11	Determined by ADV728x, depending on the input video parameters

DCFE, Digital Clamp Freeze Enable, Address 0x15[4]

This register bit allows users to freeze the digital clamp loop at any time (do their own clamping). Users can disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is set to 0 (default), the digital clamp is operational.

When DCFE is set to1, the digital clamp loop is frozen.

LUMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

- Luma antialias filter (YAA). The ADV728x receives video at a rate of 28.6363 MHz. (In the case of 4× oversampled video, the ADC samples at 57.27 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the ADV728x is always 28.6363 MHz.) The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality linear phase, low-pass filter that preserves the luma signal while, at the same time, attenuating out-of-band components. The luma antialias filter (YAA) has a fixed response.
- Luma shaping filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can be used to reduce selectively the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. If the video is low-pass filtered, a follow-on video compression stage can work more efficiently.
  The ADV728x has two responses for the shaping filter: one that is used for good quality composite, component, and SVHS type sources; and a second for nonstandard CVBS signals. The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 25 through Figure 28 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. Y/C separation must aim for the best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV728x. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (f_{SC}). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship may be disturbed, and the comb filters may not be able to remove all crosstalk artifacts in the best fashion without the assistance of the shaping filter block.

An automatic mode is provided that allows the ADV728x to evaluate the quality of the incoming video signal and select the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has the following control bits.

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (depending on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.

- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality composite (CVBS), component (YPrPb), and SVHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources (because they can be successfully combed) as well as for luma components of YPrPb and Y/C sources (because they need not be combed). For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 24.

YSFM[4:0], Y Shaping Filter Mode, Address 0x17[4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter selection is based on other register selections, such as detected video standard, as well as properties extracted from the incoming video itself, such as quality and time base stability. The automatic selection always selects the widest possible bandwidth for the video input encountered (see Table 40).

The Y-shaping filter mode operates as follows:

- If the YSFM settings specify a filter (that is, YSFM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wideband filters are used.

WYSFMOVR, Wideband Y Shaping Filter Override, Address 0x18[7]

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information on luma shaping filters, see the Y Shaping Filter section and the flowchart shown in Figure 24.

When WYSFMOVR is set to 0, the shaping filter for good quality video signals is selected automatically.

When WYSFMOVR is set to 1 (default), it enables manual override via WYSFM[4:0].

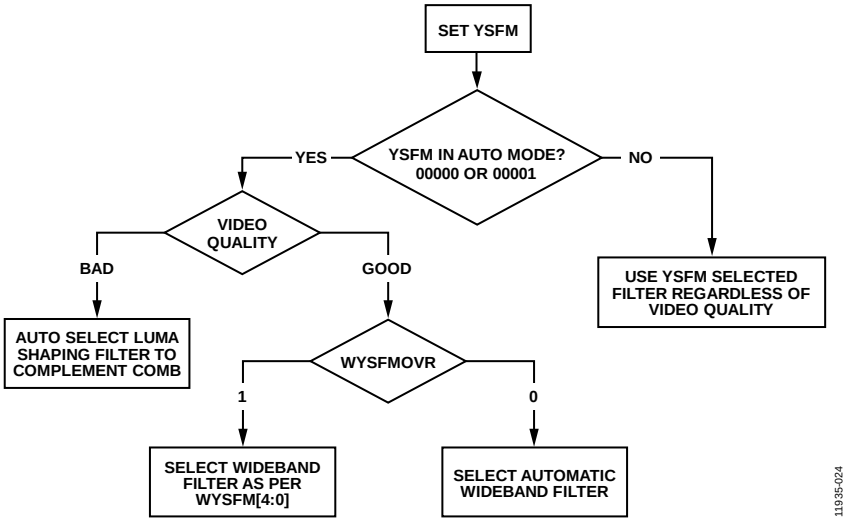

Figure 24. YSFM and WYSFM Control Flowchart

Table 40. YSFM Function

YSFM[4:0]	Description
00000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
00001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011	SVHS 18 (CCIR 601)
10100	PAL NN1
10101	PAL NN2
10110	PAL NN3
10111	PAL WN1
11000	PAL WN2
11001	NTSC NN1
11010	NTSC NN2
11011	NTSC NN3
11100	NTSC WN1
11101	NTSC WN2
11110	NTSC WN3
11111	Reserved

WYSFM[4:0], Wideband Y Shaping Filter Mode, Address 0x18[4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, such as CVBS with stable time base, luma component of YPrPb, and luma component of Y/C. The WYSFM bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 41. WYSFM Function

WYSFM[4:0]	Description
00000	Reserved, do not use
00001	Reserved, do not use
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011 (default)	SVHS 18 (CCIR 601)
10100 to 11111	Reserved, do not use

The filter plots in Figure 25 show the SVHS 1 (narrowest) to SVHS 18 (widest) shaping filter settings. Figure 27 shows the PAL notch filter responses. The NTSC notch filter responses are shown in Figure 28.

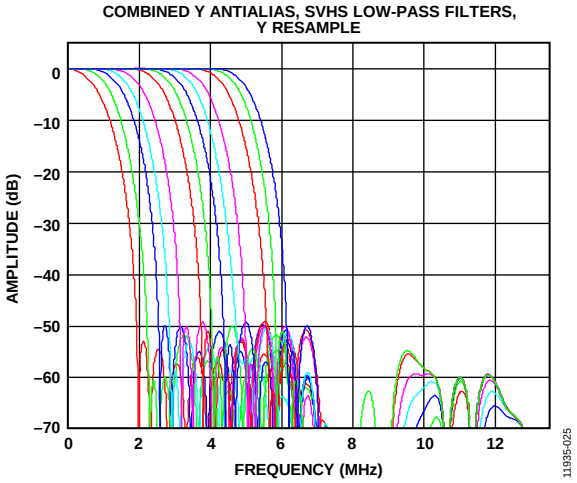

Figure 25. Y SVHS Combined Responses

CHROMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS (or differential CVBS) inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

- Chroma antialias filter (CAA). The ADV728x oversamples the CVBS by a factor of 4 and the chroma/YPrPb by a factor of 2. A decimating filter (CAA) is used to preserve the active video band and to remove any out-of-band components. The CAA filter has a fixed response.
- Chroma shaping filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters,0 such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

Figure 29 shows the overall response of all filters together.

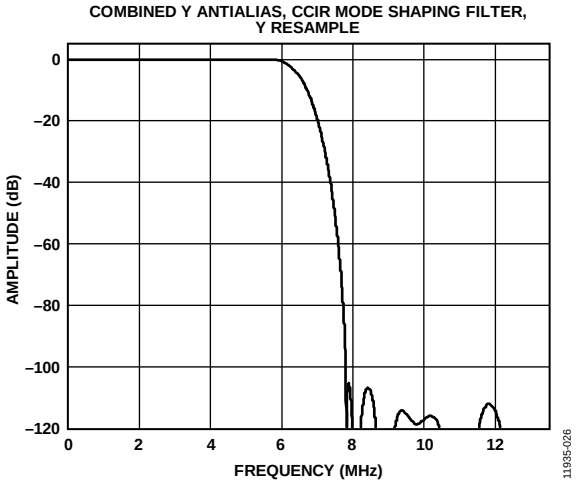

Figure 26. Combined Y Antialias, CCIR Mode Shaping Filter

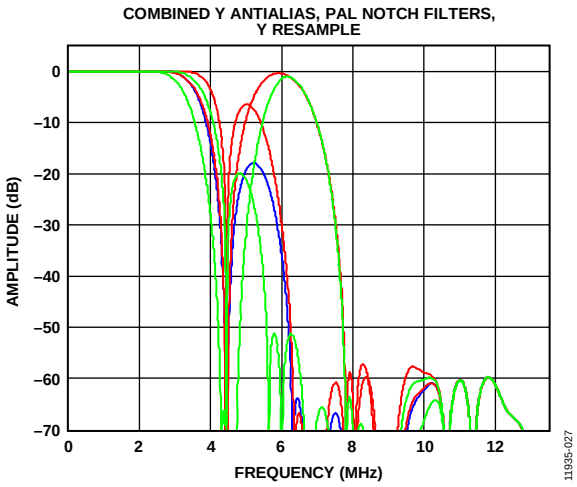

Figure 27. Combined Y Antialias, PAL Notch Filters

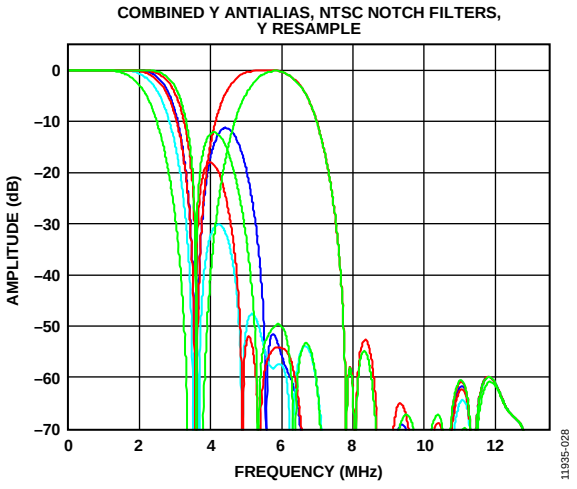

Figure 28. Combined Y Antialias Filter, NTSC Notch Filters

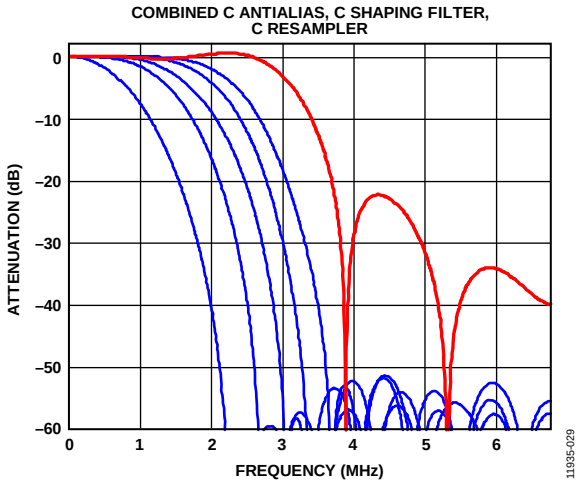

Figure 29. Chroma Shaping Filter Responses

CSFM[2:0], C Shaping Filter Mode, Address 0x17[7:5]

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see the 000 and 001 settings in Table 42).

Table 42. CSFM Function

CSFM[2:0]	Description
000 (default)	Autoselection 1.5 MHz bandwidth
001	Autoselection 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

Figure 29 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode (shown in red).

GAIN OPERATION

The gain control within the ADV728x is done on a purely digital basis. The input ADC supports a 10-bit range mapped into a 1.0 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

Advantages of this architecture over the commonly used programmable gain amplifier (PGA) before the ADC include the fact that the gain is now completely independent of supply, temperature, and process variations.

As shown in Figure 32, the ADV728x can decode a video signal as long as it fits into the ADC window. The components for this are the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

Figure 30 and Figure 31 show the typical voltage divider networks required to keep the input video signal within the allowed range of the ADC, 0 V to 1 V. The circuit in Figure 30 should be placed before all the single-ended analog inputs to the ADV728x, and place the circuit in Figure 31 before all the differential inputs to the ADV728x.

Note differential inputs can only be applied directly to the ADV7281, ADV7281-M, ADV7281-MA, ADV7282, and ADV7282-M models.

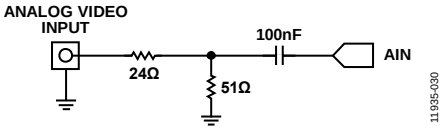

Figure 30. Single-Ended Input Voltage Divider Network

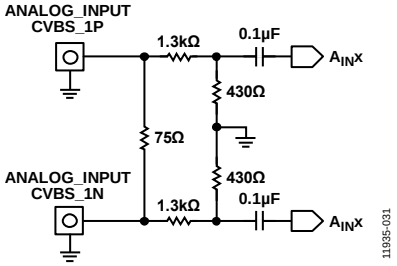

Figure 31. Differential Input Voltage Divider Network

The minimum supported amplitude of the input video is determined by the ability of the ADV728x to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are separate gain control units for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are shown in Table 43.

Table 43. AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color-burst amplitude taken from luma path
	Peak white	Dependent on color-burst amplitude taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color-burst amplitude taken from luma path
	Peak white	Dependent on color-burst amplitude
YPrPb	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops. This causes the loops to stop updating and the AGC determined gain at the time of the freeze to stay active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual-function manual gain registers, LG[11:0] luma gain and CG[11:0] chroma gain, in the Luma Gain section and Chroma Gain section, respectively.

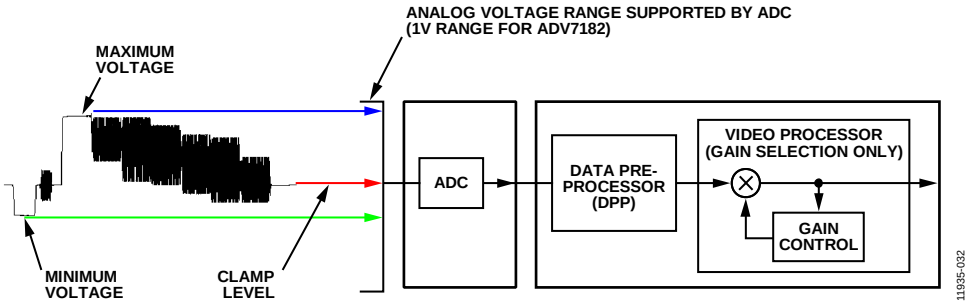

Figure 32. Gain Control Overview

Luma Gain

LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4]

The luma automatic gain control mode bits select the operating mode for the gain control in the luma path.

The peak white algorithm is used to detect if the input video amplitude exceeds the ADC input range of the ADV728x. If this is so, then the ADV728x reduces its internal luma gain to prevent the signal from becoming saturated.

Table 44. LAGC Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip), peak white algorithm off
010 (default)	AGC (blank level to sync tip), peak white algorithm on
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0], Luma Automatic Gain Timing, Address 0x2F[7:6]

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. This register has an effect only if the LAGC[2:0] register is set to 001 or 010 (automatic gain control modes).

If peak white AGC is enabled and active (see the Status 1[7:0], Address 0x10[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white AGC, LAGT becomes relevant again.

The update speed for the peak white algorithm can be customized by the use of internal parameters.

Table 45. LAGT Function

LAGT[1:0]	Description
00	Slow (*time constant* = 2 sec)
01	Medium (*time constant* = 1 sec)
10	Fast (*time constant* = 0.2 sec)
11 (default)	Adaptive

PW_UPD, Peak White Update, Address 0x2B[0]

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, see the LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4] section.

Setting PW_UPD to 0 updates the gain once per video line.

Setting PW_UPD to 1 (default) updates the gain once per field.

LG[11:0], Luma Gain, Address 0x2F[3:0], Address 0x30[7:0]

LMG[11:0], Luma Manual Gain, Address 0x2F[3:0], Address 0x30[7:0]

Luma gain[11:0] is a dual-function register. If all of these bits are written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the LAGC[2:0] bits, the value is one of the following:

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to either of the automatic modes)

Table 46. LG/LMG Function

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = x	Write	Manual gain for luma path
LG[11:0] = x	Read	Actual used gain

$$Luma\ Gain \cong \frac{LMG[11:0]}{Luma\ Calibration\ Factor} \quad (1)$$

where *LMG[11:0]* is a decimal value between 1024 and 4095.

Calculation of the Luma Calibration Factor

1. Using a video source, set the content to a gray field and apply a standard CVBS signal to the CVBS input of the board.
2. Using an oscilloscope, measure the signal at the CVBS input to ensure that its sync depth, color burst, and luma are at the standard levels.
3. Connect the output of the ADV728x to a backend system that has unity gain and monitor the output voltage.
4. Measure the luma level correctly from the black level. Turn off the luma AGC and manually change the value of the luma manual gain control register, LMG[11:0], until the output luma level matches the input measured in Step 2.

This value, in decimal, is the luma calibration factor.

Chroma Gain

CAGC[1:0], Chroma Automatic Gain Control, Address 0x2C[1:0]

The two bits of the color automatic gain control mode select the basic mode of operation for the automatic gain control in the chroma path.

Table 47. CAGC Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Use luma gain for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

CAGT[1:0], Chroma Automatic Gain Timing, Address 0x2D[7:6]

The chroma automatic gain timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register has an effect only if the CAGC[1:0] bits are set to 10 (automatic gain).

Table 48. CAGT Function

CAGT[1:0]	Description
00	Slow (*time constant* = 2 sec)
01	Medium (*time constant* = 1 sec)
10	Reserved
11 (default)	Adaptive

CG[11:0], Chroma Gain, Address 0x2D[3:0], Address 0x2E[7:0]; CMG[11:0], Chroma Manual Gain, Address 0x2D[3:0], Address 0x2E[7:0]

Chroma gain[11:0] is a dual-function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] function is switched to manual fixed gain. See Equation 2 for calculating a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this is either:

- The chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
- The chroma automatic gain value (CAGC[1:0] set to either of the automatic modes).

Table 49. CG/CMG Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma\_Gain \cong \frac{CMG[11:0]_{decimal}}{ChromaCalibrationFactor} \quad (2)$$

where *ChromaCalibrationFactor* is a decimal value between 0 and 4095.

Calculation of Chroma Calibration Factor

Take the following steps to calculate the chroma calibration factor:

1. Apply a CVBS signal with the color bars/SMPTE bars test pattern content directly to the measurement equipment.
2. Ensure correct termination of 75 Ω on the measurement equipment. Measure chroma output levels.
3. Reconnect the source to the CVBS input of the ADV728x system that has a back end gain of 1. Repeat the measurement of chroma levels.
4. Turn off the chroma AGC and manually change the chroma gain control register, CMG[11:0], until the chroma level matches that measured directly from the source.

This value, in decimal, is the chroma calibration factor.

CKE, Color Kill Enable, Address 0x2B[6]

The color kill enable bit allows the optional color kill function to be switched on or off.

For QAM-based video standards (PAL and NTSC), as well as FM-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled and the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Set CKE to 0 to disable color kill.

Set CKE to 1 (default) to enable color kill.

CKILLTHR[2:0], Color Kill Threshold, Address 0x3D[6:4]

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM-based (NTSC and PAL) or FM-modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For the 000, 001, 010, and 011 settings, chroma demodulation inside the ADV728x may not work satisfactorily for poor input video signals.

Table 50. CKILLTHR Function

	Description	
CKILLTHR[2:0]	NTSC, PAL	SECAM
000	Kill at <0.5%	No color kill
001	Kill at <1.5%	Kill at <5%
010 (default)	Kill at <2.5%	Kill at <7%
011	Kill at <4%	Kill at <8%
100	Kill at <8.5%	Kill at <9.5%
101	Kill at <16%	Kill at <15%
110	Kill at <32%	Kill at <32%
111	Reserved for Analog Devices internal use only; do not select	

CHROMA TRANSIENT IMPROVEMENT (CTI)

The signal bandwidth allocated for chroma is typically much smaller than that for luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, may lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 33). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than that of the chroma component. The color edge is not sharp, and in the worst case, it can be blurred over several pixels.

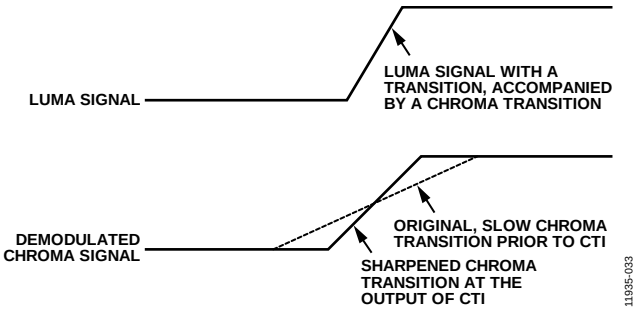

Figure 33. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to create steeper chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure that noise is not emphasized. Care was taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that have severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN, Chroma Transient Improvement (CTI) Enable, Address 0x4D[0]

Set CTI_EN to 0 to disable the CTI block.

Set CTI_EN to 1 (default) to enable the CTI block.

CTI_AB_EN, Chroma Transient Improvement Alpha Blend Enable, Address 0x4D[1]

The CTI_AB_EN bit enables an alpha blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI_EN bit.

Set CTI_AB_EN to 0 to disable the CTI alpha blender.

Set CTI_AB_EN to 1 (default) to enable the CTI alpha-blend mixing function.

CTI_AB[1:0], Chroma Transient Improvement Alpha Blend, Address 0x4D[3:2]

The CTI_AB[1:0] controls the behavior of alpha blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become active, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture; however, it may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 51. CTI_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 (default)	Smoothest mixing between sharpened and original chroma signal

CTI_C_TH[7:0], CTI Chroma Threshold, Address 0x4E[7:0]

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition must be if it is going to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI_C_TH[7:0] is 0x08.

DIGITAL NOISE REDUCTION (DNR) AND LUMA PEAKING FILTER

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise and that their removal, therefore, improves picture quality. The two DNR blocks in the ADV728x are the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 34.

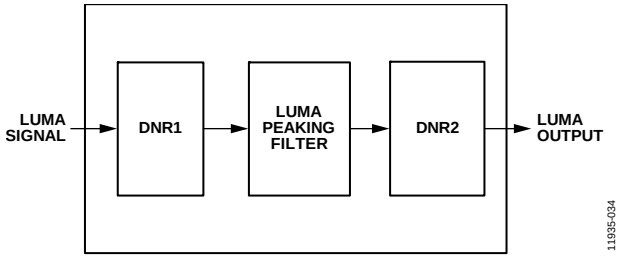

Figure 34. DNR and Peaking Block Diagram

DNR and Peaking

DNR_EN, Digital Noise Reduction Enable, Address 0x4D[5]

The DNR_EN bit enables the DNR block or bypasses it.

Table 52. DNR_EN Function

Setting	Description
0	Bypasses the DNR block (disable)
1 (default)	Enables the DNR block

DNR_TH[7:0], DNR Noise Threshold 1, Address 0x50[7:0]

The DNR1 block is positioned before the luma peaking block. The DNR_TH[7:0] value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 53. DNR_TH[7:0] Function

Setting	Description
0x08 (default)	Threshold for maximum luma edges to be interpreted as noise

PEAKING_GAIN[7:0], Luma Peaking Gain, Address 0xFB[7:0]

This filter can be manually enabled. The user can select to boost or to attenuate the midregion of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the luma data unaltered. A lower value attenuates the signal, and a higher value gains the luma signal. A plot of the responses of the filter is shown in Figure 35.

Table 54. PEAKING_GAIN[7:0] Function

Setting	Description
0x40 (default)	0 dB response

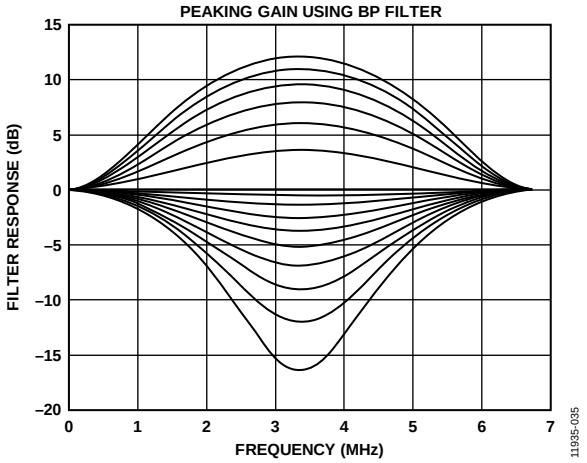

Figure 35. Peaking Filter Responses

DNR_TH2[7:0], DNR Noise Threshold 2, Address 0xFC[7:0]

The DNR2 block is positioned after the luma peaking block and, therefore, affects the gained luma signal. It operates in the same way as the DNR1 block; however, there is an independent threshold control, DNR_TH2[7:0], for this block. This value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH2[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 55. DNR_TH2[7:0] Function

Setting	Description
0x04 (default)	Threshold for maximum luma edges to be interpreted as noise

COMB FILTERS

The comb filters of the ADV728x can automatically handle video of all types, standards, and levels of quality. The NTSC and PAL configuration registers allow the user to customize the comb filter operation depending on which video standard is detected (by autodetection) or selected (by manual programming).

NTSC Comb Filter Settings

These settings are used for NTSC M/NTSC J CVBS inputs.

NSFSEL[1:0], Split Filter Selection, NTSC, Address 0x19[3:2]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection results in better performance on diagonal lines but more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Table 56. NSFSEL Function

NSFSEL[1:0]	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

CTAPSN[1:0], Chroma Comb Taps, NTSC, Address 0x38[7:6]

Table 57. CTAPSN Function

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts three lines to two lines
10 (default)	NTSC chroma comb adapts five lines to three lines
11	NTSC chroma comb adapts five lines to four lines

CCMN[2:0], Chroma Comb Mode, NTSC, Address 0x38[5:3]

Table 58. CCMN Function

CCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Three-line adaptive chroma comb for CTAPSN = 01 Four-line adaptive chroma comb for CTAPSN = 10 Five-line adaptive chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMN[2:0], Luma Comb Mode, NTSC, Address 0x38[2:0]

Table 59. YCMN Function

YCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed luma comb two-line (two taps)
110	Fixed luma comb (all lines of line memory)	Fixed luma comb three-line (three taps)
111	Fixed luma comb (bottom lines of line memory)	Fixed luma comb two-line (two taps)

PAL Comb Filter Settings

These settings are used for PAL B/PAL G/PAL H/PAL I/PAL D, PAL M, PAL Combinational N, PAL 60, and NTSC 4.43 CVBS inputs.

PSFSEL[1:0], Split Filter Selection, PAL, Address 0x19[1:0]

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 60. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

CTAPSP[1:0], Chroma Comb Taps, PAL, Address 0x39[7:6]

Table 61. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use
01	PAL chroma comb adapts five lines (three taps) to three lines (two taps); cancels cross luma only
10	PAL chroma comb adapts five lines (five taps) to three lines (three taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts five lines (five taps) to four lines (four taps); cancels cross luma and hue error well

CCMP[2:0], Chroma Comb Mode, PAL, Address 0x39[5:3]

Table 62. CCMP Function

CCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01 Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

YCMP[2:0], Luma Comb Mode, PAL, Address 0x39[2:0]

Table 63. YCMP Function

YCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive five lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed three lines (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed five lines (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed three lines (two taps) luma comb

IF FILTER COMPENSATION

IFFILTSEL[2:0], IF Filter Select, Address 0xF8[2:0]

The IFFILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input, as would be observed on tuner outputs. Figure 36 and Figure 37 show IF filter compensation for NTSC and PAL, respectively.

The options for this feature are as follows:

- Bypass mode
- NTSC, consisting of three filter characteristics
- PAL, consisting of three filter characteristics

See Table 95 for programming details.

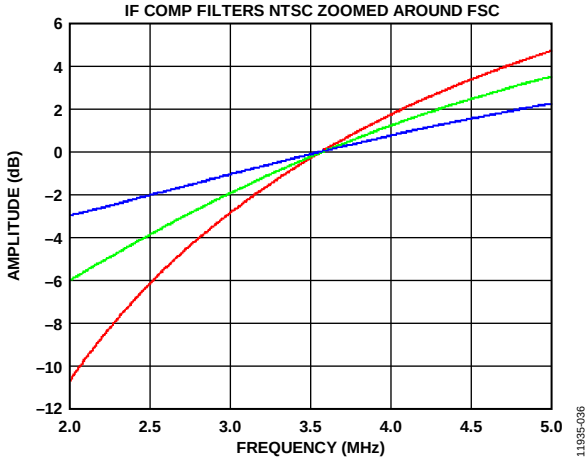

Figure 36. NTSC IF Filter Compensation

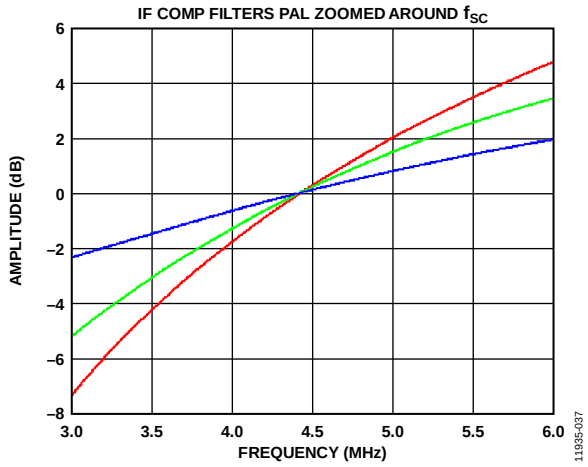

Figure 37. PAL IF Filter Compensation

ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The ADV728x can increase the contrast of an image depending on the content of the picture, allowing bright areas to be made brighter and dark areas to be made darker. The optional ACE feature allows for the contrast within dark areas to be increased without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to be able to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 64. To disable the ACE function, execute the register writes shown in Table 65.

The ACE feature works by sampling the chroma and luma levels in the input image. This information is then histogrammed, and the resulting correction is applied to the entire image. This correction is done in a nonlinear fashion so that more correction can be applied to dark areas, if required.

For normal use, the luma and chroma gain controls can be used; however, in automotive applications, where dark areas may need to be further enhanced, the gamma gain controls are also used.

The reaction time of the ACE function can be set using the ACE_RESPONSE_SPEED[7:4] bits (see Table 96). The corrected image is faded over the original image using alpha blending, giving a gradual change in contrast with scene changes. The ACE_RESPONSE_SPEED[7:4] bits determine the duration of the transition from the original to the corrected image. A larger value for these bits results in a faster transition time; however, a smaller value gives more stability to rapid scene changes.

The ACE_CHROMA_MAX[7:4] bits are used to set a maximum value that clips the chroma gain regardless of the ACE_CHROMA_GAIN[3:0] settings.

The ACE_GAMMA_GAIN[3:0] bits are particularly useful in automotive applications because they allow dramatic image enhancement in dark regions by stretching the contrast of pixels at the low (dark) values of the image histogram. The luma and chroma gain controls are normally used; however, the ACE_GAMMA_GAIN[3:0] bits should be used when further stretching of the contrast in the dark areas of an image is needed.

Table 64. Register Writes to Enable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x80	Enable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter User Sub Map

Table 65. Register Writes to Disable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x00	Disable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter User Sub Map

Note that the I^2C registers that control the ACE operation of the ADV728x are contained in the User Sub Map 2. See the Power Supply Requirements section for information on how to program the ADV728x into User Sub Map 2.)

ACE_ENABLE, User Sub Map 2, Address 0x80[7]

This control enables ACE.

Table 66. ACE_ENABLE Function

ACE_ENABLE	Description
0 (default)	Disable ACE
1	Enable ACE

ACE_LUMA_GAIN[4:0], User Sub Map 2, Address 0x83[4:0]

This is a control to set the auto-contrast level for the luma channel when ACE_ENABLE is set to 1.

Table 67. ACE_LUMA_GAIN Function

ACE_LUMA_GAIN[4:0]	Description
00000	Set ACE luma auto-contrast level to minimum value
01101 (default)	Set ACE luma auto-contrast level to default value
11111	Set ACE luma auto-contrast level to maximum value

ACE_RESPONSE_SPEED[3:0], User Sub Map 2, Address 0x85[7:4]

This control sets the reaction time of the ACE function.

Table 68. ACE_RESPONSE_SPEED Function

ACE_ RESPONSE_SPEED[3:0]	Description
0000	Set speed of ACE response to slowest value
1111 (default)	Set speed of ACE response to fastest value

ACE_CHROMA_GAIN[3:0], User Sub Map 2, Address 0x84[3:0]

This control sets the color saturation level for the color channels when ACE_ENABLE is set to 1.

Table 69. ACE_CHROMA_GAIN Function

ACE_CHROMA_GAIN[3:0]	Description
0000	Set ACE color auto-saturation level to minimum value
1000 (default)	Set ACE color auto-saturation level to default value
1111	Set ACE color auto-saturation level to maximum value

ACE_CHROMA_MAX[3:0], User Sub Map 2, Address 0x84[7:4]

This control sets a maximum threshold value that clips the chroma gain regardless of the ACE_CHROMA_GAIN[3:0] settings.

Table 70. ACE_CHROMA_MAX Function

ACE_CHROMA_MAX[3:0]	Description
0000	Set maximum threshold for ACE color auto-saturation level to minimum value
1000 (default)	Set maximum threshold for ACE color auto-saturation level to default value
1111	Set maximum threshold for ACE color auto-saturation level to maximum value

ACE_GAMMA_GAIN[3:0], User Sub Map 2, Address 0x85[3:0]

This control provides further contrast enhancement to the luma and chroma gain controls and is particularly effective in the darker areas of an image.

Table 71. ACE_GAMMA_GAIN[3:0] Function

ACE_GAMMA_GAIN[3:0]	Description
0000	Set further contrast enhancement to minimum value
1000 (default)	Set further contrast enhancements to default value
1111	Set further contrast enhancement to maximum value

DITHER FUNCTION

The dither function converts the digital output of the ADV728x from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV728x to communicate with some LCD panels. The dither function is turned off by default. It is activated by the BR_DITHER_MODE bit.

BR_DITHER_MODE, User Sub Map 2, Address 0x92[0]

BR_DITHER_MODE is contained in the I²C map User Sub Map 2. See the Register Maps section for a description of how to enter User Sub Map 2.

Table 72. BR_DITHER_MODE Function

BR_DITHER_MODE	Description
0 (default)	8-bit to 6-bit down dither disabled
1	8-bit to 6-bit down dither enabled

The script described in Table 73 and Table 74 explains how to enable and disable the 8-bit to 6-bit down dither function.

Table 73. Register Writes to Enable the Dither Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x92	0x07	Enable 8-bit to 6-bit down dither
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter User Sub Map

Table 74. Register Writes to Disable the Dither Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x92	0x06	Disable 8-bit to 6-bit down dither
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter User Sub Map

I2P FUNCTION

This section applies only to the ADV7280, ADV7280-M, ADV7282, and ADV7282-M models.

The interlaced-to-progressive (I2P) function converts an interlaced video input into a progressive video output. This function is performed without the need for external memory. Edge adaptive technology is used to minimize video defects on low angle lines.

The I2P function is disabled by default. To enable the I2P function, see the Analog Devices' recommended scripts available online.

ITU-R BT.656 OUTPUT

This section applies to the ADV728x-T models only (ADV7280, ADV7281, and ADV7282).

The ADV728x-T receives analog video and outputs digital video according to the ITU-R BT.656 specification. The ADV728x-T outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins and has a line-locked clock (LLC) pin.

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output is used to clock the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

Two synchronization pins (HS and VS/FIELD/SFL) are available on the ADV7280 model. The two synchronization pins are not available on the ADV7281 and ADV7282 models. The two synchronization pins (HS and VS/FIELD/SFL) output a variety of synchronization signals such as horizontal sync, vertical sync, field sync, and color subcarrier frequency lock (SFL) sync. The majority of these synchronization signals are already embedded in the video data. Therefore, the use of the synchronization pins is optional.

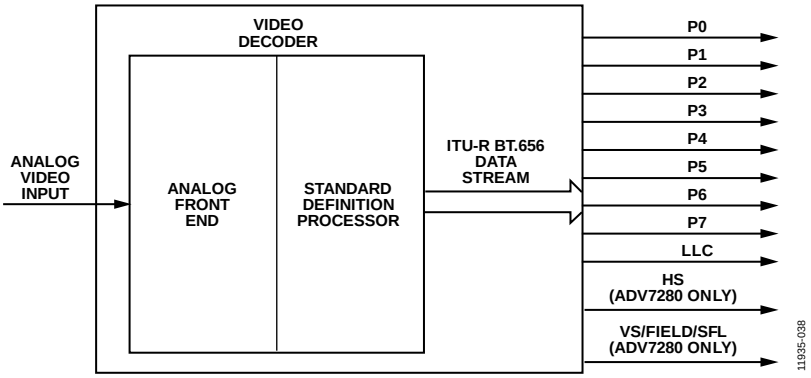

Figure 38. ITU-R BT.656 Output Stage of the ADV728x-T

ITU-R BT.656 OUTPUT CONTROL REGISTERS

The following are controls for the ITU-R BT.656 output for the ADV728x-T models. See the Global Control Registers for further control registers.

Tristate Output Drivers

This section applies only to the ADV728x-T models (ADV7280, ADV7281, and ADV7282 models).

TOD, Address 0x03[6]

This bit allows the user to tristate the output drivers of the ADV7280.

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL pins) can be forced active via the TIM_OE bit. Note the HS and VS/FIELD/SFL pins are only available on the ADV7280 model.

When TOD is set to 0, the output drivers are enabled.

When TOD is set to 1(default), the output drivers are tristated.

Tristate LLC Driver

This section applies only to the ADV728x-T models (ADV7280, ADV7281, and ADV7282 models.)

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC pin of the ADV728x-T to be tristated.

When TRI_LLC is set to 0, the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is set to 1 (default), the LLC pin drivers are tristated.

Timing Signals Output Enable

This section applies only to the ADV7280 model.

TIM_OE, Address 0x04[3]

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS/FIELD/SFL into the active state (that is, driving state) even if the TOD bit is set. If TIM_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator. This may be the case if only the timing signals are extracted from an incoming signal or if the part is in free-run mode, where a separate chip can output a company logo, for example.

When TIM_OE is set to 0 (default), HS and VS/FIELD/SFL are tristated according to the TOD bit.

When TIM_OE is set to 1, HS and VS/FIELD/SFL are forced active all the time.

VS/FIELD/SFL Sync Mux Selection

This section applies only to the ADV7280 model.

FLD_OUT_SEL[2:0], Address 0x6B[2:0]

The FLD_OUT_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the ITU-R BT.656 Output Control Registers section for more information.

Table 75. FLD_OUT_SEL Function

FLD_OUT_SEL[2:0]	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information.
001	The VS/FIELD/SFL pin outputs vertical sync information.
010 (default)	The VS/FIELD/SFL pin outputs field sync information.
011	The VS/FIELD/SFL pin outputs data enable (DE) information.
100	The VS/FIELD/SFL pin outputs subcarrier frequency lock information.

HS Sync Mux Selection

This section applies only to the ADV7280 model.

HS_OUT_SEL[2:0], Address 0x6A[2:0]

The HS_OUT_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) information.

Note that the HS pin must be active for this selection to occur. See the ITU-R BT.656 Output Control Registers section for more information.

Table 76. HS_OUT_SEL Function

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs data enable (DE) information.
100	The HS pin outputs subcarrier frequency lock (SFL) information.

Drive Strength Selection (Data)

This section applies only to the ADV728x-T models (ADV7280, ADV7281, and ADV7282 models.)

DR_STR[1:0], Address 0xF4[5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the drive strength for the pixel output pins (P[7:0]) and the timing pins (HS and VS/FIELD/SFL). Note the HS and VS/FIELD/SFL pins are only available on the ADV7280 model.

Table 77. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

This section applies only to the ADV728x-T models (ADV7280, ADV7281, and ADV7282 models.)

DR_STR_C[1:0], Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin).

Table 78. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

This section applies only to the ADV7280 model.

EN_SFL_PIN, Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7280 core to an encoder in a decoder/encoder back-to-back arrangement.

When the EN_SFL_PIN is set to 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is set to 1, the subcarrier frequency lock information is presented on the SFL pin.

Polarity LLC Pin

This section applies only to the ADV728x-T models (ADV7280, ADV7281, and ADV7282 models.)

PCLK, Address 0x37[0]

The polarity of the clock that leaves the ADV728x-T via the LLC pin can be inverted using the PCLK bit. Changing the polarity of the LLC clock output may be necessary to meet the setup-and-hold time expectations of follow-on chips.

When PCLK is set to 0, the LLC output polarity is inverted.

When PCLK is set to 1 (default), the LLC output polarity is normal.

MIPI CSI-2 Tx OUTPUT

This section applies to the ADV728x-M models only (ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M models.)

The decoder in the ADV728x-M outputs an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a CSI-2 Tx module. Data from the CSI-2 Tx module is fed into a D-PHY physical layer and output serially from the device.

The output of the ADV728x-M consists of a single data channel on the D0P and D0N lanes and a clock channel on the CLKP and CLKN lanes.

Video data and ancillary data is output over the data lanes in high speed mode. The data lanes enter a low power mode during the horizontal and vertical blanking periods.

The clock lanes are used to clock the output video. After the ADV728x-M is programmed, the clock lanes exit low power mode and remain in high speed mode until the part is reset or powered down.

The ADV728x-M outputs video data in an 8-bit YCrCb 4:2:2 format. When the I2P core is disabled, the video data is output in an interlaced format at a nominal data rate of 216 Mbps. When the I2P core is enabled, the video data is output in a progressive format at a nominal data rate of 432 Mbps. Note the progressive MIPI output is only available on the ADV7280-M and ADV7282-M models.

ULTRALOW POWER STATE

The ADV728x-M MIPI Tx can be programmed to enter the ultralow power state (ULPS) by the CSITX_PWRDN bit (CSI MAP, Address 0x00[7]). In this mode, the MIPI clock and data lanes transition to V_{OL} and do not oscillate.

Alternatively, the MIPI clock and data lanes can be programmed to enter the ULPS state separately using the ESC_MODE_EN_CLK, ESC_XSHUTDOWN_CLK, ESC_MODE_EN_D0, and ESC_XSHUTDOWN_D0 bits.

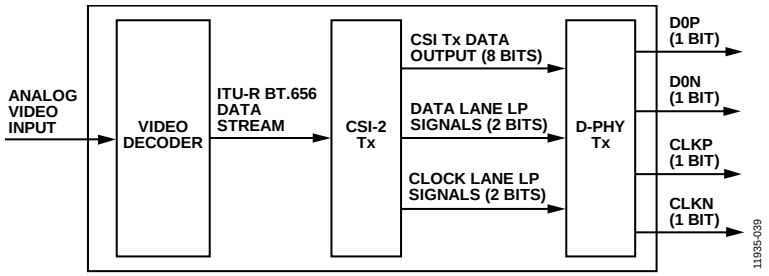

Figure 39. MIPI CSI-2 Output Stage of ADV728x-M

Table 79. CSITX_PWRDN Function

CSITX_PWRDN (CSI MAP, Address 0x00[7])	Description
0	Power up CSI output block. The clock and data lanes output the ultralow power state exit sequence, and then exit the ultralow power state.
1 (default)	Power down CSI output block. The clock and data lanes output the ultralow power state entry sequence and then enter ultralow power state.

ESC_MODE_EN_D0, User Sub Map, Address 0x26[7] and ESC_XSHUTDOWN_D0, User Sub Map, Address 0x26[6]

The MIPI CSI-2 Data lanes (D0P and D0N) can be programmed to enter and exit the ultralow power state (ULPS) using the ESC_MODE_EN_D0 and ESC_XSHUTDOWN_D0 bits.

To make the data lanes enter the ULPS state, the writes listed in Table 80 are needed.

Table 80. Writes to Force MIPI Data Lanes (D0Pand D0N) to Enter Ultralow Power State

Order of Reads/Writes	ESC_MODE_EN_D0 (User Sub Map, Address 0x26[7])	ESC_XSHUTDOWN_D0 (User Sub Map, Address 0x26[7])	Description
1st Write	0	0	Normal operation.
2nd Write	1	0	The ULPS entry sequence is transmitted and then DOP and D0N enter ULPS state. DOP and D0N go to V_{OL}.

To make the data lanes exit the ULPS state, the writes listed in Table 81 are needed.

Table 81. Writes to Force MIPI Data Lanes (D0P and D0N) to Exit Ultralow Power State

Order of Reads/Writes	ESC_MODE_EN_D0 (User Sub Map, Address 0x26[7])	ESC_XSHUTDOWN_D0 (User Sub Map, Address 0x26[7])	Description
Read	1	0	Data lanes in ULPS state.
1st Write	1	1	The ULPS exit sequence is transmitted and then DOP and D0N exit ULPS state. DOP and D0N go to V_{OH}.
2nd Write	0	1	Data lanes enter normal operation.
3rd Write	0	0	No change. Data lanes remain in normal operation.

ESC_MODE_EN_CLK, User Sub Map, Address 0x26[5] and ESC_XSHUTDOWN_CLK, User Sub Map, Address 0x26[4]

The MIPI CSI-2 clock lanes (CLKP and CLKN) can be programmed to enter and exit the ultralow power state using the ESC_MODE_EN_D0 and ESC_XSHUTDOWN_D0 bits.

To make the data lanes enter the ULPS state, the writes listed in Table 82 are needed.

Table 82. Writes to Force MIPI Clock Lanes (CLKP and CLKN) to Enter Ultralow Power State

Order of Reads/Writes	ESC_MODE_EN_CLK (User Sub Map, Address 0x26[5])	ESC_XSHUTDOWN_CLK (User Sub Map, Address 0x26[4])	Description
1st Write	0	0	Normal operation.
2nd Write	1	0	The ULPS entry sequence is transmitted and then CLKP and CLKN enter ULPS state. CLKP and CLKN go to V_{OL}.

To make the data lanes exit the ULPS state, the writes listed in Table 83 are needed.

Table 83. Writes to Force MIPI Clock Lanes (CLKP and CLKN) to Exit Ultralow Power State

Order of Reads/Writes	ESC_MODE_EN_CLK (User Sub Map, Address 0x26[5])	ESC_XSHUTDOWN_D0 (User Sub Map, Address 0x26[4])	Description
Read	1	0	Clock lanes in ULPS state.
1st Write	1	1	The ULPS exit sequence is transmitted and then CLKP and CLKN exit ULPS state. CLKP and CLKN go to V_{OH}.
2nd Write	0	1	Clock lanes enter normal operation.
3rd Write	0	0	No change. Clock lanes remain in normal operation.

I²C PORT DESCRIPTION

The ADV728x supports a 2-wire (I²C compatible) serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV728x and the system I²C master controller. The ADV728x I²C port allows the user to set up and configure the decoder and to read back captured VBI data.

The ADV728x has a number of possible I²C slave addresses and subaddresses (see the Register Maps section). The ADV728x Main Map has four possible slave addresses for read and write operations depending on the logic level of the ALSB pin (see Table 84).

Table 84. Main I²C Address for ADV728x

ALSB Pin	R/$\overline{W}$ Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ADV728x ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two ADV728x devices in an application without using the same I²C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation and Logic 0 corresponds to a write operation.

To control the device on the bus, a specific protocol is followed:

- The master initiates a data transfer by establishing a start condition, which is defined as a high-to-low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
- All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$bit). The bits are transferred from MSB to LSB.
- The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.
- All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV728x acts as a standard I²C slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV728x does not issue an acknowledge and returns to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, the following action is taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge, which indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. A no acknowledge is issued by the ADV728x, and the part returns to the idle condition.

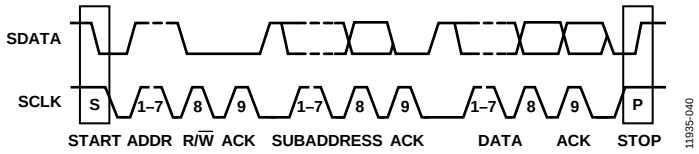

Figure 40. Bus Data Transfer

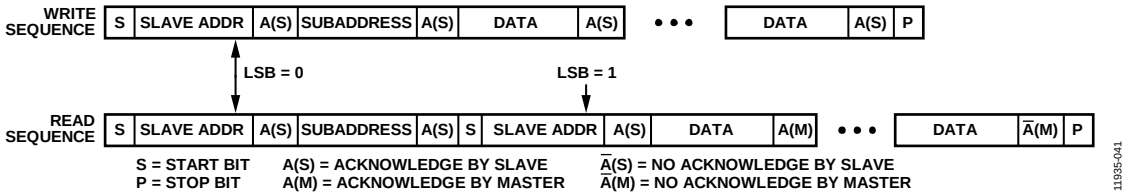

Figure 41. Read and Write Sequence

REGISTER MAPS

The ADV728x contains three register maps: the main register map, the VPP register map, and the CSI register map. The Main Map contains three sub maps: the User Sub Map, the Interrupt/VDP Sub Map, and User Sub Map 2 (see Figure 42).

Main Map

The I²C slave address of the Main Map of the ADV728x is set by the ALSB pin (see Table 84). The Main Map allows the user to program the I²C slave addresses of the VPP and CSI Maps. The Main Map contains three sub maps: the User Sub Map, the Interrupt/VDP Sub Map, and User Sub Map 2. These three sub maps are accessed by writing to the SUB_USR_EN bits (Address 0x0E[6:5]) within the Main Map (see Figure 42).

User Sub Map

The User Sub Map contains registers that program the analog front end and digital core of the ADV728x. The User Sub Map has the same I²C slave address as the Main Map. To access the User Sub Map, set the SUB_USR_EN bits in the Main Map (Address 0x0E[6:5]) to 00.

Interrupt/VDP Sub Map

The Interrupt/VDP Sub Map contains registers that can be used to program internal interrupts, control the $\overline{\text{INTRQ}}$ pin, and decode vertical blanking interval (VBI) data.

The Interrupt/VDP Sub Map has the same I²C slave address as the Main Map. To access the Interrupt/VDP Sub Map, set the SUB_USR_EN bits in the Main Map (Address 0x0E[6:5]) to 01.

User Sub Map 2

User Sub Map 2 contains registers that control the ACE, down dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the ADV728x enters free run and color kill modes.

User Sub Map 2 has the same I²C slave address as the Main Map. To access User Sub Map 2, set the SUB_USR_EN bits in the Main Map (Address 0x0E[6:5]) to 10.

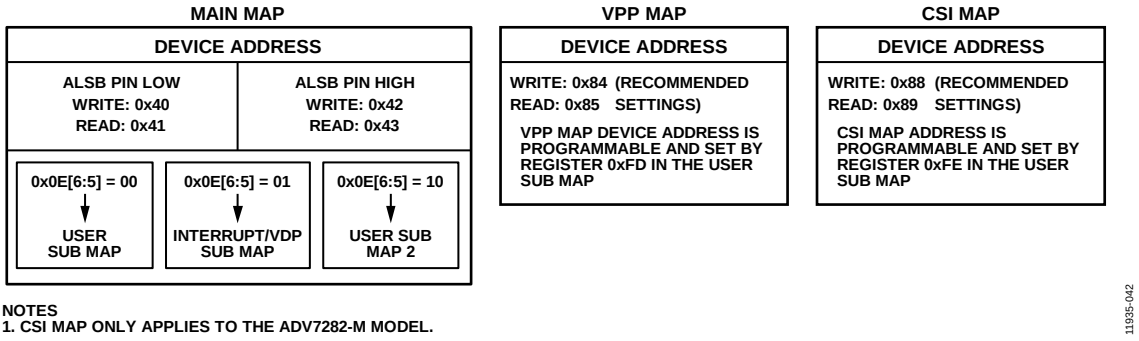

Figure 42. Register Map and Sub Map Access

Table 85. I²C Register Map and Sub Map Addresses

ALSB Pin	R/$\overline{W}$ Bit	Slave Address	SUB_USR_EN Bits (Address 0x0E[6:5])	Register Map or Sub Map
0	0 (write)	0x40	00	User Sub Map
0	1 (read)	0x41	00	User Sub Map
0	0 (write)	0x40	01	Interrupt/VDP Sub Map
0	1 (read)	0x41	01	Interrupt/VDP Sub Map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User Sub Map
1	1 (read)	0x43	00	User Sub Map
1	0 (write)	0x42	01	Interrupt/VDP Sub Map
1	1 (read)	0x43	01	Interrupt/VDP Sub Map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2
N/A	0 (write)	0x88	N/A	CSI Map
N/A	1 (read)	0x89	N/A	CSI Map
N/A	0 (write)	0x84	N/A	VPP Map
N/A	1 (read)	0x85	N/A	VPP Map

VPP Map

Note that the VPP Map applies only to the ADV7280, ADV7280-M, and ADV7282-M models.

The video postprocessor (VPP) map contains registers that control the I2P core (interlaced-to-progressive converter).

The VPP map has a programmable I²C slave address, which is programmed using Register 0xFD in the User Sub Map of the Main Map. The default value for the VPP map address is 0x00; however, the VPP map cannot be accessed until the I²C slave address is set. The recommended I²C slave address for the VPP map is 0x84.

To reset the I²C slave address of the VPP map, write to the VPP_SLAVE_ADDRESS[7:1] bits in the main register map (Address 0xFD[7:1]). Set these bits to a value of 0x84 (I²C write address; I²C read address is 0x85).

CSI Map

This section applies only to the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M models.

The camera serial interface (CSI) map contains registers that control the MIPI CSI-2 output stream from the ADV728x-M.

The CSI map has a programmable I²C slave address, which is programmed using Register 0xFE in the User Sub Map of the Main Map. The default value for the CSI map address is 0x00; however, the CSI map cannot be accessed until the I²C slave address is reset. The recommended I²C slave address for the CSI map is 0x88.

To reset the I²C slave address of the CSI map, write to the CSI_TX_SLAVE_ADDRESS[7:1] bits in the main register map (Address 0xFE[7:1]). Set these bits to a value of 0x88 (I²C write address; I²C read address is 0x89).

SUB_USR_EN Bits, Address 0x0E[6:5]

The ADV728x Main Map contains three sub maps: the User Sub Map, the Interrupt/VDP Sub Map, and the User Sub Map 2 (see Figure 42). The User Sub Map is available by default. The other two sub maps are accessed using the SUB_USR_EN bits. When programming of the interrupt/VDP map or User Sub Map 2 is completed, it is necessary to write to the SUB_USR_EN bits to return to the User Sub Map.

VPP_SLAVE_ADDRESS, Program VPP Register Map Address, User Map, Address 0xFD[7:1]

Table 86. Program VPP Register Map Address

VPP_SLAVE_ADDRESS [7:1]	Description
0000000 (default)	When set to this value, the VPP register map cannot be written to or read from.
10000100 (recommended)	This sets the VPP register map to a write address of 0x84 and a read address of 0x85. This is the recommended setting.

CSI_TX_SLAVE_ADDRESS, Program CSI Register Map address, User Map, Address 0xFE[7:1]

Table 87. Program CSI_Tx Register Map address

CSI_TX_SLAVE_ADDRESS[7:1]	Description
0000000 (default)	When set to this value, the CSI_Tx register map cannot be written to or read from.
10001000 (recommended)	This sets the CSI_Tx register map to a write address of 0x88 and a read address of 0x89. This is the recommended setting.

PCB LAYOUT RECOMMENDATIONS

The ADV728x is a high precision, high speed, mixed-signal device. To achieve the maximum performance from the part, it is important to use a well-designed PCB. This section provides guidelines for designing a PCB for use with the ADV728x.

ANALOG INTERFACE INPUTS

When routing the analog interface inputs on the PCB, keep track lengths to a minimum. Use 75 Ω trace impedances when possible; trace impedances other than 75 Ω increase the chance of reflections.

POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with 0.1 µF and 10 nF capacitors. The basic principle is to place a decoupling capacitor within approximately 0.5 cm of each power pin. Avoid placing the decoupling capacitors on the opposite side of the PCB from the ADV7282x because doing so introduces inductive vias in the path.

Locate the decoupling capacitors between the power plane and the power pin. Current should flow from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. The best approach is to place a via beneath the 100 nF capacitor pads down to the power plane (see Figure 43).

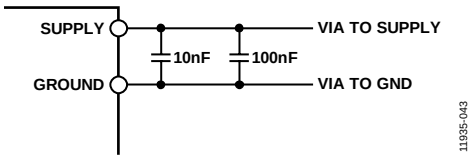

Figure 43. Recommended Power Supply Decoupling

It is especially important to maintain low noise and good stability for the P_{VDD} pin. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each circuit group (A_{VDD}, D_{VDD}, D_{VDDIO}, and P_{VDD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This disparity can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This problem can be mitigated by regulating the analog supply, or at least the P_{VDD} supply, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended. Experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

VREFN AND VREFP PINS

The capacitor between the VREFN and VREFP pins should be placed as close as possible to the ADV728x and on the same side of the PCB as the part.

DIGITAL OUTPUTS ($\overline{\text{INTRQ}}$, GPO0 TO GPO2)

Try to minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce current spikes inside the ADV7282-M. If series resistors are used, place them as close as possible to the ADV728x pins. However, try not to add vias or extra length to the output trace in an attempt to place the resistors closer.

If possible, limit the capacitance that each digital output must drive to less than 15 pF. This recommendation can be easily accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV728x, creating more digital noise on the power supplies.

EXPOSED METAL PAD

The ADV728x has an exposed metal pad on the bottom of the package. This pad must be soldered to ground. The exposed pad is used for proper heat dissipation, noise suppression and mechanical strength.

DIGITAL INPUTS

The digital inputs of the ADV728x are designed to work with 1.8 V signals (3.3 V for D_{VDDIO}) and are not tolerant of 5 V signals. Extra components are required if 5 V logic signals must be applied to the decoder.

MIPI OUTPUTS (D0P, D0N, CLKP, CLKN)

It is recommended that the MIPI output traces be kept as short as possible and on the same side of the PCB as the ADV728x-M device. It is also recommended that a solid plane—preferably a ground plane—be placed on the layer adjacent to the MIPI traces to provide a solid reference plane.

MIPI transmission operates in both differential and single-ended modes. During high speed transmission, the pair of outputs operates in differential mode; in low power mode, the pair operates as two independent single-ended traces. Therefore, it is recommended that each output pair be routed as two loosely coupled 50 Ω single-ended traces to reduce the risk of crosstalk between the two traces.

POWER SUPPLY REQUIREMENTS

Table 88 and Table 89 show the current rating recommendations for power supply design. These values should be used when designing a power supply section to ensure that an adequate current can be supplied to the ADV7280, ADV7281, or ADV7282 models.

Table 88. Current Supply Design Recommendations for the ADV7280, ADV7281, and ADV7282 Models

Parameter	Rating
I_{DVDDIO}	20 mA
I_{DVDD}	110 mA
I_{AVDD}	100 mA
I_{PVDD}	20 mA

Table 89. Current Supply Design Recommendations for the ADV7280-M, ADV7281-M, ADV7281-MA, andADV7282-M

Parameter	Rating
I_{DVDDIO}	5 mA
I_{DVDD}	110 mA
I_{AVDD}	100 mA
I_{PVDD}	20 mA
I_{MVDD}	20 mA

I²C REGISTER MAPS

To access all the registers listed in Table 90, SUB_USR_EN in Register Address 0x0E must be programmed to 00. All read only registers are left blank.

Table 90. User Sub Map Register Map Details

Address													
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
0	00	Input control	RW				INSEL[4]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]	00001110	0E
1	01	Video Selection 1	RW		ENHSPLL	BETACAM		ENVSPROC				11001000	C8
2	02	Video Selection 2	RW	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]					00000100	04
3	03	Output control	RW	VBI_EN	TOD							01001100	4C
4	04	Extended output control	RW	BT.656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	Range	00110101	35
5	05	Reserved											
6	06	Reserved											
7	07	Autodetect enable	RW	AD_SEC525_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	01111111	7F
8	08	Contrast	RW	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]	10000000	80
9	09	Reserved											
10	0A	Brightness adjust	RW	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]	00000000	00
11	0B	Hue adjust	RW	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]	00000000	00
12	0C	Default Value Y	RW	DEF_Y[5]	DEF_Y[4]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_VAL_AUTO_EN	DEF_VAL_EN	00110110	36
13	0D	Default Value C	RW	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]	01111100	7C
14	0E	ADI Control 1	RW		SUB_USR_EN[1]	SUB_USR_EN[0]						00000000	00
15	0F	Power management	RW	Reset		PWRDWN						00100000	20
16	10	Status 1	R	COL_KILL	AD_RESULT[2]	AD_RESULT[1]	AD_RESULT[0]	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK		
17	11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]	01000010	42
18	12	Status 2	R			FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET		
19	13	Status 3	R	PAL_SW_LOCK	Interlaced	STD FLD LEN	FREE_RUN_ACT	Reserved	SD_OP_50Hz	Reserved	INST_HLOCK		
20	14	Analog clamp control	RW				CCLEN		FREE_RUN_PAT_SEL.2	FREE_RUN_PAT_SEL.1	FREE_RUN_PAT_SEL.0	00010000	10
21	15	Digital Clamp Control 1	RW		DCT[1]	DCT[0]	DCFE					0000xxxx	00
22	16	Reserved											
23	17	Shaping Filter Control 1	RW	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]	00000001	01
24	18	Shaping Filter Control 2	RW	WYSFMOVR			WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]	10010011	93
25	19	Comb filter control	RW					NSFSEL[1]	NSFSEL[0]	PSFSEL[1]	PSFSEL[0]	11110001	F1
29	1D	ADI Control 2	RW	TRI_LLC								11000xxx	C0
39	27	Pixel delay control	RW	SWPC	AUTO_PDC_EN	CTA[2]	CTA[1]	CTA[0]		LTA[1]	LTA[0]	01011000	58
43	2B	Misc gain control	RW		CKE						PW_UPD	11100001	E1
44	2C	AGC mode control	RW		LAGC[2]	LAGC[1]	LAGC[0]			CAGC[1]	CAGC[0]	10101110	AE
45	2D	Chroma Gain Control 1	W	CAGT[1]	CAGT[0]			CMG[11]	CMG[10]	CMG[9]	CMG[8]	11110100	F4
45	2D	Chroma Gain 1	R					CG[11]	CG[10]	CG[9]	CG[8]		
46	2E	Chroma Gain Control 2	W	CMG[7]	CMG[6]	CMG[5]	CMG[4]	CMG[3]	CMG[2]	CMG[1]	CMG[0]	00000000	00
46	2E	Chroma Gain 2	R	CG[7]	CG[6]	CG[5]	CG[4]	CG[3]	CG[2]	CG[1]	CG[0]		
47	2F	Luma Gain Control 1	W	LAGT[1]	LAGT[0]			LMG[11]	LMG[10]	LMG[9]	LMG[8]	1111xxxx	F0
47	2F	Luma Gain 1	R					LG[11]	LG[10]	LG[9]	LG[8]		
48	30	Luma Gain Control 2	W	LMG[7]	LMG[6]	LMG[5]	LMG[4]	LMG[3]	LMG[2]	LMG[1]	LMG[0]	xxxxxxxx	00
48	30	Luma Gain 2	R	LG[7]	LG[6]	LG[5]	LG[4]	LG[3]	LG[2]	LG[1]	LG[0]		
49	31	VS/FIELD Control 1	RW				NEWAVMODE	HVSTIM				00000010	02
50	32	VS/FIELD Control 2	RW	VSBHO	VSBHE							01000001	41
51	33	VS/FIELD Control 3	RW	VSEHO	VSEHE							10000100	84
52	34	HS Position Control 1	RW		HSB[10]	HSB[9]	HSB[8]		HSE[10]	HSE[9]	HSE[8]	00000000	00
53	35	HS Position Control 2	RW	HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]	00000010	02
54	36	HS Position Control 3	RW	HSE[7]	HSE[6]	HSE[5]	HSE[4]	HSE[3]	HSE[2]	HSE[1]	HSE[0]	00000000	00
55	37	Polarity	RW	PHS		PVS		PF			PCLK	00010001	09
56	38	NTSC comb control	RW	CTAPSN[1]	CTAPSN[0]	CCMN[2]	CCMN[1]	CCMN[0]	YCMN[2]	YCMN[1]	YCMN[0]	10000000	80
57	39	PAL comb control	RW	CTAPSP[1]	CTAPSP[0]	CCMP[2]	CCMP[1]	CCMP[0]	YCMP[2]	YCMP[1]	YCMP[0]	11000000	C0
58	3A	ADC control	RW					PWRDWN_MUX_0	PWRDWN_MUX_1	PWRDWN_MUX_2	MUX PDN override	00000000	00
61	3D	Manual window control	RW		CKILLTHR[2]	CKILLTHR[1]	CKILLTHR[0]					00100010	22
65	41	Resample control	RW		SFL_INV							00000001	01
77	4D	CTI DNR Control 1	RW			DNR_EN		CTI_AB[1]	CTI_AB[0]	CTI_AB_EN	CTI_EN	11101111	EF
78	4E	CTI DNR Control 2	RW	CTI_C_TH[7]	CTI_C_TH[6]	CTI_C_TH[5]	CTI_C_TH[4]	CTI_C_TH[3]	CTI_C_TH[2]	CTI_C_TH[1]	CTI_C_TH[0]	00001000	08
80	50	DNR Noise Threshold 1	RW	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]	00001000	08
81	51	Lock count	RW	FSCLE	SRLS	COL[2]	COL[1]	COL[0]	CIL[2]	CIL[1]	CIL[0]	00100100	24
96	60	ADC Switch 3	RW						MUX3[2]	MUX3[1]	MUX3[0]	00010000	10
106	6A	Output Sync Select 1	RW						HS_OUT_SEL[2]	HS_OUT_SEL[1]	HS_OUT_SEL[0]	00000000	00
107	6B	Output Sync Select 2	RW		FLD_OUT_SEL[2]	FLD_OUT_SEL[1]	FLD_OUT_SEL[0]					00010010	12
143	8F	Free-Run Line Length 1	W		LLC_PAD_SEL[2]	LLC_PAD_SEL[1]	LLC_PAD_SEL[0]					00000000	00

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	(Hex)
153	99	CCAP1	R	CCAP1[7]	CCAP1[6]	CCAP1[5]	CCAP1[4]	CCAP1[3]	CCAP1[2]	CCAP1[1]	CCAP1[0]		
154	9A	CCAP2	R	CCAP2[7]	CCAP2[6]	CCAP2[5]	CCAP2[4]	CCAP2[3]	CCAP2[2]	CCAP2[1]	CCAP2[0]		
155	9B	Letterbox 1	R	LB_LCT[7]	LB_LCT[6]	LB_LCT[5]	LB_LCT[4]	LB_LCT[3]	LB_LCT[2]	LB_LCT[1]	LB_LCT[0]		
156	9C	Letterbox 2	R	LB_LCM[7]	LB_LCM[6]	LB_LCM[5]	LB_LCM[4]	LB_LCM[3]	LB_LCM[2]	LB_LCM[1]	LB_LCM[0]		
157	9D	Letterbox 3	R	LB_LCB[7]	LB_LCB[6]	LB_LCB[5]	LB_LCB[4]	LB_LCB[3]	LB_LCB[2]	LB_LCB[1]	LB_LCB[0]		
178	B2	CRC enable	W						CRC_ENABLE			00011100	1C
195	C3	ADC Switch 1	RW	Reserved	MUX1[2]	MUX1[1]	MUX1[0]	Reserved	MUX0[2]	MUX0[1]	MUX0[0]	xxxxxxxx	00
196	C4	ADC Switch 2	RW	MAN_MUX_EN				Reserved	MUX2[2]	MUX2[1]	MUX2[0]	0xxxxxxx	00
220	DC	Letterbox Control 1	RW				LB_TH[4]	LB_TH[3]	LB_TH[2]	LB_TH[1]	LB_TH[0]	10101100	AC
221	DD	Letterbox Control 2	RW	LB_SL[3]	LB_SL[2]	LB_SL[1]	LB_SL[0]	LB_EL[3]	LB_EL[2]	LB_EL[1]	LB_EL[0]	01001100	4C
222	DE	ST Noise Readback 1	R					ST_NOISE_VLD	ST_NOISE[10]	ST_NOISE[9]	ST_NOISE[8]		
223	DF	ST Noise Readback 2	R	ST_NOISE[7]	ST_NOISE[6]	ST_NOISE[5]	ST_NOISE[4]	ST_NOISE[3]	ST_NOISE[2]	ST_NOISE[1]	ST_NOISE[0]		
225	E1	SD offset Cb channel	RW	SD_OFF_Cb[7]	SD_OFF_Cb[6]	SD_OFF_Cb[5]	SD_OFF_Cb[4]	SD_OFF_Cb[3]	SD_OFF_Cb[2]	SD_OFF_Cb[1]	SD_OFF_Cb[0]	10000000	80
226	E2	SD offset Cr channel	RW	SD_OFF_Cr[7]	SD_OFF_Cr[6]	SD_OFF_Cr[5]	SD_OFF_Cr[4]	SD_OFF_Cr[3]	SD_OFF_Cr[2]	SD_OFF_Cr[1]	SD_OFF_Cr[0]	10000000	80
227	E3	SD saturation Cb channel	RW	SD_SAT_Cb[7]	SD_SAT_Cb[6]	SD_SAT_Cb[5]	SD_SAT_Cb[4]	SD_SAT_Cb[3]	SD_SAT_Cb[2]	SD_SAT_Cb[1]	SD_SAT_Cb[0]	10000000	80
228	E4	SD saturation Cr channel	RW	SD_SAT_Cr[7]	SD_SAT_Cr[6]	SD_SAT_Cr[5]	SD_SAT_Cr[4]	SD_SAT_Cr[3]	SD_SAT_Cr[2]	SD_SAT_Cr[1]	SD_SAT_Cr[0]	10000000	80
229	E5	NTSC V bit begin	RW	NVBEGDELO	NVBEGDELE	NVBEGSIGN	NVBEG[4]	NVBEG[3]	NVBEG[2]	NVBEG[1]	NVBEG[0]	00100101	25
230	E6	NTSC V bit end	RW	NVENDDELO	NVENDDELE	NVENDSIGN	NVEND[4]	NVEND[3]	NVEND[2]	NVEND[1]	NVEND[0]	00000100	04
231	E7	NTSC F bit toggle	RW	NFTOGDELO	NFTOGDELE	NFTOGSIGN	NFTOG[4]	NFTOG[3]	NFTOG[2]	NFTOG[1]	NFTOG[0]	01100011	63
232	E8	PAL V bit begin	RW	PVBEGDELO	PVBEGDELE	PVBEGSIGN	PVBEG[4]	PVBEG[3]	PVBEG[2]	PVBEG[1]	PVBEG[0]	01100101	65
233	E9	PAL V bit end	RW	PVENDDELO	PVENDDELE	PVENDSIGN	PVEND[4]	PVEND[3]	PVEND[2]	PVEND[1]	PVEND[0]	00010100	14
234	EA	PAL F bit toggle	RW	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG[4]	PFTOG[3]	PFTOG[2]	PFTOG[1]	PFTOG[0]	01100011	63
235	EB	Vblank Control 1	RW	NVBIOLCM[1]	NVBIOLCM[0]	NVBIELCM[1]	NVBIELCM[0]	PVBIOLCM[1]	PVBIOLCM[0]	PVBIELCM[1]	PVBIELCM[0]	01010101	55
236	EC	Vblank Control 2	RW	NVBIOCCM[1]	NVBIOCCM[0]	NVBIECCM[1]	NVBIECCM[0]	PVBIOCCM[1]	PVBIOCCM[0]	PVBIECCM[1]	PVBIECCM[0]	01010101	55
243	F3	AFE_CONTROL 1	RW				AA_FILT_MAN_OVR	AA_FILT_EN[3]	AA_FILT_EN[2]	AA_FILT_EN[1]	AA_FILT_EN[0]	00000000	00
244	F4	Drive strength	RW	GLITCH_FILT_BYP		DR_STR[1]	DR_STR[0]	DR_STR_C[1]	DR_STR_C[0]	DR_STR_S[1]	DR_STR_S[0]	0x010101	15
248	F8	IF comp control	RW						IFFILTSEL[2]	IFFILTSEL[1]	IFFILTSEL[0]	00000000	00
249	F9	VS mode control	RW					VS_COAST_MODE[1]	VS_COAST_MODE[0]	EXTEND_VS_MIN_FREQ	EXTEND_VS_MAX_FREQ	00000011	03
251	FB	Peaking gain	RW	PEAKING_GAIN[7]	PEAKING_GAIN[6]	PEAKING_GAIN[5]	PEAKING_GAIN[4]	PEAKING_GAIN[3]	PEAKING_GAIN[2]	PEAKING_GAIN[1]	PEAKING_GAIN[0]	01000000	40
252	FC	DNR Noise Threshold 2	RW	DNR_TH2[7]	DNR_TH2[6]	DNR_TH2[5]	DNR_TH2[4]	DNR_TH2[3]	DNR_TH2[2]	DNR_TH2[1]	DNR_TH2[0]	00000100	04
253	FD	VPP slave address	RW	VPP_SLAVE_ADDR[6]	VPP_SLAVE_ADDR[5]	VPP_SLAVE_ADDR[4]	VPP_SLAVE_ADDR[3]	VPP_SLAVE_ADDR[2]	VPP_SLAVE_ADDR[1]	VPP_SLAVE_ADDR[0]			
254	FE	CSI Tx slave address	RW	CSI_TX_SLAVE_ADDR[6]	CSI_TX_SLAVE_ADDR[5]	CSI_TX_SLAVE_ADDR[4]	CSI_TX_SLAVE_ADDR[3]	CSI_TX_SLAVE_ADDR[2]	CSI_TX_SLAVE_ADDR[1]	CSI_TX_SLAVE_ADDR[0]		00000000	00

To access the registers listed in Table 91, SUB_USR_EN in Register Address 0x0E must be programmed to 10. All read only registers are left blank.

Table 91. User Sub Map 2 Register Map Details

Address													Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0		Value	(Hex)
128	80	ACE Control 1	RW	ACE_ENABLE									00000000	00
131	83	ACE Control 4	RW				ACE_LUMA_ GAIN[4]	ACE_LUMA_ GAIN[3]	ACE_LUMA_ GAIN[2]	ACE_LUMA_ GAIN[1]	ACE_LUMA_ GAIN[0]		00001101	0D
132	84	ACE Control 5	RW	ACE_CHROMA_ MAX[3]	ACE_CHROMA_ MAX[2]	ACE_CHROMA_ MAX[1]	ACE_CHROMA_ MAX[0]	ACE_CHROMA_ GAIN[3]	ACE_CHROMA_ GAIN[2]	ACE_CHROMA_ GAIN[1]	ACE_CHROMA_ GAIN[0]		10001000	88
133	85	ACE Control 6	RW	ACE_RESPONSE_ SPEED[3]	ACE_RESPONSE_ SPEED[2]	ACE_RESPONSE_ SPEED[2]	ACE_RESPONSE _SPEED[1]	ACE_GAMMA_ GAIN[3]	ACE_GAMMA_ GAIN[2]	ACE_GAMMA_ GAIN[1]	ACE_GAMMA_ GAIN[0]		11111000	F8
146	92	Dither control	RW								BR_DITHER_ MODE		00000000	00
217	D9	Min Max 0	RW	MIN_THRESH_Y[7]	MIN_THRESH_Y[6]	MIN_THRESH_Y[5]	MIN_THRESH_ Y[4]	MIN_THRESH_Y[3]	MIN_THRESH_Y[2]	MIN_THRESH_ Y[1]	MIN_THRESH_ Y[0]		00000000	00
218	DA	Min Max 1	RW	MAX_THRESH_Y[7]	MAX_THRESH_Y[6]	MAX_THRESH_Y[5]	MAX_THRESH_ Y[4]	MAX_THRESH_Y[3]	MAX_THRESH_Y[2]	MAX_THRESH_ Y[1]	MAX_THRESH_ Y[0]		11111111	FF
219	DB	Min Max 2	RW	MIN_THRESH_C[7]	MIN_THRESH_C[6]	MIN_THRESH_C[5]	MIN_THRESH_ C[4]	MIN_THRESH_C[3]	MIN_THRESH_C[2]	MIN_THRESH_ C[1]	MIN_THRESH_ C[0]		00000000	00
220	DC	Min Max 3	RW	MAX_THRESH_C[7]	MAX_THRESH_C[6]	MAX_THRESH_C[5]	MAX_THRESH_ C[4]	MAX_THRESH_C[3]	MAX_THRESH_C[2]	MAX_THRESH_ C[1]	MAX_THRESH_ C[0]		11111111	FF
221	DD	Min Max 4	RW	MIN_SAMPLES_ ALLOWED_Y[3]	MIN_SAMPLES_ ALLOWED_Y[2]	MIN_SAMPLES_ ALLOWED_Y[1]	MIN_SAMPLES_ ALLOWED_Y[0]	MAX_SAMPLES_ ALLOWED_Y[3]	MAX_SAMPLES_ ALLOWED_Y[2]	MAX_SAMPLES _ALLOWED_Y[1]	MAX_SAMPLES _ALLOWED_Y[0]		11001100	CC
222	DE	Min Max 5	RW	MIN_SAMPLES_ ALLOWED_C[3]	MIN_SAMPLES_ ALLOWED_C[2]	MIN_SAMPLES_ ALLOWED_C[1]	MIN_SAMPLES_ ALLOWED_C[0]	MAX_SAMPLES_ ALLOWED_C[3]	MAX_SAMPLES_ ALLOWED_C[2]	MAX_SAMPLES_ ALLOWED_C[1]	MAX_SAMPLES_ ALLOWED_C[0]		11001100	CC
224	E0	FL control	RW								FL_ENABLE		00000000	00
225	E1	Y Average 0	RW	LINE_START[8]	LINE_START[7]	LINE_START[6]	LINE_START[5]	LINE_START[4]	LINE_START[3]	LINE_START[2]	LINE_START[1]		0001001	11
226	E2	Y Average 1	RW	LINE_END[8]	LINE_END[7]	LINE_END[6]	LINE_END[5]	LINE_END[4]	LINE_END[3]	LINE_END[2]	LINE_END[1]		10001000	88
227	E3	Y Average 2	RW	SAMPLE_START[9]	SAMPLE_START[8]	SAMPLE_START[7]	SAMPLE_ START[6]	SAMPLE_START[5]	SAMPLE_ START[4]	SAMPLE_ START[3]	SAMPLE_ START[2]		00010111	1B
228	E4	Y Average 3	RW	SAMPLE_END[9]	SAMPLE_END[8]	SAMPLE_END[7]	SAMPLE_END[6]	SAMPLE_END[5]	SAMPLE_END[4]	SAMPLE_END[3]	SAMPLE_END[2]		11010111	D7
229	E5	Y Average 4	RW	SAMPLE_END[1]	SAMPLE_END[0]	SAMPLE_START[1]	SAMPLE_ START[0]			LINE_END[0]	LINE_START[0]		00100011	23
230	E6	Y Average 5	RW				Y_AVG_TIME_ CONST[2]	Y_AVG_TIME_ CONST[1]	Y_AVG_TIME_ CONST[0]	Y_AVG_FILT_EN	CAPTURE_ VALUE		00010000	10
231	E7	Y average data MSB	R	Y_AVERAGE[9]	Y_AVERAGE[8]	Y_AVERAGE[7]	Y_AVERAGE[6]	Y_AVERAGE[5]	Y_AVERAGE[4]	Y_AVERAGE[3]	Y_AVERAGE[2]			
232	E8	Y average data LSB	R							Y_AVERAGE[1]	Y_AVERAGE[0]			

To access the registers listed in Table 92, SUB_USR_EN in Register Address 0x0E must be programmed to 01. All read only registers are left blank.

Table 92. Interrupt/VDP Sub Map Details

Address													
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value[1]	(Hex)
64	40	Interrupt Configuration 1	RW	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	MV_INTRQ_SEL[1]	MV_INTRQ_SEL[0]		MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]	0001x000	10
66	42	Interrupt Status 1	R		MV_PS_CS_Q	SD_FR_CHNG_Q				SD_UNLOCK_Q	SD_LOCK_Q		
67	43	Interrupt Clear 1	W		MV_PS_CS_CLR	SD_FR_CHNG_CLR				SD_UNLOCK_CLR	SD_LOCK_CLR	x0000000	00
68	44	Interrupt Mask 1	RW		MV_PS_CS_MSKB[2]	SD_FR_CHNG_MSKB[2]				SD_UNLOCK_MSKB[2]	SD_LOCK_MSKB[2]	x0000000	00
69	45	Raw Status 2	R	MPU_STIM_INTRQ		CHX_MIN_MAX_INTRQ	EVEN_FIELD				CCAPD		
70	46	Interrupt Status 2	R	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q				CCAPD_Q		
71	47	Interrupt Clear 2	W	MPU_STIM_INTRQ_CLR		CHX_MIN_MAX_INTRQ_CLR	SD_FIELD_CHNGD_CLR				CCAPD_CLR	0xx00000	00
72	48	Interrupt Mask 2	RW	MPU_STIM_INTRQ_MSKB[2]		CHX_MIN_MAX_INTRQ_MSKB[2]	SD_FIELD_CHNGD_MSKB[2]				CCAPD_MSKB[2]	0xx00000	00
73	49	Raw Status 3	R				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz		
74	4A	Interrupt Status 3	R			PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q		
75	4B	Interrupt Clear 3	W			PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	xx000000	00
76	4C	Interrupt Mask 3	RW			PAL_SW_LK_CHNG_MSKB[2]	SCM_LOCK_CHNG_MSKB[2]	SD_AD_CHNG_MSKB[2]	SD_H_LOCK_CHNG_MSKB[2]	SD_V_LOCK_CHNG_MSKB[2]	SD_OP_CHNG_MSKB[2]	xx000000	00
78	4E	Interrupt Status 4	R						VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q		
79	4F	Interrupt Clear 4	W						VDP_CGMS_WSS_CHNGD_CLR		VDP_CCAPD_CLR	00x0x0x0	00
80	50	Interrupt Mask 4	RW						VDP_CGMS_WSS_CHNGD_MSKB[2]		VDP_CCAPD_MSKB[2]	00x0x0x0	00
81	51	Interrupt Latch 0	R			Y_CHANNEL_MIN_VIOLATION	Y_CHANNEL_MAX_VIOLATION	CB_CHANNEL_MIN_VIOLATION	CB_CHANNEL_MAX_VIOLATION	CR_CHANNEL_MIN_VIOLATION	CR_CHANNEL_MAX_VIOLATION		
96	60	VDP_CONFIG_1	RW					WST_PKT_DECODE_DISABLE	VDP_TTXT_TYPE_MAN_ENABLE	VDP_TTXT_TYPE_MAN[1]	VDP_TTXT_TYPE_MAN[0]	10001000	88
98	62	VDP_ADF_CONFIG_1	RW	ADF_ENABLE	ADF_MODE[1]	ADF_MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]	00010101	15
99	63	VDP_ADF_CONFIG_2	RW	DUPLICATE_ADF		ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]	0x101010	2A
100	64	VDP_LINE_00E	RW	MAN_LINE_PGM				VBI_DATA_P318[3]	VBI_DATA_P318[2]	VBI_DATA_P318[1]	VBI_DATA_P318[0]	0xxx0000	00
101	65	VDP_LINE_00F	RW	VBI_DATA_P6_N23[3]	VBI_DATA_P6_N23[2]	VBI_DATA_P6_N23[1]	VBI_DATA_P6_N23[0]	VBI_DATA_P319_N286[3]	VBI_DATA_P319_N286[2]	VBI_DATA_P319_N286[1]	VBI_DATA_P319_N286[0]	00000000	00
102	66	VDP_LINE_010	RW	VBI_DATA_P7_N24[3]	VBI_DATA_P7_N24[2]	VBI_DATA_P7_N24[1]	VBI_DATA_P7_N24[0]	VBI_DATA_P320_N287[3]	VBI_DATA_P320_N287[2]	VBI_DATA_P320_N287[1]	VBI_DATA_P320_N287[0]	00000000	00
103	67	VDP_LINE_011	RW	VBI_DATA_P8_N25[3]	VBI_DATA_P8_N25[2]	VBI_DATA_P8_N25[1]	VBI_DATA_P8_N25[0]	VBI_DATA_P321_N288[3]	VBI_DATA_P321_N288[2]	VBI_DATA_P321_N288[1]	VBI_DATA_P321_N288[0]	00000000	00
104	68	VDP_LINE_012	RW	VBI_DATA_P9[3]	VBI_DATA_P9[2]	VBI_DATA_P9[1]	VBI_DATA_P9[0]	VBI_DATA_P322[3]	VBI_DATA_P322[2]	VBI_DATA_P322[1]	VBI_DATA_P322[0]	00000000	00
105	69	VDP_LINE_013	RW	VBI_DATA_P10[3]	VBI_DATA_P10[2]	VBI_DATA_P10[1]	VBI_DATA_P10[0]	VBI_DATA_P323[3]	VBI_DATA_P323[2]	VBI_DATA_P323[1]	VBI_DATA_P323[0]	00000000	00
106	6A	VDP_LINE_014	RW	VBI_DATA_P11[3]	VBI_DATA_P11[2]	VBI_DATA_P11[1]	VBI_DATA_P11[0]	VBI_DATA_P324_N272[3]	VBI_DATA_P324_N272[2]	VBI_DATA_P324_N272[1]	VBI_DATA_P324_N272[0]	00000000	00
107	6B	VDP_LINE_015	RW	VBI_DATA_P12_N10[3]	VBI_DATA_P12_N10[2]	VBI_DATA_P12_N10[1]	VBI_DATA_P12_N10[0]	VBI_DATA_P325_N273[3]	VBI_DATA_P325_N273[2]	VBI_DATA_P325_N273[1]	VBI_DATA_P325_N273[0]	00000000	00
108	6C	VDP_LINE_016	RW	VBI_DATA_P13_N11[3]	VBI_DATA_P13_N11[2]	VBI_DATA_P13_N11[1]	VBI_DATA_P13_N11[0]	VBI_DATA_P326_N274[3]	VBI_DATA_P326_N274[2]	VBI_DATA_P326_N274[1]	VBI_DATA_P326_N274[0]	00000000	00
109	6D	VDP_LINE_017	RW	VBI_DATA_P14_N12[3]	VBI_DATA_P14_N12[2]	VBI_DATA_P14_N12[1]	VBI_DATA_P14_N12[0]	VBI_DATA_P327_N275[3]	VBI_DATA_P327_N275[2]	VBI_DATA_P327_N275[1]	VBI_DATA_P327_N275[0]	00000000	00
110	6E	VDP_LINE_018	RW	VBI_DATA_P15_N13[3]	VBI_DATA_P15_N13[2]	VBI_DATA_P15_N13[1]	VBI_DATA_P15_N13[0]	VBI_DATA_P328_N276[3]	VBI_DATA_P328_N276[2]	VBI_DATA_P328_N276[1]	VBI_DATA_P328_N276[0]	00000000	00
111	6F	VDP_LINE_019	RW	VBI_DATA_P16_N14[3]	VBI_DATA_P16_N14[2]	VBI_DATA_P16_N14[1]	VBI_DATA_P16_N14[0]	VBI_DATA_P329_N277[3]	VBI_DATA_P329_N277[2]	VBI_DATA_P329_N277[1]	VBI_DATA_P329_N277[0]	00000000	00
112	70	VDP_LINE_01A	RW	VBI_DATA_P17_N15[3]	VBI_DATA_P17_N15[2]	VBI_DATA_P17_N15[1]	VBI_DATA_P17_N15[0]	VBI_DATA_P330_N278[3]	VBI_DATA_P330_N278[2]	VBI_DATA_P330_N278[1]	VBI_DATA_P330_N278[0]	00000000	00
113	71	VDP_LINE_01B	RW	VBI_DATA_P18_N16[3]	VBI_DATA_P18_N16[2]	VBI_DATA_P18_N16[1]	VBI_DATA_P18_N16[0]	VBI_DATA_P331_N279[3]	VBI_DATA_P331_N279[2]	VBI_DATA_P331_N279[1]	VBI_DATA_P331_N279[0]	00000000	00
114	72	VDP_LINE_01C	RW	VBI_DATA_P19_N17[3]	VBI_DATA_P19_N17[2]	VBI_DATA_P19_N17[1]	VBI_DATA_P19_N17[0]	VBI_DATA_P332_N280[3]	VBI_DATA_P332_N280[2]	VBI_DATA_P332_N280[1]	VBI_DATA_P332_N280[0]	00000000	00
115	73	VDP_LINE_01D	RW	VBI_DATA_P20_N18[3]	VBI_DATA_P20_N18[2]	VBI_DATA_P20_N18[1]	VBI_DATA_P20_N18[0]	VBI_DATA_P333_N281[3]	VBI_DATA_P333_N281[2]	VBI_DATA_P333_N281[1]	VBI_DATA_P333_N281[0]	00000000	00
116	74	VDP_LINE_01E	RW	VBI_DATA_P21_N19[3]	VBI_DATA_P21_N19[2]	VBI_DATA_P21_N19[1]	VBI_DATA_P21_N19[0]	VBI_DATA_P334_N282[3]	VBI_DATA_P334_N282[2]	VBI_DATA_P334_N282[1]	VBI_DATA_P334_N282[0]	00000000	00

Address													
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value[1]	(Hex)
117	75	VDP_LINE_01F	RW	VBI_DATA_ P22_N20[3]	VBI_DATA_ P22_N20[2]	VBI_DATA_ P22_N20[1]	VBI_DATA_ P22_N20[0]	VBI_DATA_ P335_N283[3]	VBI_DATA_ P335_N283[2]	VBI_DATA_ P335_N283[1]	VBI_DATA_ P335_N283[0]	00000000	00
118	76	VDP_LINE_020	RW	VBI_DATA_ P23_N21[3]	VBI_DATA_ P23_N21[2]	VBI_DATA_ P23_N21[1]	VBI_DATA_ P23_N21[0]	VBI_DATA_ P336_N284[3]	VBI_DATA_ P336_N284[2]	VBI_DATA_ P336_N284[1]	VBI_DATA_ P336_N284[0]	00000000	00
119	77	VDP_LINE_021	RW	VBI_DATA_ P24_N22[3]	VBI_DATA_ P24_N22[2]	VBI_DATA_ P24_N22[1]	VBI_DATA_ P24_N22[0]	VBI_DATA_ P337_N285[3]	VBI_DATA_ P337_N285[2]	VBI_DATA_ P337_N285[1]	VBI_DATA_ P337_N285[0]	00000000	00
120	78	VDP_STATUS	R	TTXT_AVL					CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL		
120	78	VDP_STATUS_ CLEAR	W						CGMS_WSS_ CLEAR		CC_CLEAR	00000000	00
121	79	VDP_CCAP_ DATA_0	R	CCAP_BYTE_1[7]	CCAP_BYTE_1[6]	CCAP_BYTE_1[5]	CCAP_BYTE_1[4]	CCAP_BYTE_1[3]	CCAP_BYTE_1[2]	CCAP_BYTE_1[1]	CCAP_BYTE_1[0]		
122	7A	VDP_CCAP_ DATA_1	R	CCAP_BYTE_2[7]	CCAP_BYTE_2[6]	CCAP_BYTE_2[5]	CCAP_BYTE_2[4]	CCAP_BYTE_2[3]	CCAP_BYTE_2[2]	CCAP_BYTE_2[1]	CCAP_BYTE_2[0]		
125	7D	VDP_CGMS_ WSS_DATA_0	R					CGMS_CRC[5]	CGMS_CRC[4]	CGMS_CRC[3]	CGMS_CRC[2]		
126	7E	VDP_CGMS_ WSS_DATA_1	R	CGMS_CRC[1]	CGMS_CRC[0]	CGMS_WSS[13]	CGMS_WSS[12]	CGMS_WSS[11]	CGMS_WSS[10]	CGMS_WSS[9]	CGMS_WSS[8]		
127	7F	VDP_CGMS_ WSS_DATA_2	R	CGMS_WSS[7]	CGMS_WSS[6]	CGMS_WSS[5]	CGMS_WSS[4]	CGMS_WSS[3]	CGMS_WSS[2]	CGMS_WSS[1]	CGMS_WSS[0]		
156	9C	VDP_OUTPUT_SEL	RW				WSS_CGMS_CB_ CHANGE					00110000	30

[1] x in a reset value indicates do not care.
[2] B at the end of the bit name equals an overbar for the whole bit name.

To access the registers listed in Table 93 the VPP I²C slave address needs to be set. The VPP Map address is set by writing to register 0xFD in the User Map. See the I²C Port Description section. All read only registers are left blank.

Table 93. VPP Map Details

Address													
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
65	41	DEINT_RESET	RW								DEINT_RESET	00000000	00
85	55	I2C_DEINT_ ENABLE	RW	I2C_DEINT_ ENABLE								00000000	00
91	5B	ADV_TIMING_ MODE_EN	RW	ADV_TIMING_ MODE_EN								10000000	00

To access the registers listed in Table 94, the CSI I²C slave address needs to be set. The CSI Map address is set by writing to register 0xFE in the User Map. See the I²C Port Description section. All read only registers are left blank.

Table 94. CSI Map Details

Address												Reset	
Dec	Hex	Register Name	RW	7	6	5	4	3	2	1	0	Value	(Hex)
00	0x00	CSITX_PWRDN	RW	CSITX_PWRDN								10000000	0x80
01	0x01	TLPX	RW	TLPX[4]	TLPX[3]	TLPX[2]	TLPX[1]	TLPX[0]				00011000	0x18
02	0x02	THSPREP	RW	THSPREP[4]	THSPREP[3]	THSPREP[2]	THSPREP[1]	THSPREP[0]				00011000	0x18
03	0x03	THSZEROS	RW	THSZEROS[4]	THSZEROS[3]	THSZEROS[2]	THSZEROS[1]	THSZEROS[0]				00110000	0x30
04	0x04	THSTRAIL	RW	THSTRAIL[4]	THSTRAIL[3]	THSTRAIL[2]	THSTRAIL[1]	THSTRAIL[0]				00100000	0x20
05	0x05	THSEXIT	RW	THSEXIT[4]	THSEXIT[3]	THSEXIT[2]	THSEXIT[1]	THSEXIT[0]				00101000	0x28
06	0x06	TCLK_PREP	RW	TCLK_PREP[2]	TCLK_PREP[1]	TCLK_ PREP[0]						01000000	0x40
07	0x07	TCLK_ZEROS	RW	TCLK_ZEROS[4]	TCLK_ZEROS[3]	TCLK_ ZEROS[2]	TCLK_ZEROS[1]	TCLK_ ZEROS[0]				01011000	0x58
08	0x08	TCLK_TRAIL	RW	TCLK_TRAIL[3]	TCLK_TRAIL[2]	TCLK_ TRAIL[1]	TCLK_TRAIL[0]					00110000	0x30
09	0x09	ANCILLARY_DI	RW	ANCILLARY_DI[5]	ANCILLARY_ DI[4]	ANCILLARY_ DI[3]	ANCILLARY_ DI[2]	ANCILLARY_ DI[1]	ANCILLARY_ DI[0]			11000000	0xC0
10	0x0A	VBIVIDEO_DI	RW	VBIVIDEO_DI[5]	VBIVIDEO_DI[4]	VBIVIDEO_ DI[3]	VBIVIDEO_DI[2]	VBIVIDEO_ DI[1]	VBIVIDEO_ DI[0]			11000100	0xC4
11	0x0B	LSPKT_DI	RW	LSPKT_DI[5]	LSPKT_DI[4]	LSPKT_DI[3]	LSPKT_DI[2]	LSPKT_DI[1]	LSPKT_DI[0]			00001000	0x08
12	0x0C	LEPKT_DI	RW	LEPKT_DI[5]	LEPKT_DI[4]	LEPKT_DI[3]	LEPKT_DI[2]	LEPKT_DI[1]	LEPKT_DI[0]			00001100	0x0C
13	0x0D	VC_REF	RW	VC_REF[1]	VC_REF[0]							00000000	0x00
14	0x0E	CKSUM_EN	RW	CKSUM_EN								10000000	0x80
31	0x1F	CSI_FRAME_NUM_ CTL	RW	FRAMENUMBER_ INTERLACED	FBIT_VAL_AT_ FIELD1START_ INTERLACED							01000000	0x40
32	0x20	CSI_LINENUM_ INCR_INTERLACED	RW	LINENUMBER_ INCR_ INTERLACED								00000000	0x00
33	0x21	LINENUMBER1_F1_ INTERLACED	RW	LINENUMBER1 _F1_ INTERLACED[7]	LINENUMBER1 _F1_ INTERLACED[6]	LINENUMBER1 _F1_ INTERLACED[5]	LINENUMBER1 _F1_ INTERLACED[4]	LINENUMBER1 _FF1_ INTERLACED[3]	LINENUMBER1 _F1_ INTERLACED[2]	LINENUMBER1 _F1_ INTERLACED[1]	LINENUMBER1 _F1_ INTERLACED[0]	00000011	0x03
34	0x22	LINENUMBER1_F2_ INTERLACED	RW	LINENUMBER1 _F2_ INTERLACED[7]	LINENUMBER1 _F2_ INTERLACED[6]	LINENUMBER1 _F2_ INTERLACED[5]	LINENUMBER1 _F2_ INTERLACED[4]	LINENUMBER1 _FF2_ INTERLACED[3]	LINENUMBER1 _F2_ INTERLACED[2]	LINENUMBER1 _F2_ INTERLACED[1]	LINENUMBER1 _F2_ INTERLACED[0]	00000010	0x02
38	0x26	ESC_MODE_CTL	RW	ESC_MODE_EN_ D0	ESC_ XSHUTDOWN_ D0	ESC_MODE_ EN_CLK	ESC_ XSHUTDOWN_ CLK	EN_ESC_CMD _CLK_LANE				01010000	0x50
222	0xDE	DPHY_PWDN_CTL	RW							DPHY_PWDN_ OVERRIDE	DPHY_PWDN	00000001	0x01

USER SUB MAP DESCRIPTION

To access all the registers listed in Table 95, SUB_USR_EN in Register Address 0x0E must be programmed to 00. The gray shading is the default.

Table 95. User Sub Map Register Descriptions

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x00	Input control	INSEL[4:0]; the INSEL bits allow the user to select an input channel and the input format				0	0	0	0	0	CVBS input on $A_{IN}1$	
						0	0	0	0	1	CVBS input on $A_{IN}2$	
						0	0	0	1	0	CVBS input on $A_{IN}3$	
						0	0	0	1	1	CVBS input on $A_{IN}4$	
						0	1	0	0	0	Y input on $A_{IN}1$, C input on $A_{IN}2$	
						0	1	0	0	1	Y input on $A_{IN}3$, C input on $A_{IN}4$	
						0	1	1	0	0	Y input on $A_{IN}1$, Pb input on $A_{IN}2$, Pr input on $A_{IN}3$	
						0	1	1	1	0	Differential positive on $A_{IN}1$, differential negative on $A_{IN}2$	
						0	1	1	1	1	Differential positive on $A_{IN}3$, differential negative on $A_{IN}4$	
0x01	Video Selection 1	Reserved						0	0	0	Sets to default	
		ENVSPROC					0				Disables VSYNC processor	
							1				Enables VSYNC processor	
		Reserved				0					Sets to default	
		BETACAM; enables BETACAM levels			0						Standard video input	
					1						Betacam input enable	
		ENHSPLL		0							Disables HSYNC processor	
				1							Enables HSYNC processor	
		Reserved	1								Sets to default	
0x02	Video Selection 2	Reserved					0	1	0	0	Set to default	
		VID_SEL[3:0]; the VID_SEL bits allow the user to select the input video standard	0	0	0	0					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC J (no pedestal), SECAM	
			0	0	0	1					Autodetects PAL B/PAL G/PAL H/ PAL I/PAL D, NTSC M (pedestal), SECAM	
			0	0	1	0					Autodetects PAL N (pedestal), NTSC J (no pedestal), SECAM	
			0	0	1	1					Autodetects PAL N (pedestal), NTSC M (pedestal) SECAM	
			0	1	0	0					NTSC J	
			0	1	0	1					NTSC M	
			0	1	1	0					PAL 60	
			0	1	1	1					NTSC 4.43	
			1	0	0	0					PAL B/G/H/I/D	
			1	0	0	1					PAL N = PAL B/PAL G/PAL H/ PAL I/PAL D (with pedestal)	
			1	0	1	0					PAL M (without pedestal)	
			1	0	1	1					PAL M	
			1	1	0	0					PAL Combination N	
			1	1	0	1					PAL Combination N (with pedestal)	
			1	1	1	0					SECAM	
			1	1	1	1					SECAM	
0x03	Output control	Reserved			0	0	1	1	0	0	Reserved	
		TOD; tristate output drivers; this bit allows the user to tristate the output drivers; pixel outputs, HS and VS/FIELD/SFL		0							Output drivers enabled	See also TIM_OE and TRI_LLC
				1							Output drivers tristated	
		VBI_EN; vertical blanking interval data enable; allows VBI data (Line 1 to Line 21) to be passed through with only a minimum amount of filtering performed	0								All lines filtered and scaled	
			1								Only active video region filtered	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x04	Extended output control	Range; allows the user to select the range of output values; can be ITU-R BT.656 compliant or can fill the whole accessible number range								0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240	ITU-R BT.656
										1	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254	Extended range
		EN_SFL_PIN							0		Disables SFL output	SFL output enables encoder and decoder to be connected directly
									1		Outputs SFL information on the SFL pin	
		BL_C_VBI; blank chroma during VBI; if set, it enables data in the VBI region to be passed through the decoder undistorted						0			Decode and output color during VBI	during VBI
								1			Blank Cr and Cb values during VBI	
		TIM_OE; enables timing signals output					0				HS, VS, FIELD tristated	Controlled by TOD
							1				HS, VS, FIELD forced active	
		Reserved		0	1	1						
		BT.656-4; allows the user to select an output mode compatible with ITU-R BT.656-3/-4	0								ITU-R BT.656-3 compatible	
			1								ITU-R BT.656-4 compatible	
0x07	Autodetect enable	AD_PAL_EN; PAL B/PAL D/PAL I/ PAL G/PAL H autodetect enable								0	Disables	
										1	Enables	
		AD_NTSC_EN; NTSC autodetect enable							0		Disables	
									1		Enables	
		AD_PALM_EN; PAL M autodetect enable						0			Disables	
								1			Enables	
		AD_PALN_EN; PAL N autodetect enable					0				Disables	
							1				Enables	
		AD_P60_EN; PAL 60 autodetect enable				0					Disables	
						1					Enables	
		AD_N443_EN; NTSC 4.43 autodetect enable			0						Disables	
					1						Enables	
		AD_SECAM_EN; SECAM autodetect enable		0							Disables	
				1							Enables	
		AD_SEC525_EN; SECAM 525 autodetect enable	0								Disables	
			1								Enables	
0x08	Contrast	CON[7:0]; contrast adjust; this is the user control for contrast adjustment	1	0	0	0	0	0	0	0	Luma gain = 1	0x00 gain = 0, 0x80 gain = 1, 0xFF gain = 2
0x0A	Brightness adjust	BRI[7:0]; this register controls the brightness of the video signal	0	0	0	0	0	0	0	0		0x00 = 0 IRE, 0x7F = +30 IRE, 0x80 = −30 IRE
0x0B	Hue adjust	HUE[7:0]; this register contains the value for the color hue adjustment	0	0	0	0	0	0	0	0		Hue range = −90° to +90°
0x0C	Default Value Y	DEF_VAL_EN; default value enable								0	Free-run mode dependent on DEF_VAL_AUTO_EN	
										1	Forces free-run mode on	
		DEF_VAL_AUTO_EN; default value automatic enable							0		Disables free-run mode	When lock is lost, free-run mode can be enabled to output stable timing, clock, and a set color
									1		Enables automatic free-run mode	
		DEF_Y[5:0]; default value is Y; this register holds the Y default value	0	0	1	1	0	1			Y[7:0] = {DEF_Y[5:0], 0, 0}	Default Y value output in free-run mode
0x0D	Default Value C	DEF_C[7:0]; default value is C; the Cr and Cb default values are defined in this register	0	1	1	1	1	1	0	0	Cr[3:0] = {DEF_C[7:4]}, Cb[3:0] = {DEF_C[3:0]}	Default Cb/Cr value output in free-run mode; default values give blue screen output

User Sub Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x0E	ADI Control 1	Reserved				0	0	0	0	0	Sets as default	
		SUB_USR_EN[1:0]; enables user to access the interrupt/VDP map and User Sub Map 2		0	0						Accesses main register space	See Figure 42
				0	1						Accesses interrupt/VDP register space	
				1	0						Accesses User Sub Map 2	
		Reserved	0								Sets as default	
0x0F	Power management	Reserved							0	0	Sets to default	
		Reserved				0	0				Sets to default	
		PWRDWN; power-down places the decoder into a full power-down mode			0						System functional	
					1						Powered down	
		Reserved		0							Sets to default	
		Reset; chip reset, loads all I^2C bits with default values	0								Normal operation	
			1								Starts reset sequence	Executing reset takes approximately 2 ms; this bit is self-clearing
0x10	Status 1 (read only)	IN_LOCK								x	1 = in lock (now)	Provides info about the internal status of the decoder
		LOST_LOCK							x		1 = lost lock (since last read)	
		FSC_LOCK						x			1 = f_{SC} lock (now)	
		FOLLOW_PW					x				1 = peak white AGC mode active	
		AD_RESULT[2:0]; autodetection result reports the standard of the input video		0	0	0					NTSC M/NTSC J	Detected standard
				0	0	1					NTSC 4.43	
				0	1	0					PAL M	
				0	1	1					PAL 60	
				1	0	0					PAL B/PAL G/PAL H/PAL I/PAL D	
				1	0	1					SECAM	
				1	1	0					PAL Combination N	
				1	1	1					SECAM 525	
		COL_KILL	x								1 = color kill is active	Color kill
0x11	IDENT (read only)	IDENT[7:0]; provides ID on the revision of the part	0	1	0	0	0	0	1	0		Power-up value = 0x42
0x12	Status 2 (read only)	MVCS DET								x	MV color striping detected	1 = detected
		MVCS T3							x		MV color striping type	0 = Type 2, 1 = Type 3
		MV PS DET						x			MV pseudosync detected	1 = detected
		MV AGC DET					x				MV AGC pulses detected	1 = detected
		LL NSTD				x					Nonstandard line length	1 = detected
		FSC NSTD			x						f_{SC} frequency nonstandard	1 = detected
		Reserved	x	x								

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x13	Status 3 (read only)	INST_HLOCK								x	1 = horizontal lock achieved	Unfiltered
		Reserved							x		Reserved	
		SD_OP_50Hz						0			SD 60 Hz detected	SD field rate detect
								1			SD 50 Hz detected	
		Reserved					x					
		FREE_RUN_ACT				x					1 = free-run mode active	
		STD FLD LEN			x						1 = field length standard	Correct field length found
		Interlaced		x							1 = interlaced video detected	Field sequence found
		PAL_SW_LOCK	x								1 = swinging burst detected	Reliable swinging burst sequence
0x14	Analog clamp control	FREE_RUN_PAT_SEL[2:0]						0	0	0	Single color set by DEF_C and DEF_Y; see the Color Controls section	
								0	0	1	100% color bars	
								0	1	0	Luma ramp	
								1	0	1	Boundary box	
		Reserved					0				Sets to default	
		CCLEN; current clamp enable allows the user to switch off the current sources in the analog front				0					Current sources switched off	
						1					Current sources enabled	
		Reserved	0	0	0						Sets to default	
0x15	Digital Clamp Control 1	Reserved					x	x	x	x	Sets to default	
		DCFE; digital clamp freeze enable				0					Digital clamp on	
						1					Digital clamp off	
		DCT[1:0]; digital clamp timing determines the time constant of the digital fine clamp circuitry		0	0						Slow (TC = 1 sec)	
				0	1						Medium (TC = 0.5 sec)	
				1	0						Fast (TC = 0.1 sec)	
				1	1						TC dependent on video	
		Reserved	0								Set to default	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x17	Shaping Filter Control 1	YSFM[4:0]; selects Y shaping filter mode in CVBS-only mode; allows the user to select a wide range of low-pass/notch filters; if either auto mode is selected, the decoder selects the optimum Y filter depending on the CVBS video source quality (good vs. poor)				0	0	0	0	0	Autowide notch for poor quality sources or wideband filter with comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality
						0	0	0	0	1	Autonarrow notch for poor quality sources or wideband filter with comb for good quality input	
						0	0	0	1	0	SVHS 1	If one of these modes is selected, the decoder does not change filter modes; depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	PAL NN1	
						1	0	1	0	1	PAL NN2	
						1	0	1	1	0	PAL NN3	
						1	0	1	1	1	PAL WN1	
						1	1	0	0	0	PAL WN2	
						1	1	0	0	1	NTSC NN1	
						1	1	0	1	0	NTSC NN2	
						1	1	0	1	1	NTSC NN3	
						1	1	1	0	0	NTSC WN1	
						1	1	1	0	1	NTSC WN2	
						1	1	1	1	0	NTSC WN3	
						1	1	1	1	1	Reserved	
		CSFM[2:0]: C shaping filter mode allows selection from a range of low-pass chrominance filters; if either auto mode is selected, the decoder selects the optimum C filter depending on the CVBS video source quality (good vs. bad); nonauto settings force a C filter for all standards and quality of CVBS video	0	0	0						Autoselection 1.5 MHz	Automatically selects a C filter based on video standard and quality
			0	0	1						Autoselection 2.17 MHz	
			0	1	0						SH1	Selects a C filter for all video standards and for good and bad video
			0	1	1						SH2	
			1	0	0						SH3	
			1	0	1						SH4	
			1	1	0						SH5	
			1	1	1						Wideband mode	

User Sub Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x18	Shaping Filter Control 2	WYSFM[4:0]; wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPrPb, B/W input signals; it is also used when a good quality input CVBS signal is detected; for all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0]				0	0	0	0	0	Reserved, do not use	
						0	0	0	0	1	Reserved, do not use	
						0	0	0	1	0	SVHS 1	
						0	0	0	1	1	SVHS 2	
						0	0	1	0	0	SVHS 3	
						0	0	1	0	1	SVHS 4	
						0	0	1	1	0	SVHS 5	
						0	0	1	1	1	SVHS 6	
						0	1	0	0	0	SVHS 7	
						0	1	0	0	1	SVHS 8	
						0	1	0	1	0	SVHS 9	
						0	1	0	1	1	SVHS 10	
						0	1	1	0	0	SVHS 11	
						0	1	1	0	1	SVHS 12	
						0	1	1	1	0	SVHS 13	
						0	1	1	1	1	SVHS 14	
						1	0	0	0	0	SVHS 15	
						1	0	0	0	1	SVHS 16	
						1	0	0	1	0	SVHS 17	
						1	0	0	1	1	SVHS 18 (CCIR 601)	
						1	0	1	0	0	Reserved, do not use	
						~	~	~	~	~	Reserved, do not use	
						1	1	1	1	1	Reserved, do not use	
		Reserved		0	0						Set to default	
		WYSFMOVR; enables use of the automatic WYSFM filter	0								Autoselection of best filter	
			1								Manual select filter using WYSFM[4:0]	
0x19	Comb filter control	PSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (PAL)							0	0	Narrow	
									0	1	Medium	
									1	0	Wide	
									1	1	Widest	
		NSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (NTSC)					0	0			Narrow	
							0	1			Medium	
							1	0			Medium	
							1	1			Wide	
		Reserved	1	1	1	1						
0x1D	ADI Control 2	Reserved			0	0	0	x	x	x		
		Reserved		1								
		TRI_LLC; tristate LLC driver	0								LLC pin active	
			1								LLC pin tristated	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x27	Pixel delay control	LTA[1:0]; luma timing adjust allows the user to specify a timing difference between chroma and luma samples							0	0	No delay	CVBS mode, LTA[1:0] = 00b, Y/C mode, LTA[1:0] = 01b, YPrPb mode, LTA[1:0] = 01b
									0	1	Luma one clock (37 ns) late	
									1	0	Luma two clocks (74 ns) early	
									1	1	Luma one clock (37 ns) early	
		Reserved						0			Sets to 0	
		CTA[2:0]; chroma timing adjust allows a specified timing difference between the luma and chroma samples			0	0	0				Reserved	CVBS mode CTA[2:0] = 011b, Y/C mode, CTA[2:0] = 101b, YPrPb mode, CTA[2:0] = 110b
					0	0	1				Chroma + two pixels (early)	
					0	1	0				Chroma + one pixel (early)	
					0	1	1				No delay	
					1	0	0				Chroma – one pixel (late)	
					1	0	1				Chroma – two pixels (late)	
					1	1	0				Chroma – three pixels (late)	
					1	1	1				Reserved	
		AUTO_PDC_EN; automatic programmed delay control. automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma	
				1							LTA and CTA values determined automatically	
		SWPC; allows the Cr and Cb samples to be swapped	0								No swapping	
			1								Swaps the Cr and Cb output samples	
0x2B	Misc gain control	PW_UPD; peak white update determines the rate of gain								0	Updates once per video line	Peak white must be enabled; see LAGC[2:0]
										1	Updates once per field	
		Reserved			1	0	0	0	0		Sets to default	
		CKE; color kill enable allows the color kill function to be switched on and off		0							Color kill disabled	For SECAM color kill, the threshold is set at 8%; see CKILLTHR[2:0]
				1							Color kill enabled	
		Reserved	1								Sets to default	
0x2C	AGC mode control	CAGC[1:0]; chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path							0	0	Manual fixed gain	Use CMG[11:0]
									0	1	Uses luma gain for chroma	
									1	0	Automatic gain	Based on color burst
									1	1	Freeze chroma gain	
		Reserved					1	1			Sets to 1	
		LAGC[2:0]; luma automatic gain control selects the mode of operation for the gain control in the luma path		0	0	0					Manual fixed gain	Uses LMG[11:0]
				0	0	1					AGC peak white algorithm off	Blank level to sync tip
				0	1	0					AGC peak white algorithm on	Blank level to sync tip
				0	1	1					Reserved	
				1	0	0					Reserved	
				1	0	1					Reserved	
				1	1	0					Reserved	
				1	1	1					Freeze gain	
		Reserved	1								Sets to 1	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x2D	Chroma Gain Control 1, Chroma Gain 1 (CG)	CMG[11:8]/CG[11:8]; in manual mode, the chroma gain control can be used to program a desired manual chroma gain; in auto mode, it can be used to read back the current gain value					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates
		Reserved			1	1					Set to 1	Has an effect only if CAGC[1:0] is set to autogain (10)
		CAGT[1:0]; chroma automatic gain timing allows adjustment of the chroma AGC tracking speed	0	0							Slow (TC = 2 sec)	
			0	1							Medium (TC = 1 sec)	
			1	0							Reserved	
			1	1							Adaptive	
0x2E	Chroma Gain Control 2, Chroma Gain 2 (CG)	CMG[7:0]/CG[7:0]; chroma manual gain lower eight bits; see CMG[11:8]/CG[11:8] for description	0	0	0	0	0	0	0	0	CMG[11:0] = see the CMG section	Minimum value = 0d, maximum value = 4095d
0x2F	Luma Gain Control 1, Luma Gain 1 (LG)	LMG[11:8]/LG[11:8]; in manual mode, luma gain control can be used to program a desired manual luma gain; in auto mode, it can be used to read back the actual gain value used					x	x	x	x	LAGC[1:0] settings decide in which mode LMG[11:0] operates	
		Reserved			1	1					Sets to 1	
		LAGT[1:0]; luma automatic gain timing allows adjustment of the luma AGC tracking speed	0	0							Slow (TC = 2 sec)	Has an effect only if LAGC[1:0] is set to autogain (001, 010)
			0	1							Medium (TC = 1 sec)	
			1	0							Fast (TC = 0.2 sec)	
			1	1							Adaptive	
0x30	Luma Gain Control 2, Luma Gain 2 (LG)	LMG[7:0]/LG[7:0]; luma manual gain/ luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	x	x	x	x	x	x	x	x	LMG[7:0]/LG[7:0]; luma manual gain/luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	Minimum value = 1024d, Maximum value = 4095d
0x31	VS/FIELD Control 1	Reserved						0	1	0	Sets to default	
		HVSTIM; horizontal VSYNC timing; selects where within a line of video the VSYNC signal is asserted					0				Start of line relative to HSE	HSE = HSYNC end
							1				Start of line relative to HSB	HSB = HSYNC begin
		NEWAVMODE; sets the EAV/SAV mode				0					EAV/SAV codes generated to suit Analog Devices encoders	
						1					Manual VS/FIELD position controlled by the Register 0x32, Register 0x33, and Register 0xE5 to Register 0xEA	
		Reserved	0	0	0						Sets to default	
0x32	VS/FIELD Control 2	Reserved			0	0	0	0	0	1	Sets to default	NEWAVMODE bit must be set high
		VSBHE		0							VSYNC signal goes high in the middle of the line (even field)	
				1							VSYNC signal changes state at the start of the line (even field)	
		VSBHO	0								VSYNC signal goes high in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line (odd field)	
0x33	VS/FIELD Control 3	Reserved			0	0	0	1	0	0	Sets to default	
		VSEHE		0							VSYNC signal goes low in the middle of the line (even field)	NEWAVMODE bit must be set high
				1							VSYNC signal changes state at the start of the line (even field)	
		VSEHO	0								VSYNC signal goes low in the middle of the line (odd field)	
			1								VSYNC signal changes state at the start of the line odd field	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x34	HS Position Control 1	HSE[10:8]; HSYNC end allows positioning of the HSYNC output within the video line						0	0	0	HSYNC output ends HSE[10:0] pixels after the falling edge of HSYNC	Using HSB and HSE, the position/length of the output HSYNC can be programmed
		Reserved					0				Sets to 0	
		HSB[10:8]; HSYNC begin allows positioning of the HSYNC output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSYNC	
		Reserved	0								Sets to 0	
0x35	HS Position Control 2	HSB[7:0]; see Address 0x34, using HSB[10:0] and HSE[10:0], users can program the position and length of the HSYNC output signal	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	HSE[7:0]; see Address 0x35 description	0	0	0	0	0	0	0	0		
0x37	Polarity	PCLK; sets polarity of LLC								0	Inverts polarity	
										1	Normal polarity as per the timing diagrams	
		Reserved						0	0		Set to 0	
		PF; sets the FIELD polarity					0					
							1					
		Reserved				0						
		PVS; sets the VSYNC polarity			0						Active high	
					1						Active low	
		Reserved		0							Sets to 0	
		PHS; sets HSYNC polarity	0		0						Active high	
			1		1						Active low	
0x38	NTSC comb control	YCMN[2:0]; luma comb mode, NTSC						0	0	0	Adaptive three-line, three-tap luma comb	
								1	0	0	Uses low-pass/notch filter	
								1	0	1	Fixed luma comb two-line (two taps)	Top lines of memory
								1	1	0	Fixed luma comb three-line (three taps)	All lines of memory
								1	1	1	Fixed luma comb two-line (two taps)	Bottom lines of memory
		CCMN[2:0]; chroma comb mode, NTSC			0	0	0				Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN = 10, five-line adaptive for CTAPSN = 11	
					1	0	0				Disables chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSN[1:0]; chroma comb taps, NTSC	0	0							Not used	
			0	1							Adapts three lines to two lines	
			1	0							Adapts five lines to three lines	
			1	1							Adapts five lines to four lines	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x39	PAL comb control	YCMP[2:0]; luma comb mode, PAL						0	0	0	Adaptive five-line, three-tap luma comb	
								1	0	0	Use low-pass notch filter	
								1	0	1	Fixed luma comb (three-line)	Top lines of memory
								1	1	0	Fixed luma comb (five-line)	All lines of memory
								1	1	1	Fixed luma comb (three-line)	Bottom lines of memory
		CCMP[2:0]; chroma comb mode, PAL			0	0	0				Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN = 10, five-line adaptive for CTAPSN = 11	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory
					1	1	0				Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory
					1	1	1				Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory
		CTAPSP[1:0]; chroma comb taps, PAL	0	0							Not used	
			0	1							Adapts five lines to three lines (two taps)	
			1	0							Adapts five lines to three lines (three taps)	
			1	1							Adapts five lines to four lines (four taps)	
0x3A	ADC control	MUX PDN override; mux power-down override								0		No control over power-down for muxes and associated channel circuit
										1		Allows power-down of MUX0/MUX1/ MUX2 and associated channel circuit; when INSEL[4:0] is used, unused channels are automatically powered down
		PWRDWN_MUX_2; enables power-down of MUX2 and associated channel clamp and buffer							0		MUX2 and associated channel in normal operation	
									1		Power down MUX2 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_1; enables power-down of MUX1 and associated channel clamp and buffer						0			MUX1 and associated channel in normal operation	
								1			Power down MUX1 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_0; enables power-down of MUX0 and associated channel clamp and buffer					0				MUX0 and associated channel in normal operation	
							1				Power down MUX0 and associated channel operation	MUX PDN override = 1
		Reserved	0	0	0	0					Sets as default	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x3D	Manual window control	Reserved					0	0	1	0	Sets to default	
		CKILLTHR[2:0]; color kill threshold		0	0	0					NTSC, PAL color kill at <0.5%, SECAM no color kill	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1					NTSC, PAL color kill at <1.5%, SECAM color kill at <5%	
				0	1	0					NTSC, PAL color kill at <2.5%, SECAM color kill at <7%	
				0	1	1					NTSC, PAL color kill at <4%, SECAM color kill at <8%	
				1	0	0					NTSC, PAL color kill at <8.5%, SECAM color kill at <9.5%	
				1	0	1					NTSC, PAL color kill at <16%, SECAM color kill at <15%	
				1	1	0					NTSC, PAL color kill at <32%, SECAM color kill at <32%	
				1	1	1					Reserved	
		Reserved	0								Sets to default	
0x41	Resample control	Reserved			0	0	0	0	0	1	Sets to default	
		SFL_INV; controls the behavior of the PAL switch bit		0							SFL-compatible with the ADV717x and ADV73xx video encoders	
				1							SFL-compatible with older video encoders such as the ADV7194.	
		Reserved	0								Set to default	
0x4D	CTI DNR Control 1	CTI_EN; CTI enable								0	Disables CTI	
										1	Enables CTI	
		CTI_AB_EN; enables the mixing of the transient improved chroma with the original signal							0		Disables CTI alpha blender	
									1		Enables CTI alpha blender	
		CTI_AB[1:0]; controls the behavior of the alpha-blend circuitry					0	0			Sharpest mixing between sharpened/original chroma signal	
							0	1			Sharp mixing between sharpened and original chroma signal	
							1	0			Smooth mixing between sharpened/original chroma signal	
							1	1			Smoothest mixing between sharpened and original chroma signal	
		Reserved				0					Sets to default	
		DNR_EN; enables or bypasses the DNR block			0						Bypasses the DNR block	
					1						Enables the DNR block	
		Reserved	1	1							Sets to default	
0x4E	CTI DNR Control 2	CTI_C_TH[7:0]; specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0		
0x50	DNR Noise Threshold 1	DNR_TH[7:0]; specifies the maximum luma edge that is interpreted as noise and is therefore blanked	0	0	0	0	1	0	0	0		

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x51	Lock count	CIL[2:0]; count into lock determines the number of lines the system must remain in lock before showing a locked status						0	0	0	One line of video	
								0	0	1	Two lines of video	
								0	1	0	Five lines of video	
								0	1	1	10 lines of video	
								1	0	0	100 lines of video	
								1	0	1	500 lines of video	
								1	1	0	1000 lines of video	
								1	1	1	100,000 lines of video	
		COL[2:0]; count out of lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status			0	0	0				One line of video	
					0	0	1				Two lines of video	
					0	1	0				Five lines of video	
					0	1	1				10 lines of video	
					1	0	0				100 lines of video	
					1	0	1				500 lines of video	
					1	1	0				1000 lines of video	
					1	1	1				100,000 lines of video	
		SRLS; select raw lock signal and selects the determination of the lock status		0							Over field with vertical info	
				1							Line-to-line evaluation	
		FSCLE; f_{SC} lock enable	0								Lock status set only by horizontal lock	
			1								Lock status set by horizontal lock and subcarrier lock	
0x5D	DIAG1 Control	Reserved							0	1		
		DIAG1_SLICE_LEVEL[2:0]				0	0	0			Set the DIAG1 slice level to 75 mV	
						0	0	1			Set the DIAG1 slice level to 225 mV	
						0	1	0			Set the DIAG1 slice level to 375 mV	
						0	1	1			Set the DIAG1 slice level to 525 mV	
						1	0	0			Set the DIAG1 slice level to 675 mV	
						1	0	1			Set the DIAG1 slice level to 825 mV	
						1	1	0			Set the DIAG1 slice level to 975 mV	
						1	1	1			Set the DIAG1 slice level to 1.125 V	
		Reserved			1						Reserved	
		.DIAG1_SLICER_PWRDN		0							Power up the DIAG1 slicer	
				1							Power down the DIAG1 slicer	
		Reserved	0								Reserved	
0x5E	DIAG2 Control	Reserved							0	1		
		DIAG2_SLICE_LEVEL[2:0]				0	0	0			Set the DIAG2 slice level to 75 mV	
						0	0	1			Set the DIAG2 slice level to 225 mV	
						0	1	0			Set the DIAG2 slice level to 375 mV	
						0	1	1			Set the DIAG2 slice level to 525 mV	
						1	0	0			Set the DIAG2 slice level to 675 mV	
						1	0	1			Set the DIAG2 slice level to 825 mV	
						1	1	0			Set the DIAG2 slice level to 975 mV	
						1	1	1			Set the DIAG2 slice level to 1.125 V	
		Reserved			1						Reserved	
		.DIAG1_SLICER_PWRDN		0							Power up the DIAG1 slicer	
				1							Power down the DIAG1 slicer	
		Reserved	0								Reserved	
0x59	GPO	GPO[0]								0	Logic 0 output from GPO0 pin	GPO_ENABLE must be set to 1 in order for GPO outputs to be enabled. GPO outputs only available on ADV728x-M models.
										1	Logic 1 output from GPO0 pin	
		GPO[1]							0		Logic 0 output from GPO1 pin	
									1		Logic 1 output from GPO1 pin	
		GPO[2]						0			Logic 0 output from GPO2 pin	
								1			Logic 1 output from GPO2 pin	
		Reserved					0				Reserved	
		GPO_ENABLE				0					GPO pins are tristated	
						1					GPO pins are enabled	
		Reserved	0	0	0							

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x60	ADC Switch 3	MUX3[2:0]					0	0	0	0	No connect	
							0	0	0	1	No connect	
							0	0	1	0	$A_{IN}2$	
							0	0	1	1	No connect	
							0	1	0	0	$A_{IN}4$	
		Reserved	0	0	0	1	0					
0x6A	Output Sync Select 1	HS_OUT_SEL[2:0] selects which sync comes out on the HS pin						0	0	0	HSYNC	
								0	0	1	VSYNC	
								0	1	0	FIELD	
								0	1	1	DE	
								1	0	0	SFL	
		Reserved	0	0	0	0	0					
0x6B	Output Sync Select 2	FLD_OUT_SEL[2:0] selects which sync comes out on the VS/FIELD/SFL pin						0	0	0	HSYNC	
								0	0	1	VSYNC	
								0	1	0	FIELD	
								0	1	1	DE	
								1	0	0	SFL	
		Reserved	0	0	0	1	0				Set as default	
0x8F	Free-Run Line Length 1	Reserved					0	0	0	0	Set as default	
		LLC_PAD_SEL[2:0]; enables manual selection of the clock for the LLC pin		0	0	0					LLC (nominal 27 MHz) selected out on LLC pin	
				1	0	1					LLC (nominal 13.5 MHz) selected out on LLC pin	
		Reserved	0								Sets to default	
0x99	CCAP1 (read only)	CCAP1[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP1[7] contains parity bit for Byte 0	
0x9A	CCAP2 (read only)	CCAP2[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP2[7] contains parity bit for Byte 0	
0x9B	Letterbox 1 (read only)	LB_LCT[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the top of active video	This feature examines the active video at the start and end of each field; it enables format detection even if the video is not accompanied by a CGMS or WSS sequence
0x9C	Letterbox 2 (read only)	LB_LCM[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected in the middle half of active video if subtitles are detected	
0x9D	Letterbox 3 (read only)	LB_LCB[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the bottom of active video	
0xB2	CRC enable (write only)	Reserved							0	0	Sets as default	
		CRC_ENABLE; enable CRC checksum decoded from FMS packet to validate CGMSD						0			Turns off CRC check	
								1			CGMSD goes high with valid checksum	
		Reserved	0	0	0	1	1				Sets as default	
0xC3	ADC Switch 1	MUX0[2:0]; manual muxing control for MUX0; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	$A_{IN}1$	
								0	1	0	$A_{IN}2$	
								0	1	1	$A_{IN}3$	
								1	0	0	$A_{IN}4$	
		Reserved					0					
		MUX1[2:0]; manual muxing control for MUX1; this setting controls which input is routed to the ADC for processing		0	0	0					No connect	
				0	0	1					No connect	
				0	1	0					$A_{IN}2$	
				0	1	1					No connect	
				1	0	0					$A_{IN}4$	
		Reserved	0									

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xC4	ADC Switch 2	MUX2[2:0]; manual muxing control for MUX2; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	No connect	
								0	1	0	$A_{IN}2$	
								0	1	1	$A_{IN}3$	
								1	0	0	No connect	
		Reserved		0	0	0	0					
		MAN_MUX_EN; enable manual setting of input signal muxing	0								Disables	This bit must be set to 1 for manual muxing
			1								Enables	
0xDC	Letterbox Control 1	LB_TH[4:0]; sets the threshold value that determines if a line is black				0	1	1	0	0	Default threshold for the detection of black lines 01101 to 10000—increase threshold, 00000 to 01011—decrease threshold	
		Reserved	1	0	1						Sets as default	
0xDD	Letterbox Control 2	LB_EL[3:0]; programs the end line of the activity window for LB detection (end of field)					1	1	0	0	LB detection ends with the last line of active video on a field, 1100b: 262/525	
		LB_SL[3:0]; programs the start line of the activity window for LB detection (start of field)	1	1	0	0					Letterbox detection aligned with the start of active video, 0100b: 23/286 NTSC	
0xDE	ST Noise Readback 1 (read only)	ST_NOISE[10:8]						x	x	x		ST noise[10:0] measures the noise on the horizontal sync tip of video source
		ST_NOISE_VLD					x				When = 1, ST_NOISE[10:0] is valid	
0xDF	ST Noise Readback 2 (read only)	ST_NOISE[7:0]	x	x	x	x	x	x	x	x		
0xE1	SD offset Cb channel	SD_OFF_Cb[7:0]; adjusts the hue by selecting the offset for the Cb channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cb channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cb channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cb channel	
0xE2	SD offset Cr channel	SD_OFF_Cr[7:0]; adjusts the hue by selecting the offset for the Cr channel	0	0	0	0	0	0	0	0	−312 mV offset applied to the Cr channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cr channel	
			1	1	1	1	1	1	1	1	+312 mV offset applied to the Cr channel	
0xE3	SD saturation Cb channel	SD_SAT_Cb[7:0]; adjusts the saturation by affecting gain on the Cb channel	0	0	0	0	0	0	0	0	Gain on Cb channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB	
0xE4	SD saturation Cr channel	SD_SAT_Cr[7:0]; adjusts the saturation by affecting gain on the Cr channel	0	0	0	0	0	0	0	0	Gain on Cr channel = −42 dB	
			1	0	0	0	0	0	0	0	Gain on Cr channel = 0 dB	
			1	1	1	1	1	1	1	1	Gain on Cr channel = +6 dB	
0xE5	NTSC VSYNC begin	NVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	NTSC default (ITU-R BT.656)	
		NVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVBEGDELE; delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		NVBEGDELO; delay V bit going high by one line relative to NVBEG (odd field)	0								No delay	
			1								Additional delay by one line	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xE6	NTSC VSYNC end	NVEND[4:0]; number of lines after I_{COUNT} rollover to set V low				0	0	1	0	0	NTSC default (ITU-R BT.656)	
		NVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NVENDDELE; delay V bit going low by one line relative to NVEND (even field)		0							No delay	
				1							Additional delay by one line	
		NVENDDELO; delay V bit going low by one line relative to NVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xE7	NTSC FIELD toggle	NFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	NTSC default	
		NFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		NFTOGDELE; delay F transition by one line relative to NFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		NFTOGDELO; delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE8	PAL VSYNC begin	PVBEG[4:0]; number of lines after I_{COUNT} rollover to set V high				0	0	1	0	1	PAL default (ITU-R BT.656)	
		PVBEGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVBEGDELE; delay V bit going high by one line relative to PVBEG (even field)		0							No delay	
				1							Additional delay by one line	
		PVBEGDELO; delay V bit going high by one line relative to PVBEG (odd field)	0								No delay	
			1								Additional delay by one line	
0xE9	PAL VSYNC end	PVEND[4:0]; number of lines after I_{COUNT} rollover to set V low.				1	0	1	0	0	PAL default (ITU-R BT.656)	
		PVENDSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PVENDDELE; delay V bit going low by one line relative to PVEND (even field)		0							No delay	
				1							Additional delay by one line	
		PVENDDELO; delay V bit going low by one line relative to PVEND (odd field)	0								No delay	
			1								Additional delay by one line	
0xEA	PAL FIELD toggle	PFTOG[4:0]; number of lines after I_{COUNT} rollover to toggle F signal				0	0	0	1	1	PAL default (ITU-R BT.656)	
		PFTOGSIGN			0						Sets to low when manual programming	
					1						Not suitable for user programming	
		PFTOGDELE; delay F transition by one line relative to PFTOG (even field)		0							No delay	
				1							Additional delay by one line	
		PFTOGDELO; delay F transition by one line relative to PFTOG (odd field)	0								No delay	
			1								Additional delay by one line	

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xEB	Vblank Control 1	PVBIELCM[1:0]; PAL VBI even field line control							0	0	VBI ends one line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant (Line 336)	
									1	0	VBI ends one line later (Line 337)	
									1	1	VBI ends two lines later (Line 338)	
		PVBIOLCM[1:0]; PAL VBI odd field line control					0	0			VBI ends one line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on odd field in PAL
							0	1			ITU-R BT.470 compliant (Line 23)	
							1	0			VBI ends one line later (Line 24)	
							1	1			VBI ends two lines later (Line 25)	
		NVBIELCM[1:0]; NTSC VBI even field line control			0	0					VBI ends one line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on even field in NTSC
					0	1					ITU-R BT.470 compliant (Line 283)	
					1	0					VBI ends one line later (Line 284)	
					1	1					VBI ends two lines later (Line 285)	
		NVBIOLCM[1:0]; NTSC VBI odd field line control	0	0							VBI ends one line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant (Line 21)	
			1	0							VBI ends one line later (Line 22)	
			1	1							VBI ends two lines later (Line 23)	
0xEC	Vblank Control 2	PVBIECCM[1:0]; PAL VBI even field color control							0	0	Color output beginning Line 335	Controls the position of first line that outputs color after VBI on even field in PAL
									0	1	ITU-R BT.470 compliant color output beginning Line 336	
									1	0	Color output beginning Line 337	
									1	1	Color output beginning Line 338	
		PVBIOCCM[1:0]; PAL VBI odd field color control					0	0			Color output beginning Line 22	Controls the position of first line that outputs color after VBI on odd field in PAL
							0	1			ITU-R BT.470-compliant color output beginning Line 23	
							1	0			Color output beginning Line 24	
							1	1			Color output beginning Line 25	
		NVBIECCM[1:0]; NTSC VBI even field color control			0	0					Color output beginning Line 282	Controls the position of first line that outputs color after VBI on even field in NTSC
					0	1					ITU-R BT.470-compliant color output beginning Line 283	
					1	0					VBI ends one line later (Line 284)	
					1	1					Color output beginning Line 285	
		NVBIOCCM[1:0]; NTSC VBI odd field color control	0	0							Color output beginning Line 20	Controls the position of first line that outputs color after VBI on odd field in NTSC
			0	1							ITU-R BT.470 compliant color output beginning Line 21	
			1	0							Color output beginning Line 22	
			1	1							Color output beginning Line 23	
0xF3	AFE_ CONTROL 1	AA_FILT_EN[3:0] antialiasing filter enable								0	Antialiasing Filter 1 disabled	AA_FILT_MAN_OVR must be enabled to change settings defined by INSEL[4:0]
										1	Antialiasing Filter 1 enabled	
									0		Antialiasing Filter 2 disabled	
									1		Antialiasing Filter 2 enabled	
								0			Antialiasing Filter 3 disabled	
								1			Antialiasing Filter 3 enabled	
							0				Antialiasing Filter 4 enabled	
							1				Antialiasing Filter 4 enabled	
		AA_FILT_MAN_OVR; antialiasing filter override				0					Override disabled	
						1					Override enabled	
		Reserved	0	0	0							

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xF4	Drive strength	DR_STR_S[1:0]; selects the drive strength for the sync output signals							0	0	Low drive strength (1×)	
									0	1	Medium low drive strength (2×)	
									1	0	Medium high drive strength (3×)	
									1	1	High drive strength (4×)	
		DR_STR_C[1:0]; selects the drive strength for the clock output signal					0	0			Low drive strength (1×)	
							0	1			Medium low drive strength (2×)	
							1	0			Medium high drive strength (3×)	
							1	1			High drive strength (4×)	
		DR_STR[1:0]; selects the drive strength for the data output signals; can be increased or decreased for EMC or crosstalk reasons			0	0					Low drive strength (1×)	
					0	1					Medium low drive strength (2×)	
					1	0					Medium high drive strength (3×)	
					1	1					High drive strength (4×)	
		Reserved		x								
		GLITCH_FILT_BYP	0									
			1									
0xF8	IF comp control	IFFILTSEL[2:0]; IF filter selection for PAL and NTSC						0	0	0	Bypass mode	0 dB
											2 MHz NTSC filters	
								0	0	1	−3 dB	
								0	1	0	−6 dB	
								0	1	1	−10 dB	
								1	0	0	Reserved	
											3 MHz PAL filters	
								1	0	1	−2 dB	
								1	1	0	−5 dB	
								1	1	1	−7 dB	
		Reserved	0	0	0	0	0					
0xF9	VS mode control	EXTEND_VS_MAX_FREQ								0	Limits maximum VSYNC frequency to 66.25 Hz (475 lines/frame)	
										1	Limits maximum VSYNC frequency to 70.09 Hz (449 lines/frame)	
		EXTEND_VS_MIN_FREQ							0		Limits minimum VSYNC frequency to 42.75 Hz (731 lines/frame)	
									1		Limits minimum VSYNC frequency to 39.51 Hz (791 lines/frame)	
		VS_COAST_MODE[1:0]					0	0			Autocoast mode	This value forces the video standard output during free-run mode
							0	1			576i 50 Hz coast mode	
							1	0			480i 60 Hz coast mode	
							1	1			Reserved	
		Reserved	0	0	0	0						
0xFB	Peaking gain	PEAKING_GAIN[7:0]	0	1	0	0	0	0	0	0	Increases/decreases the gain for high frequency portions of the video signal	
0xFC	DNR Noise Threshold 2	DNR_TH2[7:0]	0	0	0	0	0	1	0	0	Specifies the maximum luma edge that is interpreted as noise and therefore blanked	
0xFD	VPP slave address	Reserved								0	Reserved	
		VPP_SLAVE_ADDR[6:0]	0	0	0	0	0	0	0		Programs the I^2C address of the Video Post Processor (VPP) Map	Applies only to the ADV7280, ADV7280-M, and ADV7282-M models. VPP map cannot be accessed when this register is set to 0x00. Analog Devices recommended scripts set this register to 0x84.

User Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0xFE	CSI Tx slave address	Reserved								0	Reserved	
		CSI_TX_SLAVE_ADDR(6:0)	0	0	0	0	0	0	0		Programs the I^2C address of the CSI Map	Applies only to the ADV7280-M, ADV7281-M, ADV7281-MA, and ADV7282-M models. CSI Map cannot be accessed when this register is set to 0x00. Analog Devices recommended script sets this register to 0x88.

USER SUB MAP 2 DESCRIPTION

To access the registers listed in Table 96, SUB_USR_EN in Register Address 0x0E must be programmed to 10. The gray shading is the default.

Table 96. User Sub Map 2 Register Map Descriptions

User Sub Map 2			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x80	ACE Control 1	Reserved		0	0	0	0	0	0	0	Reserved.	
		ACE_ENABLE	0								Disable ACE.	
			1								Enable ACE.	
0x83	ACE Control 4	ACE_LUMA_GAIN[4:0]				0	1	1	0	1	Set ACE luma auto-contrast level to default value. 5b'00000 minimum value … 5b'11111 maximum value	When ACE_ ENABLE is set to 1
		Reserved	0	0	0							
0x84	ACE Control 5	ACE_CHROMA_GAIN[3:0]					1	0	0	0	Set ACE color auto-saturation level. 4b'0000 minimum value … 4b'1111 maximum value	
		ACE_CHROMA_MAX[3:0]	1	0	0	0					Set maximum threshold for ACE color color-saturation level. 4b'0000 = minimum value … 4b'1111 = maximum value	
0x85	ACE Control 6	ACE_GAMMA_GAIN[3:0]					1	0	0	0	Set further contrast enhancement. 4b'0000 = minimum value … 4b'1111 = maximum value	
		ACE_RESPONSE_SPEED[3:0]	1	1	1	1					Set speed of ACE response. 4b'0000 slowest value … 4b'1111 fastest value	
0x92	Dither control	BR_DITHER_MODE								0	8-bit to 6-bit down dither disabled	
										1	8-bit to 6-bit down dither enabled	
		Reserved	0	0	0	0	0	0	0			
0xD9	Min Max 0	MIN_THRESH_Y[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming luma video signal.	
0xDA	Min Max 1	MAX_THRESH_Y[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming luma video signal.	
0xDB	Min Max 2	MIN_THRESH_C[7:0]	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming chroma video signal.	
0xDC	Min Max 3	MAX_THRESH_C[7:0]	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming chroma video signal.	
0xDD	Min Max 4	MAX_SAMPLES_ALLOWED_ Y[3:0]					1	1	0	0	Selects the number of maximum luma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_ Y[3:0]	1	1	0	0					Selects the number of minimum luma samples allowed in a given window before an interrupt is triggered.	
0xDE	Min Max 5	MAX_SAMPLES_ALLOWED_ C[3:0]					1	1	0	0	Selects the number of maximum chroma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_ C[3:0]	1	1	0	0					Selects the number of minimum chroma samples allowed in a given window before an interrupt is triggered.	
0xE0	FL Control	FL_ENABLE								0	Fast lock mode not enabled	
										1	Enables fast lock mode	
		Reserved	0	0	0	0	0	0	0			See Subaddress 0xE5 for least significant bits

User Sub Map 2			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0xE1	Y Average 0	LINE_START[8:1]	0	0	0	1	0	0	0	1	Selects starting line for field averaging.	See Subaddress 0xE5 for least significant bits
0xE2	Y Average 1	LINE_END[8:1]	1	0	0	0	1	0	0	0	Selects end line for field averaging.	
0xE3	Y Average 2	SAMPLE_START[9:2]	0	0	0	1	0	1	1	1	Selects starting sample for line averaging.	
0xE4	Y Average 3	SAMPLE_END[9:2]	1	1	0	1	0	1	1	1	Selects end sample for line averaging.	
0xE5	Y Average 4	LINE_START[0]								1		
		LINE_END[0]							1			
		Reserved					0	0				
		SAMPLE_START[1:0]			1	0						
		SAMPLE_END[1:0]	0	0								
0xE6	Y Average 5	CAPTURE_VALUE								0	Trigger used to store the readback value.	
		Y_AVG_FILT_EN							0		Enable low pass filtering of the y_averaged signal.	
		Y_AVG_TIME_CONST[2:0]				1	0	0			Selects the filter cutoff to be used for filtering the y averaged data. 3'b1xx = least filtered. 3'b000 = next least. … 3'b011 = heavily filtered.	
		Reserved	0	0	0							Note these are read only registers
0xE7	Y Average Data MSB	Y_AVERAGE[9:2]	x	x	x	x	x	x	x	x	Contains the averaged video data.	
0xE8	Y Average Data LSB	Y_AVERAGE[1:0]							x	x		

INTERRUPT/VDP SUB MAP DESCRIPTION

To access the registers listed in Table 97, SUB_USR_EN in Register Address 0x0E must be programmed to 01. The gray shading is the default.

Table 97. Interrupt/VDP Sub Map Register Descriptions

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x40	Interrupt Configuration 1	INTRQ_OP_SEL[1:0]; interrupt drive level select							0	0	Open drain	
									0	1	Drive low when active	
									1	0	Drive high when active	
									1	1	Reserved	
		MPU_STIM_INTRQ; manual interrupt set mode						0			Manual interrupt mode disabled	
								1			Manual interrupt mode enabled	
		Reserved					x				Not used	
		MV_INTRQ_SEL[1:0]; Rovi interrupt select			0	0					Reserved	
					0	1					Pseudo sync only	
					1	0					Color stripe only	
					1	1					Pseudo sync or color stripe	
		INTRQ_DUR_SEL[1:0]; interrupt duration select	0	0							Three XTAL periods	
			0	1							15 XTAL periods	
			1	0							63 XTAL periods	
			1	1							Active until cleared	
0x42	Interrupt Status 1 (read only)	SD_LOCK_Q								0	No change	These bits can be cleared or masked in Register 0x43 and Register 0x44, respectively
										1	SD input has caused the decoder to go from an unlocked state to a locked state	
		SD_UNLOCK_Q							0		No change	
									1		SD input has caused the decoder to go from a locked state to an unlocked state	
		Reserved				x	x	x				
		SD_FR_CHNG_Q			0						No change	
					1						Denotes a change in the free-run status	
		MV_PS_CS_Q		0							No change	
				1							Pseudo sync/color striping detected; see Register 0x40 MV_INTRQ_SEL[1:0] for selection	
		Reserved	x									
0x43	Interrupt Clear 1 (write only)	SD_LOCK_CLR								0	Do not clear	
										1	Clears SD_LOCK_Q bit	
		SD_UNLOCK_CLR							0		Do not clear	
									1		Clears SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		SD_FR_CHNG_CLR			0						Do not clear	
					1						Clears SD_FR_CHNG_Q bit	
		MV_PS_CS_CLR		0							Do not clear	
				1							Clears MV_PS_CS_Q bit	
		Reserved	x								Not used	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x44	Interrupt Mask 1 (read/write)	$\overline{\text{SD\_LOCK\_MSK}}$								0	Masks SD_LOCK_Q bit	
										1	Unmasks SD_LOCK_Q bit	
		$\overline{\text{SD\_UNLOCK\_MSK}}$							0		Masks SD_UNLOCK_Q bit	
									1		Unmasks SD_UNLOCK_Q bit	
		Reserved				0	0	0			Not used	
		$\overline{\text{SD\_FR\_CHNG\_MSK}}$			0						Masks SD_FR_CHNG_Q bit	
					1						Unmasks SD_FR_CHNG_Q bit	
		$\overline{\text{MV\_PS\_CS\_MSK}}$		0							Masks MV_PS_CS_Q bit	
				1							Unmasks MV_PS_CS_Q bit	
		Reserved	x								Not used	
0x45	Raw Status 2 (read only)	CCAPD								0	No CCAPD data detected— VBI System 2	These bits are status bits only; they cannot be cleared or masked; Register 0x46 is used for this purpose
										1	CCAPD data detected—VBI System 2	
		Reserved					x	x	x			
		EVEN_FIELD				0					Current SD field is odd numbered	
						1					Current SD field is even numbered	
		CHX_MIN_MAX_INTRQ			0						If the input to the ADC is within the correct range this is 0	
					1						If the input to the ADC is outside the range this is set to 1. The range is set by User Sub Map 2	
		Reserved		x							Not used	
		MPU_STIM_INTRQ	0								MPU_STIM_INTRQ = 0	
			1								MPU_STIM_INTRQ = 1	
0x46	Interrupt Status 2 (read only)	CCAPD_Q								0	Closed captioning not detected in the input video signal—VBI System 2	These bits can be cleared or masked by Register 0x47 and Register 0x48, respectively; note that the interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Closed captioning data detected in the video input signal—VBI System 2	
		Reserved							x		Not used	
		Reserved					x	x			Not used	
		SD_FIELD_CHNGD_Q				0					SD signal has not changed field from odd to even or vice versa	
						1					SD signal has changed Field from odd to even or vice versa	
		Reserved		x	x						Not used	
		MPU_STIM_INTRQ_Q	0								Manual interrupt not set	
			1								Manual interrupt set	
0x47	Interrupt Clear 2 (write only)	CCAPD_CLR								0	Do not clear—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Clears CCAPD_Q bit—VBI System 2	
		Reserved							x		Not used	
		Reserved					x	x				
		SD_FIELD_CHNGD_CLR				0					Do not clear	
						1					Clears SD_FIELD_CHNGD_Q bit	
		CHX_MIN_MAX_INTRQ_CLR			0						Do not clear	
					1						Clears CHX_MIN_MAX_INTRQ bit	
		Reserved		x							Not used	
		MPU_STIM_INTRQ_CLR	0								Do not clear	
			1								Clears MPU_STIM_INTRQ_Q bit	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x48	Interrupt Mask 2 (read/write)	$\overline{\text{CCAPD\_MSK}}$								0	Masks CCAPD_Q bit—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer
										1	Unmasks CCAPD_Q bit—VBI System 2	
		Reserved							0		Not used	
		Reserved					0	0			Not used	
		$\overline{\text{SD\_FIELD\_CHNGD\_MSK}}$				0					Masks SD_FIELD_CHNGD_Q bit	
						1					Unmasks SD_FIELD_CHNGD_Q bit	
		$\overline{\text{CHX\_MIN\_MAX\_INTRQ\_MSKB}}$			0						Masks CHX_MIN_MAX_INTRQ bit	
					1						Unmasks CHX_MIN_MAX_INTRQ bit	
		Reserved		0							Not used	
		$\overline{\text{MPU\_STIM\_INTRQ\_MSK}}$	0								Masks MPU_STIM_INTRQ_Q bit	
			1								Unmasks MPU_STIM_INTRQ_Q bit	
0x49	Raw Status 3 (read only)	SD_OP_50Hz; SD 60 Hz/50 Hz frame rate at output								0	SD 60 Hz signal output	These bits are status bits only; they cannot be cleared or masked; Register 0x4A is used for this purpose
										1	SD 50 Hz signal output	
		SD_V_LOCK							0		SD vertical sync lock is not established	
									1		SD vertical sync lock established	
		SD_H_LOCK						0			SD horizontal sync lock is not established	
								1			SD horizontal sync lock established	
		Reserved					x				Not used	
		SCM_LOCK				0					SECAM lock is not established	
						1					SECAM lock established	
		Reserved	x	x	x						Not used	
0x4A	Interrupt Status 3 (read only)	SD_OP_CHNG_Q; SD 60 Hz/50 Hz frame rate at output								0	No change in SD signal standard detected at the output	These bits can be cleared and masked by Register 0x4B and Register 0x4C, respectively
										1	A change in SD signal standard is detected at the output	
		SD_V_LOCK_CHNG_Q							0		No change in SD VSYNC lock status	
									1		SD VSYNC lock status has changed	
		SD_H_LOCK_CHNG_Q						0			No change in HSYNC lock status	
								1			SD HSYNC lock status has changed	
		SD_AD_CHNG_Q; SD autodetect changed					0				No change in AD_RESULT[2:0] bits in Status 1 register	
							1				AD_RESULT[2:0] bits in Status 1 register have changed	
		SCM_LOCK_CHNG_Q; SECAM lock				0					No change in SECAM lock status	
						1					SECAM lock status has changed	
		PAL_SW_LK_CHNG_Q			0						No change in PAL swinging burst lock status	
					1						PAL swinging burst lock status has changed	
		Reserved	x	x							Not used	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x4B	Interrupt Clear 3 (write only)	SD_OP_CHNG_CLR								0	Do not clear	
										1	Clears SD_OP_CHNG_Q bit	
		SD_V_LOCK_CHNG_CLR							0		Do not clear	
									1		Clears SD_V_LOCK_CHNG_Q bit	
		SD_H_LOCK_CHNG_CLR						0			Do not clear	
								1			Clears SD_H_LOCK_CHNG_Q bit	
		SD_AD_CHNG_CLR					0				Do not clear	
							1				Clears SD_AD_CHNG_Q bit	
		SCM_LOCK_CHNG_CLR				0					Do not clear	
						1					Clears SCM_LOCK_CHNG_Q bit	
		PAL_SW_LK_CHNG_CLR			0						Do not clear	
					1						Clears PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	
0x4C	Interrupt Mask 3 (read/write)	$\overline{\text{SD\_OP\_CHNG\_MSK}}$								0	Masks SD_OP_CHNG_Q bit	
										1	Unmasks SD_OP_CHNG_Q bit	
		$\overline{\text{SD\_V\_LOCK\_CHNG\_MSK}}$							0		Masks SD_V_LOCK_CHNG_Q bit	
									1		Unmasks SD_V_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_H\_LOCK\_CHNG\_MSK}}$						0			Masks SD_H_LOCK_CHNG_Q bit	
								1			Unmasks SD_H_LOCK_CHNG_Q bit	
		$\overline{\text{SD\_AD\_CHNG\_MSK}}$					0				Masks SD_AD_CHNG_Q bit	
							1				Unmasks SD_AD_CHNG_Q bit	
		$\overline{\text{SCM\_LOCK\_CHNG\_MSK}}$				0					Masks SCM_LOCK_CHNG_Q bit	
						1					Unmasks SCM_LOCK_CHNG_Q bit	
		$\overline{\text{PAL\_SW\_LK\_CHNG\_MSK}}$			0						Masks PAL_SW_LK_CHNG_Q bit	
					1						Unmasks PAL_SW_LK_CHNG_Q bit	
		Reserved	x	x							Not used	
0x4E	Interrupt Status 4 (read only)	VDP_CCAPD_Q								0	Closed captioning not detected	These bits can be cleared and masked by Register 0x4F and Register 0x50, respectively; note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Closed captioning detected	
		Reserved							x			
		VDP_CGMS_WSS_CHNGD_Q; see Address 0x9C, Bit 4, of User Sub Map to determine whether interrupt is issued for a change in detected data or for when data is detected, regardless of content						0			CGMS/WSS data is not changed/not available	
								1			CGMS/WSS data is changed/available	
		Reserved					x					
		Reserved				x						
		Reserved			x							
		Reserved		x								
		Reserved	x									
0x4F	Interrupt Clear 4 (write only)	VDP_CCAPD_CLR								0	Do not clear	In Register 0x4E, CCAP/CGMS/WSS data uses VDP data slicer
										1	Clears VDP_CCAPD_Q	
		Reserved							0			
		VDP_CGMS_WSS_CHNGD_CLR						0			Do not clear	
								1			Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0							Do not clear	
		Reserved	0									
		VDP_CCAPD_CLR								0	Do not clear	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x50	Interrupt Mask 4	$\overline{\text{VDP\_CCAPD\_MSK}}$								0	Masks VDP_CCAPD_Q	Note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer
										1	Unmasks VDP_CCAPD_Q	
		Reserved							0			
		$\overline{\text{VDP\_CGMS\_WSS\_CHNGD\_MSK}}$						0			Masks VDP_CGMS_WSS_CHNGD_Q	
								1			Unmasks VDP_CGMS_WSS_CHNGD_Q	
		Reserved					0					
		Reserved				0						
		Reserved			0							
		Reserved		0								
		Reserved	0									
0x51	Interrupt Latch 0 (read only)	CR_CHANNEL_MAX_VIOLATION								0	Cr value is below programmed maximum value	This register is cleared by CHX_MIN_MAX_INTRQ_CLR
										1	Cr value is above programmed maximum value	
		CR_CHANNEL_MIN_VIOLATION							0		Cr value is above programmed minimum value	
									1		Cr value is below programmed minimum value	
		CB_CHANNEL_MAX_VIOLATION						0			Cb value is below programmed maximum value	
								1			Cb value is above programmed maximum value	
		CB_CHANNEL_MIN_VIOLATION					0				Cb value is above programmed minimum value	
							1				Cb value is below programmed minimum value	
		Y_CHANNEL_MAX_VIOLATION				0					Y value is below programmed maximum value	
						1					Y value is above programmed maximum value	
		Y_CHANNEL_MIN_VIOLATION			0						Y value is above programmed minimum value	
					1						Y value is below programmed minimum value	
		Reserved	0	0								

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x60	VDP_CONFIG_1	VDP_TTXT_TYPE_MAN[1:0]							0	0	PAL: Teletext-ITU-BT.653-625/ 50-A, NTSC: reserved	
									0	1	PAL: Teletext-ITU-BT.653-625/ 50-B (WST), NTSC: Teletext-ITU-BT.653-525/ 60-B	
									1	0	PAL: Teletext-ITU-BT.653-625/ 50-C, NTSC: Teletext-ITU-BT.653-525/ 60-C, or EIA516 (NABTS)	
									1	1	PAL: Teletext-ITU-BT.653-625/ 50-D, NTSC: Teletext-ITU-BT.653-525/ 60-D	
		VDP_TTXT_TYPE_MAN_ENABLE						0			User programming of teletext type disabled	
								1			User programming of teletext type enabled	
		WST_PKT_DECODE_DISABLE					0				Enables hamming decoding of WST packets	
							1				Disables hamming decoding of WST packets	
		Reserved	1	0	0	0						
0x62	VDP_ADF_ CONFIG_1	ADF_DID[4:0]				1	0	1	0	1	User-specified DID sent in the ancillary data stream with VDP decoded data	
		ADF_MODE[1:0]		0	0						Nibble mode	Sets whether ancillary data output mode in byte mode or nibble mode
				0	1						Byte mode, no code restrictions	
				1	0						Byte mode with 0x00 and 0xFF prevented	
				1	1						Reserved	
		ADF_ENABLE	0								Disables insertion of VBI decoded data into ancillary 656 stream	
			1								Enables insertion of VBI decoded data into ancillary 656 stream	
0x63	VDP_ADF_ CONFIG_2	ADF_SDID[5:0]			1	0	1	0	1	0	User-specified SDID sent in the ancillary data stream with VDP decoded data	
		Reserved		x								
		DUPLICATE_ADF	0								Ancillary data packet is spread across the Y and C data streams	
			1								Ancillary data packet is duplicated on the Y and C data streams	
0x64	VDP_LINE_00E	VBI_DATA_P318[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 318 (PAL), NTSC—not applicable	
		Reserved		0	0	0						
		MAN_LINE_PGM	0								Decode default VDP standards on the expected lines.	
			1								Manually program the VBI standard to be decoded on each line.	If set to 1, all VBI_DATA_Px_Ny bits can be set as desired
0x65	VDP_LINE_00F	VBI_DATA_P319_N286[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 319 (PAL), Line 286 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P6_N23[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 6 (PAL), Line 23 (NTSC)	
0x66	VDP_LINE_010	VBI_DATA_P320_N287[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 320 (PAL), Line 287 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 7 (PAL), Line 24 (NTSC)	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x67	VDP_LINE_011	VBI_DATA_P321_N288[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 321 (PAL), Line 288 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 8 (PAL), Line 25 (NTSC)	
0x68	VDP_LINE_012	VBI_DATA_P322[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 322 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 9 (PAL), NTSC—not applicable	
0x69	VDP_LINE_013	VBI_DATA_P323[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 323 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 10 (PAL), NTSC—not applicable	
0x6A	VDP_LINE_014	VBI_DATA_P324_N272[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 324 (PAL), Line 272 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 11 (PAL); NTSC—not applicable	
0x6B	VDP_LINE_015	VBI_DATA_P325_N273[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 325 (PAL), Line 273 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 12 (PAL), Line 10 (NTSC)	
0x6C	VDP_LINE_016	VBI_DATA_P326_N274[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 326 (PAL), Line 274 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 13 (PAL), Line 11 (NTSC)	
0x6D	VDP_LINE_017	VBI_DATA_P327_N275[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 327 (PAL), Line 275 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 14 (PAL), Line 12 (NTSC)	
0x6E	VDP_LINE_018	VBI_DATA_P328_N276[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 328 (PAL), Line 276 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 15 (PAL), Line 13 (NTSC)	
0x6F	VDP_LINE_019	VBI_DATA_P329_N277[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 329 (PAL), Line 277 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 16 (PAL), Line 14 (NTSC)	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x70	VDP_LINE_01A	VBI_DATA_P330_N278[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 330 (PAL), Line 278 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 17 (PAL), Line 15 (NTSC)	
0x71	VDP_LINE_01B	VBI_DATA_P331_N279[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 331 (PAL), Line 279 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 18 (PAL), Line 16 (NTSC)	
0x72	VDP_LINE_01C	VBI_DATA_P332_N280[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 332 (PAL), Line 280 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 19 (PAL), Line 17 (NTSC)	
0x73	VDP_LINE_01D	VBI_DATA_P333_N281[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 333 (PAL), Line 281 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 20 (PAL), Line 18 (NTSC)	
0x74	VDP_LINE_01E	VBI_DATA_P334_N282[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 334 (PAL), Line 282 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 21 (PAL), Line 19 (NTSC)	
0x75	VDP_LINE_01F	VBI_DATA_P335_N283[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 335 (PAL), Line 283 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 22 (PAL), Line 20 (NTSC)	
0x76	VDP_LINE_020	VBI_DATA_P336_N284[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 336 (PAL), Line 284 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 23 (PAL), Line 21 (NTSC)	
0x77	VDP_LINE_021	VBI_DATA_P337_N285[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 337 (PAL), Line 285 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P24_N22[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 24 (PAL), Line 22 (NTSC)	

Interrupt/VDP Sub Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x78	VDP_STATUS (read only)	CC_AVL								0	Closed captioning not detected	CC_CLEAR resets the CC_AVL bit
										1	Closed captioning is detected	
		CC_EVEN_FIELD							0		Closed captioning decoded from odd field	
									1		Closed captioning decoded from even field	
		CGMS_WSS_AVL						0			CGMS/WSS is not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
								1			CGMS/WSS detected	
		Reserved		0	0	0	0					
		TTXT_AVL	0								Teletext not detected	
			1								Teletext detected	
	VDP_STATUS_ CLEAR (write only)	CC_CLEAR								0	Does not reinitialize the CCAP readback registers	This is a self-clearing bit
										1	Reinitializes the CCAP readback registers	
		Reserved							0			
		CGMS_WSS_CLEAR						0			Does not reinitialize the CGMS/WSS readback registers	This is a self-clearing bit
								1			Reinitializes the CGMS/WSS readback registers	
		Reserved	0	0	0	0	0					
0x79	VDP_CCAP_ DATA_0 (read only)	CCAP_BYTE_1[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 1 of CCAP	
0x7A	VDP_CCAP_ DATA_1 (read only)	CCAP_BYTE_2[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 2 of CCAP	
0x7D	VDP_CGMS_ WSS_DATA_0 (read only)	CGMS_CRC[5:2]					x	x	x	x	Decoded CRC sequence for CGMS	
		Reserved	0	0	0	0						
0x7E	VDP_CGMS_ WSS_DATA_1 (read only)	CGMS_WSS[13:8]			x	x	x	x	x	x	Decoded CGMS/WSS data	
		CGMS_CRC[1:0]	x	x							Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_ WSS_DATA_2 (read only)	CGMS_WSS[7:0]	x	x	x	x	x	x	x	x	Decoded CGMS/WSS data	
0x9C	VDP_OUTPUT_ SEL	Reserved					0	0	0	0		
		WSS_CGMS_CB_CHANGE				0					Disable content-based updating of CGMS and WSS data	The available bit shows the availability of data only when its content has changed
						1					Enable content-based updating of CGMS and WSS data	
		Reserved	0	0	0							

VPP MAP DESCRIPTION

To access the registers listed in Table 98, the user must set the VPP I²C device address by writing to VPP_SLAVE_ADDR[6:0]. VPP_SLAVE_ADDR[6:0] can be found in User Map Register 0xFD. Analog Devices recommended scripts set the VPP I²C device address to 0x84. The default bits are indicated by the gray shading.

Table 98. VPP Map Register Descriptions

VPP Map			Bits (Shading Indicates Default)									
Address	**Register**	**Bit Description**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**	**Notes**
0x41	DEINT_RESET	DEINT_RESET								0		
										1	Reset the I2P core	
		Reserved	0	0	0	0	0	0	0		Reserved	
0x55	I2C_DEINT_ENABLE	Reserved		0	0	0	0	0	0	0	Reserved	
		I2C_DEINT_ENABLE	0								Disable I2P converter	In order for the I2P converter to operate correctly, the ADV_TIMING_MODE_EN bit must be set to 1. Also changes to the output timing video are needed. Refer to the Analog Devices recommended scripts.
			1								Enable I2P converter	
0x5B	ADV_TIMING_MODE_EN	Reserved		0	0	0	0	0	0	0	Reserved	
		ADV_TIMING_MODE_EN	0								Disable advanced timing mode	
			1								Enable advanced timing mode	Advanced timing mode must be enabled in order for the I2P converter to work correctly

CSI MAP DESCRIPTION

To access the registers listed in Table 99, the user must set the CSI I²C device address by writing to CSI_TX_SLAVE_ADDR[6:0]. CSI_TX_SLAVE_ADDR[6:0] can be found in User Map Register 0xFE. Analog Devices recommended scripts set the CSI I²C device address to 0x88. The gray shading is indicates the default.

Table 99. MIPI CSI Map Register Descriptions

MIPI CSI Map			Bit (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x00	CSITX_PWRDN	Reserved		0	0	0	0	0	0	0	Reserved	
		CSITX_PWRDN	0								CSI Tx on	
			1								CSI Tx off	
0x01	TLPX	Reserved						0	0	0	Reserved	
		TLPX[4:0]	0	0	0	1	1				These bits set the duration of the T_{LPX} period of the D0P/D0N MIPI CSI-2 data lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. TLPX[4:0]must be greater than or equal to 2. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. TLPX[4:0] must be greater than or equal to 3.
0x02	THSPREP	Reserved						0	0	0	Reserved	
		THSPREP[4:0]	0	0	0	1	1				These bits set the duration of the $T_{HS-PREPARE}$ period of the D0P/D0N MIPI CSI-2 data lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. THSPREP[4:0] must be greater than or equal to 2. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. THSPREP[4:0] must be greater than or equal to 3.
0x03	THSZEROS	Reserved						0	0	0	Reserved	
		THSZEROS[4:0]	0	0	1	1	0				These bits set the duration of the HS-ZERO period of the D0P/D0N MIPI CSI-2 data lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. THSZEROS[4:0]must be greater than or equal to 4. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. THSZEROS[4:0] must be greater than or equal to 7.
0x04	THSTRAIL	Reserved						0	0	0	Reserved	
		THSTRAIL[4:0]	0	0	1	0	0				These bits set the duration of the HS-TRAIL period of the D0P/D0N MIPI CSI-2 data lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. THSTRAIL[4:0] must be greater than or equal to 3. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. THSTRAIL[4:0]must be greater than or equal to 4.
0x05	THSEXIT	Reserved						0	0	0	Reserved	
		THSEXIT[4:0]	0	0	1	0	1				These bits set the duration of the HS-EXIT period of the D0P/D0N MIPI CSI-2 data lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns. THSEXIT[4:0]must be greater than or equal to 3. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. THSEXIT[4:0]must be greater than or equal to 6.

MIPI CSI Map			Bit (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x06	TCLK_PREP	Reserved				0	0	0	0	0	Reserved	
		TCLK_PREP[4:0]	0	1	0						These bits set the duration of the HS-PREPARE period of the CLKP/CLKN MIPI CSI-2 clock lanes	For normal operation: A 1 bit increase results in an increase of 37.04 ns. TCLK_PREP[4:0] must be greater than or equal to 2. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. TCLK_PREP[4:0] must be greater than or equal to 4.
0x07	TCLK_ZEROS	Reserved						0	0	0		
		TCLK_ZEROS[4:0]	0	1	0	1	1				These bits set the duration of the HS-ZERO period of the CLKP/CLKN MIPI CSI-2 clock lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. TCLK_ZEROS [4:0] must be greater than or equal to 7. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. TCLK_ZEROS [4:0] must be greater than or equal to 14.
0x08	TCLK_TRAIL	Reserved					0	0	0	0	Reserved	
		TCLK_TRAIL[3:0]	0	0	1	1					These bits set the duration of the HS-TRAIL period of the CLKP/CLKN MIPI CSI-2 clock lanes.	For normal operation: A 1 bit increase results in an increase of 37.04 ns. TCLK_TRAIL[3:0] must be greater than or equal to 3. In I2P mode: A 1 bit increase results in an increase of 18.52 ns. TCLK_TRAIL[3:0] must be greater than or equal to 4.
0x09	ANCILLARY_DI	Reserved							0	0	Reserved	
		ANCILLARY_DI	1	1	0	0	0	0			Data type for ancillary data packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for ancillary data packets.
0x0A	VBIVIDEO_DI	Reserved							0	0		
		VBIVIDEO_DI	1	1	0	0	0	1			Data type for VBI data packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for Vertical Blanking Interval data packets.
0x0B	LSPKT_DI	Reserved							0	0	Reserved	
		LSPKT_DI	0	0	0	0	1	0			Data type for line start packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for line start packets.
0x0C	LEPKT_DI	Reserved							0	0	Reserved	
		LEPKT_DI	0	0	0	0	1	1			Data type for line end packets.	Sets the 6 data type bits used in the data identifier byte. In this case the data identifier byte is for line end packets.

MIPI CSI Map			Bit (Shading Indicates Default)									
Address	Register	Bit Description	7	6	5	4	3	2	1	0	Comments	Notes
0x0D	VC_REF	Reserved			0	0	0	0	0	0	Reserved	
		VC_REF	0	0							Virtual channel identifier	Sets the virtual channel identifier bits used in Data Identifier bytes. Data identifier bytes are used in MIPI CSI-2 data packets.
0x0E	CKSUM_EN	Reserved		0	0	0	0	0	0	0	Reserved	
		CKSUM_EN	0								High speed long packet checksum replaced with 0xFFFF	
			1								High speed long packet checksum appended to MIPI CSI stream	
0x1F	CSI_FRAME_ NUM_CTL	Reserved			0	0	0	0	0	0	Reserved	
		FBIT_VAL_AT_ FIELD1START_ INTERLACED		0							The field number is set to 0 at the start of the first field output.	Sets frame number used in MIPI CSI-2 frame start/end packets of first frame.
				1							The field number is set to 1 at the start of the first field output.	
		FRAMENUMBER_ INTERLACED	0								Frame number is 1 for odd fields and 2 for even fields.	Sets frame number in frame start/end packets This I2C bit only applies for interlaced video.
			1								Frame number is 2 for even fields and 1 for odd fields.	
0x20	CSI_ LINENUMBER_ INCR_ INTERLACED	Reserved		0	0	0	0	0	0	0	Reserved	
		LINENUMBER_INCR_ INTERLACED	0								Increment line numbers by 2 (default).	The line numbers in the line start (LS) and line end (LE) packets for interlaced video have to increment by more than 1. This bit gives the option of whether line numbers are incremented in steps of 2 or 3. This bit only applies for interlaced video.
			1								Increment line numbers by 3.	
0x26	ESC_MODE_CTL	Reserved					0	0	0	0	Reserved	
		ESC_XSHUTDOWN_CLK				0					These two bits are used to force the MIPI Clock lanes (CLKP and CLKN) to enter and exit the Ultralow Power State	See MIPI CSI-2 Tx Output section for more information.
						1						
		ESC_MODE_EN_CLK			0							
					1							
		ESC_XSHUTDOWN_D0		0							These two bits are used to force the MIPI Data lane (D0P and D0N) to enter and exit the Ultralow Power State	See MIPI CSI-2 Tx Output section for more information.
				1								
		ESC_MODE_EN_D0	0									
			1									
0xDE	DPHY_PWDN_ CTL	DPHY_PWDN								0	MIPI D-PHY Block is not powered-down	In order to use this bit, the DPHY_PWDN_OVERRIDE bit must be set to 1.
										1	MIPI D-PHY Block is powered-down	
		DPHY_PWDN_ OVERRIDE							0		Disable manual control of MIPI D-PHY powerdown.	
									1		Enable manual control of MIPI D-PHY powerdown.	The MIPI D-PHY block can now be powered down by using the DPHY_PWDN bit.
		Reserved	0	0	0	0	0	0			Reserved	

REFERENCES

CEA-861-D Standard, A DTV Profile for Uncompressed High Speed Digital Interfaces, Revision D, July 18, 2006.

ITU-R BT.656-4 Recommendation, *Interface for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation*
ITU-R BT.601, February 1998.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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