Dual 14 BIT, 65 MSPS™ Analog-to-Digital Converter

FEATURES

- Dual ADC
- 14 Bit Resolution
- 65 MSPS Sample Rate
- High SNR = 74 dBFs at 70 MHz f_{IN}
- High SFDR = 84 dBc at 70 MHz f_{IN}
- 2.3 V_{PP} Differential Input Voltage
- Internal / External Voltage Reference
- 3.3 V Single-Supply Voltage
- Analog Power Dissipation = 0.72 W
- Output Supply Power Dissipation = 0.17 W
- 80 Lead PowerPad™ TQFP Package
- Two's Complement Output Format

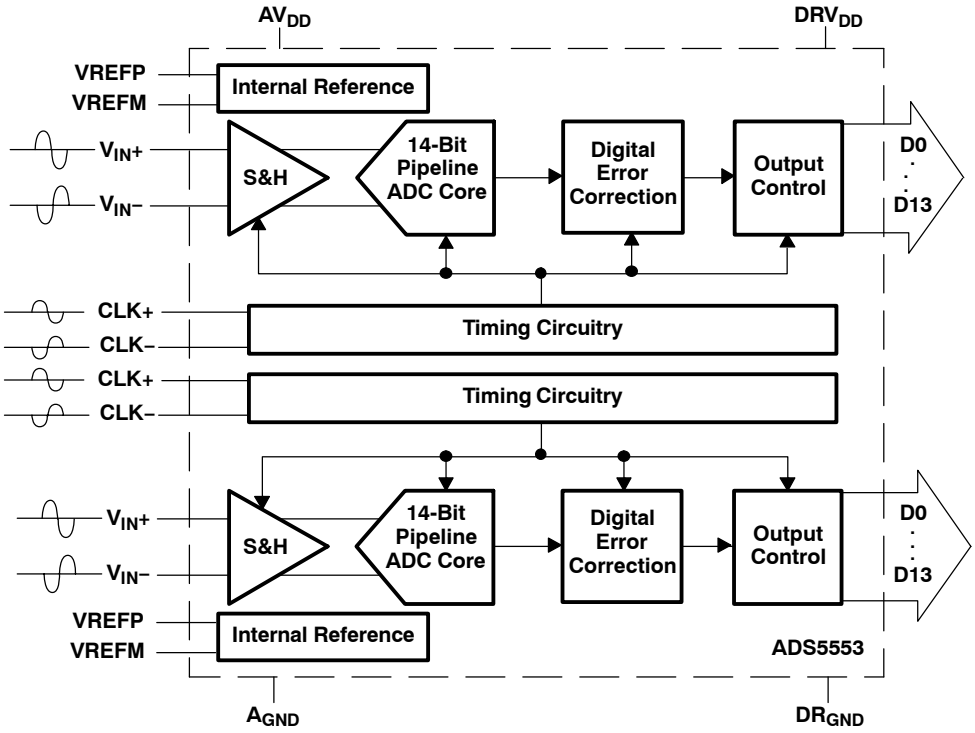
APPLICATIONS

- Communication Receivers
- Base Station Infrastructure
- Test and Measurement Instrumentation

DESCRIPTION

The ADS5553 is a high-performance, dual channel, 14 bit, 65 MSPS analog-to-digital converter (ADC). To provide a complete solution, each channel includes a high-bandwidth linear sample-and-hold stage (S&H) and an internal reference. Designed for applications demanding high dynamic performance in a small space, the ADS5553 has excellent power consumption of 0.9 W at 3.3 V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements, yet an external reference can be used optionally to suit the accuracy and low drift requirements of the application. The outputs are parallel CMOS compatible.

The ADS5553 is available in a 80 lead TQFP PowerPAD package and is specified over the full temperature range of –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE–LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5553	HTQFP-80(2) PowerPAD	PFP	–40°C to 85°C	ADS5553I	ADS5553IPFP	Tray, 96
					ADS5553IPFPR	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 6.17 mm x 6.17 mm (min), 7,5 mm x 7,5 mm (max). θ_{ja} = 21°C/W (no airflow) or 15°C/W (with 200 LPFM airflow), θ_{jc} = 13.5°C/W, and θ_{jp} (to the bottom PowerPad) = 2°C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in x 3 in PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		ADS5553	UNIT
Supply Voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}	–0.3 to 3.7	V
	A_{GND} to DR_{GND}	±0.1	V
Analog input to A_{GND}(2)		–0.3 to 3.6	V
Logic input to DR_{GND}		–0.3 to DRV_{DD} + 0.3	V
Digital data output to DR_{GND}		–0.3 to DRV_{DD} + 0.3	V
Operating temperature range		–40 to 85	°C
Junction temperature		105	°C
Storage temperature range		–65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) For more details, see the *Input Voltage Overstress* section in this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supplies				
Analog supply voltage, AV_{DD}	3	3.3	3.6	V
Output driver supply voltage, DRV_{DD}	3	3.3	3.6	V
Analog Input				
Differential input range		2.3		V_{PP}
Input common-mode voltage, V_{CM}(1)	1.45	1.55	1.65	V
Digital Output				
Maximum output load		10		pF
Clock Input				
ADCLK input sample rate (sine wave) $1/t_C$	10		65	MSPS
Clock amplitude, sine wave, differential(2)		3		V_{PP}
Clock duty cycle(3)		50%		
Open free-air temperature range	–40		85	°C

(1) Input common-mode should be connected to CM.
(2) See Figure 20 for more information.
(3) See Figure 21 for more information.

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 65 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, –1-dBFS differential input, 3-V_{PP} differential clock, and internal reference, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				14		Bits
Analog Inputs						
Differential input range				2.3		V_{PP}
Differential input capacitance	See Figure 28			3.2		pF
Total analog input common-mode current				200(1)		µA
Analog input bandwidth	Source impedance = 50 Ω			750		MHz
Internal Reference Voltages						
Reference bottom voltage, V_{REFM}				1.01		V
Reference top voltage, V_{REFP}				2.16		V
Total gain error(2)				±3.5		%FS
Common-mode voltage output, V_{CM}				1.57		V
Dynamic Linearity and Accuracy						
No missing codes				Tested		
Differential linearity error, DNL	f_{IN} = 46MHz		–0.95	±0.6	1	LSB
Integral linearity error, INL	f_{IN} = 46 MHz		–4	±2.5	4	LSB
Offset error				±4		mV
Offset temperature coefficient				7		µV/°C
Offset matching				±0.7		mV
Gain error(3)				±0.5		%FS
Gain temperature coefficient(3)				0.0015		Δ%/°C
Gain matching(3)				±0.1		%FS
Dynamic AC Characteristics						
Signal-to-noise ratio, SNR	f_{IN} = 10 MHz			74.4		dBFS
	f_{IN} = 46 MHz			74		
	f_{IN} = 70 MHz	25°C to 85°C	72.4	74		
		Full temp range	71.4	74		
	f_{IN} = 100 MHz			73.5		
	f_{IN} = 150 MHz			72.5		
	f_{IN} = 225 MHz			71		
RMS output noise	Input tied to common-mode			1		LSB
Spurious-free dynamic range, SFDR	f_{IN} = 10 MHz			85		dBc
	f_{IN} = 46 MHz			84		
	f_{IN} = 70 MHz	Room temp	80	84		
		Full temp range	78	83		
	f_{IN} = 100 MHz			83		
	f_{IN} = 150 MHz			81		
	f_{IN} = 225 MHz			75		

(1) 100-µA per input

(2) Includes error due to references. The total gain error will become smaller (see gain error in the *Dynamic Linearity and Accuracy* section of this table) if an external reference is used.

(3) Gain error left assuming ideal references: V_{REFP} – V_{REFM} = 1.15 V

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 65 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, –1-dBFS differential input, 3-V_{PP} differential clock, and internal reference, unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Second-harmonic, HD2	f_{IN} = 10 MHz			93		dBc
	f_{IN} = 46 MHz			93		
	f_{IN} = 70 MHz	Room temp	80	86		
		Full temp range	78	85		
	f_{IN} = 100 MHz			86		
	f_{IN} = 150 MHz			82		
	f_{IN} = 225 MHz			79		
Third-harmonic, HD3	f_{IN} = 10 MHz			85		dBc
	f_{IN} = 46 MHz			84		
	f_{IN} = 70 MHz	Room temp	80	84		
		Full temp range	78	83		
	f_{IN} = 100 MHz			83		
	f_{IN} = 150 MHz			81		
	f_{IN} = 225 MHz			75		
Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	Room temp		86		dBc
	f_{IN} = 70 MHz	Room temp		85		
Signal-to-noise + distortion, SINAD	f_{IN} = 10 MHz			74		dBFS
	f_{IN} = 46 MHz			73.5		
	f_{IN} = 70 MHz	25°C to 85°C	71.8	73.4		
		Full temp range	71	73		
	f_{IN} = 100 MHz			73		
	f_{IN} = 150 MHz			71.8		
	f_{IN} = 225 MHz			69.5		
Total harmonic distortion, THD	f_{IN} = 10 MHz			83		dBc
	f_{IN} = 46 MHz			82		
	f_{IN} = 70 MHz	Room temp		82		
		Full temp range		82		
	f_{IN} = 100 MHz			81		
	f_{IN} = 150 MHz			81		
	f_{IN} = 225 MHz			74		
Effective number of bits, ENOB	f_{IN} = 70 MHz			11.9		Bits
Two-tone intermodulation distortion, IMD3	f = 10.1 MHz, 15.1 MHz (–7dBFS each tone)			94		dBc
	f = 48 MHz, 53 MHz (–7 dBFS each tone)			84		
	f = 147 MHz, 152 MHz (–7 dBFS each tone)			75		
Crosstalk	f_{IN} = 70 MHz[4]			–100	–95	dBc

(4) Inject one tone at –1 dBFS on one channel and measure the ampltitude on the other channel, then repeat for the other channel

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 65 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, –1-dBFS differential input, 3-V_{PP} differential clock, and internal reference, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply					
Total supply current, I_{CC}	V_{IN} = full-scale, f_{IN} = 70 MHz		270	288	mA
Analog supply current, I_{AVDD}	V_{IN} = full-scale, f_{IN} = 70 MHz		220	230	mA
Output buffer supply current, I_{DRVDD}	V_{IN} = full-scale, f_{IN} = 70 MHz, with 10 pF load on digital outputs to ground		50	58	mA
Power dissipation	Analog only, f_{IN} = 70 MHz		725	760	mW
	Digital power with 10-pF load on digital outputs to ground, f_{IN} = 70 MHz		165	190	
Power dissipation with external reference	Total power with 10-pF load on digital outputs to ground, f_{IN} = 70 MHz		780	820	mW
Standby power	With clocks running (both channels off and outputs disabled)		220	250	mW

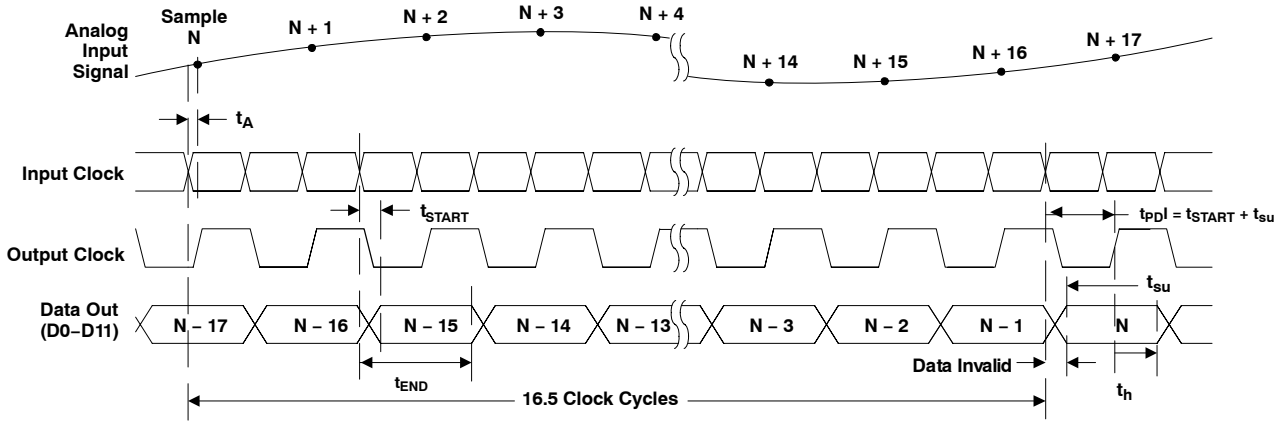
DIGITAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, and AV_{DD} = DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current				10	µA
Low-level input current				10	µA
Input capacitance			4		pF
Digital Outputs(1)					
Low-level output voltage	C_{LOAD} = 10 pF(2)		0.3	0.4	V
High-level output voltage	C_{LOAD} = 10 pF(2)	2.8	3		V
Output capacitance			3		pF

(1) For optimal performance, all digital output lines (D0:D13), including the output clock, should see a similar load.
(2) Equivalent capacitance to ground of (load + parasitics of transmission lines).

TIMING CHARACTERISTICS



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 1. Timing Diagram

TIMING CHARACTERISTICS(3)

Over full temperature range (T_{MIN} = –40°C to T_{MAX} = +85°C), sampling rate = 65 MSPS, 50% clock duty cycle, and AV_{DD} = DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification					
Aperture delay, t_A	Input CLK falling edge to data sampling point		1		ns
Aperture delay matching, t_A	Channel-to-channel aperture delay matching		50		ps
Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
Latency			16.5		Clock Cyles
Data setup time, t_{su}	Data valid(1) to 50% of CLKOUT rising edge	4.3	6		ns
Data hold time, t_h	50% of CLKOUT rising edge to data becoming invalid(1)	2	2.8		ns
Data start time, t_{START}	50% of clock input to beginning of valid data(1)		2.5	4.5	ns
Data stop time, t_{END}	50% of clock input to end of valid data(1)	9	10.6		ns
Data rise time, t_r	Data rise time measured from 20% to 80% of DRV_{DD}		6.6		ns
Data fall time, t_f	Data fall time measured from 80% to 20% of DRV_{DD}		5.5		ns
Data setup time, t_{su}	Data valid(1) to 50% of CLKOUT rising edge, f_S = 40 MSPS	8.5	11		ns
Data hold time, t_h	50% of CLKOUT rising edge to data becoming invalid(1), f_S = 40 MSPS	2.6	4		ns
Data start time, t_{START}	50% of clock input to beginning of valid data(1), F_S = 40 MSPS		–2.5	1	ns
Data stop time, t_{END}	50% of clock input to end of valid data(1), F_S = 40 MSPS	11.5	13		ns
Data rise time, t_r	Data rise time measured from 20% to 80% of DRV_{DD}, f_S = 40 MSPS		7.5		ns
Data fall time, t_f	Data fall time measured from 80% to 20% of DRV_{DD}, f_S = 40 MSPS		7.3		ns
Output enable (OE) to data output delay	Time required for outputs to have stable timings with respect to the input clock(2) after OE is activated			1000	Clock Cycles

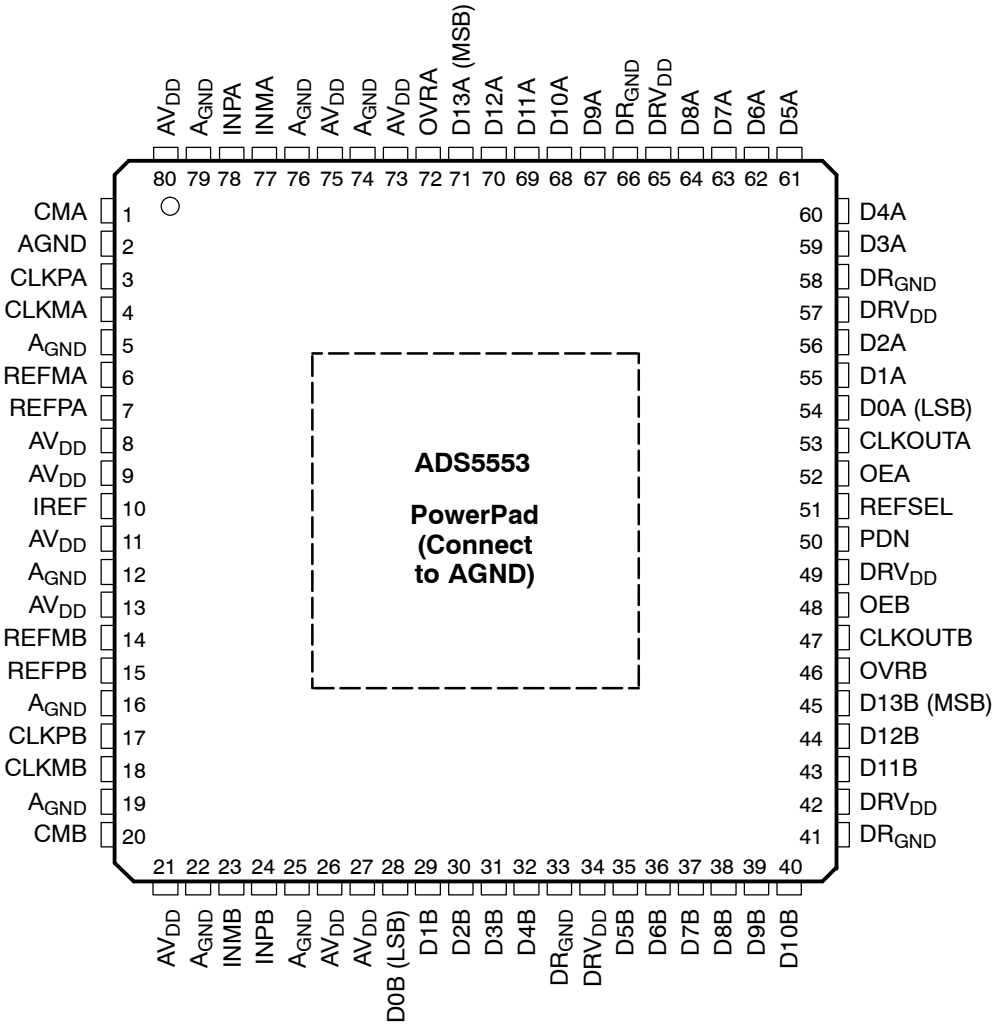
(1) Data valid refers to 2 V for logic high and 0.8 V for logic low.

(2): Data outputs are available within a clock from assertion of OE; however it takes 1000 clock cycles to ensure stable timing with respect to input clock.

(3): Timing parameters are ensured by design and characterization and not tested in production.

PIN CONFIGURATION

PFP PACKAGE
(TOP VIEW)



PIN ASSIGNMENTS

TERMINAL NAME	NO.	NO. OF PINS	I/O	DESCRIPTION
AV_{DD}	8, 9, 11, 13, 21, 26, 27, 73, 75, 80	10	I	Analog power supply
A_{GND}	2, 5, 12, 16, 19, 22, 25, 74, 76, 79	10	I	Analog ground
CLKMA	4	1	I	Channel A differential input clock (negative)
CLKMB	18	1	I	Channel B differential input clock (negative)
CLKOUTA	53	1	O	Channel A clock out in sync with data
CLKOUTB		1	O	Channel B clock out in sync with data
CLKPA	3	1	I	Channel A differential input clock (positive)
CLKPB	17	1	I	Channel B differential input clock (positive)
CMA	1	1	O	Channel A common-mode output voltage
CMB	20	1	O	Channel B common-mode output voltage
D0A (LSB)–D13A (MSB)	54–56, 59–64, 67–71	14	O	Channel A parallel data
D0B (LSB)–D13B (MSB)	28–32, 35–40, 43–45	14	O	Channel B parallel data
DRV_{DD}	34, 42, 49, 57, 65	4	I	Output driver power supply
DR_{GND}	33, 41, 58, 66	4	I	Output driver ground
INMA	77	1	I	Channel A differential analog input (negative)
INMB	23	1	I	Channel B differential analog input (negative)
INPA	78	1	I	Channel A differential analog input (positive)
INPB	24	1	I	Channel B differential analog input (positive)
IREF	10	1	I	Current set, 56-kΩ resistor to GND
OEA	52	1	I	Channel A output enable (active high)
OEB	48	1	I	Channel B output enable (active high)
OVRA	72	1	O	Channel A over-range indicator bit
OVRB	46	1	O	Channel B over-range indicator bit
REFMA	6	1	I	Channel A reference voltage (negative); 0.1 μF to GND
REFMB	14	1	I	Channel B reference voltage (negative); 0.1 μF to GND
REFPA	7	1	I	Channel A reference voltage (positive); 0.1 μF to GND
REFPB	15	1	I	Channel B reference voltage (positive); 0.1 μF to GND
PDN	50	1	I	Power down active high. See Table 2
REFSEL	51	1	I	Reference select. 1 → EXT. REF; 0 → INT. REF

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the *Electrical Specifications* section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree celcius of the parameter from T_{MIN} to T_{MAX}. It is calcuated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}-T_{MIN}$.

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

DEFINITION OF SPECIFICATIONS

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1-f_2$ or $2f_2-f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 65 MSPS, unless otherwise noted

SPECTRAL PERFORMANCE

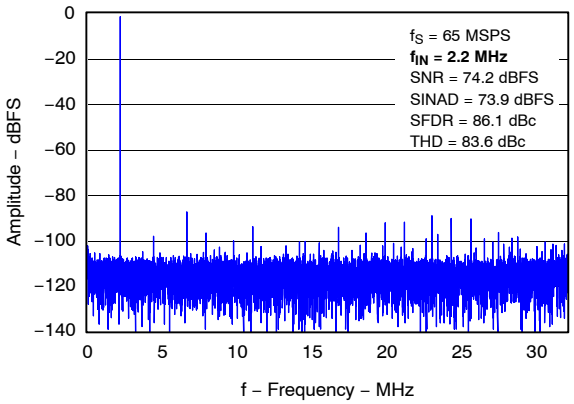


Figure 2

SPECTRAL PERFORMANCE

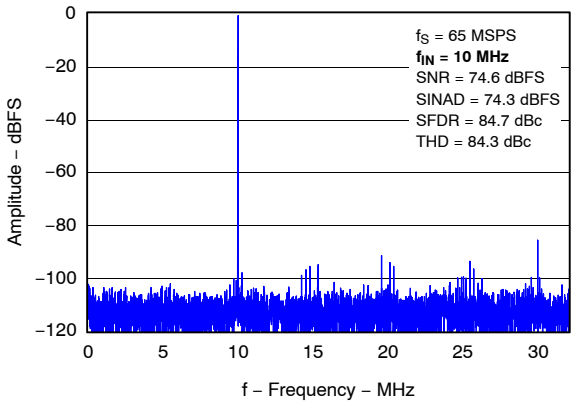


Figure 3

SPECTRAL PERFORMANCE

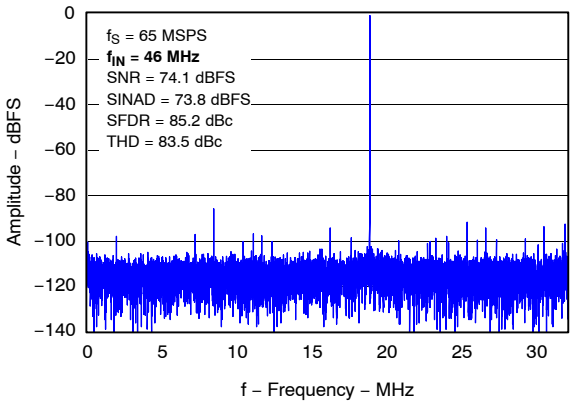


Figure 4

SPECTRAL PERFORMANCE

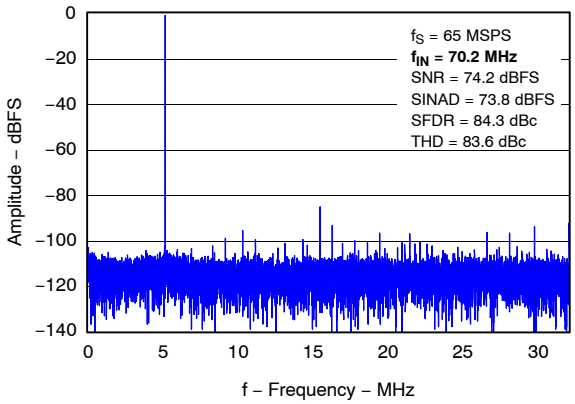


Figure 5

SPECTRAL PERFORMANCE

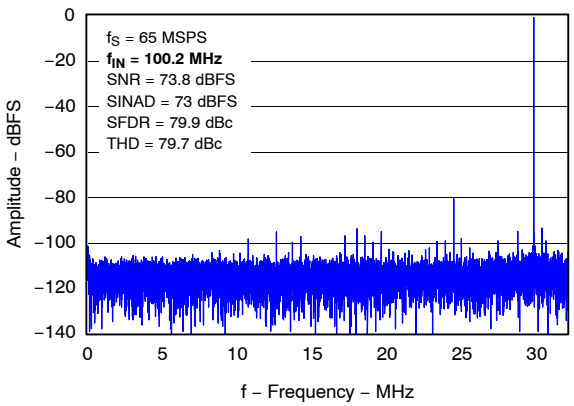


Figure 6

SPECTRAL PERFORMANCE

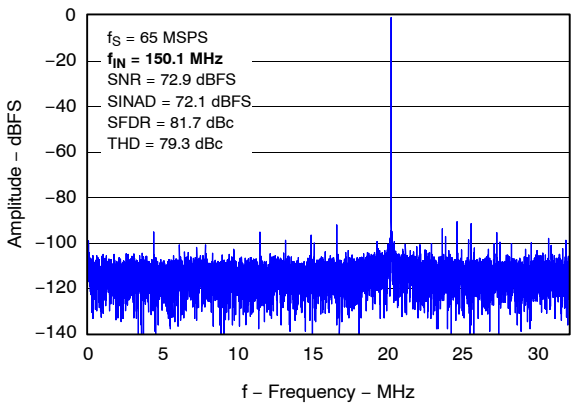


Figure 7

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 65 MSPS, unless otherwise noted

SPECTRAL PERFORMANCE

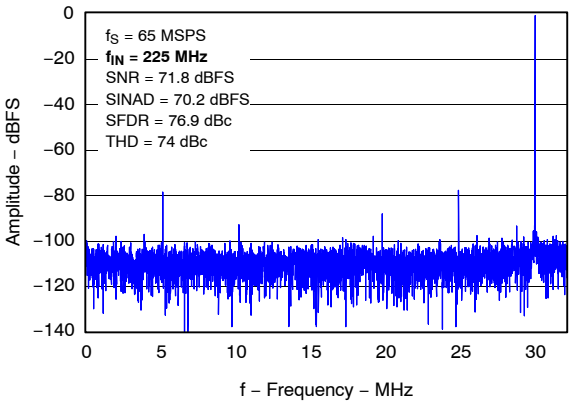


Figure 8

SPECTRAL PERFORMANCE

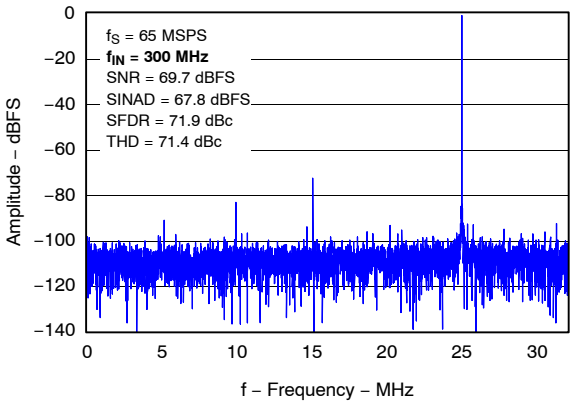


Figure 9

SPECTRAL PERFORMANCE

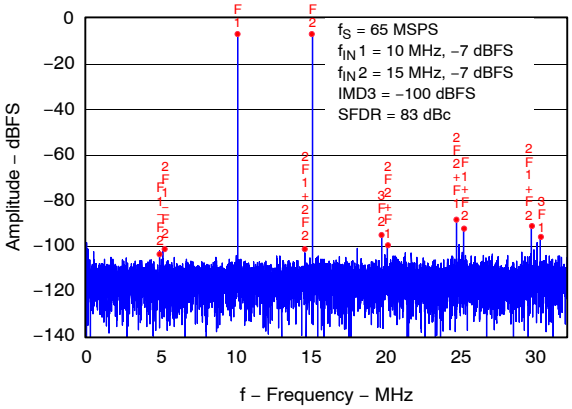


Figure 10

SPECTRAL PERFORMANCE

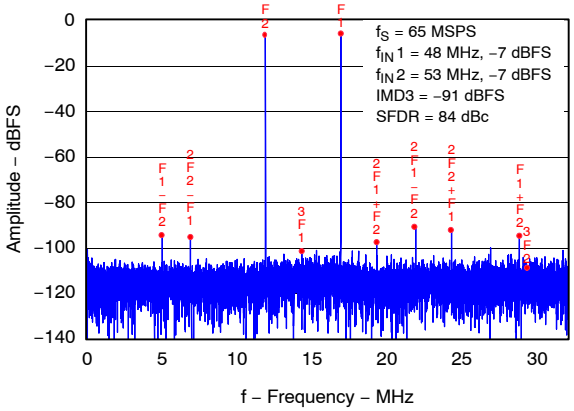


Figure 11

SPECTRAL PERFORMANCE

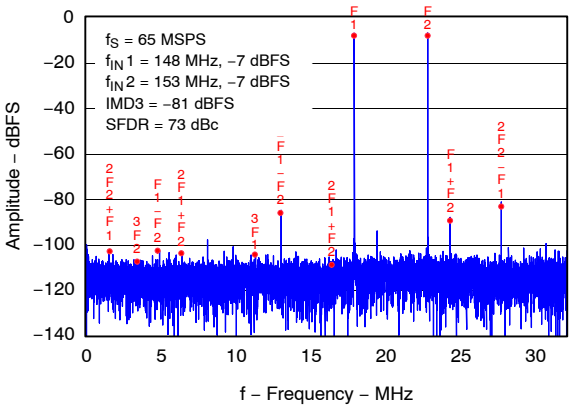


Figure 12

NOISE HISTOGRAM WITH INPUTS SHORTED

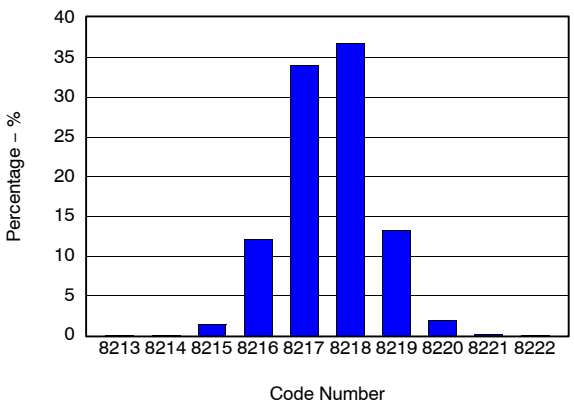


Figure 13

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 65 MSPS, unless otherwise noted

WCDMA CARRIER

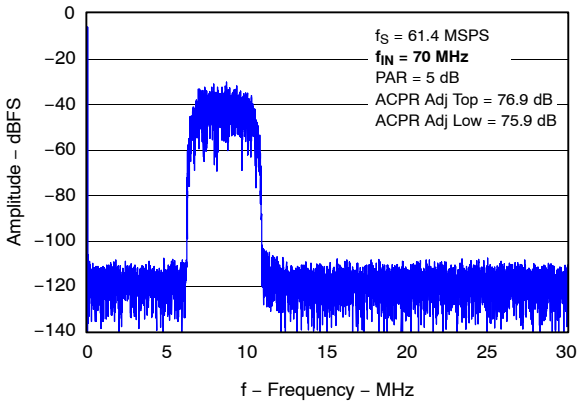


Figure 14

WCDMA CARRIER

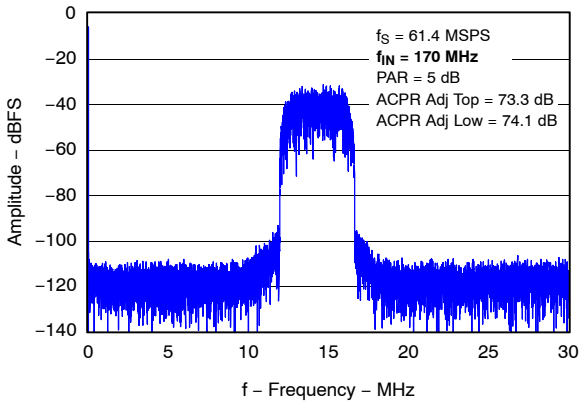


Figure 15

AC PERFORMANCE vs INPUT AMPLITUDE

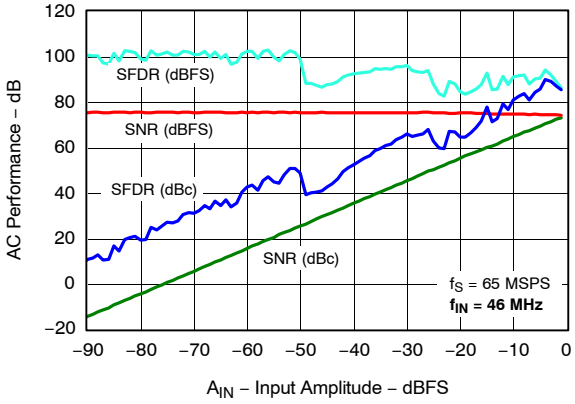


Figure 16

AC PERFORMANCE vs INPUT AMPLITUDE

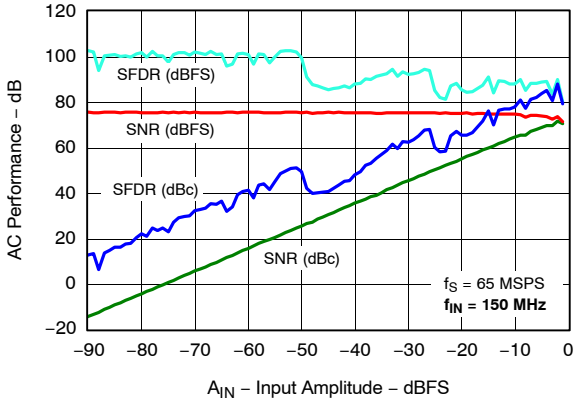


Figure 17

AC PERFORMANCE vs INPUT AMPLITUDE

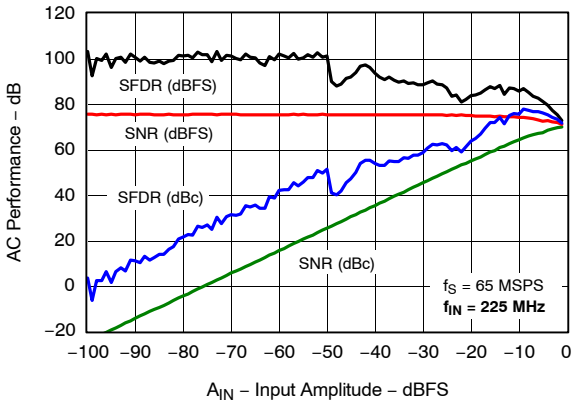


Figure 18

POWER DISSIPATION vs SAMPLING RATE

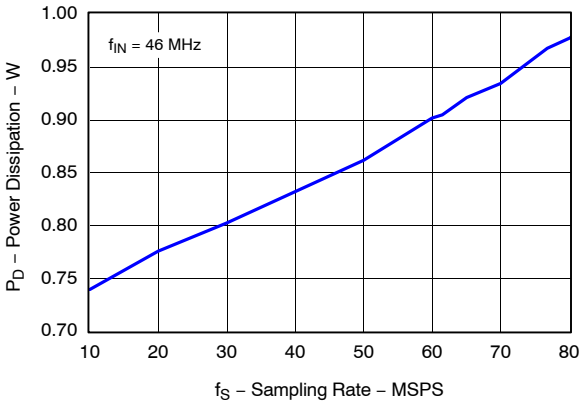


Figure 19

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 65 MSPS, unless otherwise noted

AC PERFORMANCE vs DIFFERENTIAL CLOCK AMPLITUDE

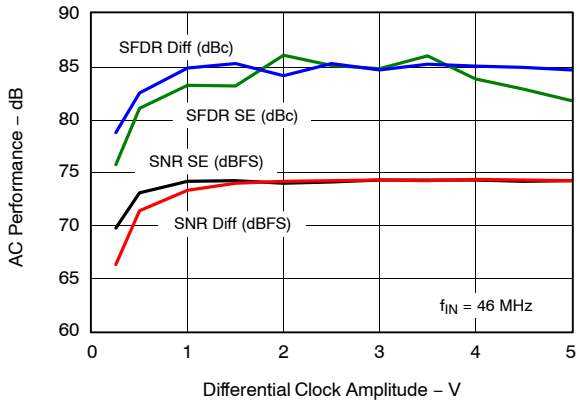


Figure 20

AC PERFORMANCE vs DUTY CYCLE

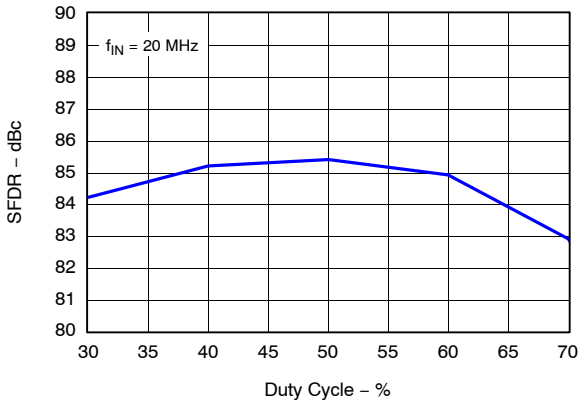


Figure 21

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

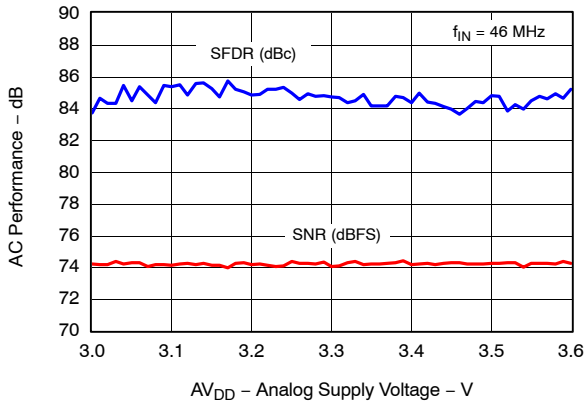


Figure 22

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

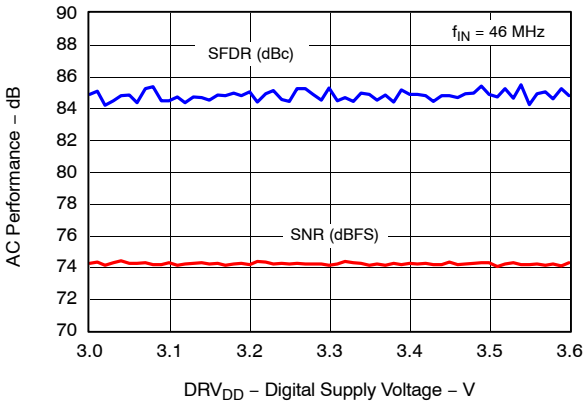


Figure 23

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

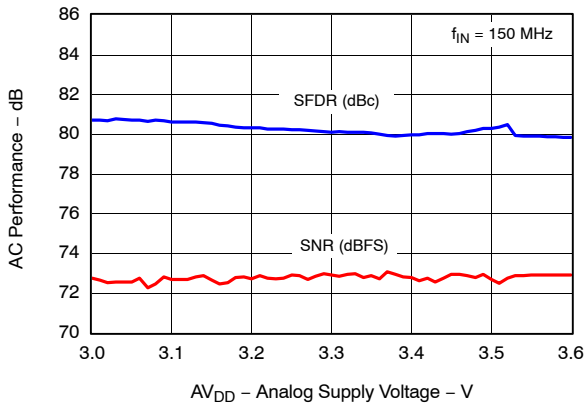


Figure 24

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

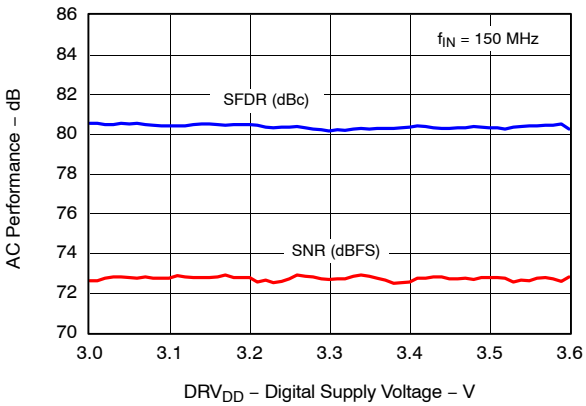


Figure 25

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 65 MSPS, unless otherwise noted

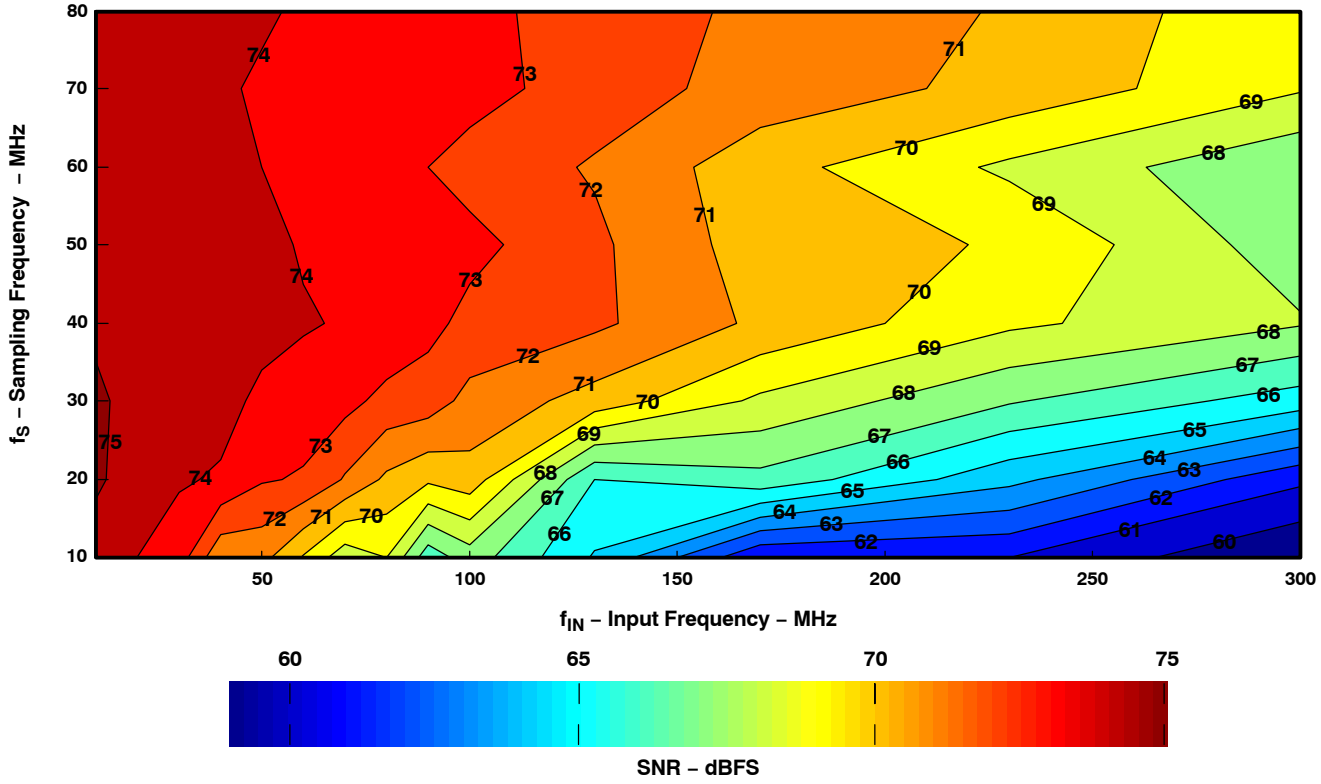


Figure 26.

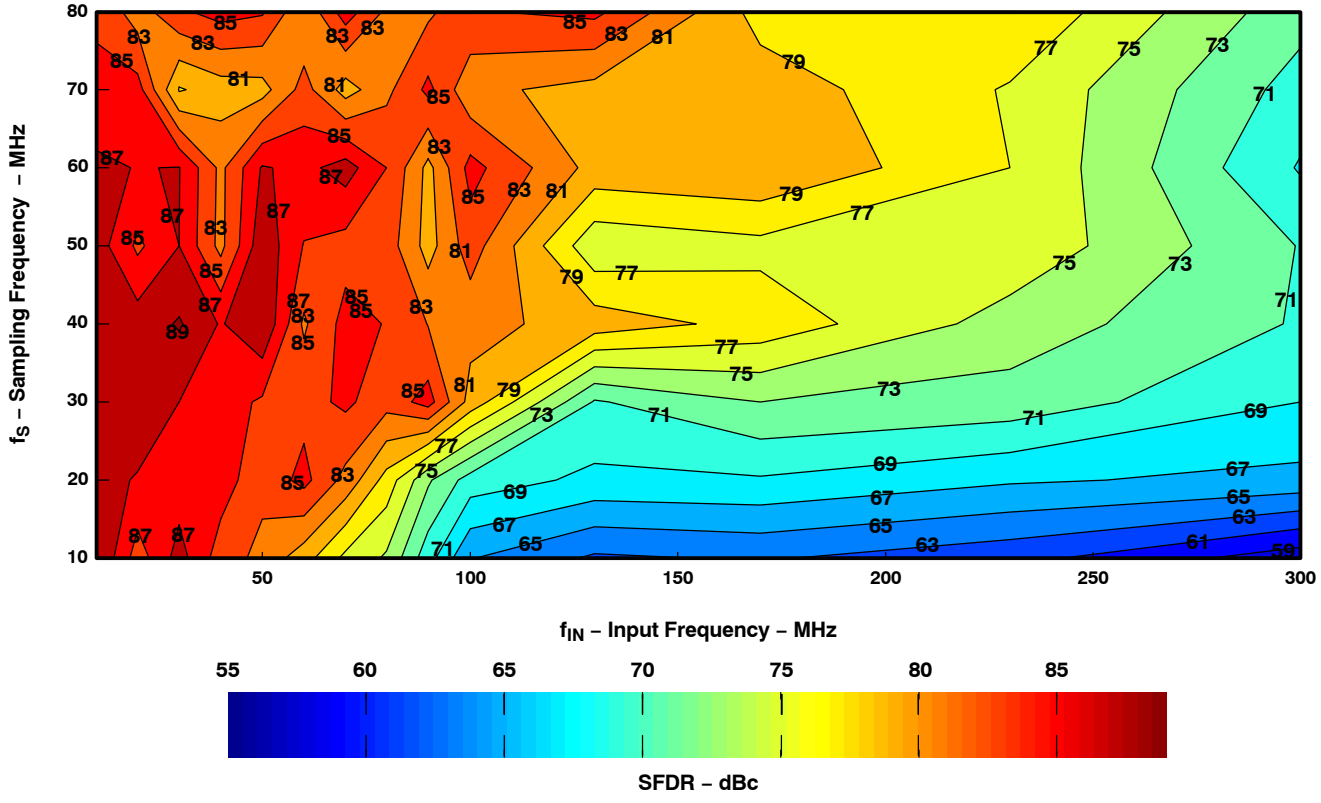


Figure 27.

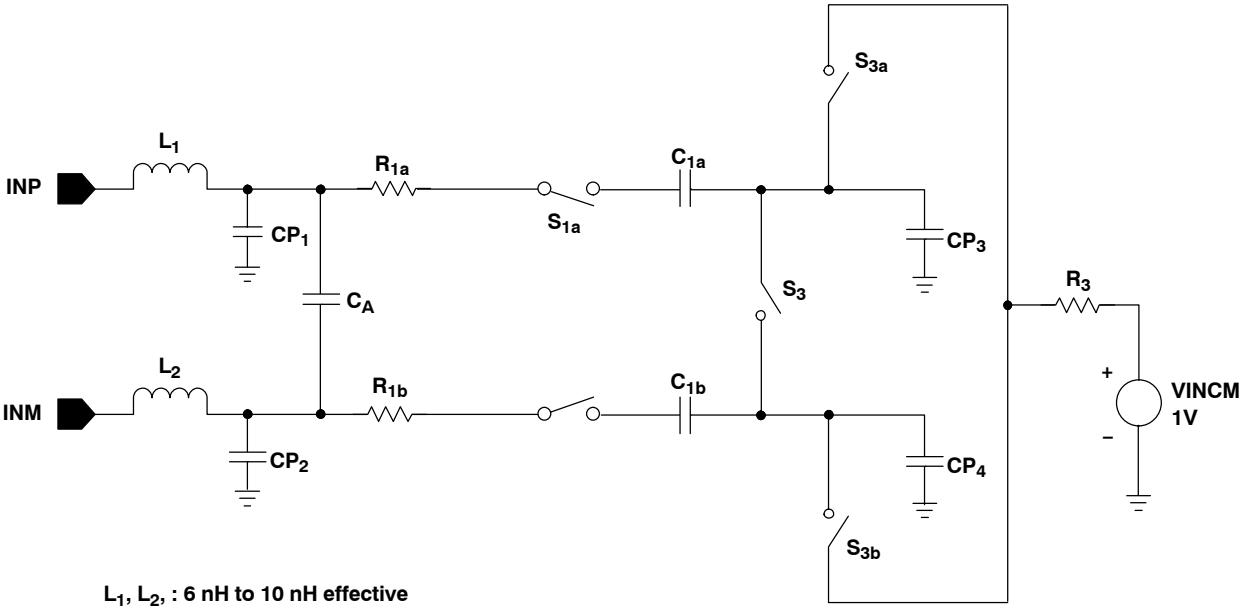
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5553 is a low-power, dual 14 bit, 65 MSPS, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3 V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 16.5 clock cycles, after which the output data is available as a 14 bit parallel word, coded in binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5553 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique, shown in Figure 28.



L_1, L_2, : 6 nH to 10 nH effective
R_{1a}, R_{1b} : 5 Ω to 8 Ω
C_{1a}, C_{1b} : 2.2 pF to 2.6 pF
CP_1, CP_2 : 1.8 pF to 2.2 pF
CP_3, CP_4 : 1.2 pF to 1.8 pF
C_A : 0.8 pF to 1.2 pF
R_3 : 80 Ω to 120 Ω
Switches : S_{1a}, S_{1b} : On Resistance : 35 Ω to 50 Ω
S2, : On Resistance : 7.5 Ω to 15 Ω
S_{3a}, S_{3b} : On Resistance : 40 Ω to 60 Ω
All switches Off Resistance : 10 GΩ

All switches are on in sampling phase which is approximately one half of a clock period.

Figure 28. Analog Input Stage

This differential input topology produces a high level of ac performance for high sampling rates. It also results in a high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5553 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pins 1 and 20). For a full-scale differential input, each of the differential lines of the input signal swings symmetrically between CM + 0.575 V and CM – 0.575 V. This means that each input is driven with a signal of up to CM ±0.575 V, so that each input has a maximum differential signal of 1.15 V_{PP} for a total differential input signal swing of 2.3 V_{PP}. The maximum swing is determined by the two reference voltages, the top reference (REFPA, pin 7 and REFPB, pin 15) and the bottom reference (REFMA, pin 6 and REFMB, pin 18).

The ADS5553 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 29 shows one possible configuration using an RF transformer.

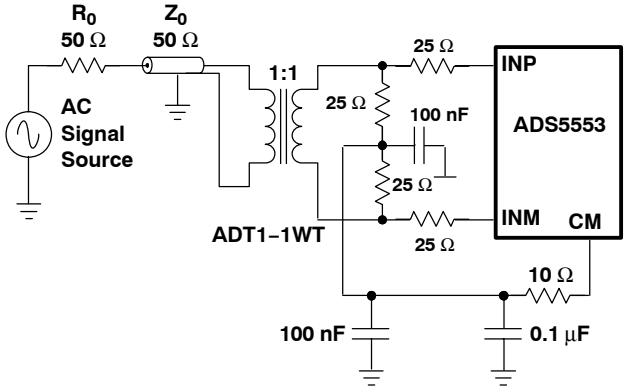


Figure 29. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5553 is connected to the center-tap of the secondary winding. To ensure a steady low-noise V_{CM} reference, best performance is obtained when the CM output (pins 1 and 20) is filtered to ground with a 10 Ω series resistor and parallel 0.1 μF and 0.001 μF low-inductance capacitors as shown in Figure 29.

Output V_{CM} (pins 1 and 20) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 200 μA (100 μA per input). Equation (1) describes the dependency of the common-mode current and the sampling frequency:

$$20 + \frac{400\ \mu A \times f_s(\text{in MSPS})}{125\text{MSPS}} \quad (1)$$

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5553. Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA847, and OPA695) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instruments THS9001, can also be used with an RF transformer for high input frequency applications. The THS4503/6 are recommended differential input/output amplifiers. Table 1 lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA847, or OPA695) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5553. These three amplifier circuits minimize even-order harmonics. For high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5553 directly, as shown in Figure 29 or with the addition of the filter circuit shown in Figure 30.

Figure 30 illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5553 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5553 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications

requiring dc coupling of the input. Flexible in their configurations (see Figure 31), such amplifiers can be used for single-ended-to-differential conversion, signal amplification.

Table 1. Recommended Amplifiers to Drive the Input of the ADS5553

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20 MHz	THS4503/6	Differential In/Out Amp	No
DC to 50 MHz	OPA847	Operational Amp	Yes
10 MHz to 120 MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100 MHz	THS9001	RF Gain Block	Yes

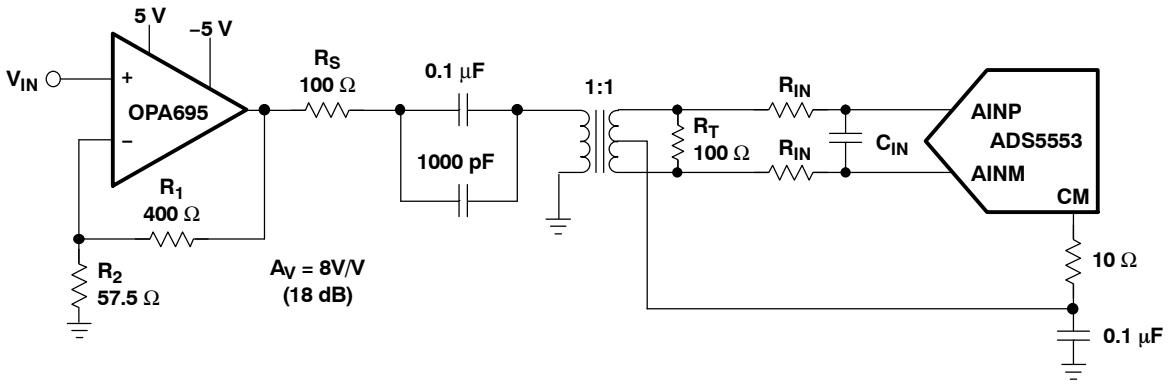


Figure 30. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

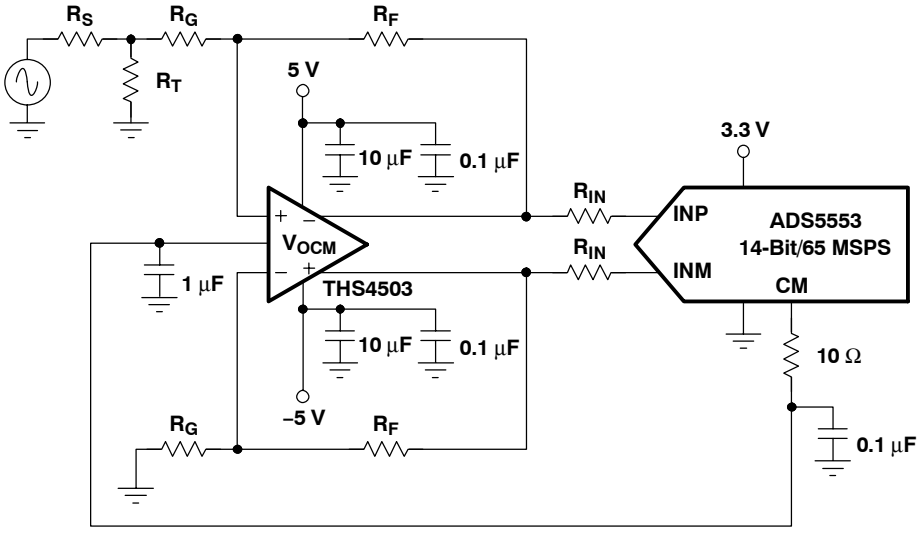


Figure 31. Using the THS4503 With the ADS5553

INPUT VOLTAGE OVER-STRESS

The ADS5553 can handle absolute maximum voltages of 3.6 V DC on the input pins INP and INM. For DC inputs between 3.6 V and 3.8 V, a 25 Ω resistor is required in series with the input pins. For inputs above 3.8 V, the device can handle only transients, which need to have less than 5% duty cycle of overstress. The input pins connect internally to an ESD diode to AV_{DD}, as well as a switched capacitor circuit. The sampling capacitor of the switched capacitor circuit connects to the input pins through a switch in the sample phase. In this phase, an input larger then 2.65 V would cause the switched capacitor circuit to present an equivalent load of a forward biased diode to 2.65 V, in series with a 60Ω impedance. Also, beyond the voltage on AV_{DD}, the ESD diode to AV_{DD} starts to become forward biased.

In the phase where the sampling switch is off, the diode loading from the input switched capacitor circuit is disconnected from the pin, while the ESD loading to AV_{DD} is still present.

CAUTION:

A violation of any of the previously stated conditions could damage the device (or reduce its lifetime) either due to electromigration or gate oxide integrity. Care should be taken not to expose the device to input over-voltage for extended periods of time as it may degrade device reliability.

POWER SUPPLY SEQUENCE

The preferred mode of power supply sequencing is to power up AV_{DD} first, followed by DRV_{DD}. Raising both supplies simultaneously is also a valid power supply sequence. In the event that DRV_{DD} powers up before AV_{DD} in the system, AV_{DD} must power up within 10 ms of DRV_{DD}.

POWER DOWN

The device enters power down in one of two ways: either by reducing the clock speed to between dc and 1 MHz or by selecting any of the modes in Table 2. If reducing the clock speed, power-down may be initiated for any clock frequency below 10 MHz. The actual frequency at which the device powers down varies from device to device.

Table 2. Powerdown Mode Selection

PDN (Pin 50)	OEA (Pin 52)	OEB (Pin 48)	Out A	Out B	ADC A	ADC B
0	0	0	Off	Off	On	On
0	0	1	Off	On	On	On
0	1	0	On	Off	On	On
0	**1**	**1**	**On**	**On**	**On**	**On**
1	0	0	Off	Off	Off	Off
1	0	1	Off	On	Off	On
1	1	0	On	Off	On	Off
1	1	1	On	On	On	On

REFERENCE CIRCUIT

The ADS5553 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1 μF decoupling capacitor in series with a 20 Ω resistor, as shown in Figure 32. In addition, an external 56.2-kΩ resistor should be connected from IREF (pin 10) to AGND to set the proper current for the operation of the ADC, as shown in Figure 32. No capacitor should be connected between pin 31 and ground; only the 56.2 kΩ resistor should be used.

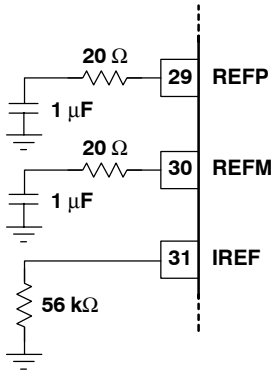


Figure 32. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5553 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM using internal 5-kΩ resistors that connect CLKP and CLKM to CM , as shown in Figure 33.

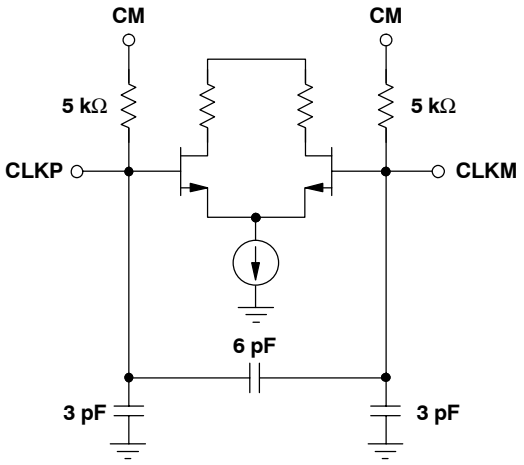


Figure 33. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM to ground with a 0.01 μF capacitor, while CLKP is ac-coupled with a 0.01 μF capacitor to the clock source, as shown in Figure 34.

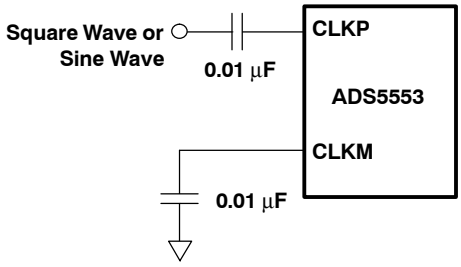


Figure 34. AC-Coupled, Single-Ended Clock Input

The ADS5553 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01 μF capacitors, as shown in Figure 35.

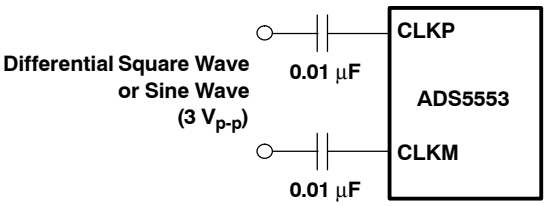


Figure 35. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 24 shows the performance variation of the ADC versus clock duty cycle.

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter further improves as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 23 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, see the ADS5553EVM user's guide (SLWU010), available for download from www.ti.com.

OUTPUT INFORMATION

Each of the two ADCs provide 14 data outputs in two's complement format (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT), and an out-of-range indicator (OVR) that equals 1 when the output reaches the full-scale limits.

In addition, output enable control (pins 48 and 52) are provided to tri-state the outputs. See Table 2 for details.

The output circuitry of the ADS5553 has been designed to minimize the noise produced by the transients of the data switching and in particular its coupling to the ADC analog circuitry. Output D0 senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1, as long as all outputs (including CLKOUT) have a similar load as the one at D0. This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. External series resistors with the output are not necessary.

PowerPAD PACKAGE

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the *Mechanical Data* section.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the SLMA004B Application Brief *PowerPAD Made Easy* or the SLMA002 Technical Brief *PowerPAD Thermally Enhanced Package.*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5553IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5553I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

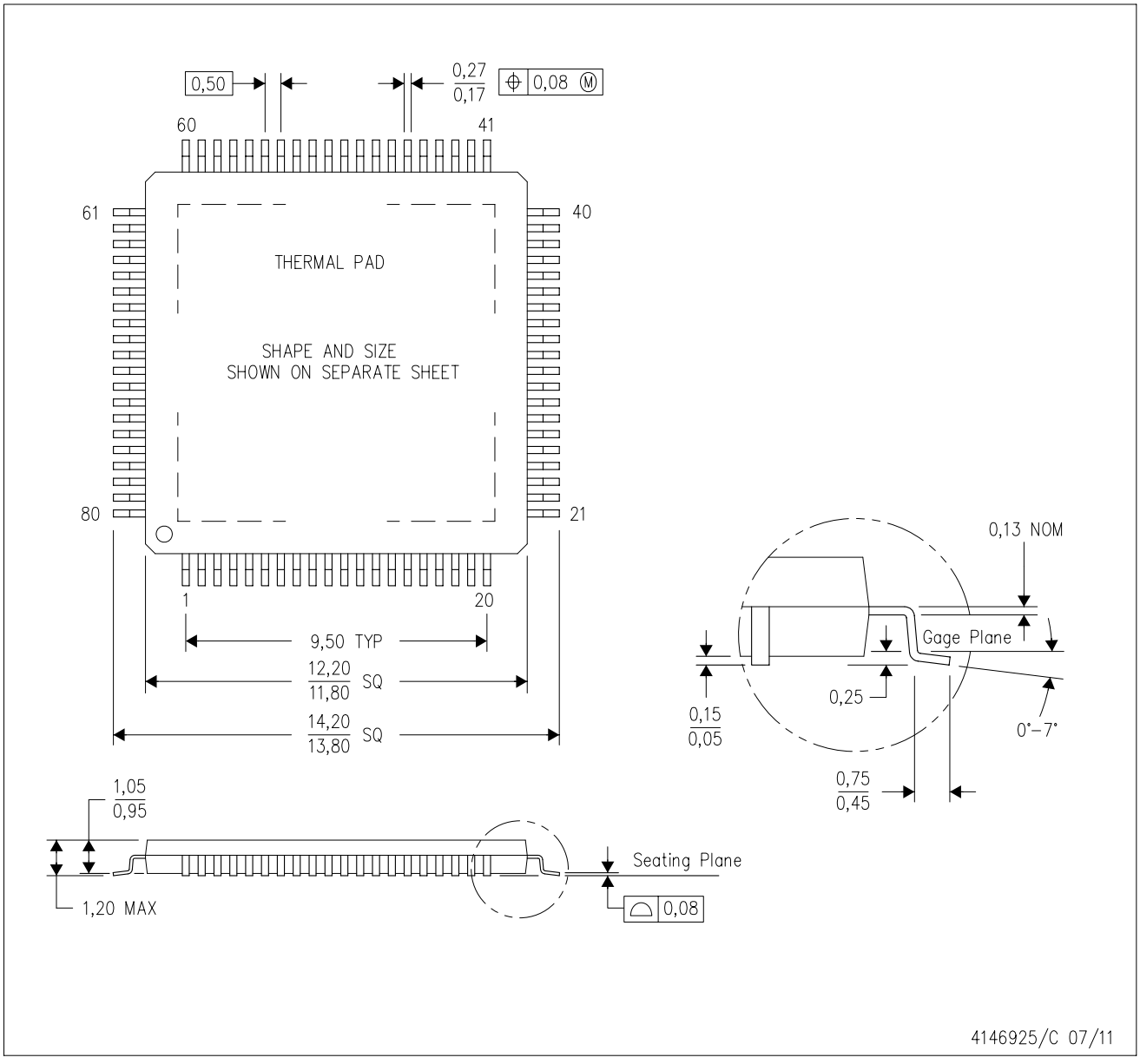
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

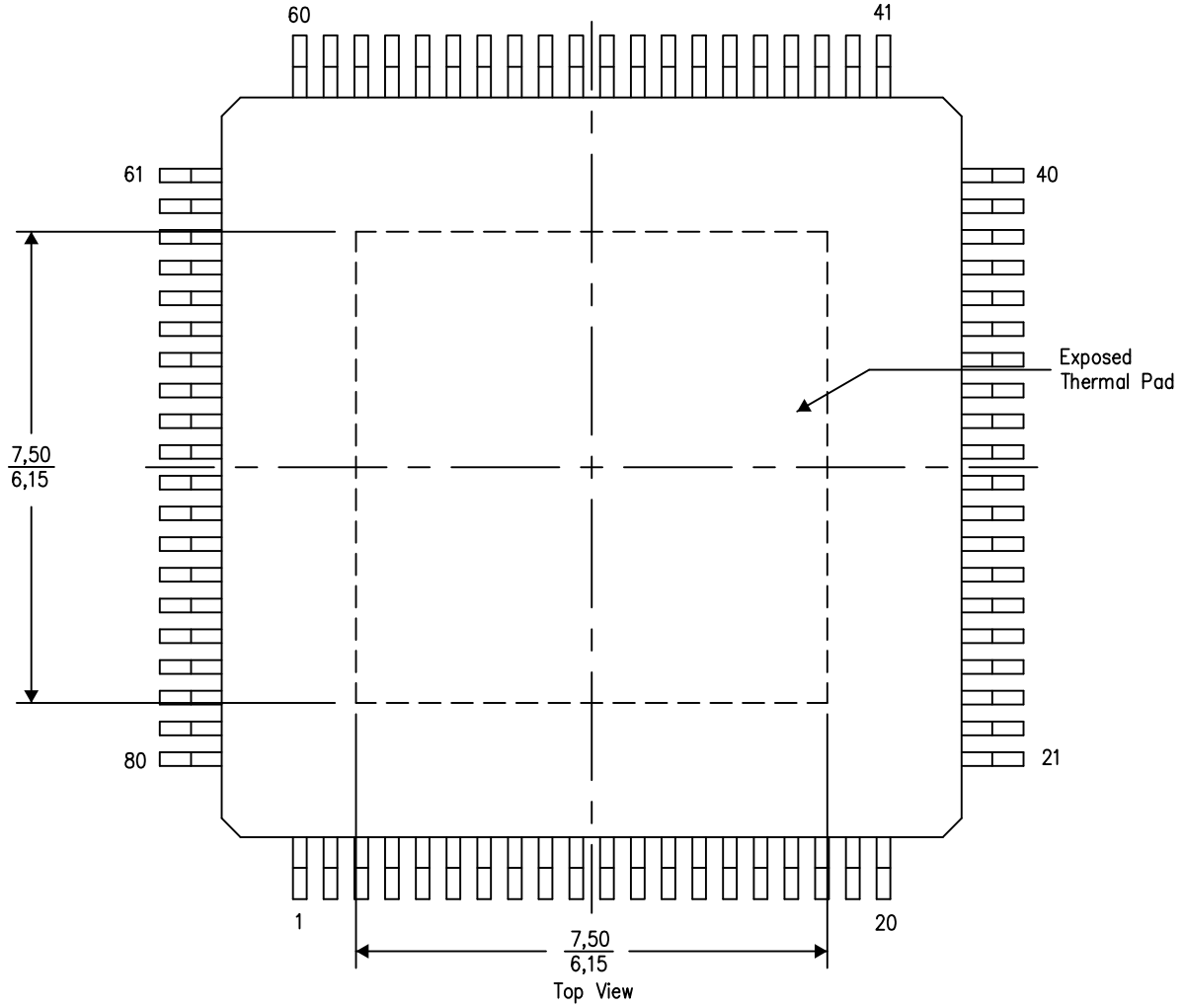
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–2/P 05/14

NOTE: A. All linear dimensions are in millimeters

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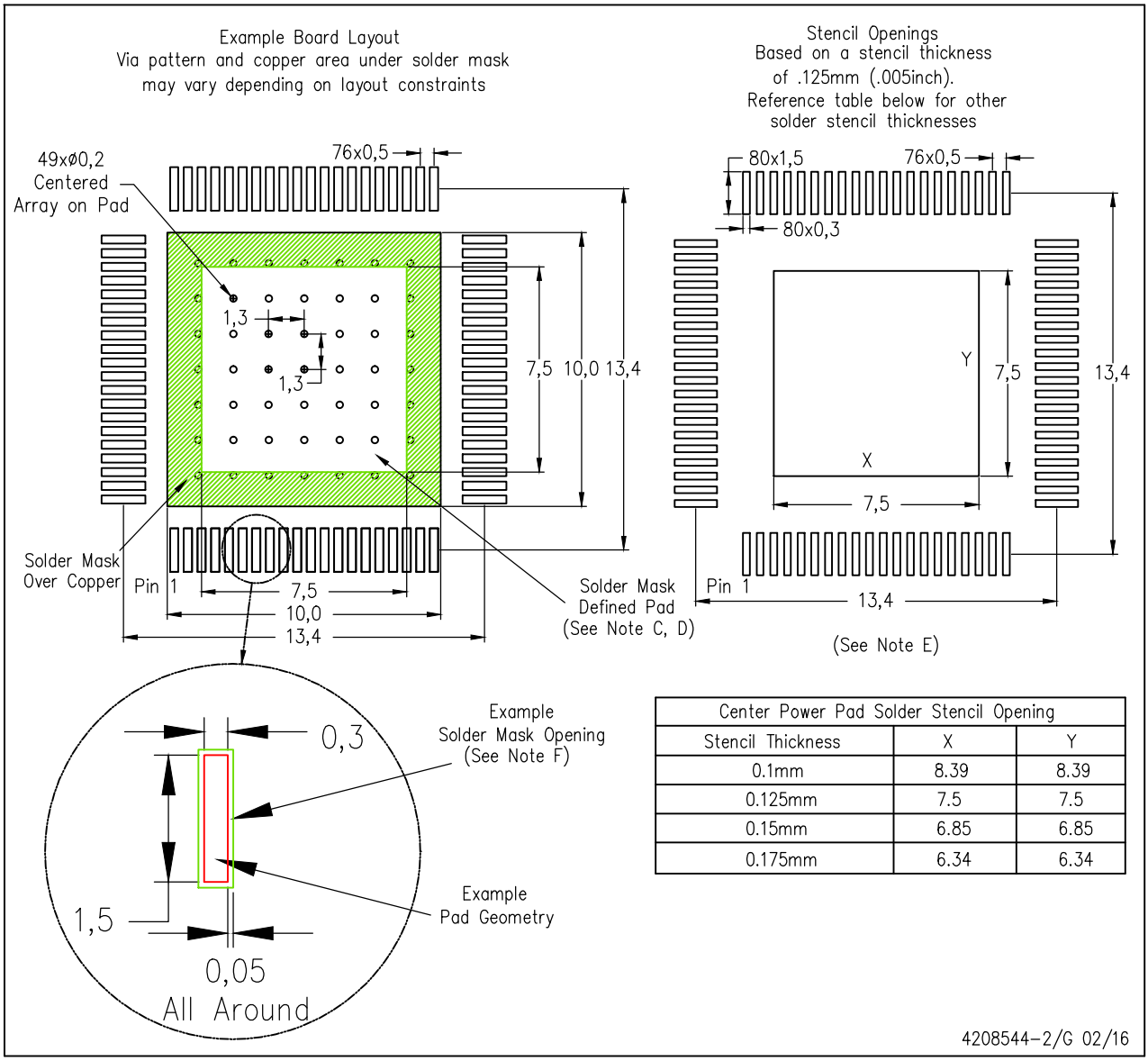
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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