

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 200 MHz
- Low Jitter (cycle-cycle):  $\pm 50$  ps
- Low Static Phase Offset:  $\pm 50$  ps
- Low Jitter (Period):  $\pm 35$  ps
- Distributes One Differential Clock Input to 10 Differential Outputs
- Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low
- Operates From Dual 2.5-V Supplies
- Available in a 48-Pin TSSOP Package or 56-Ball MicroStar Junior™ BGA Package
- Consumes  $< 100\text{-}\mu\text{A}$  Quiescent Current
- External Feedback Pins (FBIN, FBIN) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds the Latest DDR JEDEC Spec JESD82–1

### Description

The CDCV857B is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to 10 differential pairs of clock outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and one differential pair of feedback clock outputs (FBOUT,  $\overline{\text{FBOUT}}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), and the analog power input (AV<sub>DD</sub>). When  $\overline{\text{PWRDWN}}$  is high, the outputs switch in phase and frequency with CLK. When  $\overline{\text{PWRDWN}}$  is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a  $>20\text{-MHz}$  input signal, this detection circuit turns the PLL on and enables the outputs.

When AV<sub>DD</sub> is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857B is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857B is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857B is characterized for both commercial and industrial temperature ranges.

#### AVAILABLE OPTIONS

T <sub>A</sub>	TSSOP (DGG)	MicroStar Junior™ BGA (GQL)
0°C to 85°C	CDCV857BDGG	CDCV857BGQL
–40°C to 85°C	CDCV857BIDGG	—

#### FUNCTION TABLE (Select Functions)

INPUTS				OUTPUTS				PLL
AV <sub>DD</sub>	PWRDWN	CLK	$\overline{\text{CLK}}$	Y[0:9]	$\overline{\text{Y}}[0:9]$	FBOUT	$\overline{\text{FBOUT}}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	$<20$ MHz	$<20$ MHz	Z	Z	Z	Z	Off



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



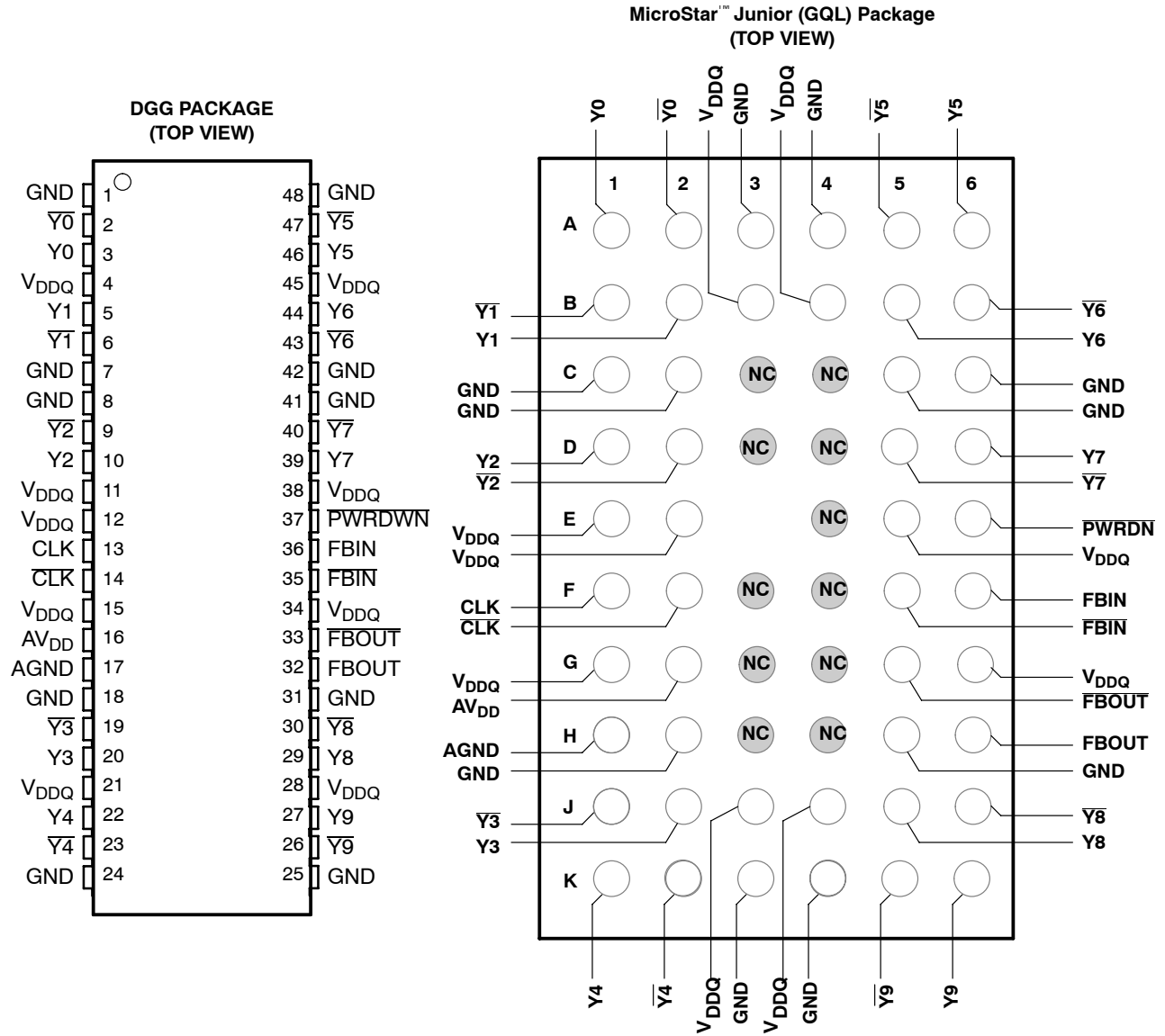
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# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

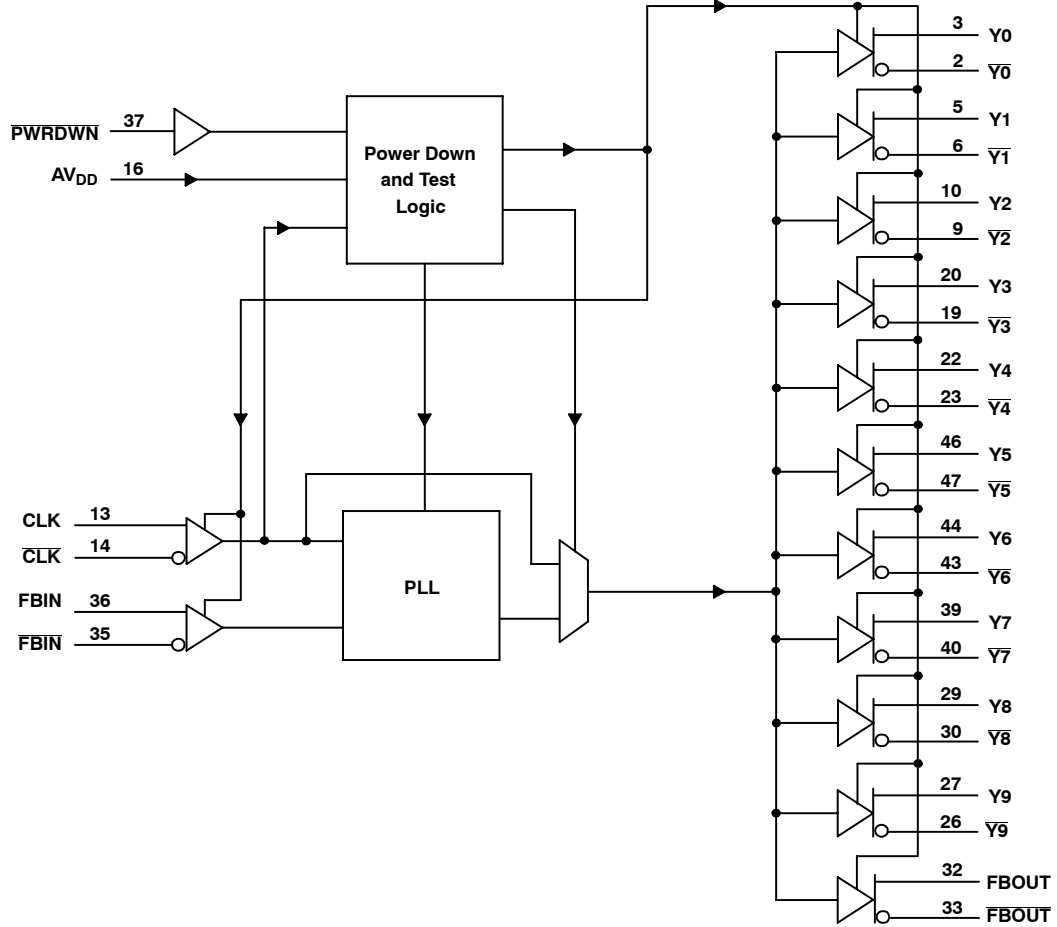
SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010



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SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

## functional block diagram



# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

### Terminal Functions

TERMINAL				DESCRIPTION
NAME	DGG	GQL		
AGND	17	H1		Ground for 2.5-V analog supply
AV <sub>DD</sub>	16	G2		2.5-V Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	F1, F2	I	Differential clock input
$\overline{\text{FBIN}}$ , FBIN	35, 36	F5, F6	I	Feedback differential clock input
FBO <sub>UT</sub> , $\overline{\text{FBOU}}\overline{\text{T}}$	32, 33	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{\text{PWRDWN}}$	37	E6	I	Output enable for Y and $\overline{\text{Y}}$
V <sub>DDQ</sub>	4, 11, 12, 15, 21, 28, 34, 38, 45	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	A1, B2, D1, J2, K1, A6, B5, D6, J5, K6	O	Buffered output copies of input clock, CLK
$\overline{\text{Y}}[0:9]$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	A2, B1, D2, J1, K2, A5, B6, D5, J6, K5	O	Buffered output copies of input clock, $\overline{\text{CLK}}$

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DDQ</sub> , AV <sub>DD</sub>	0.5 V to 3.6 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )	±50 mA
Continuous current to GND or V <sub>DDQ</sub>	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): GQL package	137.6°C/W
Storage temperature range T <sub>stg</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. This value is limited to 3.6 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51.



# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

### recommended operating conditions (see Note 4)

		MIN	TYP	MAX	UNIT
Supply voltage	$V_{DDQ}$	2.3		2.7	V
	$AV_{DD}$	$V_{DDQ} - 0.12$		2.7	V
Low-level input voltage, $V_{IL}$	CLK, $\overline{CLK}$ , FBIN, $\overline{FBIN}$		$V_{DDQ}/2 - 0.18$		V
	PWRDWN	-0.3		0.7	
High-level input voltage, $V_{IH}$	CLK, $\overline{CLK}$ , FBIN, $\overline{FBIN}$	$V_{DDQ}/2 + 0.18$			V
	PWRDWN	1.7		$V_{DDQ} + 0.3$	
DC input signal voltage (see Note 5)		-0.3		$V_{DDQ} + 0.3$	V
Differential input signal voltage, $V_{ID}$ (see Note 6)	dc   CLK, FBIN	0.36		$V_{DDQ} + 0.6$	V
	ac   CLK, FBIN	0.7		$V_{DDQ} + 0.6$	
Input differential pair cross voltage, $V_{IX}$ (see Note 7)		$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, $I_{OH}$				-12	mA
Low-level output current, $I_{OL}$				12	mA
Input slew rate, SR		1		4	V/ns
Operating free-air temperature, $T_A$	Commercial	0		85	°C
	Industrial	-40		85	

- NOTES:
- The unused inputs must be held high or low to prevent them from floating.
  - The dc input signal voltage specifies the allowable dc execution of the differential input.
  - The differential input signal voltage specifies the differential voltage  $|VTR - VCP|$  required for switching, where VTR is the true input level and VCP is the complementary input level.
  - The differential cross-point voltage is expected to track variations of  $V_{CC}$  and is the voltage at which the differential signals must be crossing.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{IK}$	Input voltage	All inputs $V_{DDQ} = 2.3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	High-level output voltage	$V_{DDQ} = \text{min to max}$ , $I_{OH} = -1\text{ mA}$	$V_{DDQ} - 0.1$			V
		$V_{DDQ} = 2.3\text{ V}$ , $I_{OH} = -12\text{ mA}$	1.7			
$V_{OL}$	Low-level output voltage	$V_{DDQ} = \text{min to max}$ , $I_{OL} = 1\text{ mA}$			0.1	V
		$V_{DDQ} = 2.3\text{ V}$ , $I_{OL} = 12\text{ mA}$			0.6	
$V_{OD}$	Output voltage swing <sup>‡</sup>	Differential outputs are terminated with $120\ \Omega / CL = 14\text{ pF}$ (See Figure 3)	1.1		$V_{DDQ} - 0.4$	V
$V_{OX}$	Output differential cross-voltage <sup>§</sup>		$V_{DDQ}/2 - 0.15$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.15$	
$I_I$	Input current	$V_{DDQ} = 2.7\text{ V}$ , $V_I = 0\text{ V to } 2.7\text{ V}$			$\pm 10$	$\mu\text{A}$
$I_{OZ}$	High-impedance state output current	$V_{DDQ} = 2.7\text{ V}$ , $V_O = V_{DDQ}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{DDPD}$	Power-down current on $V_{DDQ} + AV_{DD}$	CLK and $\overline{CLK} = 0\text{ MHz}$ ; PWRDWN = Low; $\Sigma$ of $I_{DD}$ and $AI_{DD}$		20	100	$\mu\text{A}$
$AI_{DD}$	Supply current on $AV_{DD}$	$f_O = 170\text{ MHz}$		7	10	mA
		$f_O = 200\text{ MHz}$		9	12	
$C_I$	Input capacitance	$V_{DDQ} = 2.5\text{ V}$ , $V_I = V_{DDQ}$ or GND	2	2.5	3.5	pF

<sup>†</sup> All typical values are at a respective nominal  $V_{DDQ}$ .

<sup>‡</sup> The differential output signal voltage specifies the differential voltage  $|VTR - VCP|$ , where VTR is the true output level and VCP is the complementary output level.

<sup>§</sup> The differential cross-point voltage is expected to track variations of  $V_{DDQ}$  and is the voltage at which the differential signals must be crossing. The frequency range is 100 MHz to 200 MHz.



# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Without load	f <sub>O</sub> = 170 MHz	100	110	mA
			f <sub>O</sub> = 200 MHz	105	120	
		Differential outputs terminated with 120 Ω/CL = 0 pF	f <sub>O</sub> = 170 MHz	200	240	
			f <sub>O</sub> = 200 MHz	210	250	
		Differential outputs terminated with 120 Ω/CL = 14 pF	f <sub>O</sub> = 170 MHz	260	300	
			f <sub>O</sub> = 200 MHz	280	320	
ΔC	Part-to-part input capacitance variation	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			1	pF
C <sub>I(Δ)</sub>	Input capacitance difference between CLK and CLKB, FBIN, and FBINB	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			0.25	pF
C <sub>O</sub>	Output capacitance	V <sub>DDQ</sub> = 2.5 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND	2.5	3	3.5	pF

<sup>†</sup> All typical values are at a respective nominal V<sub>DDQ</sub>.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	200	MHz
	Application clock frequency			
Input clock duty cycle		40%	60%	
Stabilization time <sup>†</sup> (PLL mode)			10	μs
Stabilization time <sup>‡</sup> (Bypass mode)			30	ns

<sup>†</sup> The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V<sub>DD</sub> must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

<sup>‡</sup> A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

### switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> <sup>§</sup>	Low to high level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>PHL</sub> <sup>§</sup>	High-to low level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>jit(per)</sub> <sup>¶</sup>	Jitter (period), See Figure 7	66 MHz	-60		60	ps
		100/133/167/200 MHz	-35		35	ps
t <sub>jit(cc)</sub> <sup>¶</sup>	Jitter (cycle-to-cycle), See Figure 4	66 MHz	-75		75	ps
		100/133/167/200 MHz	-50		50	ps
t <sub>jit(hper)</sub> <sup>¶</sup>	Half-period jitter, See Figure 8	66 MHz	-100		100	ps
		100/133/167/200 MHz	-75		75	ps
t <sub>slr(o)</sub>	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF	1		2	V/ns
t <sub>(∅)</sub>	Static phase offset, See Figure 5	66 MHz	-100		100	ps
		100/133/167/200 MHz	-50		50	ps
t <sub>sk(o)</sub>	Output skew, See Figure 6	Load: 120 Ω/14 pF		70	100	ps
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF	600		900	ps

<sup>§</sup> Refers to the transition of the noninverting output.

<sup>¶</sup> This parameter is assured by design but can not be 100% production tested.



PARAMETER MEASUREMENT INFORMATION

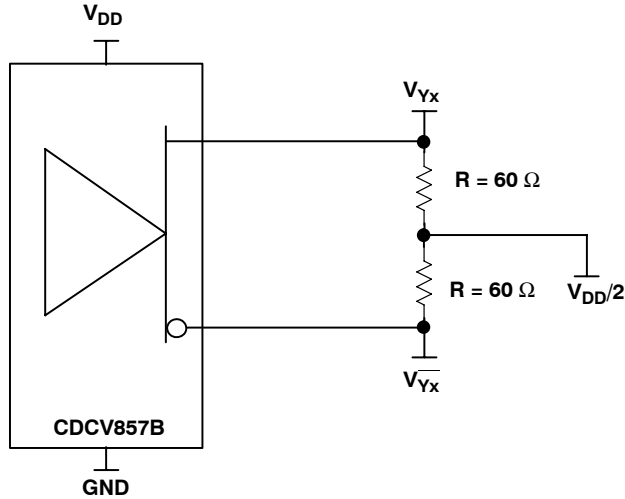


Figure 1. IBIS Model Output Load

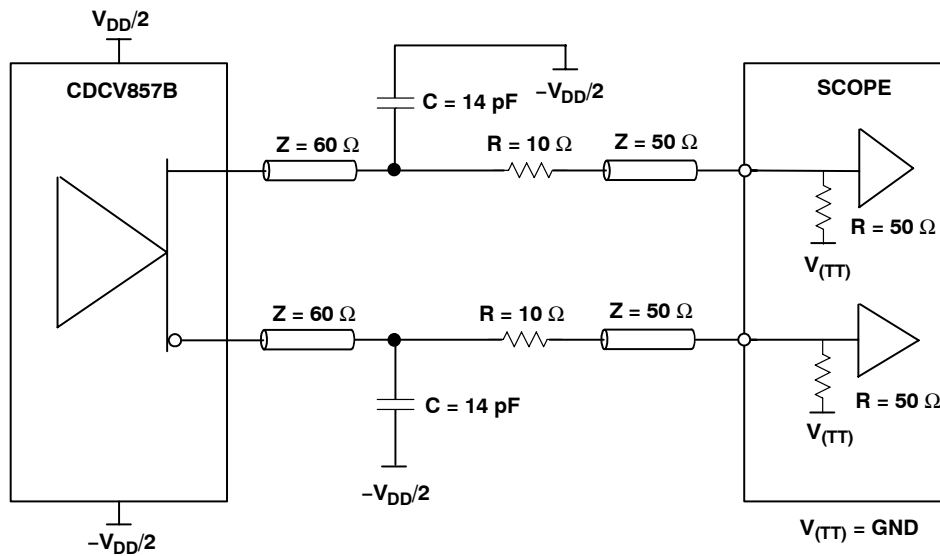


Figure 2. Output Load Test Circuit

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

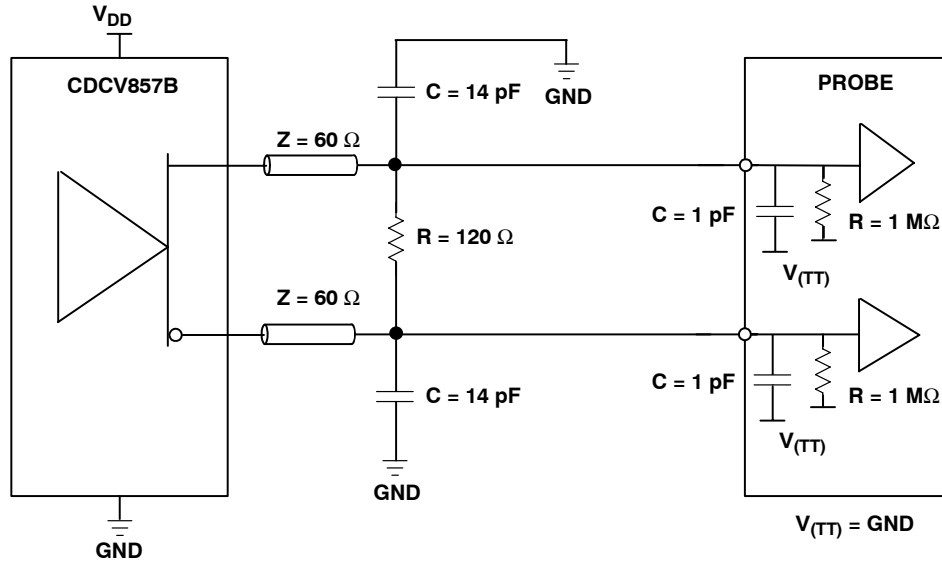


Figure 3. Output Load Test Circuit for Crossing Point

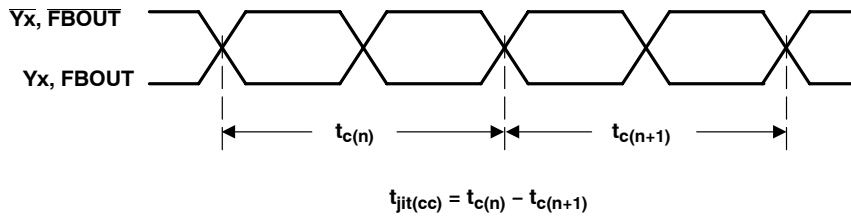


Figure 4. Cycle-to-Cycle Jitter



PARAMETER MEASUREMENT INFORMATION

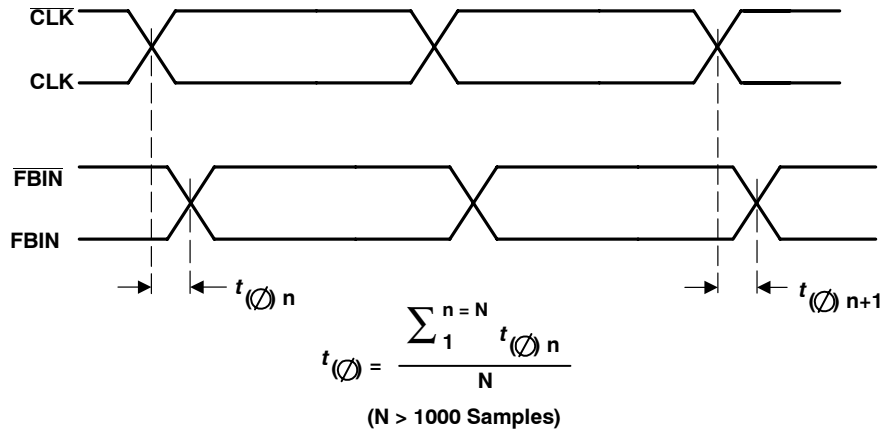


Figure 5. Phase Offset

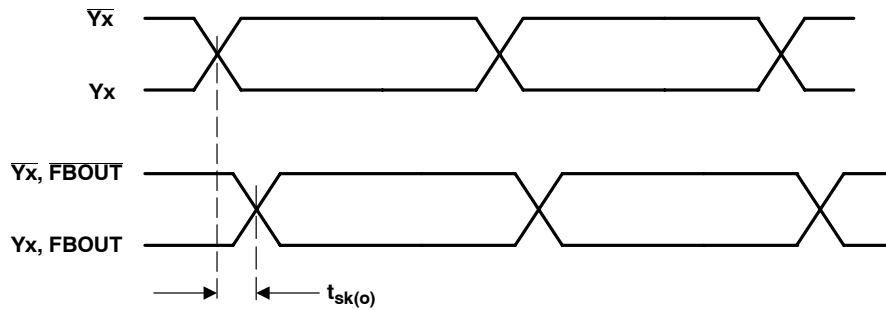


Figure 6. Output Skew

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689A – FEBRUARY 2003 – REVISED NOVEMBER 2010

### PARAMETER MEASUREMENT INFORMATION

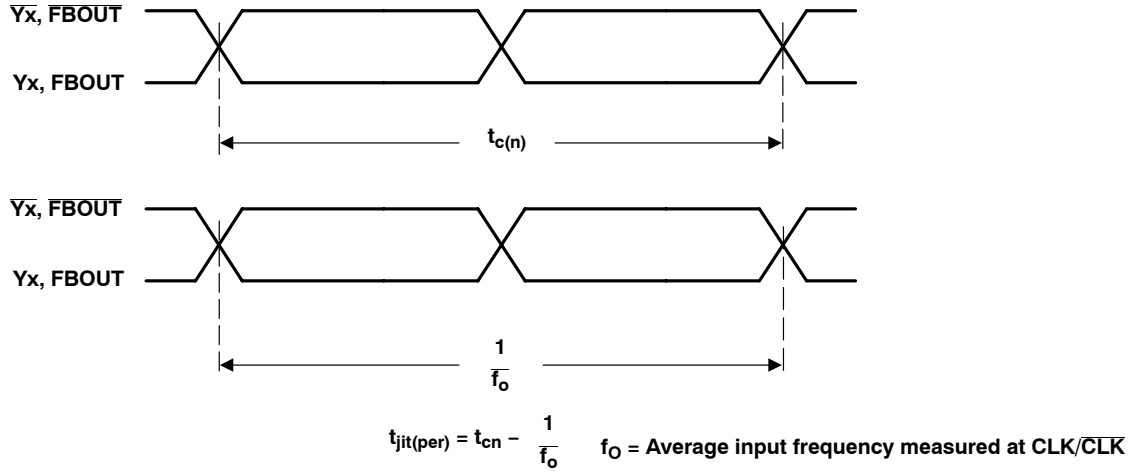


Figure 7. Period Jitter

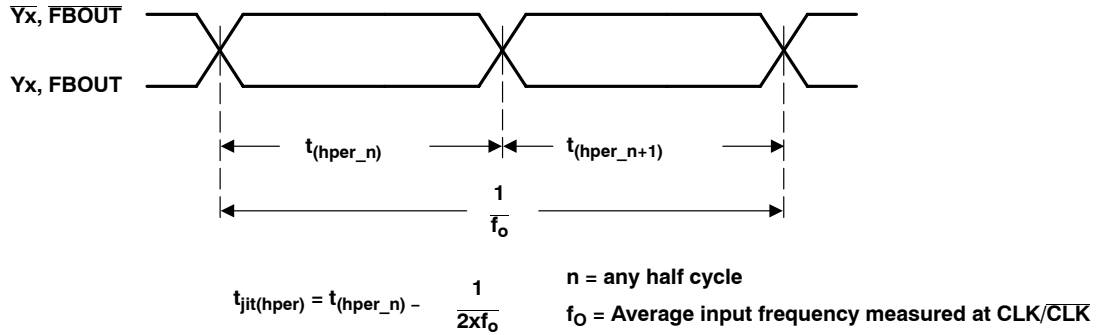


Figure 8. Half-Period Jitter

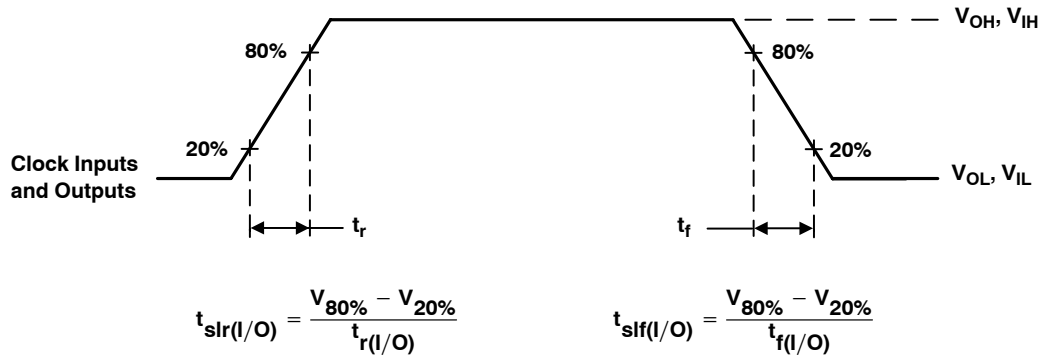


Figure 9. Input and Output Slew Rates

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCV857BDGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDCV857B	<a href="#">Samples</a>
CDCV857BDGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDCV857B	<a href="#">Samples</a>
CDCV857BDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDCV857B	<a href="#">Samples</a>
CDCV857BDGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDCV857B	<a href="#">Samples</a>
CDCV857BIDGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCV857B-I	<a href="#">Samples</a>
CDCV857BIDGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCV857B-I	<a href="#">Samples</a>
CDCV857BIDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCV857B-I	<a href="#">Samples</a>
CDCV857BIDGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCV857B-I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCV857BIDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



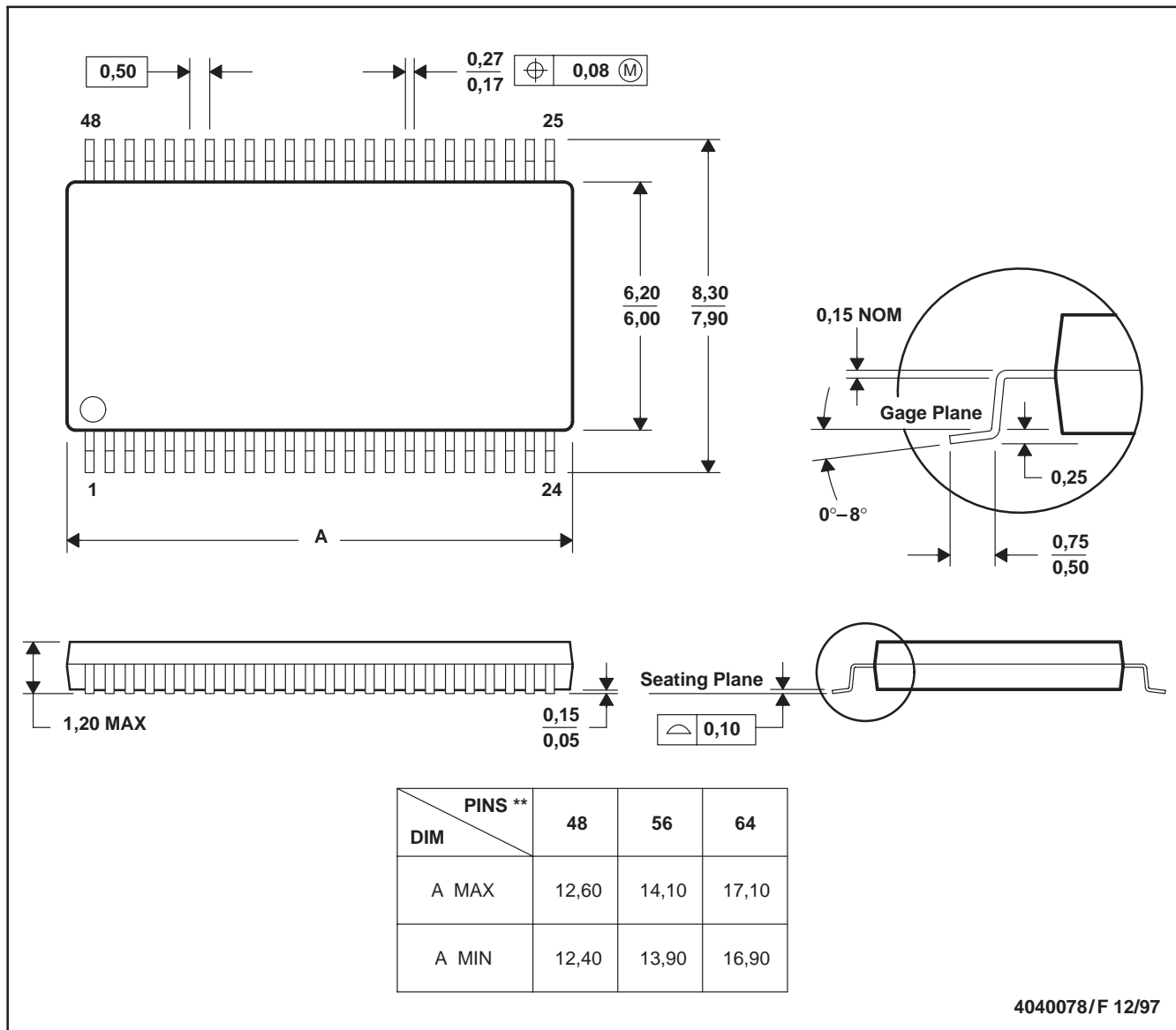
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCV857BIDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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