Octal, 12-Bit, Low-Power, High-Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

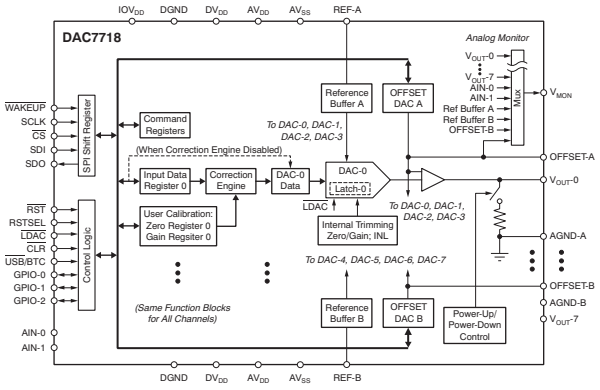
Check for Samples: DAC7718

FEATURES

- **Bipolar Output: ±2V to ±16.5V**
- **Unipolar Output: 0V to +33V**
- **12-Bit Resolution**
- **Low Power: 14.4mW/Ch (Bipolar Supply)**
- **Relative Accuracy: 1 LSB Max**
- **Low Zero/Full-Scale Error: ±1 LSB Max**
- **Flexible System Calibration**
- **Low Glitch: 4nV-s**
- **Settling Time: 15μs**
- **Channel Monitor Output**
- **Programmable Gain: x4/x6**
- **Programmable Offset**
- **SPI™: Up to 50MHz, 1.8V/3V/5V Logic**
- **Schmitt Trigger Inputs**
- **Daisy-Chain with Sleep Mode Enhancement**
- **Packages: QFN-48 (7x7mm), TQFP-64 (10x10mm)**

APPLICATIONS

- **Automatic Test Equipment**
- **PLC and Industrial Process Control**
- **Communications**



DESCRIPTION

The DAC7718 is a low-power, octal, 12-bit digital-to-analog converter (DAC). With a 5V reference, the output can either be a bipolar ±15V voltage when operating from dual ±15.5V (or higher) power supplies, or a unipolar 0V to +30V voltage when operating from a +30.5V (or higher) power supply. With a 5.5V reference, the output can either be a bipolar ±16.5V voltage when operating from dual ±17V (or higher) power supplies, or a unipolar 0V to +33V voltage when operating from a +33.5V (or higher) power supply. This DAC provides low-power operation, good linearity, and low glitch over the specified temperature range of –40°C to +105°C. This device is trimmed in manufacturing and has very low zero-code and gain error. In addition, system level calibration can be performed over the entire signal chain. The output range can be offset by using the DAC offset register.

The DAC7718 features a standard, high-speed serial peripheral interface (SPI) that operates at up to 50MHz and is 1.8V, 3V, and 5V logic compatible, to communicate with a DSP or microprocessor. The input data of the device are double-buffered. An asynchronous load input (LDAC) transfers data from the DAC data register to the DAC latch. The asynchronous CLR input sets the output of all eight DACs to AGND. The V_{MON} pin is a monitor output that connects to the individual analog outputs, the offset DAC, the reference buffer outputs, and two external inputs through a multiplexer (mux).

The DAC7718 is pin-to-pin and function-compatible with the DAC8718 (16-bit) and the DAC8218 (14-bit).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL LINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7718	±1	±1	QFN-48	RGZ	–40°C to +105°C	DAC7718
	±1	±1	TQFP-64	PAG	–40°C to +105°C	DAC7718

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			DAC7718	UNIT
AV_{DD} to AV_{SS}			–0.3 to 38	V
AV_{DD} to AGND			–0.3 to 38	V
AV_{SS} to AGND, DGND			–19 to 0.3	V
DV_{DD} to DGND			–0.3 to 6	V
IOV_{DD} to DGND			–0.3 to min of (6 or DV_{DD} + 0.3)	V
AGND-x to DGND			–0.3 to 0.3	V
Digital input voltage to DGND			–0.3 to IOV_{DD} + 0.3	V
SDO to DGND			–0.3 to IOV_{DD} + 0.3	V
V_{OUT}-x, V_{MON}, AIN-x to AV_{SS}			–0.3 to AV_{DD} + 0.3	V
REF-A, REF-B to AGND			–0.3 to DV_{DD}	V
GPIO-n to DGND			–0.3 to IOV_{DD} + 0.3	V
GPIO-n input current			5	mA
Maximum current from V_{MON}			3	mA
Operating temperature range			–40 to +105	°C
Storage temperature range			–65 to +150	°C
Maximum junction temperature (T_J max)			+150	°C
ESD ratings	Human body model (HBM)		2.5	kV
	Charged device model (CDM)		1000	V
	Machine model (MM)		200	V
Thermal impedance	Junction-to-ambient, θ_{JA}	TQFP	55	°C/W
		QFN	27.5	°C/W
	Junction-to-case, θ_{JC}	TQFP	21	°C/W
		QFN	10.8	°C/W
Power dissipation			(T_J max – T_A) / θ_{JA}	W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Dual-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and Offset DAC A and Offset DAC B are at default values(1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE(2)					
Resolution		12			Bits
Linearity error	Measured by line passing through codes 000h and FFFh			±1	LSB
Differential linearity error	Measured by line passing through codes 000h and FFFh			±1	LSB
Bipolar zero error	T_A = +25°C, gain = 4 or 6, code = 800h			±1	LSB
Bipolar zero error TC	Gain = 4 or 6, code = 800h		±0.5	±2	ppm FSR/°C
Zero-code error	T_A = +25°C, gain = 6, code = 000h			±1	LSB
	T_A = +25°C, gain = 4, code = 000h			±1	LSB
Zero-code error TC	Gain = 4 or 6, code = 000h		±0.5	±3	ppm FSR/°C
Gain error	T_A = +25°C, gain = 6			±1	LSB
	T_A = +25°C, gain = 4			±1	LSB
Gain error TC	Gain = 4 or 6		±1	±3	ppm FSR/°C
Full-scale error	T_A = +25°C, gain = 4 or 6, code = FFFh			±1	LSB
Full-scale error TC	Gain = 4 or 6, code = FFFh		±0.5	±3	ppm FSR/°C
DC crosstalk(3)	Measured channel at code = 800h, full-scale change on any other channel		0.05		LSB

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±1 LSB from the nominal number listed in Table 7. The Offset DAC pins are not intended to drive an external load, and must not be connected during dual-supply operation.
(2) Gain = 4 and TC specified by design and characterization.
(3) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple AV_{DD} and AV_{SS} terminals are provided to minimize dc crosstalk.

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and Offset DAC A and Offset DAC B are at default values (1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718 MIN	DAC7718 TYP	DAC7718 MAX	UNIT
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)(4)					
Voltage output(5)	V_{REF} = +5V	–15		+15	V
	V_{REF} = +1.5V	–4.5		+4.5	V
Output impedance	Code = 800h			0.5	Ω
Short-circuit current(6)			±8		mA
Load current	See Figure 37		±3		mA
Output drift vs time	T_A = +25°C, device operating for 500 hours, full-scale output		3.4		ppm of FSR
	T_A = +25°C, device operating for 1000 hours, full-scale output		4.3		ppm of FSR
Capacitive load stability				500	pF
Settling time	To 0.03% of FSR, C_L = 200pF, R_L= 10kΩ, code from 000h to FFFh and FFFh to 000h		10		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 000h to FFFh and FFFh to 000h		15		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 7F0h to 810h and 810h to 7F0h		6		µs
Slew rate (7)			6		V/µs
Power-on delay(8)	From IOV_{DD} ≥ +1.8V and DV_{DD} ≥ +2.7V to $\overline{CS}$ low		200		µs
Power-down recovery time			60		µs
Digital-to-analog glitch(9)	Code from 7FFh to 800h and 800h to 7FFh		4		nV-s
Glitch impulse peak amplitude	Code from 7FFh to 800h and 800h to 7FFh		5		mV
Channel-to-channel isolation(10)	V_{REF} = $4V_{PP}$, f = 1kHz		88		dB
DAC-to-DAC crosstalk(11)	DACs in the same group		7.5		nV-s
	DACs among different groups		1		nV-s
Digital crosstalk(12)			1		nV-s
Digital feedthrough(13)			1		nV-s
Output noise	T_A = +25°C at 10kHz, gain = 6		200		nV/√Hz
	T_A = +25°C at 10kHz, gain = 4		130		nV/√Hz
	0.1Hz to 10Hz, gain = 6		20		μV_{PP}
Power-supply rejection(14)	AV_{DD} = ±15.5V to ±16.5V		0.05		LSB

(4) Specified by design.
(5) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to (6 × V_{REF} – 5 × OUTPUT_OFFSET_DAC) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5V), and the minimum value must not be less than (AV_{SS} + 0.5V). All specifications are for a ±16.5V power supply and a ±15V output, unless otherwise noted.
(6) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(7) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(8) *Power-on delay* is defined as the time from when the supply voltages reach the specified conditions to when $\overline{CS}$ goes low, for valid digital communication.
(9) *Digital-to-analog glitch* is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFh and 800h in straight binary format.
(10) *Channel-to-channel isolation* refers to the ratio of the signal amplitude at the output of one DAC channel to the amplitude of the sinusoidal signal on the reference input of another DAC channel. It is expressed in dB and measured at midscale.
(11) *DAC-to-DAC crosstalk* is the glitch impulse that appears at the output of one DAC as a result of both the full-scale digital code and subsequent analog output change at another DAC. It is measured with LDAC tied low and expressed in nV-s.
(12) *Digital crosstalk* is the glitch impulse transferred to the output of one converter as a result of a full-scale code change in the DAC input register of another converter. It is measured when the DAC output is not updated, and is expressed in nV-s.
(13) *Digital feedthrough* is the glitch impulse injected to the output of a DAC as a result of a digital code change in the DAC input register of the same DAC. It is measured with the full-scale digital code change without updating the DAC output, and is expressed in nV-s.
(14) The output must not be greater than (AV_{DD} – 0.5V) and not less than (AV_{SS} + 0.5V).

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and Offset DAC A and Offset DAC B are at default values (1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
OFFSET DAC OUTPUT(15) (16)					
Voltage output	V_{REF} = +5V	0		5	V
Full-scale error	T_A = +25°C		±0.25		LSB
Zero-code error	T_A = +25°C		±0.25		LSB
Linearity error			±0.5		LSB
Differential linearity error				±1	LSB
ANALOG MONITOR PIN (V_{MON})					
Output impedance(17)	T_A = +25°C		2		kΩ
Three-state leakage current			100		nA
AUXILIARY ANALOG INPUT					
Input range		AV_{SS}		AV_{DD}	V
Input impedance (AIN-x to V_{MON})	T_A = +25°C		2		kΩ
Input capacitance(15)			4		pF
Input leakage current			30		nA
REFERENCE INPUT					
Reference input voltage range(18)		1.0		5.5	V
Reference input dc impedance			10		MΩ
Reference input capacitance(15)			10		pF
DIGITAL INPUT(15)					
High-level input voltage, V_{IH}	IOV_{DD} = +4.5V to +5.5V	3.8		0.3 + IOV_{DD}	V
	IOV_{DD} = +2.7V to +3.3V	2.3		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.7V to 2.0V	1.5		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +4.5V to +5.5V	–0.3		0.8	V
	IOV_{DD} = +2.7V to +3.3V	–0.3		0.6	V
	IOV_{DD} = +1.7V to 2.0V	–0.3		0.3	V
Input current	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, $\overline{CS}$, and SDI			±1	µA
	$\overline{USB}$/BTC, RSTSEL, and GPIO-n			±5	µA
Input capacitance	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, $\overline{CS}$, and SDI		5		pF
	$\overline{USB}$/BTC and RSTSEL		12		pF
	GPIO-n		14		pF
DIGITAL OUTPUT(15)					
High-level output voltage, V_{OH} (SDO)	IOV_{DD} = +2.7V to +5.5V, sourcing 1mA	IOV_{DD} – 0.4		IOV_{DD}	V
	IOV_{DD} = +1.8V, sourcing 200µA	1.6		IOV_{DD}	V
Low-level output voltage, V_{OL} (SDO)	IOV_{DD} = +2.7V to +5.5V, sinking 1mA	0		0.4	V
	IOV_{DD} = +1.8V, sinking 200µA	0		0.2	V
GPIO-n output voltage low, V_{OL}	1mA sink from IOV_{DD}		0.15		V
GPIO-n output voltage high, V_{OH}	10kΩ pull-up resistor to IOV_{DD}	0.99 × IOV_{DD}			V
High-impedance leakage current	SDO and GPIO-n		±5		µA
High-impedance output capacitance	SDO		5		pF
	GPIO-n		14		pF

(15) Specified by design.
(16) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±1 LSB from the nominal number listed in Table 7. The Offset DAC pins are not intended to drive an external load, and must not be connected during dual-supply operation.
(17) 8kΩ when V_{MON} is connected to Reference Buffer A or B, and 4kΩ when V_{MON} is connected to Offset DAC-A or -B.
(18) Reference input voltage ≤ DV_{DD}.

ELECTRICAL CHARACTERISTICS: Dual-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +16.5V, AV_{SS} = –16.5V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and Offset DAC A and Offset DAC B are at default values (1), unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
AV_{DD}		+4.5		+18	V
AV_{SS}		–18		–4.5	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD} (19)		+1.8		+5.5	V
AI_{DD}	Normal operation, midscale code, output unloaded		4.3	6	mA
	Power down, output unloaded		35		µA
AI_{SS}	Normal operation, midscale code, output unloaded	–4	–2.7		mA
	Power down, output unloaded		35		µA
DI_{DD}	Normal operation		78		µA
	Power down		36		µA
IOI_{DD}	Normal operation, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
	Power down, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
Power dissipation	Normal operation, ±16.5V supplies, midscale code		115	165	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(19) $IOV_{DD} \le DV_{DD}$.

ELECTRICAL CHARACTERISTICS: Single-Supply

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Linearity error	Measured by line passing through codes 010h and FFFh			±1	LSB
Differential linearity error	Measured by line passing through codes 010h and FFFh			±1	LSB
Unipolar zero error	T_A = +25°C, gain = 4 or 6, code = 010h			±1	LSB
Unipolar zero error TC	Gain = 4 or 6, code = 010h		±0.5	±3	ppm FSR/°C
Gain error	T_A = +25°C, gain = 6			±1	LSB
	T_A = +25°C, gain = 4			±1	LSB
Gain error TC	Gain = 4 or 6		±1	±3	ppm FSR/°C
Full-scale error	T_A = +25°C, gain = 4 or 6, code = FFFh			±1	LSB
Full-scale error TC	Gain = 4 or 6, code = FFFh		±0.5	±3	ppm FSR/°C
DC crosstalk(2)	Measured channel at code = 800h, full-scale change on any other channel		0.05		LSB
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-7)(3)					
Voltage output(4)	V_{REF} = +5V	0		+30	V
	V_{REF} = +1.5V	0		+9	V
Output impedance	Code = 800h			0.5	Ω
Short-circuit current(5)			±8		mA
Load current	See Figure 84 and Figure 85		±3		mA
Output drift vs time	T_A = +25°C, device operating for 500 hours, full-scale output		3.4		ppm of FSR
	T_A = +25°C, device operating for 1000 hours, full-scale output		4.3		ppm of FSR
Capacitive load stability				500	pF
Settling time	To 0.03% of FSR, C_L = 200pF, R_L= 10kΩ, code from 010h to FFFh and FFFh to 010h		10		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 010h to FFFh and FFFh to 010h		15		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code from 7F0h to 810h and 810h to 7F0h		6		µs
Slew rate(6)			6		V/µs
Power-on delay(7)	From IOV_{DD} ≥ +1.8V and DV_{DD} ≥ +2.7V to $\overline{CS}$ low		200		µs
Power-down recovery time			90		µs
Digital-to-analog glitch(8)	Code from 7FFh to 800h and 800h to 7FFh		4		nV-s
Glitch impulse peak amplitude	Code from 7FFh to 800h and 800h to 7FFh		5		mV
Channel-to-channel isolation(9)	V_{REF} = $4V_{PP}$, f = 1kHz		88		dB

(1) Gain = 4 and TC specified by design and characterization.
(2) The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. DC crosstalk indicates how much dc change in one or more channel outputs may occur when the dc load current changes in one channel (because of an update). With high-impedance loads, the effect is virtually immeasurable. Multiple AV_{DD} and AV_{SS} terminals are provided to minimize dc crosstalk.
(3) Specified by design.
(4) The analog output range of V_{OUT}-0 to V_{OUT}-7 is equal to (6 × V_{REF}) for gain = 6. The maximum value of the analog output must not be greater than (AV_{DD} – 0.5V). All specifications are for a +32V power supply and a 0V to +30V output, unless otherwise noted.
(5) When the output current is greater than the specification, the current is clamped at the specified maximum value.
(6) Slew rate is measured from 10% to 90% of the transition when the output changes from 0 to full-scale.
(7) *Power-on delay* is defined as the time from when the supply voltages reach the specified conditions to when $\overline{CS}$ goes low, for valid digital communication.
(8) *Digital-to-analog glitch* is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 7FFh and 800h in straight binary format.
(9) *Channel-to-channel isolation* refers to the ratio of the signal amplitude at the output of one DAC channel to the amplitude of the sinusoidal signal on the reference input of another DAC channel. It is expressed in dB and measured at midscale.

ELECTRICAL CHARACTERISTICS: Single-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
DAC-to-DAC crosstalk(10)	DACs in the same group		10		nV-s
	DACs among different groups		1		nV-s
Digital crosstalk(11)			1		nV-s
Digital feedthrough(12)			1		nV-s
Output noise	T_A = +25°C at 10kHz, gain = 6		200		nV/√Hz
	T_A = +25°C at 10kHz, gain = 4		130		nV/√Hz
	0.1Hz to 10Hz, gain = 6		20		μV_{PP}
Power-supply rejection(13)	AV_{DD} = +33V to +36V		0.05		LSB
ANALOG MONITOR PIN (V_{MON})					
Output impedance(14)	T_A = +25°C		2		kΩ
Three-state leakage current			100		nA
AUXILIARY ANALOG INPUT					
Input range		AV_{SS}		AV_{DD}	V
Input impedance (AIN-x to V_{MON})	T_A = +25°C		2		kΩ
Input capacitance(15)			4		pF
Input leakage current			30		nA
REFERENCE INPUT					
Reference input voltage range(16)		1.0		5.5	V
Reference input dc impedance			10		MΩ
Reference input capacitance(15)			10		pF
DIGITAL INPUT(15)					
High-level input voltage, V_{IH}	IOV_{DD} = +4.5V to +5.5V	3.8		0.3 + IOV_{DD}	V
	IOV_{DD} = +2.7V to +3.3V	2.3		0.3 + IOV_{DD}	V
	IOV_{DD} = +1.7V to 2.0V	1.5		0.3 + IOV_{DD}	V
Low-level input voltage, V_{IL}	IOV_{DD} = +4.5V to +5.5V	–0.3		0.8	V
	IOV_{DD} = +2.7V to +3.3V	–0.3		0.6	V
	IOV_{DD} = +1.7V to 2.0V	–0.3		0.3	V
Input current	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, $\overline{CS}$, and SDI			±1	µA
	$\overline{USB}$/BTC, RSTSEL, and GPIO-n			±5	µA
Input capacitance	$\overline{CLR}$, $\overline{LDAC}$, $\overline{RST}$, $\overline{CS}$, and SDI		5		pF
	$\overline{USB}$/BTC and RSTSEL		12		pF
	GPIO-n		14		pF

(10) *DAC-to-DAC crosstalk* is the glitch impulse that appears at the output of one DAC as a result of both the full-scale digital code and subsequent analog output change at another DAC. It is measured with LDAC tied low and expressed in nV-s.
(11) *Digital crosstalk* is the glitch impulse transferred to the output of one converter as a result of a full-scale code change in the DAC input register of another converter. It is measured when the DAC output is not updated, and is expressed in nV-s.
(12) *Digital feedthrough* is the glitch impulse injected to the output of a DAC as a result of a digital code change in the DAC input register of the same DAC. It is measured with the full-scale digital code change without updating the DAC output, and is expressed in nV-s.
(13) The analog output must not be greater than (AV_{DD} – 0.5V).
(14) 8kΩ when V_{MON} is connected to Reference Buffer A or B, and 4kΩ when V_{MON} is connected to Offset DAC-A or -B.
(15) Specified by design.
(16) Reference input voltage ≤ DV_{DD}.

ELECTRICAL CHARACTERISTICS: Single-Supply (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +32V, AV_{SS} = 0V, $IOV_{DD} = DV_{DD}$ = +5V, REF-A and REF-B = +5V, gain = 6, AGND-x = DGND = 0V, data format = straight binary, and OFFSET-A = OFFSET-B = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7718			UNIT
		MIN	TYP	MAX	
DIGITAL OUTPUT(17)					
High-level output voltage, V_{OH} (SDO)	IOV_{DD} = +2.7V to +5.5V, sourcing 1mA	IOV_{DD} – 0.4		IOV_{DD}	V
	IOV_{DD} = +1.8V, sourcing 200µA	1.6		IOV_{DD}	V
Low-level output voltage, V_{OL} (SDO)	IOV_{DD} = +2.7V to +5.5V, sinking 1mA	0		0.4	V
	IOV_{DD} = +1.8V, sinking 200µA	0		0.2	V
GPIO-n output voltage low, V_{OL}	1mA sink from IOV_{DD}		0.15		V
GPIO-n output voltage high, V_{OH}	10kΩ pull-up resistor to IOV_{DD}	0.99 × IOV_{DD}			V
High-impedance leakage current	SDO and GPIO-n		±5		µA
High-impedance output capacitance	SDO		5		pF
	GPIO-n		14		pF
POWER SUPPLY					
AV_{DD}		+9		+36	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}(18)		+1.8		+5.5	V
AI_{DD}	Normal operation, midscale code, output unloaded		4.5	7	mA
	Power down, output unloaded		35		µA
DI_{DD}	Normal operation		70		µA
	Power down		36		µA
IOI_{DD}	Normal operation, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
	Power down, $V_{IH} = IOV_{DD}$, V_{IL} = DGND		5		µA
Power dissipation	Normal operation		140	225	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(17) Specified by design.
(18) $IOV_{DD} \le DV_{DD}$.

FUNCTIONAL BLOCK DIAGRAM

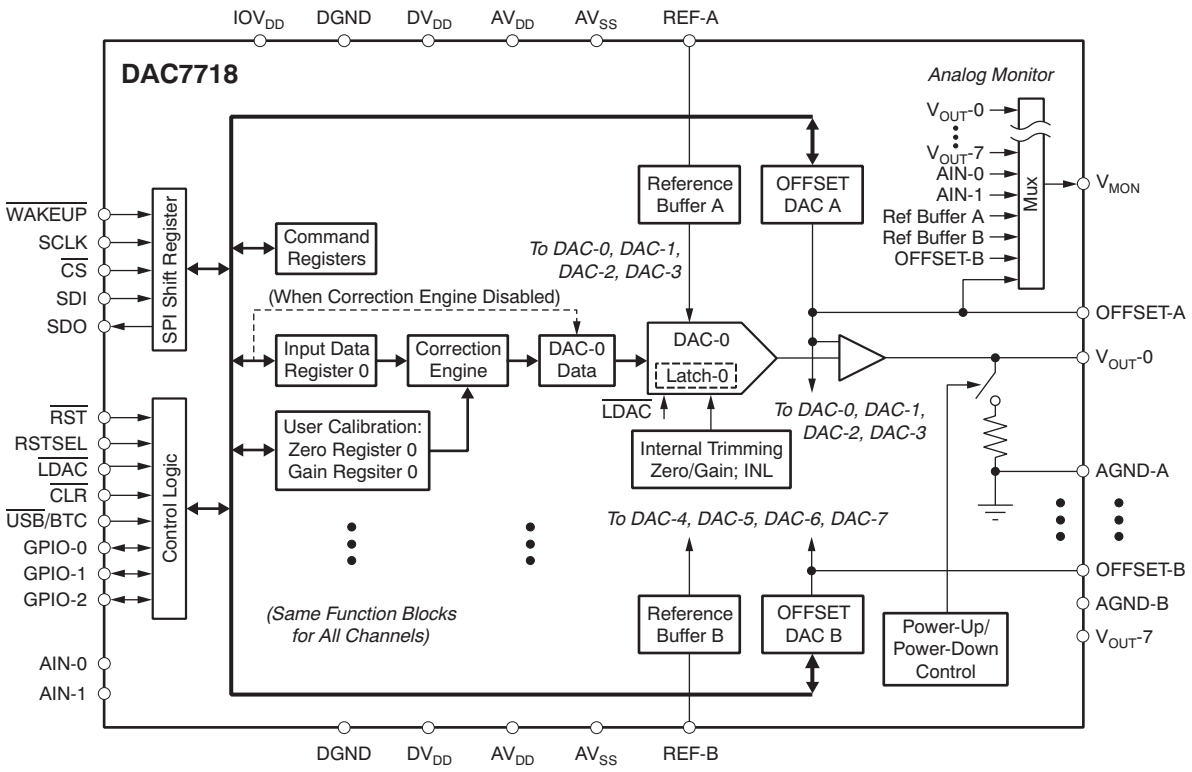
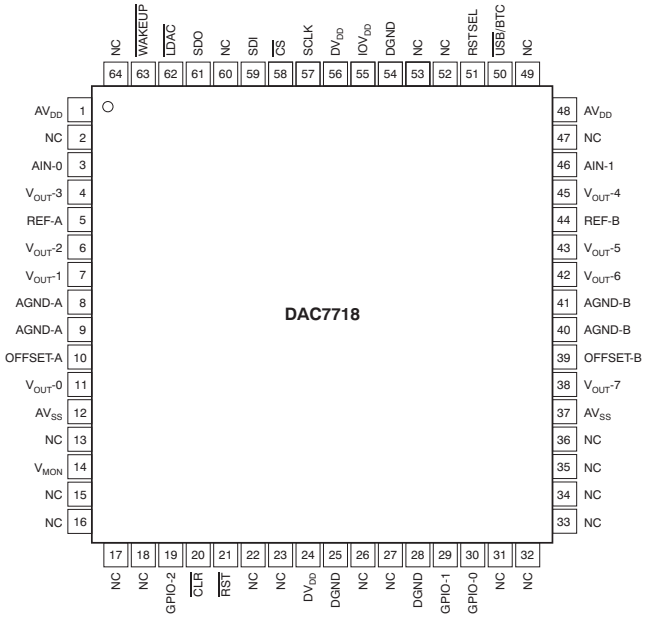


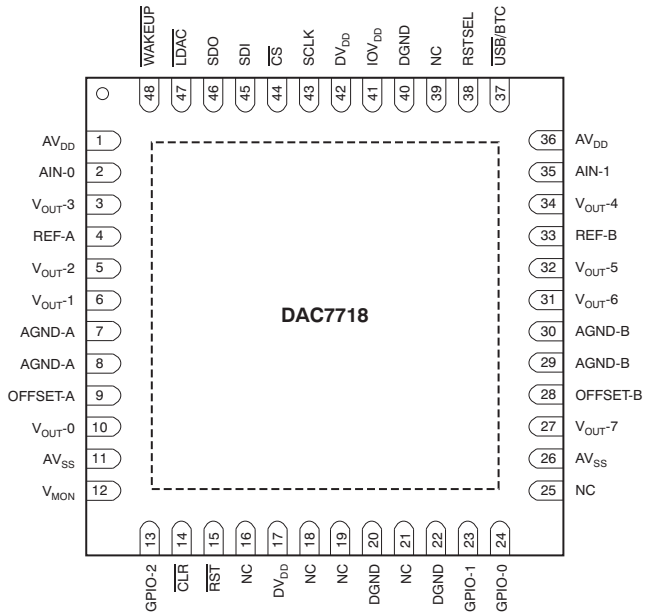
Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

PAG PACKAGE
TQFP-64
(TOP VIEW)



RGZ PACKAGE
QFN-48
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to AV_{SS} or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN DESCRIPTIONS

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-48	TQFP-64		
AV_{DD}	1	1	I	Positive analog power supply
AIN-0	2	3	I	Auxiliary analog input 0, directly routed to the analog mux
V_{OUT}-3	3	4	O	DAC-3 output
REF-A	4	5	I	Group A(1) reference input
V_{OUT}-2	5	6	O	DAC-2 output
V_{OUT}-1	6	7	O	DAC-1 output
AGND-A	7	8	I	Group A analog ground and the ground of REF-A. This pin must be tied to AGND-B and DGND.
AGND-A	8	9	I	Group A analog ground and the ground of REF-A. This pin must be tied to AGND-B and DGND.
OFFSET-A	9	10	O	OFFSET DAC-A analog output. Must be connected to AGND-A during single power-supply operation (AV_{SS} = 0V). This pin is not intended to drive an external load.
V_{OUT}-0	10	11	O	DAC-0 output
AV_{SS}	11	12	I	Negative analog power supply
V_{MON}	12	14	O	Analog monitor output. This pin is either in Hi-Z status, connected to one of the eight DAC outputs, reference buffer outputs, offset DAC outputs, or one of the auxiliary analog inputs, depending on the content of the Monitor Register. See the Monitor Register, Table 12, for details.
GPIO-2	13	19	I/O	General-purpose digital input/output 2. This pin is a bidirectional digital input/output, open-drain and requires an external pull-up resistor. See the *GPIO Pins* section for details.
$\overline{CLR}$	14	20	I	Clear input, level triggered. When the $\overline{CLR}$ pin is logic '0', all V_{OUT}-X pins connect to AGND-x through switches and internal low-impedance. When the $\overline{CLR}$ pin is logic '1', all V_{OUT}-X pins connect to the amplifier outputs.
$\overline{RST}$	15	21	I	Reset input (active low). Logic low on this pin resets the DAC registers and DACs to the values defined by the RSTSEL pin. $\overline{CS}$ must be logic high when $\overline{RST}$ is active.

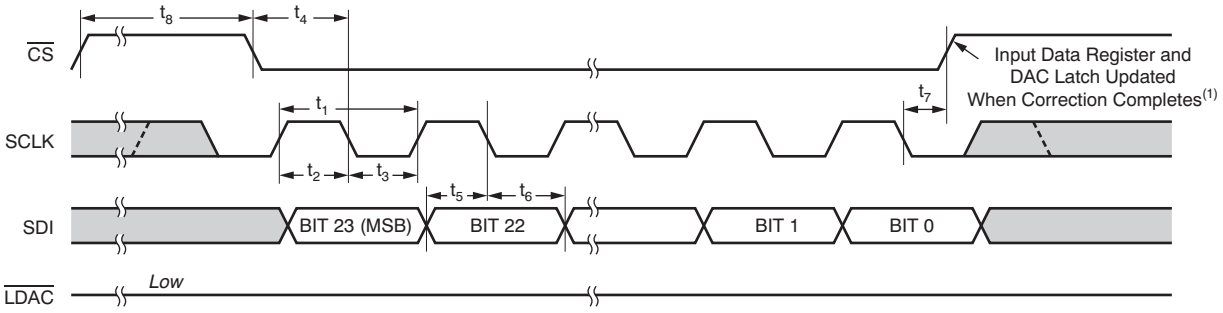
(1) Group A consists of DAC-0, DAC-1, DAC-2, and DAC-3. Group B consists of DAC-4, DAC-5, DAC-6, and DAC-7.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-48	TQFP-64		
DV_{DD}	17	24	I	Digital power supply
DGND	20	25	I	Digital ground
DGND	22	28	I	Digital ground
GPIO-1	23	29	I/O	General-purpose digital input/output 1. This pin is a bidirectional digital input/output, open-drain and requires an external resistor. See the *GPIO Pins* section for details.
GPIO-0	24	30	I/O	General-purpose digital input/output 0. This pin is a bidirectional digital input/output, open-drain and requires an external resistor. See the *GPIO Pins* section for details.
AV_{SS}	26	37	I	Negative analog power supply
V_{OUT}-7	27	38	O	DAC-7 output
OFFSET-B	28	39	O	OFFSET DAC-B analog output. Must be connected to AGND-B during single-supply operation (AV_{SS} = 0V).
AGND-B	29	40	I	Group B[(1)] analog ground and the ground of REF-B. This pin must be tied to AGND-A and DGND.
AGND-B	30	41	I	Group B analog ground and the ground of REF-B. This pin must be tied to AGND-A and DGND.
V_{OUT}-6	31	42	O	DAC-6 output
V_{OUT}-5	32	43	O	DAC-5 output
REF-B	33	44	I	Group B reference input
V_{OUT}-4	34	45	O	DAC-4 output
AIN-1	35	46	I	Auxiliary analog input 1, directly routed to the analog mux
AV_{DD}	36	48	I	Positive analog power supply
$\overline{USB}$/BTC	37	50	I	Data format selection of Input DAC data and Offset DAC data. Data are in straight binary format when connected to DGND or in twos complement format when connected to IOV_{DD}. The command data are always in straight binary format. Refer to *Input Data Format* section for details.
RSTSEL	38	51	I	Output reset selection. Selects the output voltage on the V_{OUT} pin after power-on or hardware reset. Refer to the *Power-On Reset* section for details.
DGND	40	54	I	Digital ground
IOV_{DD}	41	55	I	Interface power
DV_{DD}	42	56	I	Digital power supply
SCLK	43	57	I	SPI bus serial clock input
$\overline{CS}$	44	58	I	SPI bus chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low. When $\overline{CS}$ is high, SDO is in a high-impedance state and the SCLK and SDI signals are blocked from the device.
SDI	45	59	I	SPI bus serial data input
SDO	46	61	O	SPI bus serial data output. When the DSDO bit = '0', the SDO pin works as an output in normal operation. When the DSDO bit = '1', SDO is always in a Hi-Z state, regardless of the $\overline{CS}$ pin status. Refer to the *Timing Diagrams* section for details.
$\overline{LDAC}$	47	62	I	Load DAC latch control input (active low). When $\overline{LDAC}$ is low, the DAC latch is transparent and the contents of the DAC Data Register are transferred to it. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated. See the *Updating the DAC Outputs* section for details. If asynchronous mode is desired, $\overline{LDAC}$ must be permanently tied low before power is applied to the device. If synchronous mode is desired, $\overline{LDAC}$ must be logic high during power-on.
$\overline{WAKEUP}$	48	63	I	Wake-up input (active low). Restores the SPI from sleep to normal operation. See the *Daisy-Chain Operation* section for details.
NC	16, 18, 19, 21, 25, 39	2, 13, 15-18, 22, 23, 26, 27, 31-36, 47, 49, 52, 53, 60, 64	—	Not connected

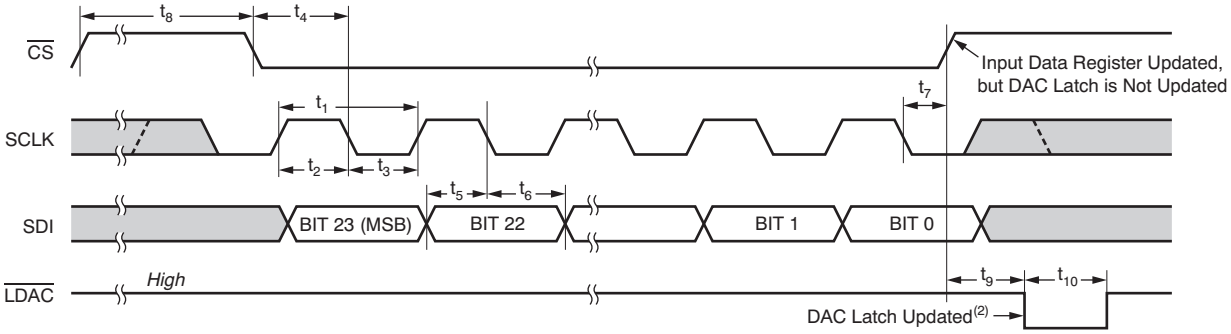
TIMING DIAGRAMS

Case 1: Standalone mode: Update without $\overline{\text{LDAC}}$ pin; $\overline{\text{LDAC}}$ pin tied to logic low.



NOTE: (1) If the correction engine is off, the DAC latch is reloaded immediately after the DAC Data Register is updated.

Case 2: Standalone mode: Update with $\overline{\text{LDAC}}$ pin.

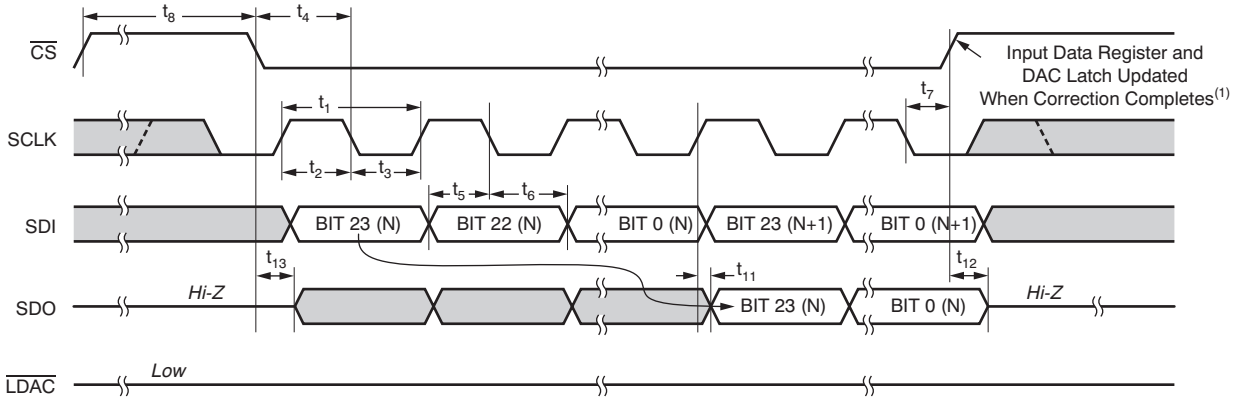


NOTE: (2) The DAC latch is updated when $\overline{\text{LDAC}}$ goes low, as long as the timing requirement of t_9 is satisfied.

Figure 2. SPI Timing for Standalone Mode

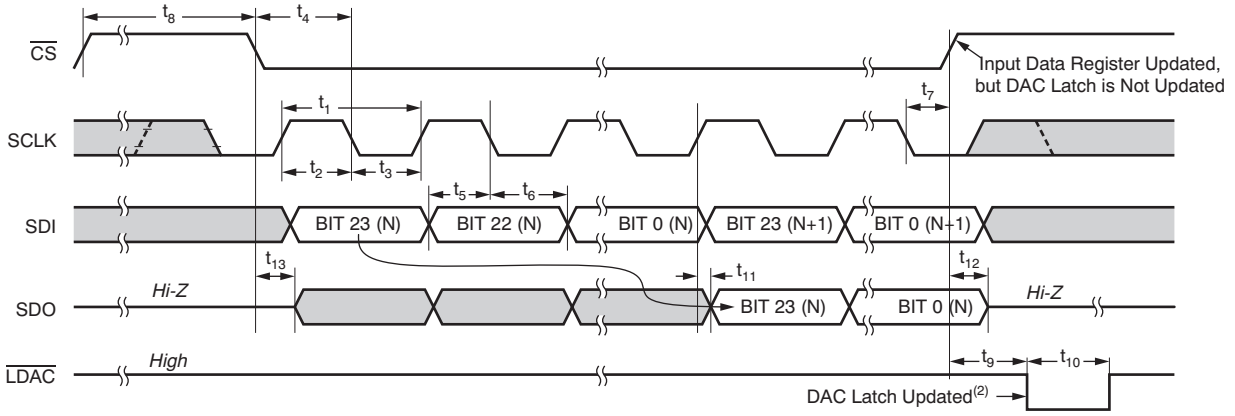
TIMING DIAGRAMS (continued)

Case 3: Daisy-Chain Mode: Update without $\overline{\text{LDAC}}$ pin; $\overline{\text{LDAC}}$ pin tied to logic low.



NOTE: (1) If the correction engine is off, the DAC latch is reloaded immediately after the DAC Data Register is updated.

Case 4: Daisy-Chain Mode: Update with $\overline{\text{LDAC}}$ pin.



NOTE: (2) The DAC latch is updated when $\overline{\text{LDAC}}$ goes low. The proper data are loaded if the t_9 timing requirement is satisfied. Otherwise, invalid data are loaded.

Case 5: Daisy-Chain Mode: Sleeping.

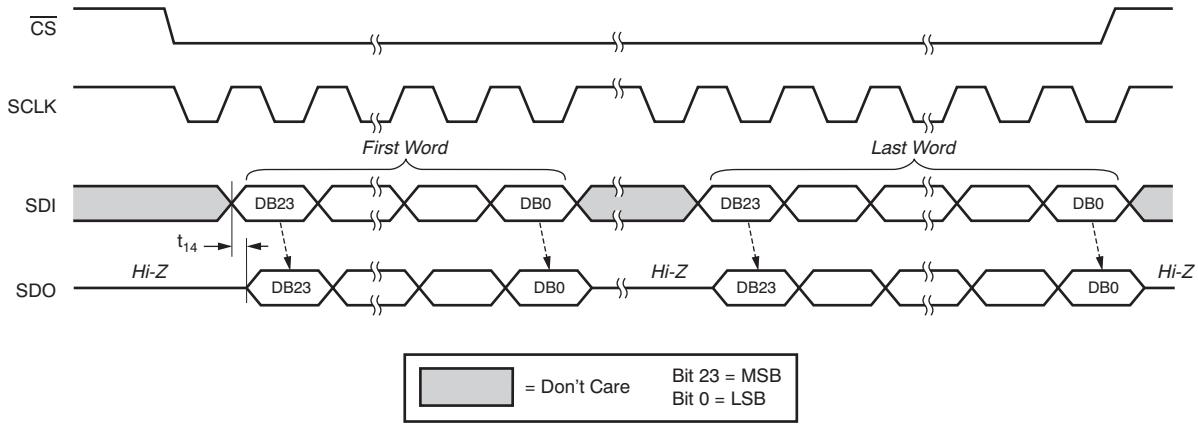


Figure 3. SPI Timing for Daisy-Chain Mode

TIMING DIAGRAMS (continued)

Case 6: Readback for Standalone mode.

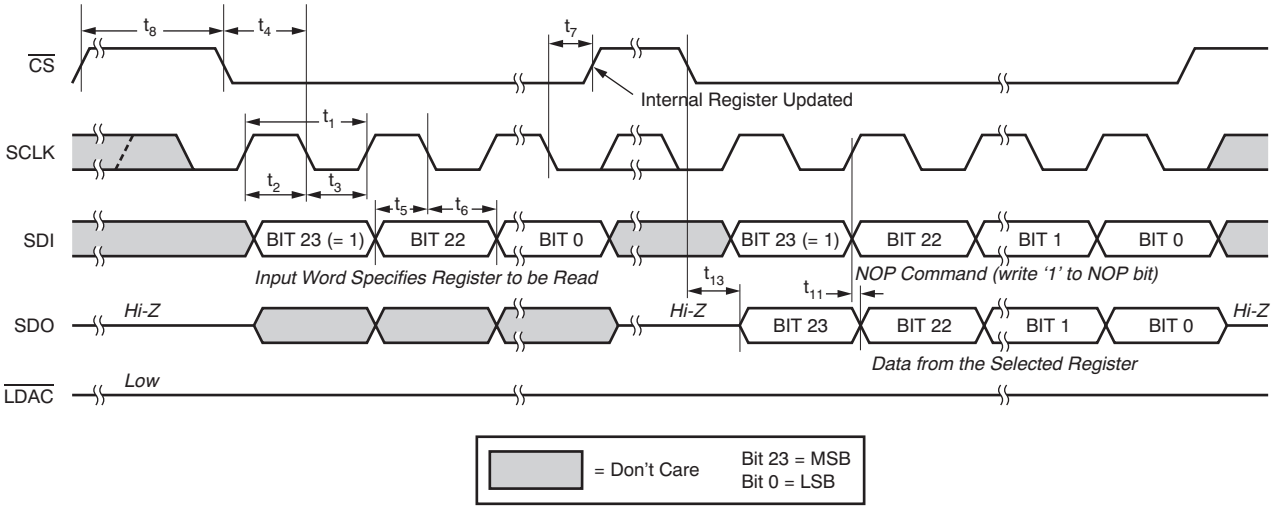


Figure 4. SPI Timing for Readback Operation in Standalone Mode

TIMING CHARACTERISTICS: IOV_{DD} = +5V(1)(2)(3)(4)

At –40°C to +105°C, DV_{DD} = +5V, and IOV_{DD} = +5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	Clock frequency		50	MHz
t_1	SCLK cycle time	20		ns
t_2	SCLK high time	10		ns
t_3	SCLK low time	7		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge setup time	8		ns
t_5	SDI setup time before falling edge of SCLK	5		ns
t_6	SDI hold time after falling edge of SCLK	5		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	5		ns
t_8	$\overline{CS}$ high time	10		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{10}	$\overline{LDAC}$ pulse duration	10		ns
t_{11}	Delay from SCLK rising edge to SDO valid	3	8	ns
t_{12}	Delay from $\overline{CS}$ rising edge to SDO Hi-Z		5	ns
t_{13}	Delay from $\overline{CS}$ falling edge to SDO valid		6	ns
t_{14}	SDI to SDO delay during sleep mode	2	5	ns

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) All input signals are specified with $t_R = t_F$ = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD}/2.
(4) SDO loaded with 10Ω series resistance and 10pF load capacitance for SDO timing specifications.

TIMING CHARACTERISTICS: IOV_{DD} = +3V(1)(2)(3)(4)

At –40°C to +105°C, DV_{DD} = +3V/+5V, and IOV_{DD} = +3V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	Clock frequency		25	MHz
t_1	SCLK cycle time	40		ns
t_2	SCLK high time	19		ns
t_3	SCLK low time	7		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge setup time	15		ns
t_5	SDI setup time before falling edge of SCLK	5		ns
t_6	SDI hold time after falling edge of SCLK	5		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	10		ns
t_8	$\overline{CS}$ high time	19		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{10}	$\overline{LDAC}$ pulse duration	10		ns
t_{11}	Delay from SCLK rising edge to SDO valid	3	15	ns
t_{12}	Delay from $\overline{CS}$ rising edge to SDO Hi-Z		7	ns
t_{13}	Delay from $\overline{CS}$ falling edge to SDO valid		10	ns
t_{14}	SDI to SDO delay during sleep mode	2	10	ns

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) All input signals are specified with $t_R = t_F$ = 3ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD}/2.
(4) SDO loaded with 10Ω series resistance and 10pF load capacitance for SDO timing specifications.

TIMING CHARACTERISTICS: IOV_{DD} = +1.8V(1)(2)(3)(4)

At –40°C to +105°C, DV_{DD} = +3V/+5V, and IOV_{DD} = +1.8V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	Clock frequency		16.6	MHz
t_1	SCLK cycle time	60		ns
t_2	SCLK high time	28		ns
t_3	SCLK low time	7		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge setup time	28		ns
t_5	SDI setup time before falling edge of SCLK	10		ns
t_6	SDI hold time after falling edge of SCLK	5		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	10		ns
t_8	$\overline{CS}$ high time	28		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	5		ns
t_{10}	$\overline{LDAC}$ pulse duration	10		ns
t_{11}	Delay from SCLK rising edge to SDO valid	3	25	ns
t_{12}	Delay from $\overline{CS}$ rising edge to SDO Hi-Z		15	ns
t_{13}	Delay from $\overline{CS}$ falling edge to SDO valid		23	ns
t_{14}	SDI to SDO delay during sleep mode	2	25	ns

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) All input signals are specified with $t_R = t_F$ = 6ns (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(4) SDO loaded with 10Ω series resistance and 10pF load capacitance for SDO timing specifications.

TYPICAL CHARACTERISTICS: Bipolar

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

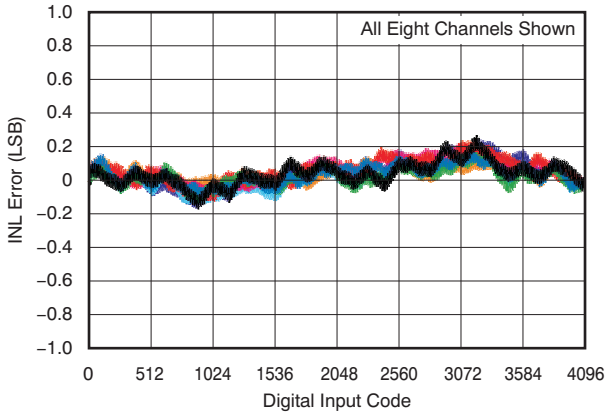


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

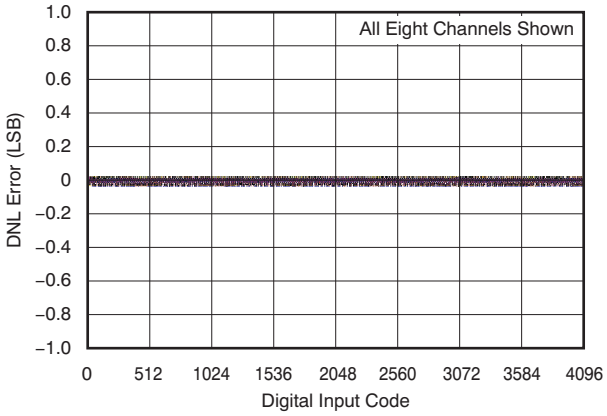


Figure 6.

LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

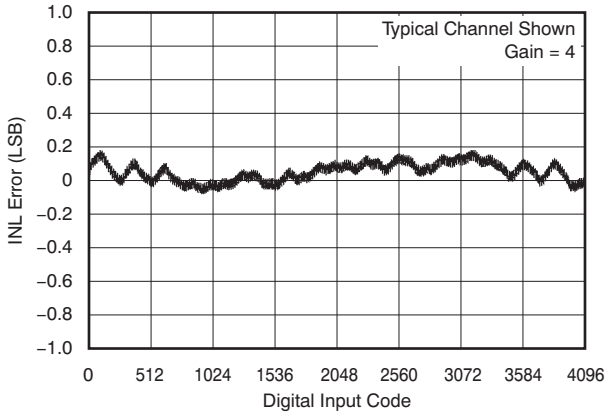


Figure 7.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

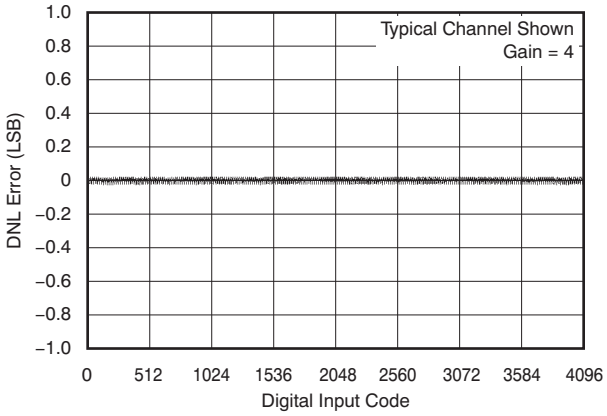


Figure 8.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

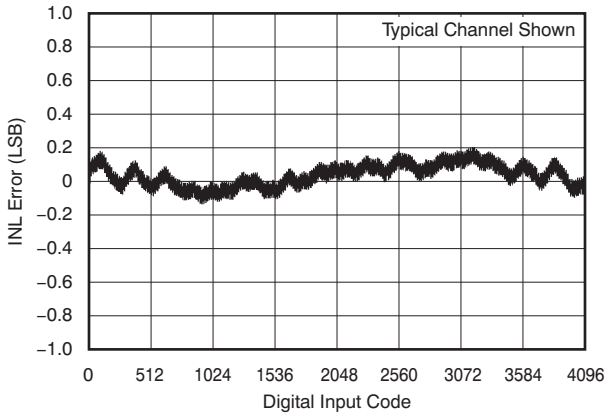


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

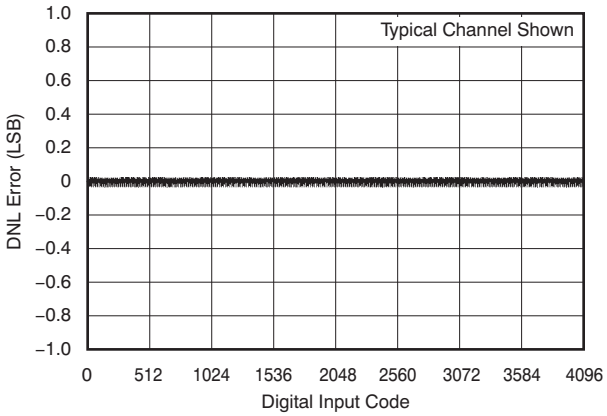


Figure 10.

LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

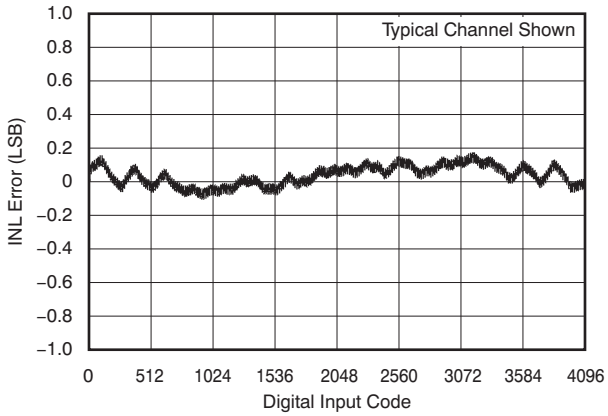


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

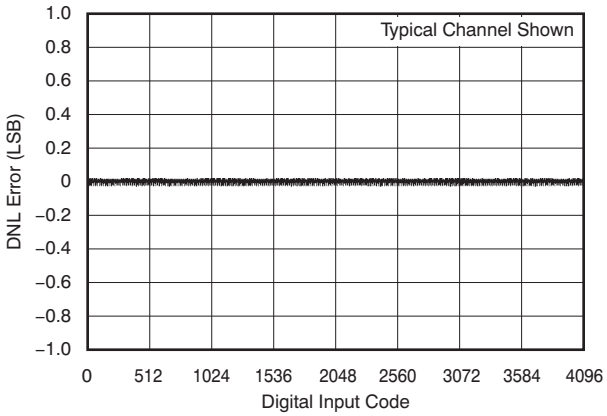


Figure 12.

LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

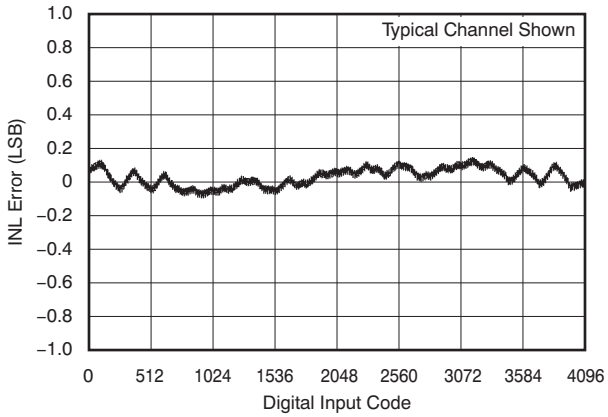


Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

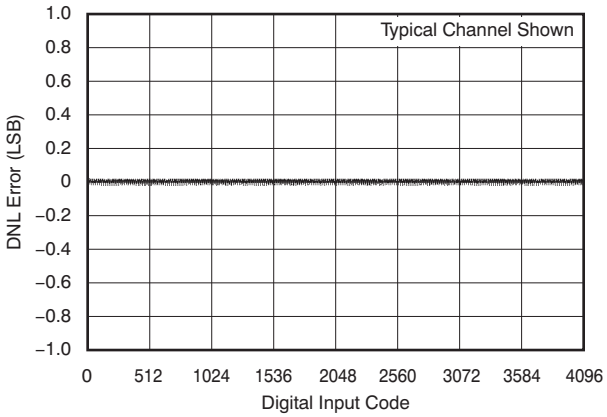


Figure 14.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

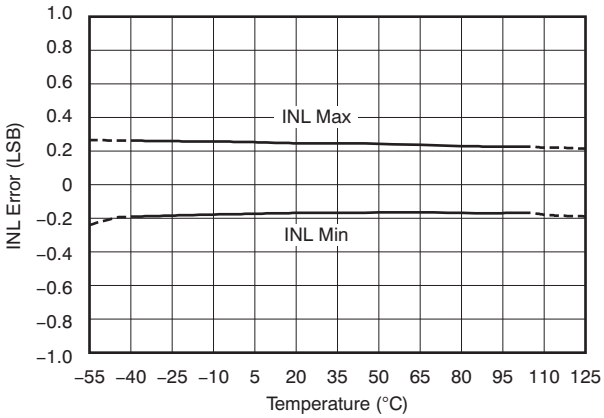


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

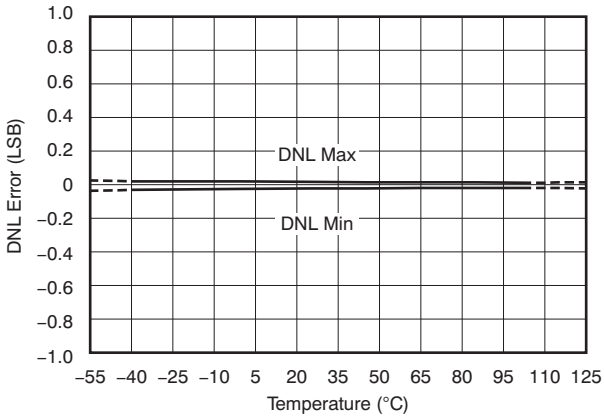


Figure 16.

LINEARITY ERROR vs TEMPERATURE

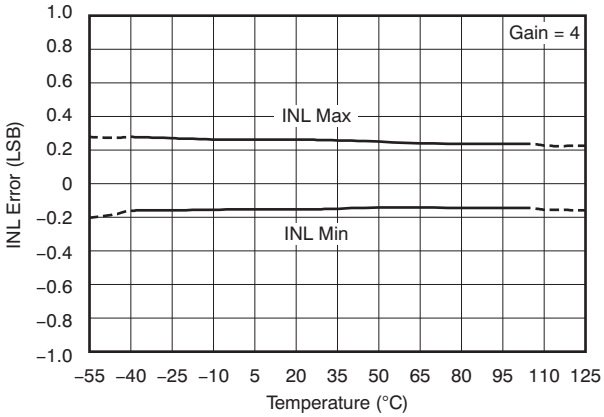


Figure 17.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

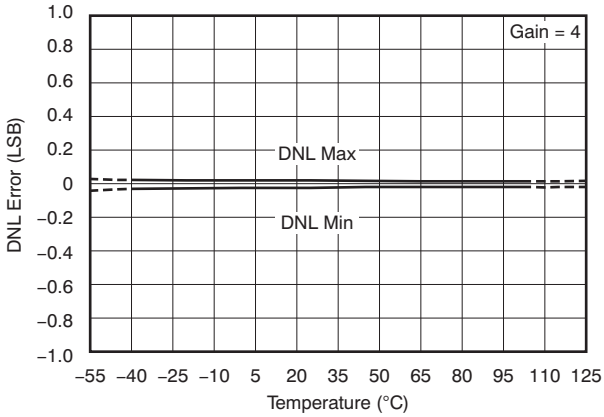


Figure 18.

LINEARITY ERROR vs REFERENCE VOLTAGE

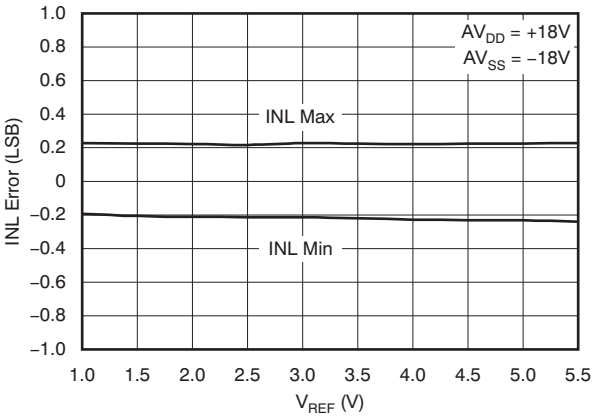


Figure 19.

DIFFERENTIAL LINEARITY ERROR vs REFERENCE VOLTAGE

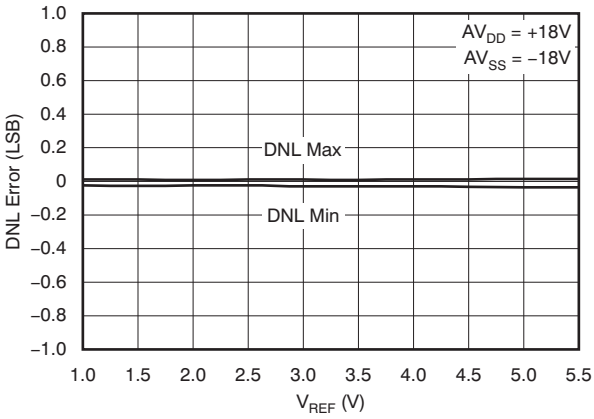


Figure 20.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs AV_{DD} AND AV_{SS}

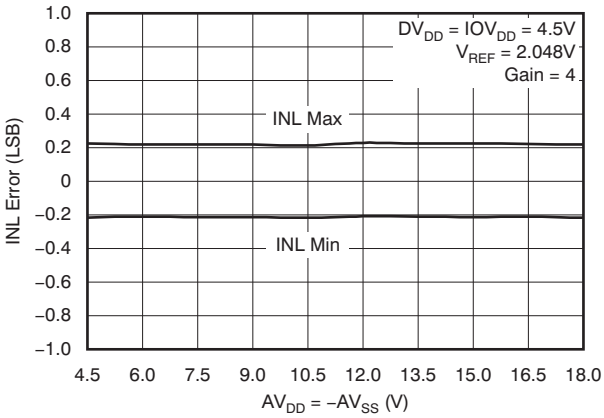


Figure 21.

DIFFERENTIAL LINEARITY ERROR vs AV_{DD} AND AV_{SS}

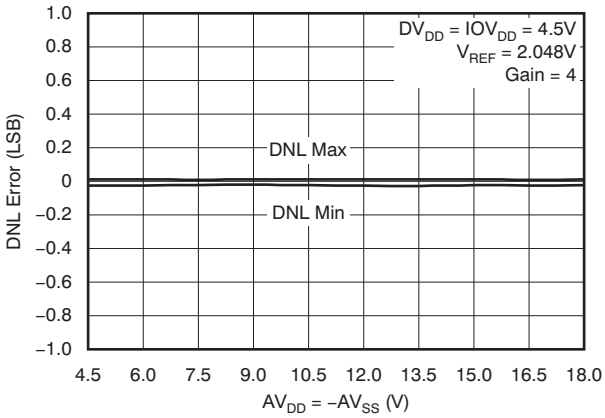


Figure 22.

BIPOLAR ZERO ERROR vs AV_{DD} AND AV_{SS}

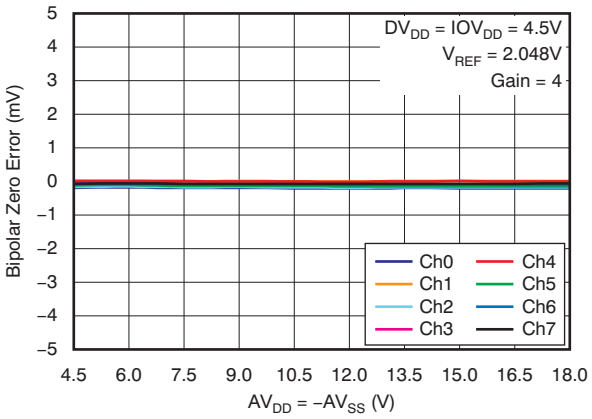


Figure 23.

BIPOLAR GAIN ERROR vs AV_{DD} AND AV_{SS}

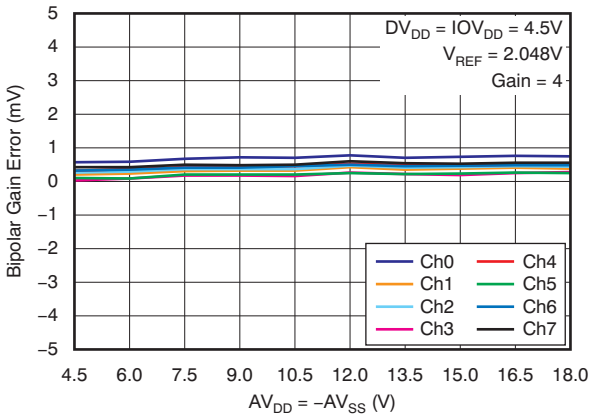


Figure 24.

BIPOLAR ZERO ERROR vs REFERENCE VOLTAGE

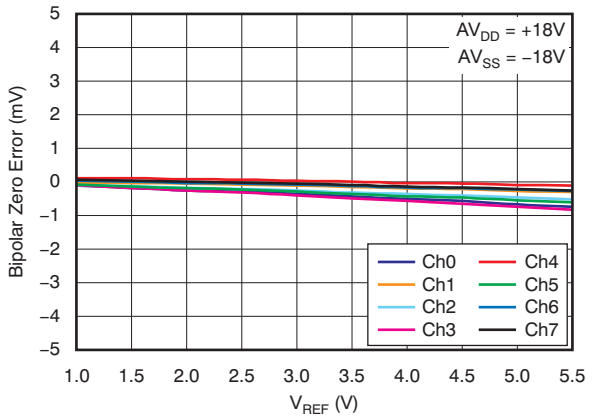


Figure 25.

BIPOLAR ZERO ERROR vs REFERENCE VOLTAGE

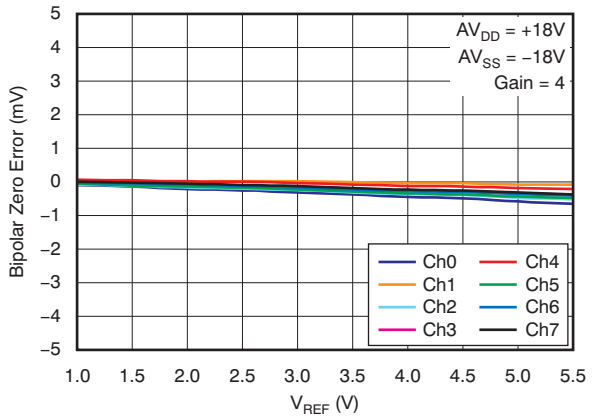


Figure 26.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

BIPOLAR GAIN ERROR vs REFERENCE VOLTAGE

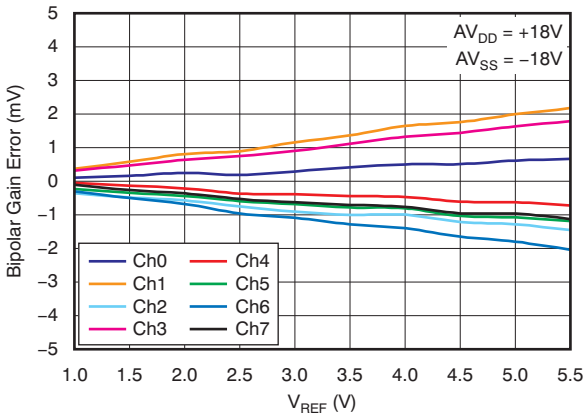


Figure 27.

BIPOLAR GAIN ERROR vs REFERENCE VOLTAGE

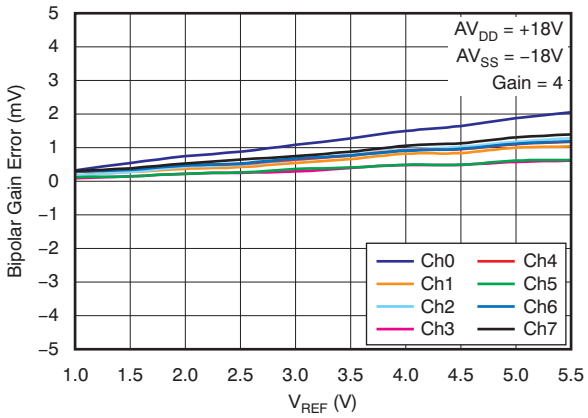


Figure 28.

BIPOLAR ZERO ERROR vs TEMPERATURE

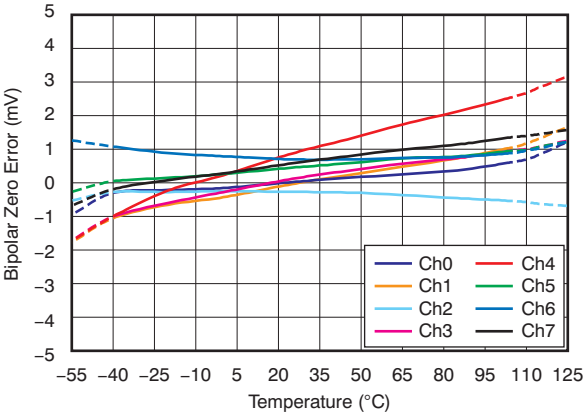


Figure 29.

BIPOLAR ZERO ERROR vs TEMPERATURE

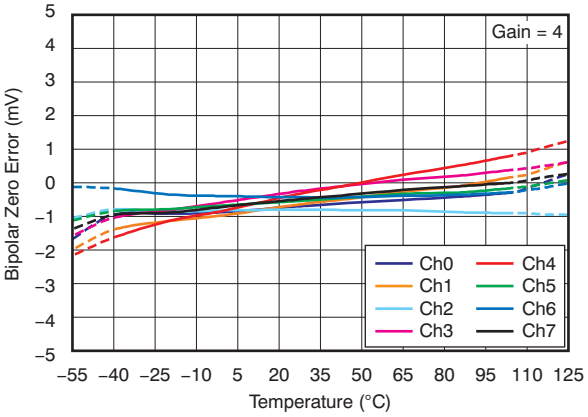


Figure 30.

BIPOLAR GAIN ERROR vs TEMPERATURE

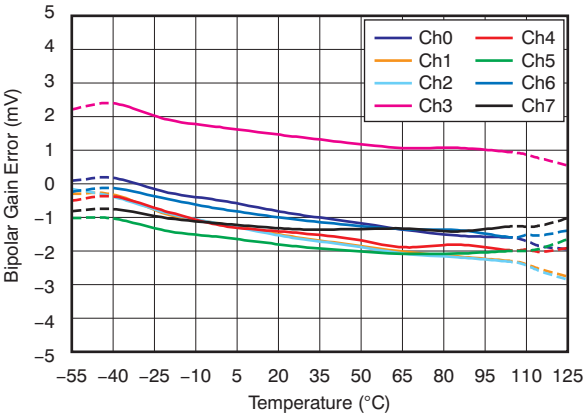


Figure 31.

BIPOLAR GAIN ERROR vs TEMPERATURE

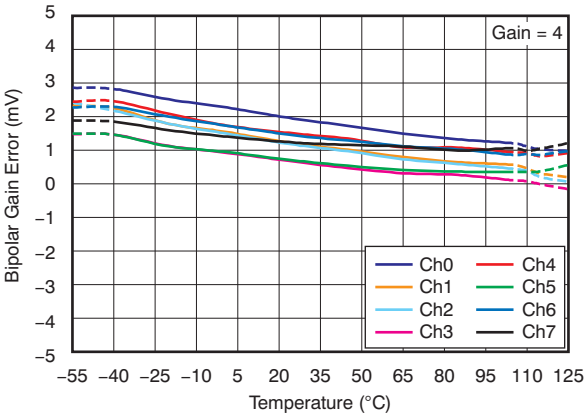


Figure 32.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

ANALOG POWER-SUPPLY CURRENT vs TEMPERATURE

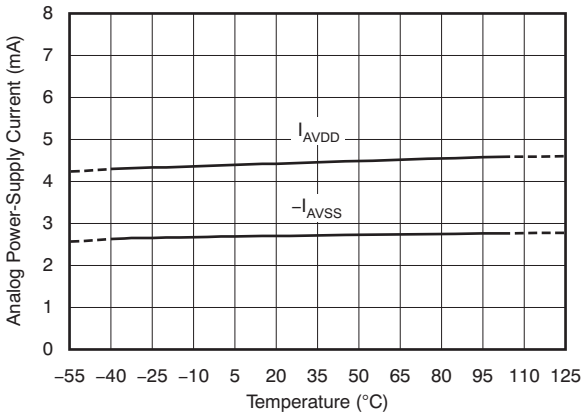


Figure 33.

ANALOG POWER-SUPPLY CURRENT vs REFERENCE VOLTAGE

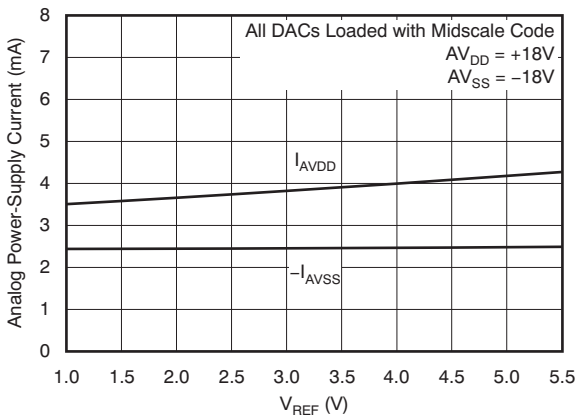


Figure 34.

ANALOG POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

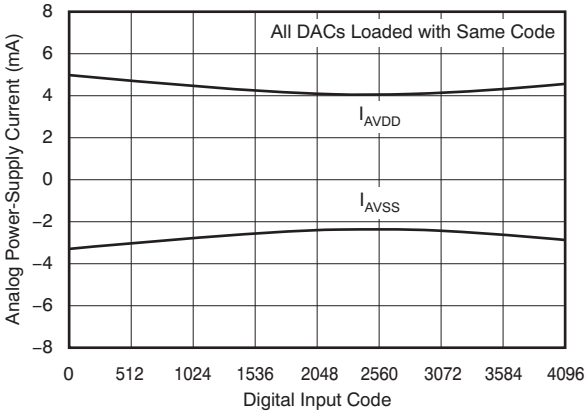


Figure 35.

DIGITAL POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

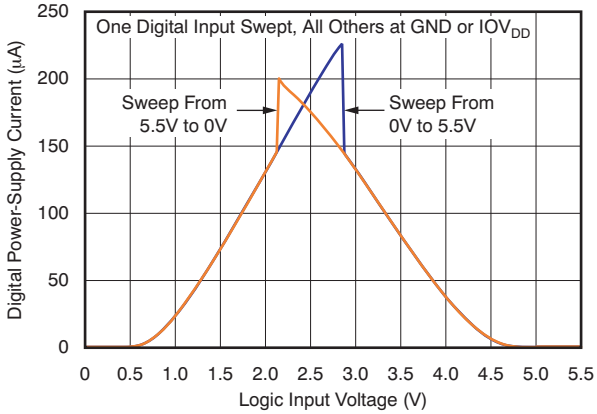


Figure 36.

DELTA OUTPUT VOLTAGE vs SOURCE AND SINK CURRENTS

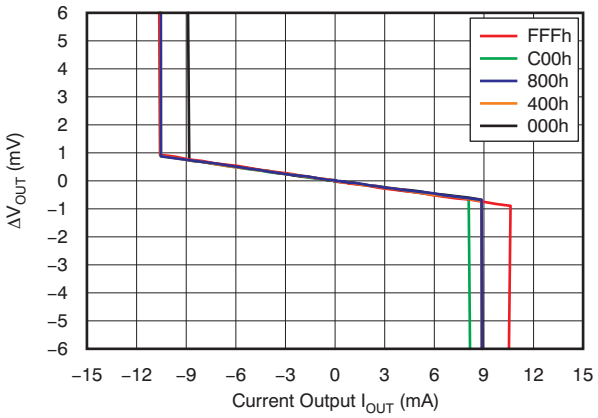


Figure 37.

DAC OUTPUT NOISE DENSITY vs FREQUENCY

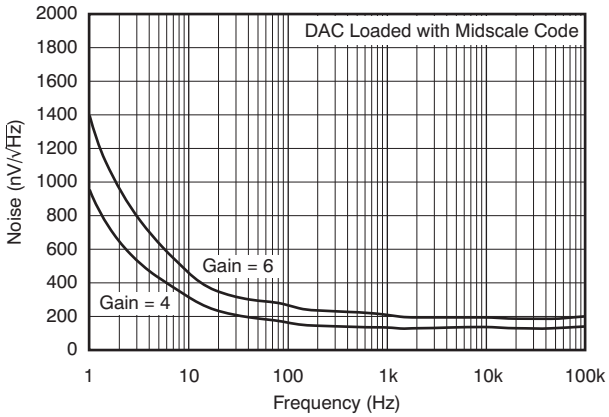


Figure 38.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

SETTLING TIME
–15V TO +15V TRANSITION

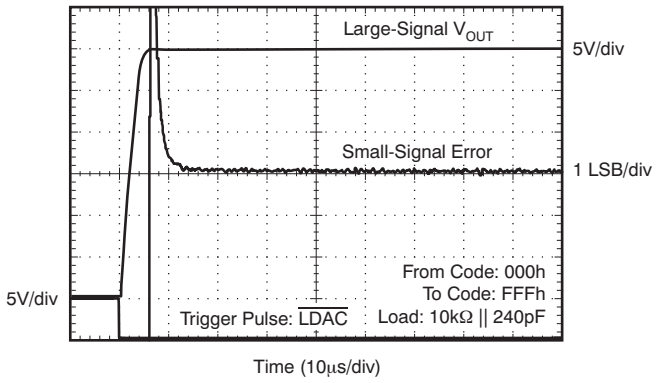


Figure 39.

SETTLING TIME
+15V TO –15V TRANSITION

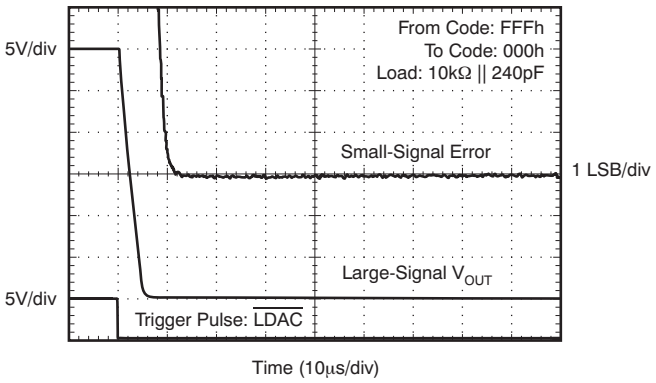


Figure 40.

SETTLING TIME
1/4 TO 3/4 FULL-SCALE TRANSITION

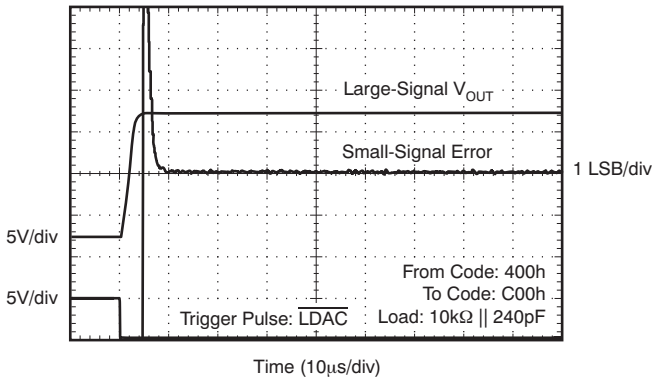


Figure 41.

SETTLING TIME
3/4 TO 1/4 FULL-SCALE TRANSITION

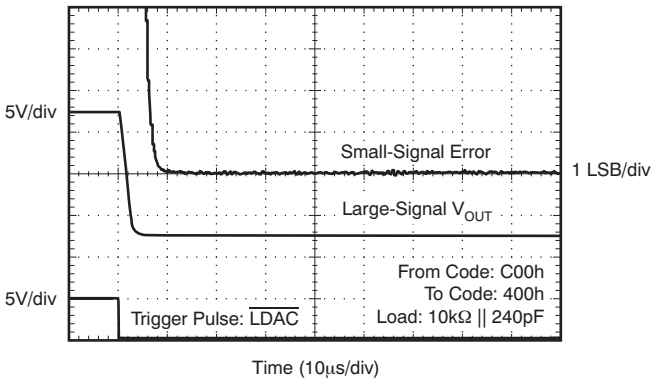


Figure 42.

GLITCH ENERGY
1 LSB STEP, RISING EDGE

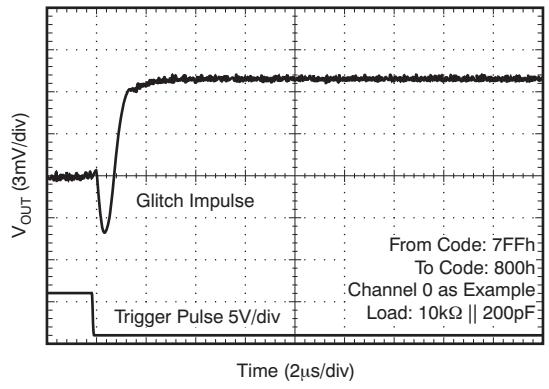


Figure 43.

GLITCH ENERGY
1 LSB STEP, FALLING EDGE

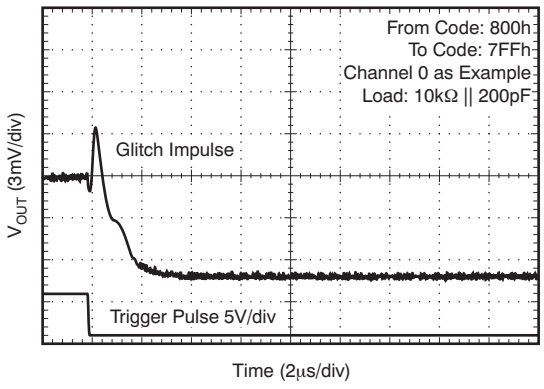


Figure 44.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

BIPOLAR ZERO ERROR HISTOGRAM

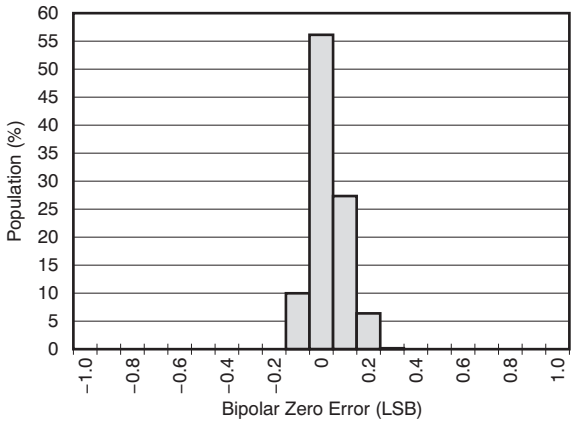


Figure 45.

BIPOLAR ZERO ERROR HISTOGRAM

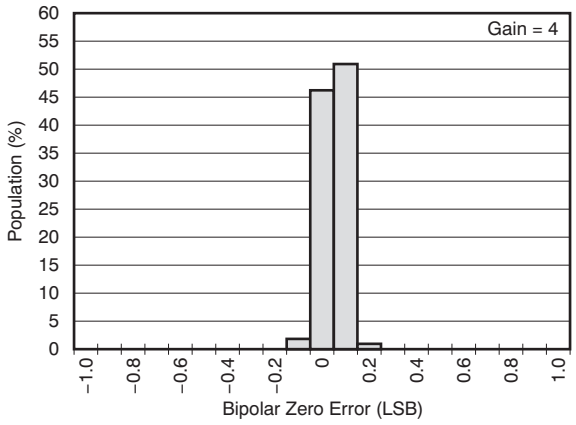


Figure 46.

BIPOLAR GAIN ERROR HISTOGRAM

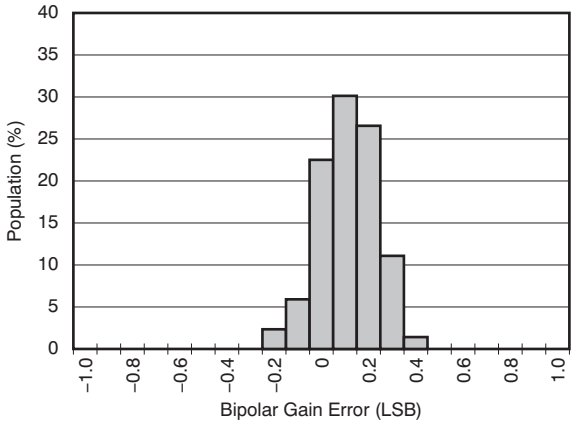


Figure 47.

BIPOLAR GAIN ERROR HISTOGRAM

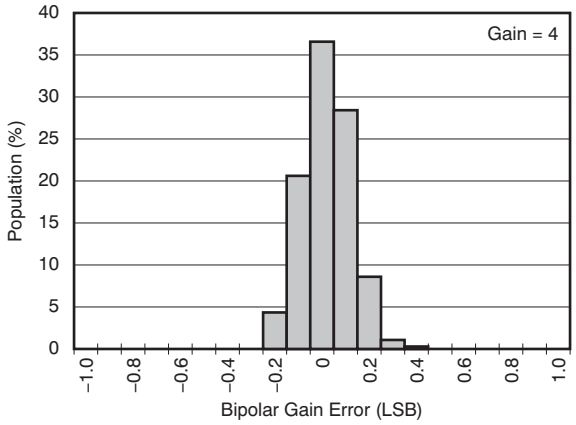


Figure 48.

NEGATIVE ANALOG POWER SUPPLY HISTOGRAM

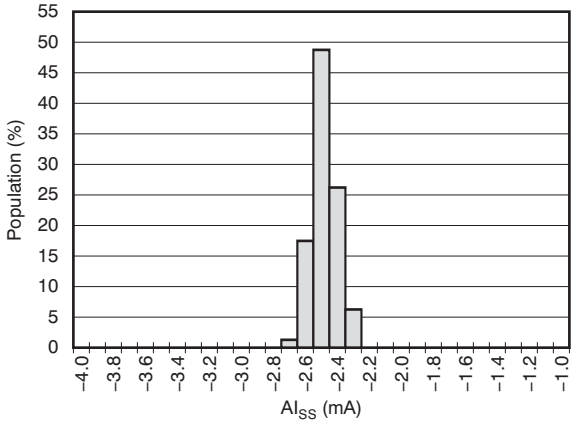


Figure 49.

POSITIVE ANALOG POWER SUPPLY HISTOGRAM

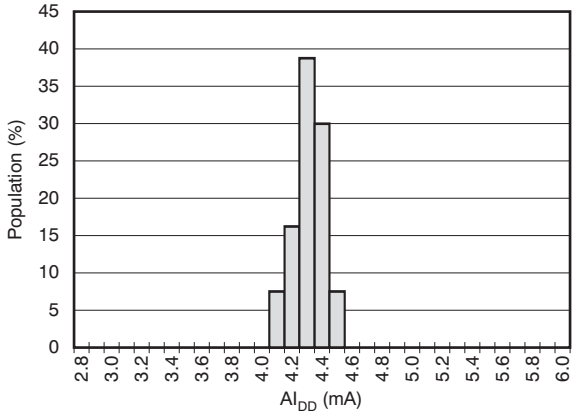


Figure 50.

TYPICAL CHARACTERISTICS: Bipolar (continued)

At T_A = 25°C, AV_{DD} = 16.5V, AV_{SS} = –16.5V, V_{REF} = IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

DAC OUTPUT NOISE
0.1Hz TO 10Hz

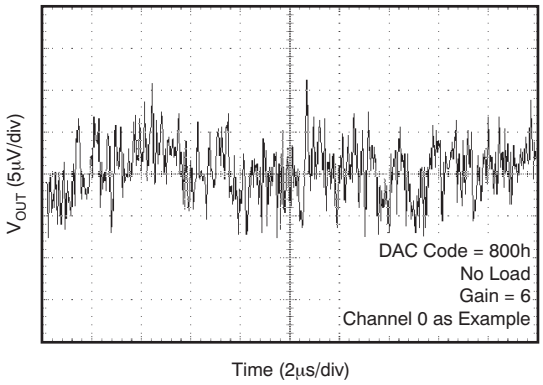


Figure 51.

DAC OUTPUT NOISE
0.1Hz TO 10Hz

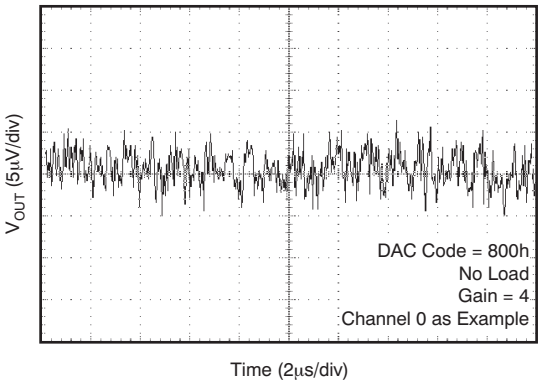


Figure 52.

TYPICAL CHARACTERISTICS: Unipolar

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

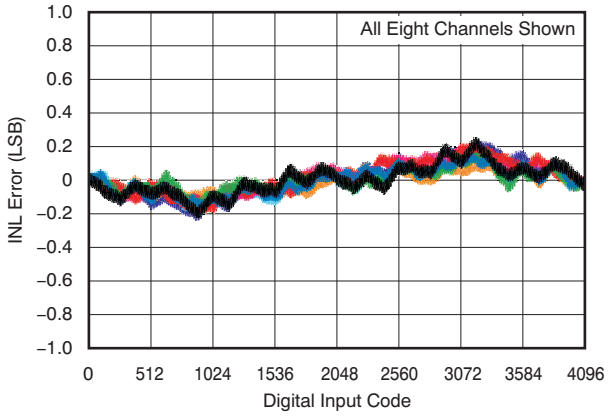


Figure 53.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (All 8 Channels)

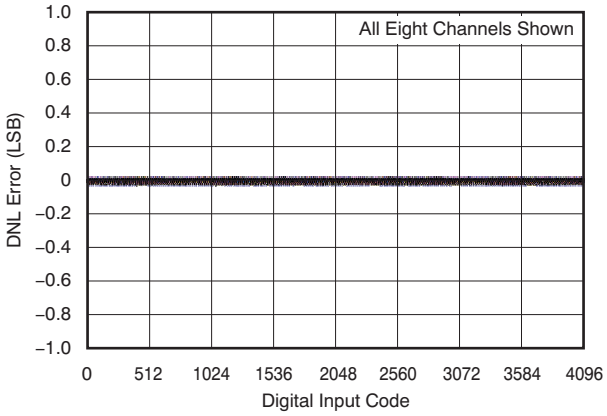


Figure 54.

LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

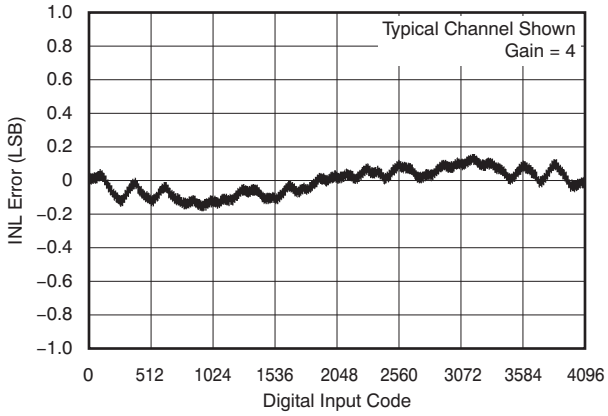


Figure 55.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

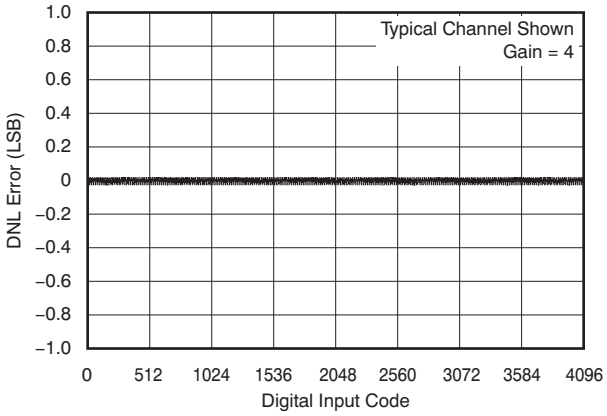


Figure 56.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

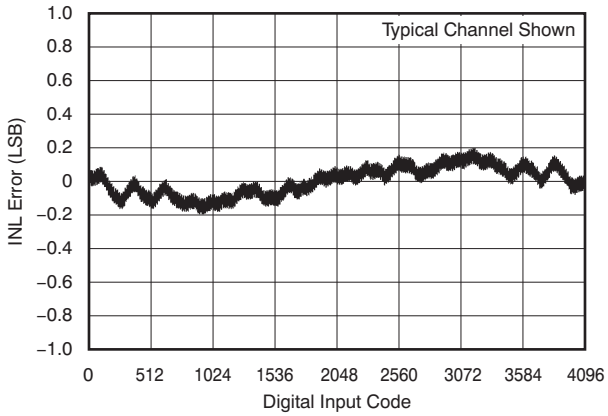


Figure 57.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

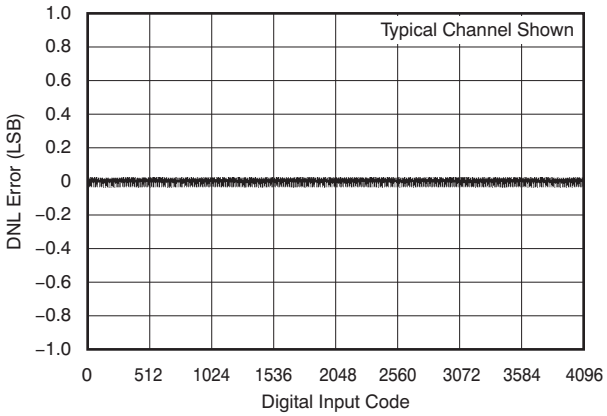


Figure 58.

LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

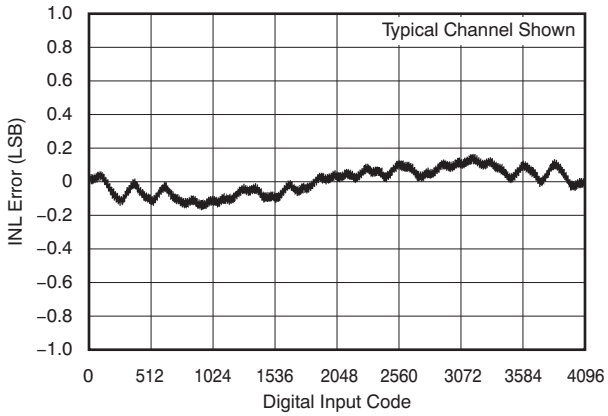


Figure 59.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

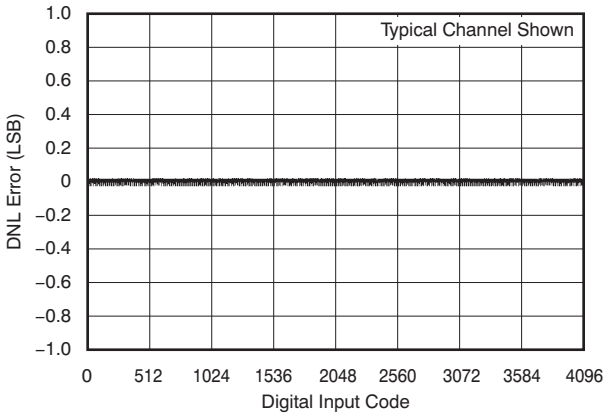


Figure 60.

LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

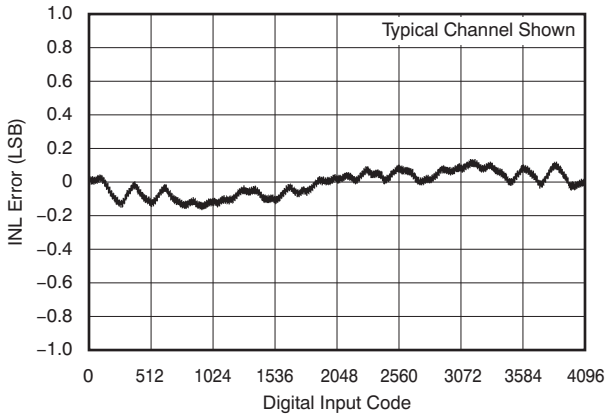


Figure 61.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

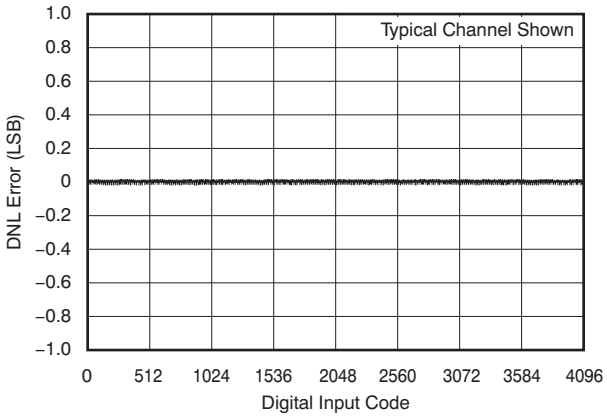


Figure 62.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

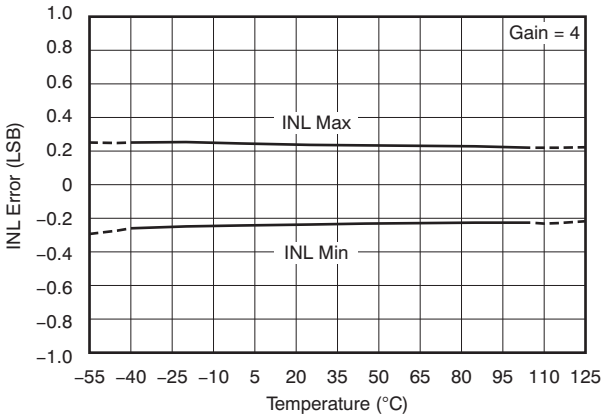


Figure 63.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

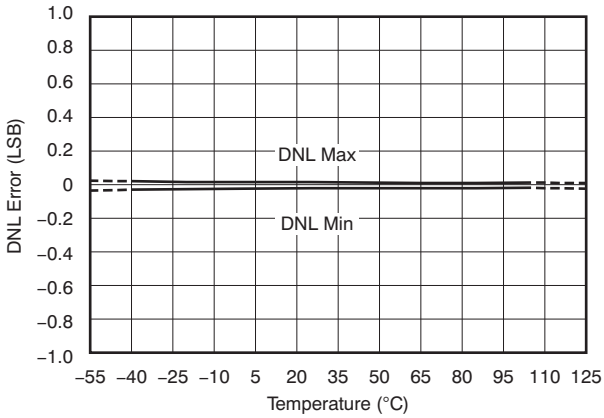


Figure 64.

LINEARITY ERROR vs TEMPERATURE

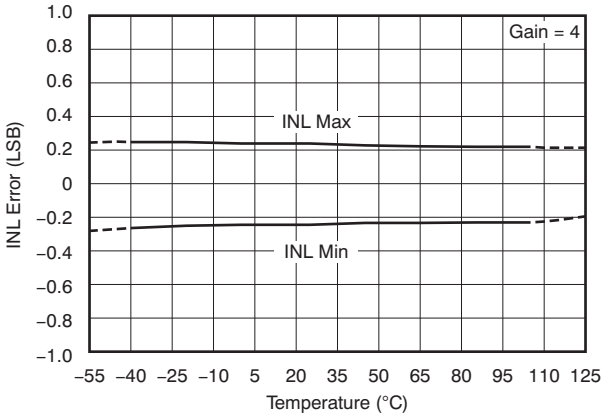


Figure 65.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

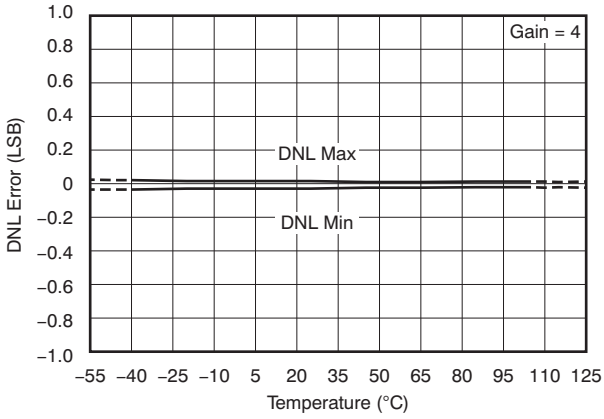


Figure 66.

LINEARITY ERROR vs REFERENCE VOLTAGE

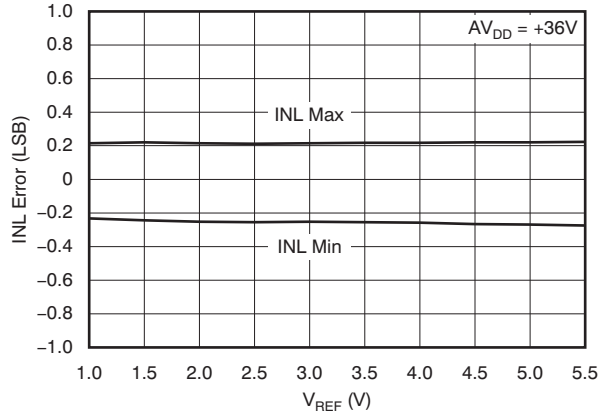


Figure 67.

DIFFERENTIAL LINEARITY ERROR vs REFERENCE VOLTAGE

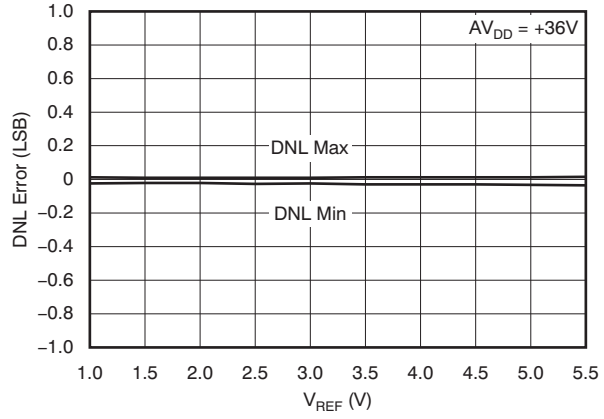


Figure 68.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

LINEARITY ERROR vs ANALOG SUPPLY VOLTAGE

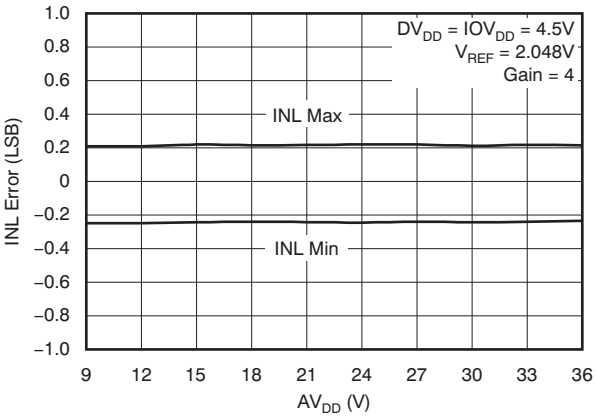


Figure 69.

DIFFERENTIAL LINEARITY ERROR vs ANALOG SUPPLY VOLTAGE

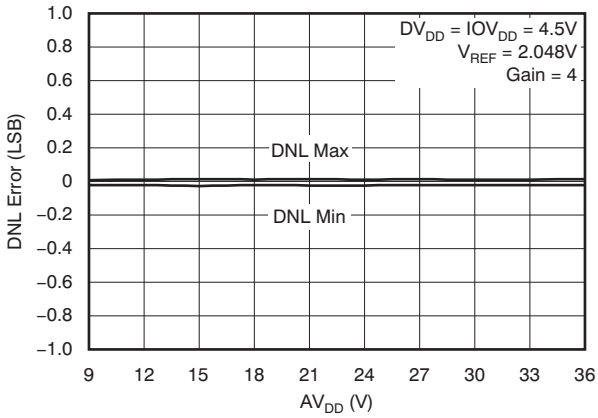


Figure 70.

ZERO-SCALE ERROR vs ANALOG SUPPLY VOLTAGE

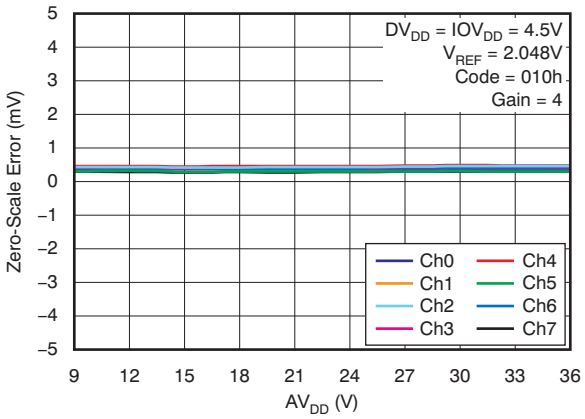


Figure 71.

UNIPOLAR GAIN ERROR vs ANALOG SUPPLY VOLTAGE

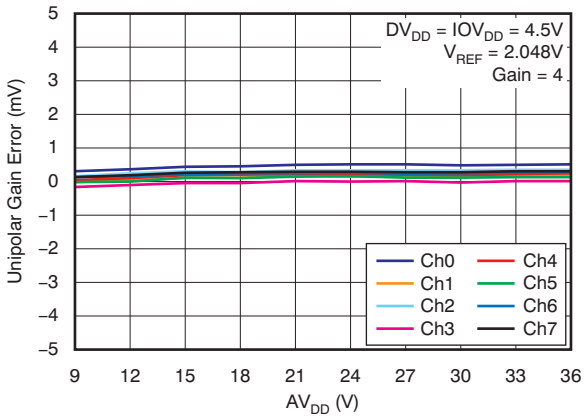


Figure 72.

ZERO-SCALE ERROR vs REFERENCE VOLTAGE

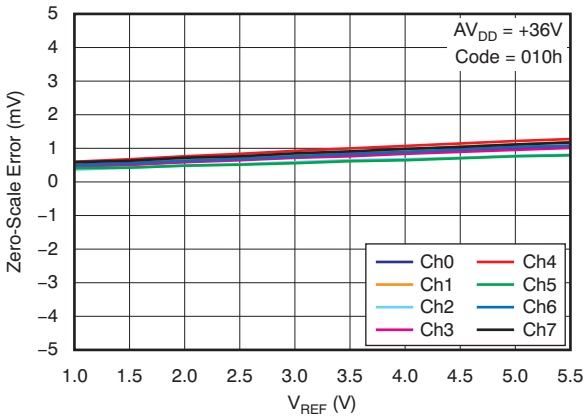


Figure 73.

ZERO-SCALE ERROR vs REFERENCE VOLTAGE

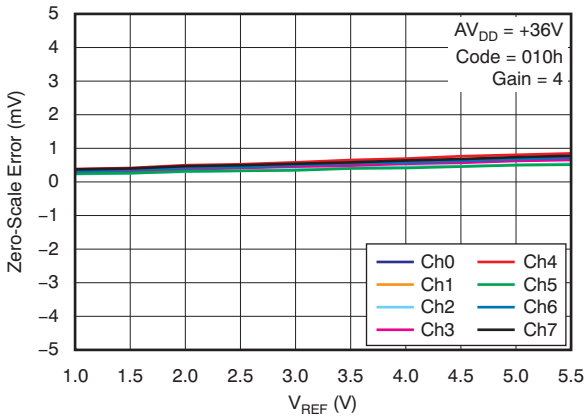


Figure 74.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

UNIPOLAR GAIN ERROR vs REFERENCE VOLTAGE

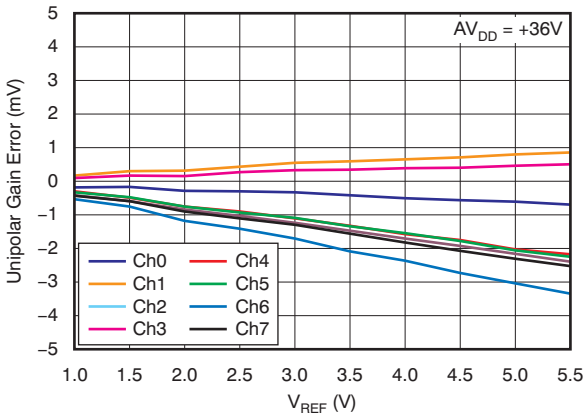


Figure 75.

UNIPOLAR GAIN ERROR vs REFERENCE VOLTAGE

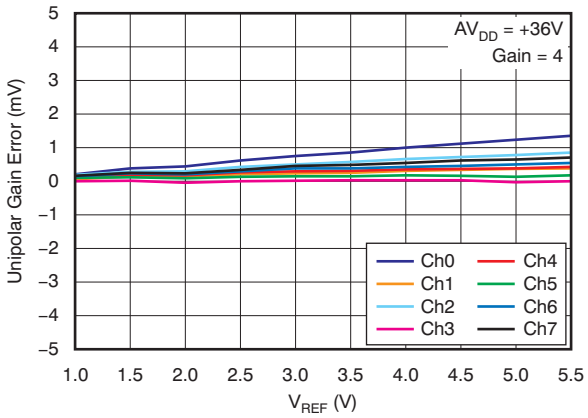


Figure 76.

ZERO-SCALE ERROR vs TEMPERATURE

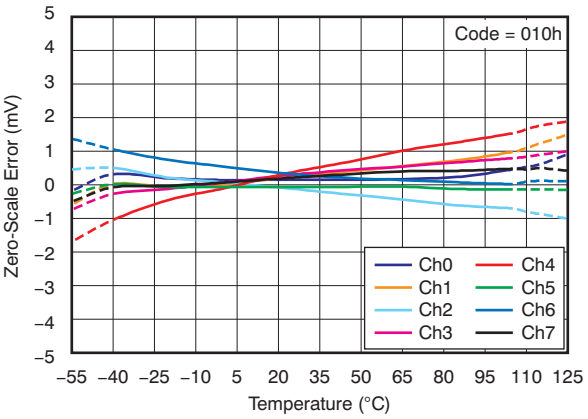


Figure 77.

ZERO-SCALE ERROR vs TEMPERATURE

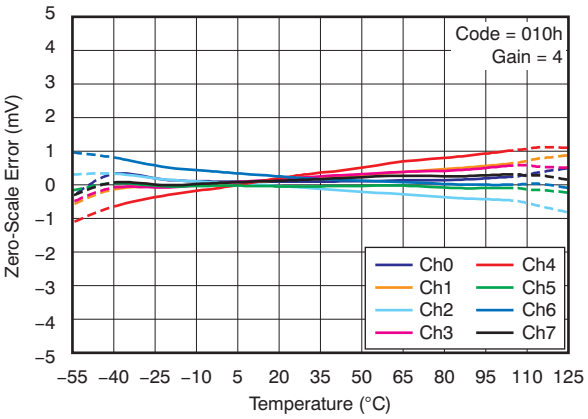


Figure 78.

UNIPOLAR GAIN ERROR vs TEMPERATURE

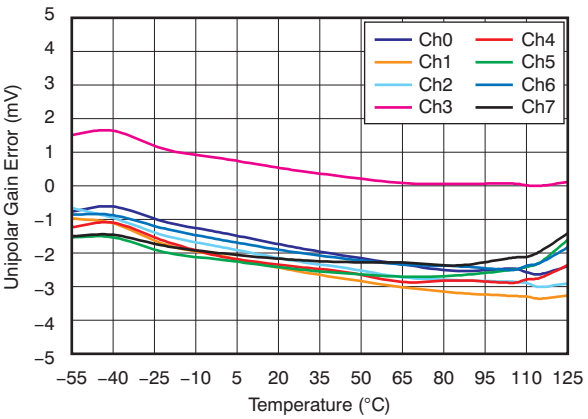


Figure 79.

UNIPOLAR GAIN ERROR vs TEMPERATURE

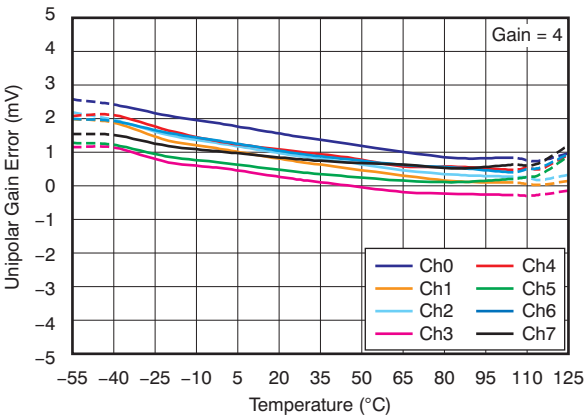


Figure 80.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

ANALOG POWER-SUPPLY CURRENT vs TEMPERATURE

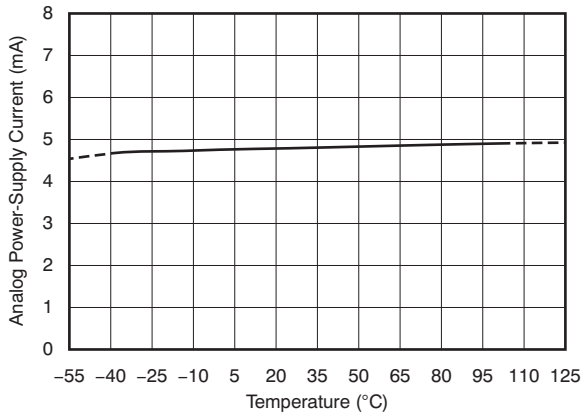


Figure 81.

ANALOG POWER-SUPPLY CURRENT vs REFERENCE VOLTAGE

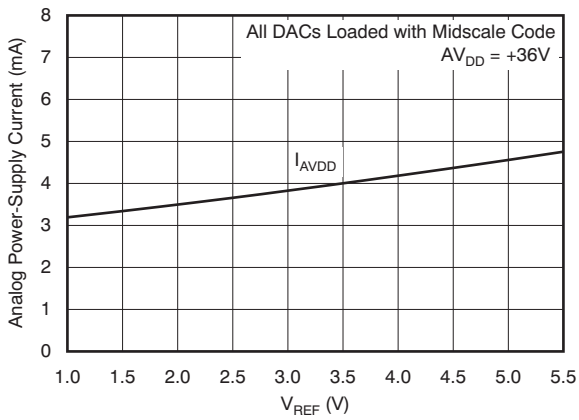


Figure 82.

ANALOG POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

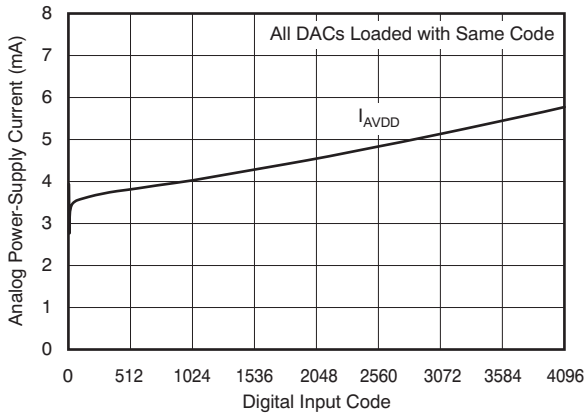


Figure 83.

OUTPUT VOLTAGE vs SOURCE CURRENT CAPABILITY

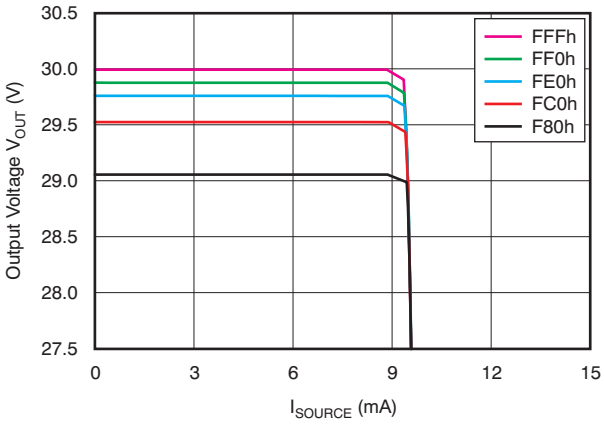


Figure 84.

OUTPUT VOLTAGE vs SINK CURRENT CAPABILITY

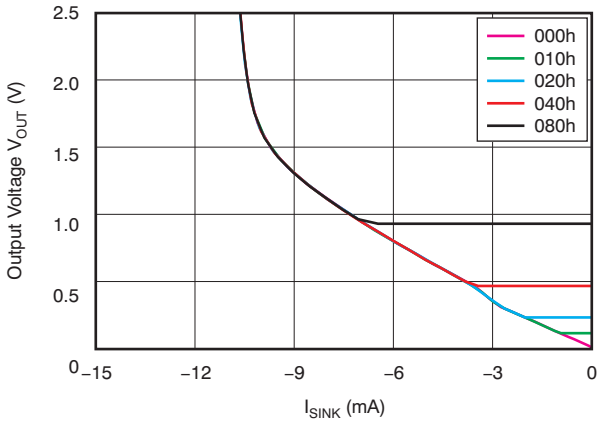


Figure 85.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

SETTLING TIME
0V TO 30V TRANSITION

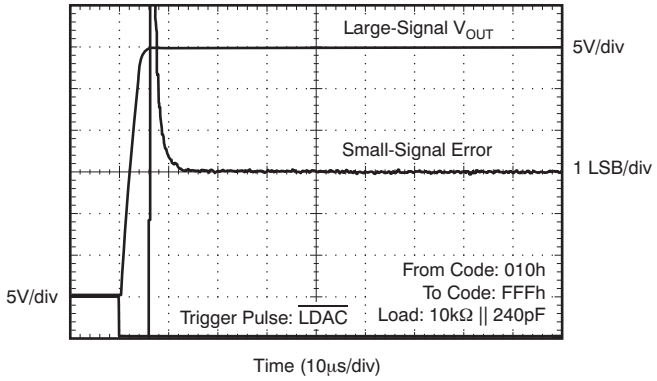


Figure 86.

SETTLING TIME
30V TO 0V TRANSITION

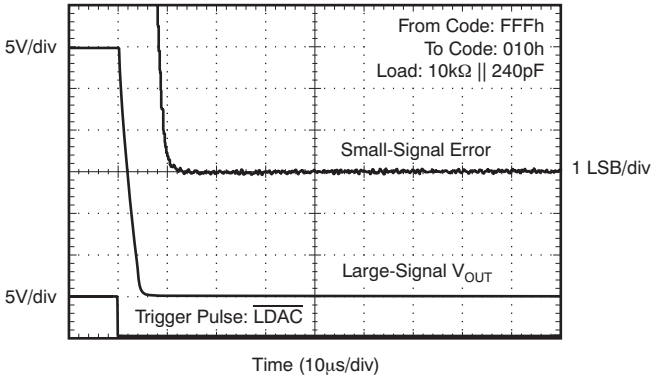


Figure 87.

SETTLING TIME
1/4 TO 3/4 TRANSITION

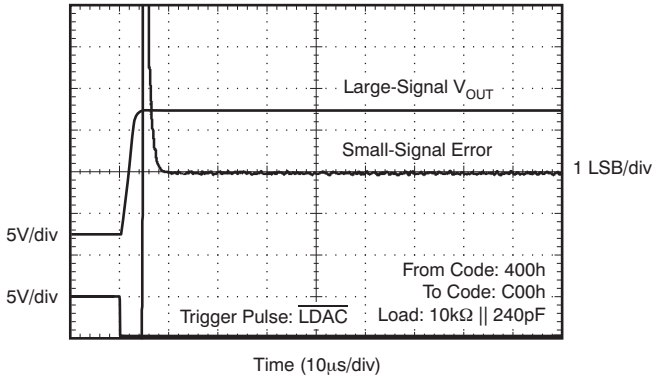


Figure 88.

SETTLING TIME
3/4 TO 1/4 TRANSITION

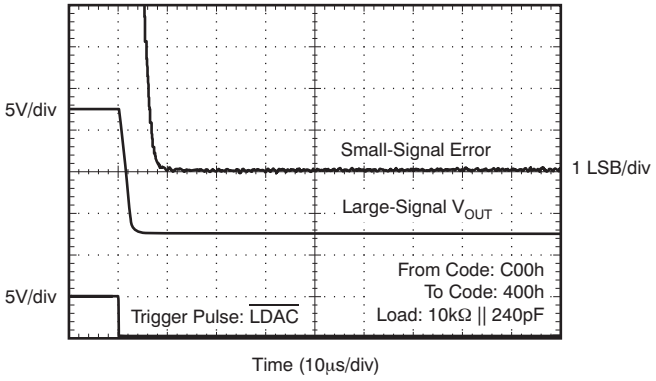


Figure 89.

GLITCH ENERGY
1 LSB STEP, RISING EDGE

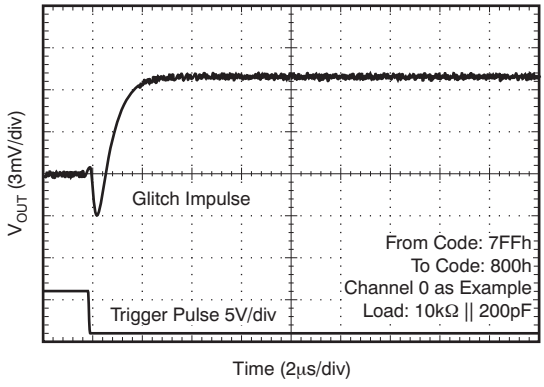


Figure 90.

GLITCH ENERGY
1 LSB STEP, FALLING EDGE

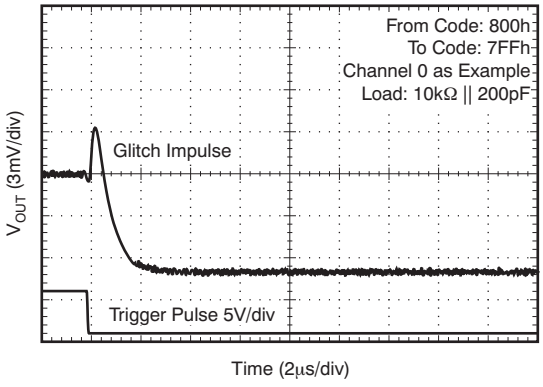


Figure 91.

TYPICAL CHARACTERISTICS: Unipolar (continued)

At T_A = 25°C, AV_{DD} = 32V, AV_{SS} = 0V, V_{REF} = 5V, IOV_{DD} = DV_{DD} = 5V, gain = 6, data format=USB, unless otherwise noted.

ZERO-SCALE ERROR HISTOGRAM

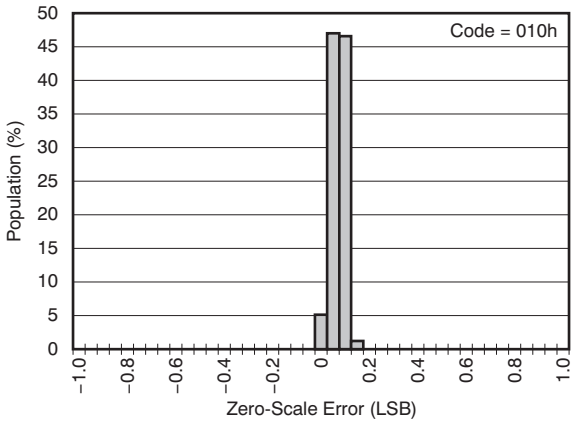


Figure 92.

ZERO-SCALE ERROR HISTOGRAM

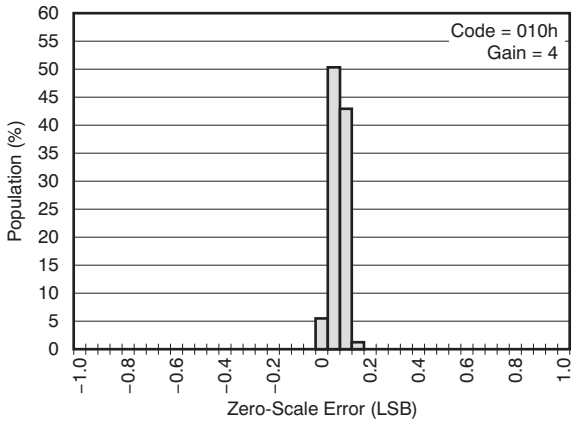


Figure 93.

UNIPOLAR GAIN ERROR HISTOGRAM

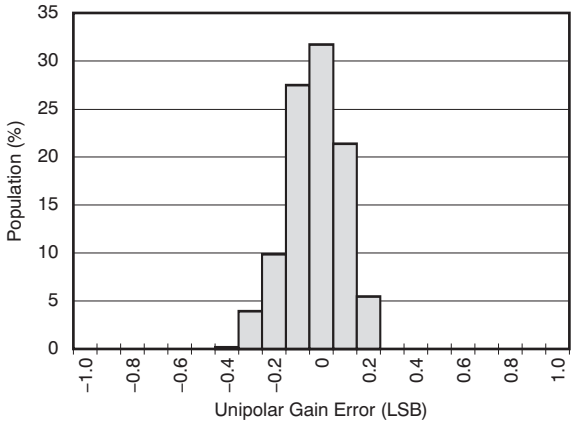


Figure 94.

UNIPOLAR GAIN ERROR HISTOGRAM

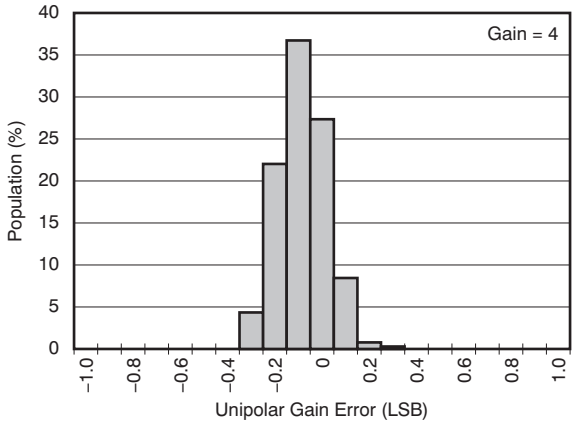


Figure 95.

ANALOG POWER-SUPPLY CURRENT HISTOGRAM

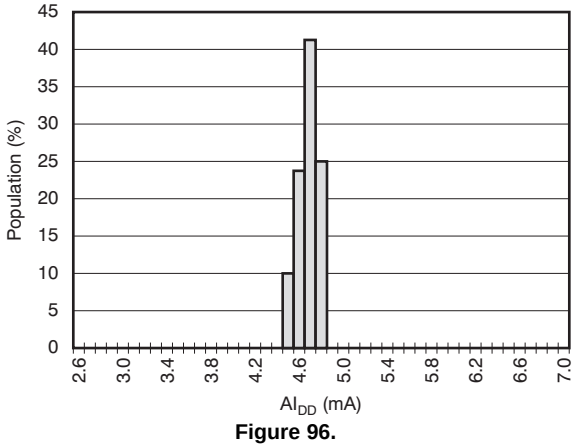


Figure 96.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC7718 contains eight DAC channels and eight output amplifiers in a single package. Each channel consists of a resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each with a value of R, from REF-x to AGND, as shown in Figure 97. This type of architecture provides DAC monotonicity. The 12-bit binary digital code loaded to the DAC latch determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage by a gain of six or four. Using a gain of 6 and power supplies allowing for at least 0.5V headroom, the output span is 9V with a 1.5V reference, 18V with a 3V reference, and 30V with a 5V reference.

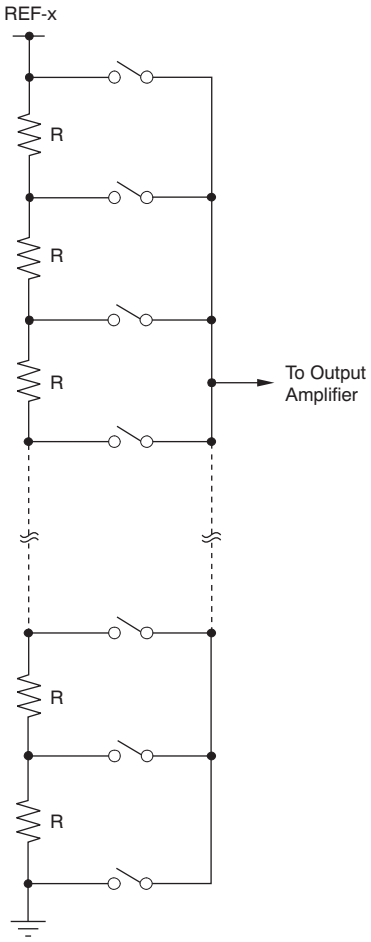


Figure 97. Resistor String

CHANNEL GROUPS

The eight DAC channels and two Offset DACs are arranged into two groups (A and B) with four channels and one Offset DAC per group. Group A consists of DAC-0, DAC-1, DAC-2, DAC-3, and Offset DAC-A. Group B consists of DAC-4, DAC-5, DAC-6, DAC-7, and Offset DAC-B. Group A derives its reference voltage from REF-A, and Group B derives its reference voltage from REF-B.

USER-CALIBRATION FOR ZERO-CODE ERROR AND GAIN ERROR

The DAC7718 implements a digital user-calibration function that allows for trimming gain and zero errors on the entire signal chain. This function can eliminate the need for external adjustment circuits. Each DAC channel has a Zero Register and Gain Register. Using the correction engine, the data from the Input Data Register are operated on by a digital adder and multiplier controlled by the contents of the Zero and Gain registers, respectively. The calibrated DAC data are then stored in the DAC Data Register where they are finally transferred into the DAC latch and set the DAC output. Each time the data are written to the Input Data Register (or to the Gain or Zero registers), the data in the Input Data Register are corrected, and the results automatically transferred to the DAC Data Register.

The range of the gain adjustment coefficient is 0.5 to 1.5. The range of the zero adjustment is –2048 LSB to +2047 LSB, or ±50% of full scale.

There is only one correction engine in the DAC7718, which is shared among all channels.

If the user-calibration function is not needed, the correction engine can be turned off. Setting the SCE bit in the Configuration Register to '0' turns off the correction engine. Setting SCE to '1' enables the correction engine. When SCE = '0', the data are directly transferred to the DAC Data Register. In this case, writing to the Gain Register or Zero Register updates the Gain and Zero registers but does not start a math engine calculation. Reading these registers returns the written values.

ANALOG OUTPUTS (V_{OUT}-0 to V_{OUT}-7, with reference to the ground of REF-x)

When the correction engine is off (SCE = '0'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{INPUT\_CODE}{4096} \right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{4096} \right) \quad (1)$$

When the correction engine is on (SCE = '1'):

$$V_{OUT} = V_{REF} \times Gain \times \left(\frac{DAC\_DATA\_CODE}{4096} \right) - V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{4096} \right) \quad (2)$$

Where:

$$DAC\_DATA\_CODE = \left(\frac{INPUT\_CODE \times (USER\_GAIN + 2^{11})}{2^{12}} \right) + USER\_ZERO$$

Gain = the DAC gain defined by the GAIN bit in the Configuration Register.

INPUT_CODE = data written into the Input Data Register (SCE = '1') or DAC Data Register (SCE = '0').

OFFSETDAC_CODE = the data written into the Offset DAC Register.

USER_GAIN = the code of the Gain Register.

USER_ZERO = the code of the Zero Register.

For single-supply operation, the OFFSET-A pin must be connected to the AGND-A pin and the OFFSET-B pin must be connected to the AGND-B pin through low-impedance connections (see the *Layout* section for details). Offset DAC-A and Offset DAC-B are in a power-down state.

For dual-supply operation, the OFFSET-A and OFFSET-B default codes for a gain of 6 are 2458 with a ±1 LSB variation, depending on the linearity of the Offset DACs. The default code for a gain of 4 is 2731 with a ±1 LSB variation. The default codes of OFFSET-A and OFFSET-B are independently factory trimmed for both gains of 6 and 4.

The power-on default value of the Gain Register is 2048, and the default value of the Zero Register is '0'. The DAC input registers are set to a default value of 000h.

Note that the maximum output voltage must not be greater than (AV_{DD} – 0.5V) and the minimum output voltage must not be less than (AV_{SS} + 0.5V); otherwise, the output may be saturated.

INPUT DATA FORMAT

The $\overline{USB}$/BTC pin defines the input data format and the Offset DAC format. When this pin is connected to DGND, the Input DAC data and Offset DAC data are straight binary, as shown in Table 1 and Table 3. When this pin is connected to IOV_{DD}, the Input DAC data and Offset DAC data are in twos complement format, as shown in Table 2 and Table 4.

Table 1. Bipolar Output vs Straight Binary Code Using Dual Power Supplies with Gain = 6

USB CODE	NOMINAL OUTPUT	DESCRIPTION
FFFh	+3 × V_{REF} × (2047/2048)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
801h	+3 × V_{REF} × (1/2048)	+1 LSB
800h	0	Zero
7FFh	–3 × V_{REF} × (1/2048)	–1 LSB
••• •••	••• •••	••• •••
000h	–3 × V_{REF} × (2048/2048)	–Full-Scale

Table 2. Bipolar Output vs Twos Complement Code Using Dual Power Supplies with Gain = 6

BTC CODE	NOMINAL OUTPUT	DESCRIPTION
7FFh	+3 × V_{REF} × (2047/2048)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
001h	+3 × V_{REF} × (1/2048)	+1 LSB
000h	0	Zero
FFFh	–3 × V_{REF} × (1/2048)	–1 LSB
••• •••	••• •••	••• •••
800h	–3 × V_{REF} × (2048/2048)	–Full-Scale

Table 3. Unipolar Output vs Straight Binary Code Using Single Power Supply with Gain = 6

USB CODE	NOMINAL OUTPUT	DESCRIPTION
FFFh	+6 × V_{REF} × (4095/4096)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
801h	+6 × V_{REF} × (2049/4096)	Midscale + 1 LSB
800h	+6 × V_{REF} × (2048/4096)	Midscale
7FFh	+6 × V_{REF} × (2047/4096)	Midscale – 1 LSB
••• •••	••• •••	••• •••
000h	0	0

Table 4. Unipolar Output vs Twos Complement Code Using Single Power Supply with Gain = 6

BTC CODE	NOMINAL OUTPUT	DESCRIPTION
7FFh	+6 × V_{REF} × (4095/4096)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
001h	+6 × V_{REF} × (2049/4096)	Midscale + 1 LSB
000h	+6 × V_{REF} × (2048/4096)	Midscale
FFFh	+6 × V_{REF} × (2047/4096)	Midscale – 1 LSB
••• •••	••• •••	••• •••
800h	0	0

The data written to the Gain Register are always in straight binary, data to the Zero Register are in twos complement, and data to all other control registers are as specified in the definitions, regardless of the $\overline{USB}$/BTC pin status.

In reading operation, the read-back data are in the same format as written.

OFFSET DACS

There are two 12-bit Offset DACs: one for Group A, and one for Group B. The Offset DACs allow the entire output curve of the associated DAC groups to be shifted by introducing a programmable offset. This offset allows for asymmetric bipolar operation of the DACs or unipolar operation with bipolar supplies. Thus, subject to the limitations of headroom, it is possible to set the output range of Group A and/or Group B to be unipolar positive, unipolar negative, symmetrical bipolar, or asymmetrical bipolar, as shown in Table 5 and Table 6. Increasing the digital input codes for the offset DAC shifts the outputs of the associated channels in the negative direction. The default codes for the Offset DACs in the DAC7718 are factory trimmed to provide optimal offset and gain performance for the default output range and span of symmetric bipolar operation. When the output range is adjusted by changing the value of the Offset DAC, an extra offset is introduced as a result of the linearity and offset errors of the Offset DAC. Therefore, the actual shift in the output span may vary slightly from the ideal calculations. For optimal offset and gain performance in the default symmetric bipolar operation, the Offset DAC input codes should not be changed from the default power-on values. The maximum allowable offset depends on the reference and the power supply. If INPUT_CODE from Equation 1 or DAC_DATA_CODE from Equation 2 is set to 0, then these equations simplify to Equation 3:

$$V_{OUT} = -V_{REF} \times (Gain - 1) \times \left(\frac{OFFSETDAC\_CODE}{4096} \right) \quad (3)$$

This equation shows the transfer function of the Offset DAC to the output of the DAC channels. In any case, the analog output must not go beyond the specified range shown in the *Analog Outputs* section. After power-on or reset, the Offset DAC is set to the value defined by the selected data format and the selected analog output voltage. If the DAC gain setting is changed, the offset DAC code is reset to the default value corresponding to the new DAC gain setting. Refer to the *Power-On Reset* and *Hardware Reset* sections for details.

For single-supply operation (AV_{SS} = 0V), the Offset DAC is turned off, and the output amplifier is in a Hi-Z state. The OFFSET-x pin must be connected to the AGND-x pin through a low-impedance connection (see the *Layout* section for details). For dual-supply operation, this pin provides the output of the Offset DAC. The OFFSET-x pin is not intended to drive an external load. See Figure 98 for the internal Offset DAC and output amplifier configuration.

Table 5. Example of Offset DAC Codes and Output Ranges with Gain = 6 and V_{REF} = 5V

OFFSET DAC CODE	OFFSET DAC VOLTAGE	DAC CHANNELS MFS(1) VOLTAGE	DAC CHANNELS PFS(1) VOLTAGE
99Ah(2)	3.0V	–15V	+15V – 1 LSB
000h	0V	0V	+30V – 1 LSB
FFFh	~5.0V	–25V	+5V – 1 LSB
666h	~2.0V	–10V	+20V – 1 LSB
CCDh	~4.0V	–20V	+10V – 1 LSB

(1) MFS = minus full-scale; PFS = plus full-scale.
(2) This is the default code for symmetric bipolar operation; actual codes may vary ±1 LSB. Codes are in straight binary format.

Table 6. Example of Offset DAC Codes and Output Ranges with Gain = 4 and V_{REF} = 5V

OFFSET DAC CODE	OFFSET DAC VOLTAGE	DAC CHANNELS MFS(1) VOLTAGE	DAC CHANNELS PFS(1) VOLTAGE
AABh(2)	~3.33333V	–10V	+10V – 1 LSB
000h	0V	0V	+20V – 1 LSB
FFFh	~5.0V	–15V	+5V – 1 LSB
555h	~1.666V	–5V	+15V – 1 LSB
800h	2.5V	–7.5V	+12.5V – 1 LSB
D55h	~4.1666V	–12.5V	+7.5V – 1 LSB

(1) MFS = minus full-scale; PFS = plus full-scale.
(2) This is the default code for symmetric bipolar operation; actual codes may vary ±1 LSB. Codes are in straight binary format.

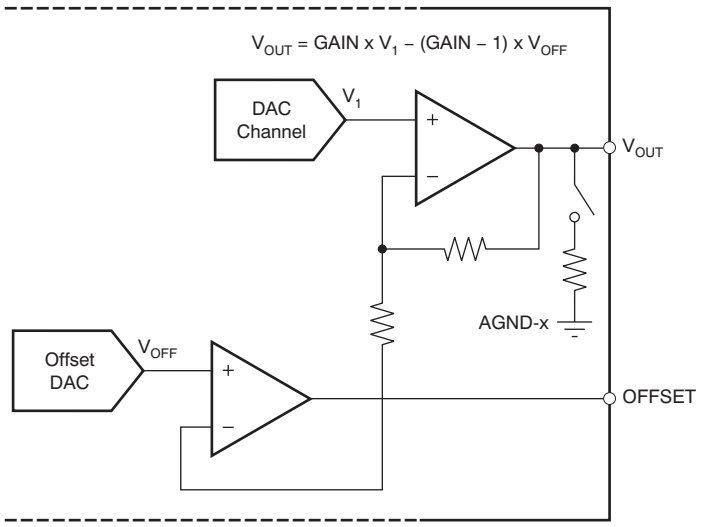


Figure 98. Output Amplifier and Offset DAC

OUTPUT AMPLIFIERS

The output amplifiers can swing to 0.5V below the positive supply and 0.5V above the negative supply. This condition limits how much the output can be offset for a given reference voltage. The maximum range of the output for ±17V power and a +5.5V reference is –16.5V to +16.5V for gain = 6.

Each output amplifier is implemented with individual over-current protection. The amplifier is clamped at 8mA, even if the output current goes over 8mA.

GENERAL-PURPOSE INPUT/OUTPUT PINS (GPIO-0 to GPIO-2)

The GPIO pins are general-purpose, bidirectional, digital input/outputs, as shown in Figure 99. When a GPIO pin acts as an output, the pin status is determined by the corresponding GPIO bit in the GPIO Register. The pin output is high-impedance when the GPIO bit is set to '1', and is logic low when the GPIO bit is cleared to '0'. Note that a pull-up resistor to IOV_{DD} is required when using a GPIO pin as an output. When a GPIO pin acts as an input, the digital value on the pin is acquired by reading the corresponding GPIO bit. After power-on reset, or any forced hardware or software reset, the GPIO bits are set to '1', and the GPIO pins are in a high-impedance state. If not used, the GPIO pins must be tied to either DGND or to IOV_{DD} through a pull-up resistor. Leaving the GPIO pins floating can cause high IOV_{DD} supply currents.

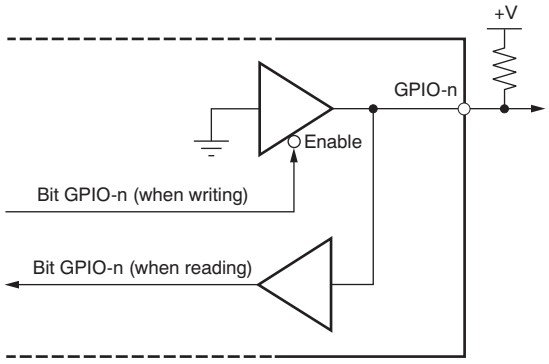


Figure 99. GPIO-n Pin

ANALOG OUTPUT PIN ($\overline{CLR}$)

The $\overline{CLR}$ pin is an active low input that should be high for normal operation. When this pin is in logic '0', all V_{OUT} outputs connect to AGND-x through internal 15kΩ resistors and are cleared to 0V, and the output buffer is in a Hi-Z state. While $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is taken high again while the $\overline{LDAC}$ is high, the DAC outputs remain cleared until $\overline{LDAC}$ is taken low. However, if $\overline{LDAC}$ is tied low, taking $\overline{CLR}$ back to high sets the DAC output to the level defined by the value of the DAC latch. The contents of the Zero Registers, Gain Registers, Input Data Registers, DAC Data Registers, and DAC latches are not affected by taking $\overline{CLR}$ low.

POWER-ON RESET

The DAC7718 contains a power-on reset circuit that controls the output during power-on and power down. This feature is useful in applications where the known state of the DAC output during power-on is important. The Offset DAC Registers, DAC Data Registers, and DAC latches are loaded with the value defined by the RSTSEL pin, as shown in Table 7. The Gain Registers and Zero Registers are loaded with default values. The Input Data Register is reset to 000h, independent of the RSTSEL state.

Table 7. Bipolar Output Reset Values for Dual Power-Supply Operation

RSTSEL PIN	$\overline{USB}$/BTC PIN	INPUT FORMAT	VALUE OF DAC DATA REGISTER AND DAC LATCH	VALUE OF OFFSET DAC REGISTER FOR GAIN = 6 (1)	V_{OUT}
DGND	DGND	Straight Binary	000h	99Ah	–Full-Scale
IOV_{DD}	DGND	Straight Binary	800h	99Ah	0 V
DGND	IOV_{DD}	Twos Complement	800h	19Ah	–Full-Scale
IOV_{DD}	IOV_{DD}	Twos Complement	000h	19Ah	0 V

(1) Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±1 LSB from the nominal number listed in this table.

In single-supply operation, the Offset DAC is turned off and the output is unipolar. The power-on reset is defined as shown in Table 8.

Table 8. Unipolar Output Reset Values for Single Power-Supply Operation

RSTSEL PIN	$\overline{USB}$/BTC PIN	INPUT FORMAT	VALUE OF DAC DATA REGISTER AND DAC LATCH	V_{OUT}
DGND	DGND	Straight Binary	000h	0 V
IOV_{DD}	DGND	Straight Binary	800h	Midscale
DGND	IOV_{DD}	Twos Complement	800h	0 V
IOV_{DD}	IOV_{DD}	Twos Complement	000h	Midscale

HARDWARE RESET

When the $\overline{RST}$ pin is low, the device is in hardware reset. All the analog outputs (V_{OUT}-0 to V_{OUT}-7), the DAC registers, and the DAC latches are set to the reset values defined by the RSTSEL pin as shown in Table 7 and Table 8. In addition, the Gain and Zero Registers are loaded with default values, communication is disabled, and the signals on $\overline{CS}$ and SDI are ignored (note that SDO is in a high-impedance state). The Input Data Register is reset to 000h, independent of the RSTSEL state. On the rising edge of $\overline{RST}$, the analog outputs (V_{OUT}-0 to V_{OUT}-7) maintain the reset value as defined by the RSTSEL pin until a new value is programmed. After $\overline{RST}$ goes high, the serial interface returns to normal operation. $\overline{CS}$ must be set to a logic high whenever $\overline{RST}$ is used.

UPDATING THE DAC OUTPUTS

Depending on the status of both $\overline{CS}$ and $\overline{LDAC}$, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode. This update mode is established at power-on. If asynchronous mode is desired, the $\overline{LDAC}$ pin must be permanently tied low before power is applied to the device. If synchronous mode is desired, $\overline{LDAC}$ must be logic high before and during power-on.

The DAC7718 updates a DAC latch only if it has been accessed since the last time $\overline{LDAC}$ was brought low or if the LD bit is set to '1', thereby eliminating any unnecessary glitch. Any DAC channels that were not accessed are not loaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

Asynchronous Mode

In this mode, the $\overline{LDAC}$ pin is set low at power-up. This action places the DAC7718 into Asynchronous mode, and the LD bit and $\overline{LDAC}$ signal are ignored. When the correction engine is off (SCE bit = '0'), the DAC Data Registers and DAC latches are updated immediately when $\overline{CS}$ goes high. When the correction engine is on (SCE bit = '1'), each DAC latch is updated individually when the correction engine updates the corresponding DAC Data Register.

Synchronous Mode

To use this mode, set $\overline{LDAC}$ high before $\overline{CS}$ goes low, and then take $\overline{LDAC}$ low or set the LD bit to '1' after $\overline{CS}$ goes high. If $\overline{LDAC}$ goes low or if the LD bit is set to '1' when SCE = '0', all DAC latches are updated simultaneously. If $\overline{LDAC}$ goes low or if the LD bit is set to '1' when SCE = '1', all DAC latches are updated simultaneously after the correction engine has updated the corresponding DAC register.

In this mode, when $\overline{LDAC}$ stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking $\overline{LDAC}$ low (or by setting the LD bit in the Configuration Register to '1') any time after the delay of t_9 from the rising edge of $\overline{CS}$. If the timing requirement of t_9 is not satisfied, invalid data are loaded. Refer to the *Timing Diagrams* and the Configuration Register (Table 11) for details.

MONITOR OUTPUT PIN (V_{MON})

The V_{MON} pin is the channel monitor output. It can be either high-impedance or monitor any one of the DAC outputs, auxiliary analog inputs, offset DAC outputs, or reference buffer outputs. The channel monitor function consists of an analog multiplexer addressed via the serial interface, allowing any channel output, reference buffer output, auxiliary analog inputs, or offset DAC output to be routed to the V_{MON} pin for monitoring using an external ADC. The monitor function is controlled by the Monitor Register, which allows the monitor output to be enabled or disabled. When disabled, the monitor output is high-impedance; therefore, several monitor outputs may be connected in parallel with only one enabled at a time.

Note that the multiplexer is implemented as a series of analog switches. Care should be taken to ensure the maximum current from the V_{MON} pin must not be greater than the given specification because this could conceivably cause a large amount of current to flow from the input of the multiplexer (that is, from V_{OUT}-X) to the output of the multiplexer (V_{MON}). Refer to the *Monitor Register* section and Table 12 for more details.

ANALOG INPUT PINS (AIN-0 and AIN-1)

Pins AIN-0 and AIN-1 are two analog inputs that directly connect to the analog mux of the analog monitor output. When AIN-0 or AIN-1 is accessed, it is routed via the mux to the V_{MON} pin. Thus, one external ADC channel can monitor eight DACs plus two extra external analog signals, AIN-0 and AIN-1.

POWER-DOWN MODE

The DAC7718 is implemented with a power-down function to reduce power consumption. Either the entire device or each individual group can be put into power-down mode. If the proper power-down bit (PD-x) in the Configuration Register is set to '1', the individual group is put into power down mode. During power-down mode, the analog outputs (V_{OUT}-0 to V_{OUT}-7) connect to AGND-X through an internal 15kΩ resistor, and the output buffer is in Hi-Z status. When the entire device is in power-down, the bus interface remains active in order to continue communication and receive commands from the host controller, but all other circuits are powered down. The host controller can wake the device from power-down mode and return to normal operation by clearing the PD-x bit; it takes 200μs or less for recovery to complete.

POWER-ON RESET SEQUENCING

The DAC7718 permanently latches the status of some of the digital pins at power-on. These digital levels should be well-defined before or while the digital supply voltages are applied. Therefore, it is advised to have a pull up resistor to IOV_{DD} for the digital initialization pins (LDAC, CLR, RST, CS, and RSTSEL) to ensure that these levels are set correctly while the digital supplies are raised.

For proper power-on initialization of the device, IOV_{DD} and the digital pins must be applied before or at the same time as DV_{DD}. If possible, it is preferred that IOV_{DD} and DV_{DD} can be connected together in order to simplify the supply sequencing requirements. Pull-up resistors should go to either supply. AV_{DD} should be applied after the digital supplies (IOV_{DD} and DV_{DD}) and digital initialization pins (LDAC, CLR, RST, CS, and RSTSEL). AV_{SS} can be applied at the same time as or after AV_{DD}. The REF-x pins must be applied last.

SERIAL INTERFACE

The DAC7718 is controlled over a versatile, three-wire serial interface that operates at clock rates of up to 50MHz and is compatible with SPI, QSPI™, Microwire™, and DSP™ standards.

SPI Shift Register

The SPI Shift Register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The SPI Shift Register consists of a read/write bit, five register address bits, 12 data bits, and six reserve bits for future devices, as shown in Table 9. The falling edge of $\overline{CS}$ starts the communication cycle. The data are latched into the SPI Shift Register on the falling edge of SCLK while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a high-impedance state. The contents of the SPI shifter register are decoded and transferred to the proper internal registers on the rising edge of $\overline{CS}$. The timing for this operation is shown in the *Timing Diagrams* section.

The serial interface works with both a continuous and non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

The serial interface requires $\overline{CS}$ to be logic high during the power-on sequencing; therefore, it is advised to have a pullup resistor to IOV_{DD} on the $\overline{CS}$ pin. Refer to the *Power-On Reset Sequencing* section for further details.

Stand-Alone Operation

The serial clock can be a continuous or a gated clock. The first falling edge of $\overline{CS}$ starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought back high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, then the data written are not transferred into the internal registers. If more than 24 falling SCLK edges are applied before $\overline{CS}$ is brought high, then the last 24 bits are used. The device internal registers are updated from the Shift Register on the rising edge of $\overline{CS}$. In order for another serial transfer to take place, $\overline{CS}$ must be brought low again.

When the data have been transferred into the chosen register of the addressed DAC, all DAC latches and analog outputs can be updated by taking $\overline{LDAC}$ low.

Daisy-Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together. Daisy-chain operation can be useful in system diagnostics and in reducing the number of serial interface lines. Note that before daisy-chain operation can begin, the SDO pin must be enabled by setting the SDO disable bit (DSDO) in the Configuration Register to '0'; this bit is cleared by default.

The DAC7718 provides two modes for daisy-chain operation: normal and sleep. The SLEEP bit in the SPI Mode register determines which mode is used.

In Normal mode (SLEEP bit = '0'), the data clocked into the SDI pin are transferred into the Shift Register. The first falling edge of $\overline{CS}$ starts the operating cycle. SCLK is continuously applied to the SPI Shift Register when $\overline{CS}$ is low. If more than 24 clock pulses are applied, the data ripple out of the Shift Register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO pin of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where *N* is the total number of DAC7718s in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action latches the data from the SPI Shift Registers to the device internal registers for each device in the daisy-chain, and prevents any further data from being clocked in. The serial clock can be a continuous or a gated clock. Note that a continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. For gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

In Sleep mode (SLEEP bit = '1'), the data clocked into SDI are routed to the SDO pin directly; the Shift Register is bypassed. The first falling edge of $\overline{CS}$ starts the operating cycle. When SCLK is continuously applied with $\overline{CS}$ low, the data clocked into the SDI pin appear on the SDO pin almost immediately (with approximately a 5 ns delay; see the *Timing Diagrams* section); there is no 24 clock delay, as there is in normal operting mode. While in Sleep mode, no data bits are clocked into the Shift Register, and the device does not receive any new data or commands. Putting the device into Sleep mode eliminates the 24 clock delay from SDI to SDO caused by the

Shift Register, thus greatly speeding up the data transfer. For example, consider three DAC7718s (A, B, and C) in a daisy-chain configuration. The data from the SPI controller are transferred first to A, then to B, and finally to C. In normal daisy-chain operation, a total of 72 clocks are needed to transfer one word to C. However, if A and B are placed into Sleep mode, the first 24 data bits are directly transferred to C (through A and B); therefore, only 24 clocks are needed.

To wake the device up from sleep mode and return to normal operation, either one of following methods can be used:

1. Pull the $\overline{\text{WAKEUP}}$ pin low, which forces the SLEEP bit to '0' and returns the device to normal operating mode.
2. Use the W2 bit and the $\overline{\text{CS}}$ pin.

When the W2 bit = '1', if $\overline{\text{CS}}$ is applied with no more than one falling edge of SCLK, then the rising edge of $\overline{\text{CS}}$ wakes the device from sleep mode back to normal operation. However, the device will not wake-up if more than one falling edge of SCLK exists while $\overline{\text{CS}}$ is low.

Read-Back Operation

The READ command is used to start read-back operation. However, before read-back operation can be initiated, the SDO pin must be enabled by setting the DSDO bit in the Configuration Register to '0'; this bit is cleared by default. Read-back operation is then started by executing a READ command (R/W bit = '1', see Table 9). Bits A4 to A0 in the READ command select the register to be read. The remaining data in the command are *don't care* bits. During the next SPI operation, the data appearing on the SDO output are from the previously addressed register. For a read of a single register, a NOP command can be used to clock out the data from the selected register on SDO. Multiple registers can be read if multiple READ commands are issued. The readback diagram in Figure 100 shows the read-back sequence.

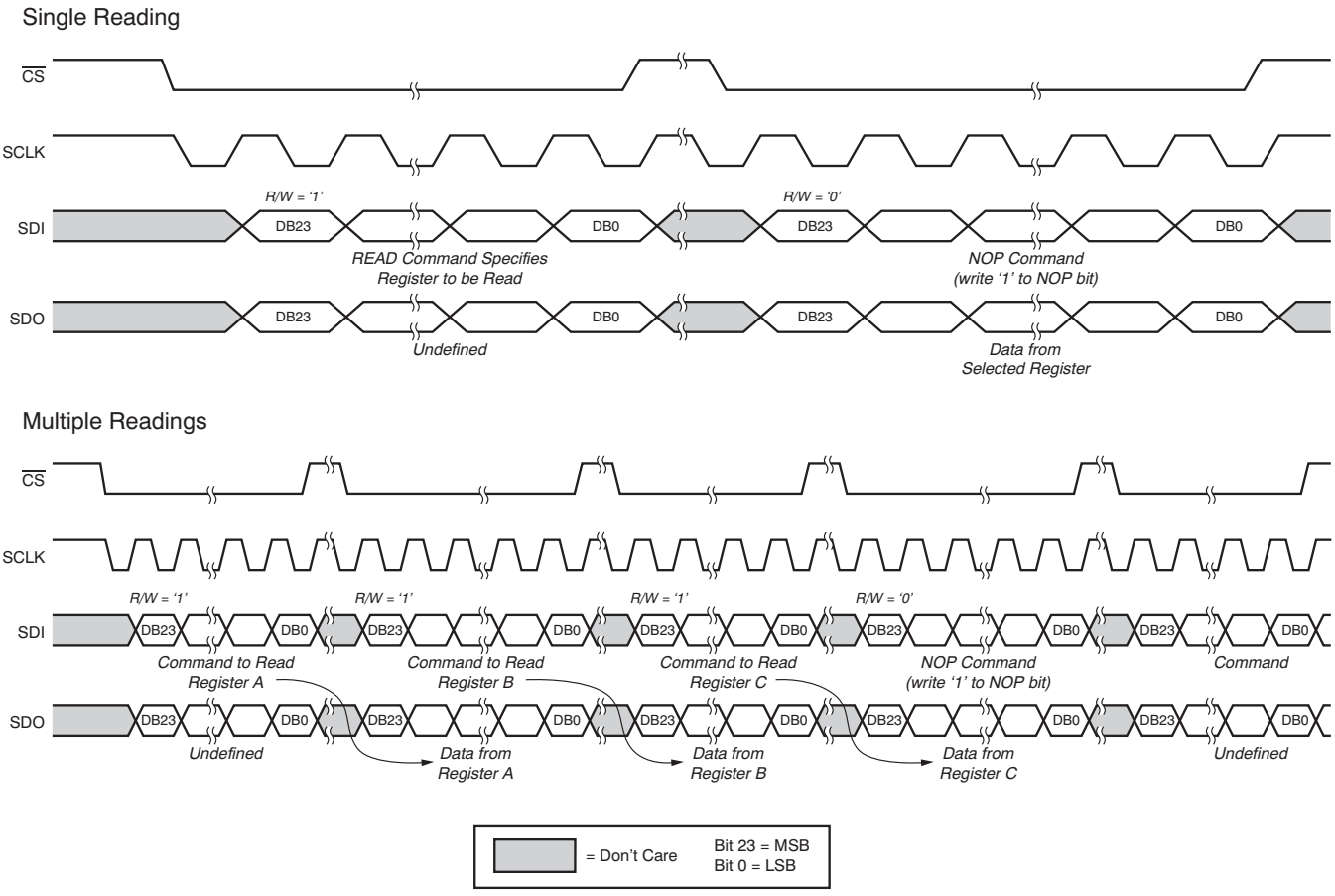


Figure 100. Read-Back Operation

SPI SHIFT REGISTER

The SPI Shift Register is 24 bits wide, as shown in Table 9. The register mapping is shown in Table 10; X = don't care—writing to it has no effect, reading it returns '0'.

Table 9. Shift Register Format

MSB									
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15:DB4	DB3:DB0
R/W	X	X	A4	A3	A2	A1	A0	DATA	X

R/W Indicates a read from or a write to the addressed register.

R/W = '0' sets a write operation and the data are written to the specified register.

R/W = '1' sets a read-back operation. Bits A4 to A0 select the register to be read. The remaining bits are *don't care* bits. During the next SPI operation, the data appearing on SDO pin are from the previously addressed register.

A4:A0 Address bits that specify which register is accessed.

DATA 12 data bits

Table 10. Register Map

ADDRESS BITS					DATA BITS													REGISTER
A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3:D0	
0	0	0	0	0	A/B	LD	RST	PD-A	PD-B	SCE	X	GAIN-A	GAIN-B	DSDO	NOP	W2	X(1)	Configuration Register
0	0	0	0	1	Analog Monitor Select												X(1)	Monitor Register
0	0	0	1	0	GPIO-2	GPIO-1	GPIO-0	X(1)										GPIO Register
0	0	0	1	1	OS11:OS0, X, X, X, X(2)													Offset DAC-A Data
0	0	1	0	0	OS11:OS0, X, X, X, X(2)													Offset DAC-B Data
0	0	1	0	1	Reserved(3)													Reserved
0	0	1	1	0	SLEEP	Reserved(3)												SPI MODE
0	0	1	1	1	DB11:DB0, X, X, X, X													Broadcast
0	1	0	0	0	DB11:DB0, X, X, X, X													DAC-0
0	1	0	0	1	DB11:DB0, X, X, X, X													DAC-1
0	1	0	1	0	DB11:DB0, X, X, X, X													DAC-2
0	1	0	1	1	DB11:DB0, X, X, X, X													DAC-3
0	1	1	0	0	DB11:DB0, X, X, X, X													DAC-4
0	1	1	0	1	DB11:DB0, X, X, X, X													DAC-5
0	1	1	1	0	DB11:DB0, X, X, X, X													DAC-6
0	1	1	1	1	DB11:DB0, X, X, X, X													DAC-7
1	0	0	0	0	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-0
1	1	0	0	0	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-0
1	0	0	0	1	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-1
1	1	0	0	1	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-1
1	0	0	1	0	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-2
1	1	0	1	0	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-2
1	0	0	1	1	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-3
1	1	0	1	1	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-3
1	0	1	0	0	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-4
1	1	1	0	0	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-4
1	0	1	0	1	Z1:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-5
1	1	1	0	1	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-5
1	0	1	1	0	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-6
1	1	1	1	0	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-6
1	0	1	1	1	Z11:Z0, X, X, X, X, default = 0 (000h), twos complement													Zero Register-7
1	1	1	1	1	G11:G0, X, X, X, X, default = 2048 (800h), straight binary													Gain Register-7

(1) X = don't care—writing to this bit has no effect; reading the bit returns '0'.
(2) Table 7 lists the default values for a dual power supply. Offset DAC A and Offset DAC B are trimmed in manufacturing to minimize the error for symmetrical output. The default value may vary no more than ±1 LSB from the nominal number listed in Table 7. For a single power supply, the Offset DACs are turned off.
(3) Writing to a reserved bit has no effect; reading the bit returns '0'.

INTERNAL REGISTERS

The DAC7718 internal registers consist of the Configuration Register, the Monitor Register, the DAC Input Data Registers, the Zero Registers, the DAC Data Registers, and the Gain Registers, and are described in the following section.

The Configuration Register specifies which actions are performed by the device. Table 11 shows the details.

Table 11. Configuration Register (Default = 800h)

BIT	NAME	DEFAULT VALUE	DESCRIPTION
D15	A/B	1	A/B bit. When A/B = '0', reading DAC-x returns the value in the Input Data Register. When A/B = '1', reading DAC-x returns the value in the DAC Data Register. When the correction engine is enabled, the data returned from the Input Data Register is the original data written to the bus, and the value in the DAC Data Register is the corrected data.
D14	LD	0	Synchronously update DACs bit. When $\overline{\text{LDAC}}$ is tied high, setting LD = '1' at any time after the write operation and the correction process complete synchronously updates all DAC latches with the content of the corresponding DAC Data Register, and sets V_{OUT} to a new level. The DAC7718 updates the DAC latch only if it has been accessed since the last time $\overline{\text{LDAC}}$ was brought low or the LD bit was set to '1', thereby eliminating unnecessary glitch. Any DACs that were not accessed are not reloaded. After updating, the bit returns to '0'. When the correction engine is turned off, bit LD can be set to '1' any time after the writing operation is complete; the DAC latch is immediately updated when bit LD is set. When the $\overline{\text{LDAC}}$ pin is tied low, this bit is ignored.
D13	RST	0	Software reset bit. Set the RST bit to '1' to reset the device; functions the same as a hardware reset. After reset completes, the RST bit returns to '0'.
D12	PD-A	0	Power-down bit for Group A (DAC-0, DAC-1, DAC-2, and DAC-3). Setting the PD-A bit to '1' places Group A (DAC-0, DAC-1, DAC-2, and DAC-3) into power-down operation. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-X) connect to AGND-A through an internal 15-kΩ resistor. The interface is still active. Setting the PD-A bit to '0' returns group A to normal operation.
D11	PD-B	0	Power-down bit for Group B (DAC-4, DAC-5, DAC-6, and DAC-7). Setting the PD-B bit to '1' places Group B (DAC-4, DAC-5, DAC-6, and DAC-7) into power-down operation. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-X) connect to AGND-B through an internal 15-kΩ resistor. The interface is still active. Setting the PD-B bit to '0' returns group B to normal operation.
D10	SCE	0	System-calibration enable bit. Set the SCE bit to '1' to enable the correction engine. When the engine is enabled, the input data are adjusted by the correction engine according to the contents of the corresponding Gain Register and Zero Register. The results are transferred to the corresponding DAC Data Register, and finally loaded into the DAC latch, which sets the V_{OUT}-x pin output level. Set the SCE bit to '0' to turn off the correction engine. When the engine is turned off, the input data are transferred to the corresponding DAC Data Register immediately, and then loaded into the DAC latch, which sets the output voltage. Refer to the *User Calibration for Zero-Code Error and Gain Error* section for details.
D9	—	0	Reserved. Writing to this bit has no effect; reading this bit returns '0'.
D8	GAIN-A	0	Gain bit for Group A (DAC-0, DAC-1, DAC-2, and DAC-3). Updating this bit to a new value automatically resets the Offset DAC-A Register to the factory-trimmed value for the new gain setting. Set the GAIN-A bit to '0' for an output span = 6 × REF-A. Set the GAIN-A bit to '1' for an output span = 4 × REF-A.
D7	GAIN-B	0	Gain bit for Group B (DAC-4, DAC-5, DAC-6, and DAC-7). Updating this bit to a new value automatically resets the Offset DAC-B Register to the factory-trimmed value for the new gain setting. Set the GAIN-B bit to '0' for an output span = 6 × REF-B. Set the GAIN-B bit to '1' for an output span = 4 × REF-B.
D6	DSDO	0	Disable SDO bit. Set the DSDO bit to '0' to enable the SDO pin (default). The SDO pin works as a normal SPI output. Set the DSDO bit to '1' to disable the SDO pin. The SDO pin is always in a Hi-Z state no matter what the status of the $\overline{\text{CS}}$ pin is.
D5	NOP	0	No operation bit. During a write operation, setting the NOP bit to '1' has no effect (the bit returns to '0' when the write operation completes). Setting the NOP bit to '0', returns the device to normal operation. During a read operation, the bit always returns “0”
D4	W2	0	Second wake-up operation bit. If the $\overline{\text{WAKEUP}}$ pin is high, an alternative method to wake-up the device from sleep in SPI is by using the $\overline{\text{CS}}$ pin. When W2 = '1', the rising edge of $\overline{\text{CS}}$ restores the device from sleep mode to normal operation, if no more than one falling edge of SCLK exists while $\overline{\text{CS}}$ is low. However, the device will not wake up if more than one falling edge of SCLK exists. Setting the W2 bit to '0' disables this function, and the rising edge of $\overline{\text{CS}}$ does not wake up the device. If the $\overline{\text{WAKEUP}}$ is low, this bit is ignored and the device is always in normal mode.
D3:D0	—	0	Reserved. Writing to these bits has no effect; reading these bits returns '0'.

Monitor Register (default = 000h).

The Monitor Register selects one of the DAC outputs, auxiliary analog inputs, reference buffer outputs, or offset DAC outputs to be monitored through the V_{MON} pin. When bits [D15:D4] = '0', the monitor is disabled and V_{MON} is in a Hi-Z state.

Note that if any value is written other than those specified in Table 12, the Monitor Register stores the invalid value; however, the V_{MON} pin is forced into a Hi-Z state.

Table 12. Monitor Register (Default = 000h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3:D0	V_{MON} CONNECTS TO
0	0	0	0	0	0	0	0	0	0	0	1	X(1)	Reference buffer B output
0	0	0	0	0	0	0	0	0	0	1	0	X	Reference buffer A output
0	0	0	0	0	0	0	0	0	1	0	1	X	Offset DAC B output
0	0	0	0	0	0	0	0	0	1	1	0	X	Offset DAC A output
0	0	0	0	0	0	0	0	0	1	0	0	X	AIN-0
0	0	0	0	0	0	0	0	1	0	0	0	X	AIN-1
0	0	0	0	0	0	0	1	0	0	0	0	X	DAC-0
0	0	0	0	0	0	1	0	0	0	0	0	X	DAC-1
0	0	0	0	0	1	0	0	0	0	0	0	X	DAC-2
0	0	0	0	1	0	0	0	0	0	0	0	X	DAC-4
0	0	0	1	0	0	0	0	0	0	0	0	X	DAC-4
0	0	1	0	0	0	0	0	0	0	0	0	X	DAC-5
0	1	0	0	0	0	0	0	0	0	0	0	X	DAC-6
1	0	0	0	0	0	0	0	0	0	0	0	X	DAC-7
0	0	0	0	0	0	0	0	0	0	0	0	X	Monitor function disabled, Hi-Z (default)

(1) X = don't care.

GPIO Register (default = E00h).

The GPIO Register determines the status of each GPIO pin.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GPIO-2	GPIO-1	GPIO-0	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO-2:0 For write operations, the GPIO-n pin operates as an output. Writing a '1' to the GPIO-n bit sets the GPIO-n pin to high impedance, and writing a '0' sets the GPIO-n pin to logic low. An external pull-up resistor is required when using the GPIO-n pin as an output.

For read operations, the GPIO-n pin operates as an input. Read the GPIO-n bit to receive the status of the corresponding GPIO-n pin. Reading a '0' indicates that the GPIO-n pin is low, and reading a '1' indicates that the GPIO-n pin is high.

After power-on reset, or any forced hardware or software reset, all GPIO-n bits are set to '1', and the GPIO pins are in a high impedance state.

Offset DAC-A/B Registers (default = 99Ah for dual supplies or 000h for single supplies).

The Offset DAC-A and Offset DAC-B registers contain, by default, the factory-trimmed Offset DAC code providing optimal offset and span for symmetric bipolar operation when dual supplies are detected, and contain code 000h when a single supply is detected.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OS11	OS10	OS9	OS8	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	X	X	X	X

OS11:0 For dual-supply operation, the default code for a gain of 6 is 99Ah with a ±1 LSB variation, depending on the linearity of each Offset DAC. The default code for a gain of 4 is AABh with a ±1 LSB variation. The default codes of Offset DAC-A and Offset DAC-B registers are independently factory trimmed for both gains of 6 and 4.

When single-supply operation is present, writing to these registers is ignored and reading returns 000h. When dual-supply operation is present, updating the GAIN-A (GAIN-B) bit on the configuration register automatically reloads the factory-trimmed code into the Offset DAC-A (Offset DAC-B) register for the new GAIN-A (GAIN-B) setting. See the *Offset DACs* for further details.

SPI MODE Register (default = 000h).

The SPI Mode Register is used to put the device into SPI sleep mode.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

SLEEP Set the SLEEP bit to '1' to put the device into SPI sleep mode.

When the SLEEP bit = '0', the SPI is in normal mode. The bit is cleared ('0') after a hardware reset (through the $\overline{\text{RST}}$ pin) or if the $\overline{\text{WAKEUP}}$ pin is low.

For normal SPI operation, the data entering the SDI pin is transferred into the Shift Register. However, for SPI sleep mode, the Shift Register is bypassed. The data entering into the SDI pin are directly transferred to the SDO pin instead of the Shift Register.

Broadcast Register.

The DAC7718 broadcast register can be used to update all eight DAC register channels simultaneously using data bits D15:D4. This write-only register uses address A4:A0 = 07h, and is only available when the SCE bit = '0' (default). If the SCE bit = '1', this register is ignored. Reading this register always returns 000h.

Input Data Register for DAC-n, where n = 0 to 7 (default = 000h).

This register stores the DAC data written to the device when the SCE bit = '1' and is controlled by the correction engine. When the SCE bit = '0' (default), the DAC Data Register stores the DAC data written to the device. When the data are loaded into the corresponding DAC latch, the DAC output changes to the new level defined by the DAC latch. The default value after power-on or reset is 000h.

Table 13. DAC-n(1) Input Data Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DB11(2)	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X	X	X

(1) n = 0, 1, 2, 3, 4, 5, 6, or 7.
(2) DB11:DB0 are the DAC data bits.

Zero Register n, where n = 0 to 7 (default = 000h).

The Zero Register stores the user-calibration data that are used to eliminate the offset error. The data are 12 bits wide, 1 LSB/step, and the total adjustment is –2048 LSB to +2047 LSB, or ±50% of full-scale range. The Zero Register uses a twos complement data format.

Table 14. Zero Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0	X	X	X	X

Z11:Z0—OFFSET BITS	ZERO ADJUSTMENT
7FFh	+2047 LSB
7FEh	+2046 LSB
••• ••• •••	••• ••• •••
001h	+1 LSB
000h	0 LSB (default)
FFFh	–1 LSB
••• ••• •••	••• ••• •••
801h	–2047 LSB
800h	–2048 LSB

Gain Register n, where n = 0 to 7 (default = 800h).

The Gain Register stores the user-calibration data that are used to eliminate the gain error. The data are 12 bits wide, 0.0015% FSR/step, and the total adjustment range 0.5 to 1.5. The Gain Register uses a straight binary data format.

Table 15. Gain Register

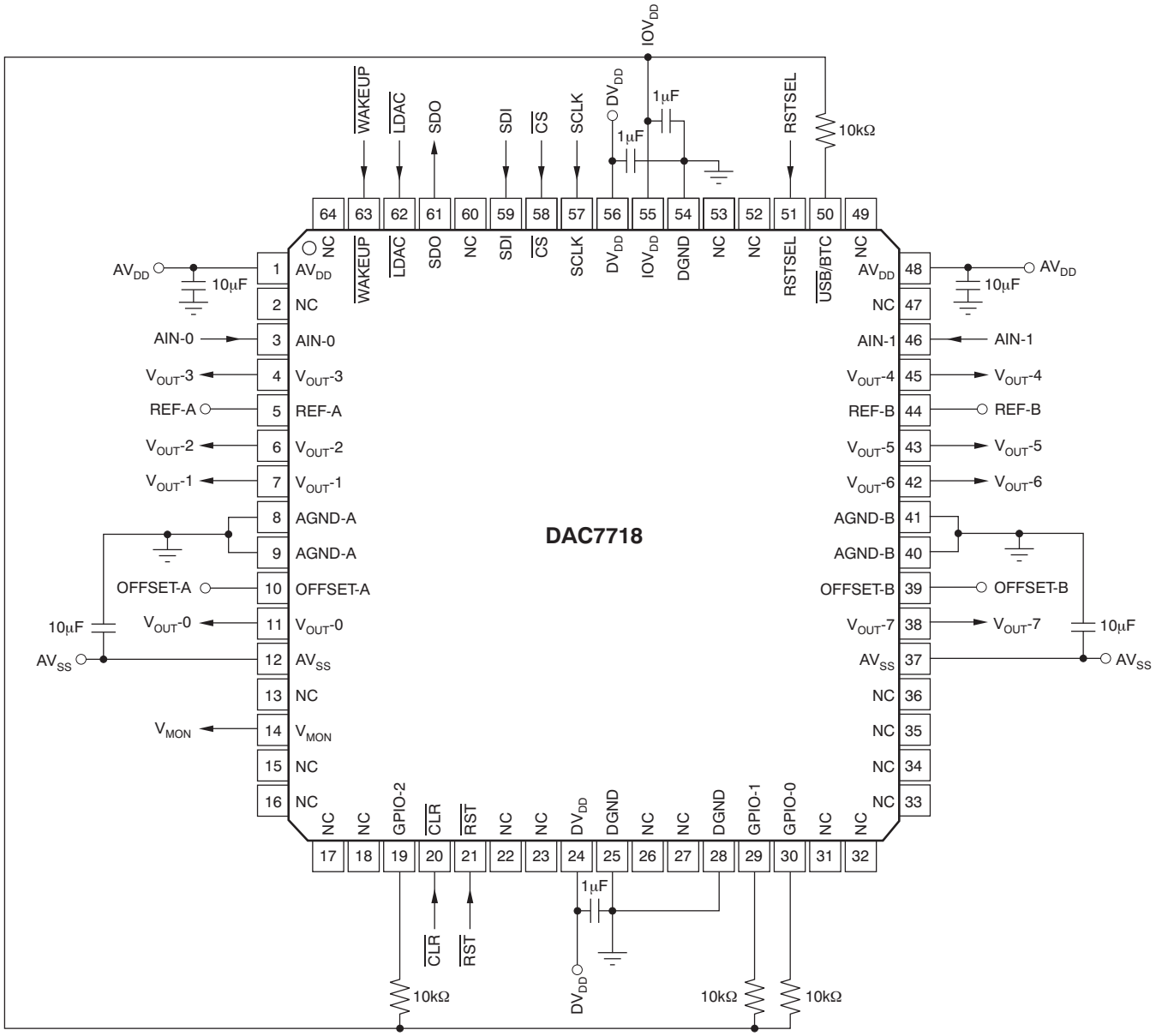
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	X	X	X	X

G11:G0—GAIN-CODE BITS	GAIN ADJUSTMENT COEFFICIENT
FFFh	1.499985
FFEh	1.499969
••• ••• •••	••• ••• •••
801h	1.000015
800h	1 (default)
7FFh	0.999985
••• ••• •••	••• ••• •••
001h	0.500015
000h	0.5

APPLICATION INFORMATION

BASIC OPERATION

The DAC7718 is a highly-integrated device with high-performance reference buffers and output buffers, greatly reducing the printed circuit board (PCB) area and production cost. On-chip reference buffers eliminate the need for a negative external reference. Figure 101 shows a basic application for the DAC7718.



NOTES: AVDD = +15V, AVSS = -15V, DVDD = +5V, IOVDD = +1.8V to +5V, REF-A = +5V, and REF-B = +2.5V.
The OFFSET-A and OFFSET-B pins must be connected to the AGND pin when used in unipolar operation.

Figure 101. Basic Application Example

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the DAC7718 over the full operating temperature range, a precision voltage reference must be used. Careful consideration should be given to the selection of a precision voltage reference. The DAC7718 has two reference inputs, REF-A and REF-B. The voltages applied to the reference inputs are used to provide a buffered positive reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device. There are four possible sources of error to consider when choosing a voltage reference for high-accuracy applications: initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise. Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight, long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime. The temperature coefficient of a reference output voltage affects the output drift when the temperature changes. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage on ambient conditions. In high-accuracy applications, which have a relatively low noise budget, the reference output voltage noise also must be considered. Choosing a reference with as low an output noise voltage as practical for the required system resolution is important. Precision voltage references such as TI's REF50xx (2V to 5V) and REF32xx (1.25V to 4V) provide a low-drift, high-accuracy reference voltage.

POWER-SUPPLY NOISE

The DAC7718 must have ample supply bypassing of 1μF to 10μF in parallel with 0.1μF on each supply, located as close to the package as possible; ideally, immediately next to the device. The 1μF to 10μF capacitors must be the tantalum-bead type. The 0.1μF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as common ceramic types, which provide a low-impedance path to ground at high frequencies to handle transient currents because of internal logic switching. The power-supply lines must be as large a trace as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Apart from these considerations, the wideband noise on the AV_{DD}, AV_{SS}, DV_{DD} and IOV_{DD} supplies should be filtered before feeding to the DAC to obtain the best possible noise performance.

LAYOUT

Precision analog circuits require careful layout, adequate bypassing, and a clean, well-regulated power supply to obtain the best possible dc and ac performance. Careful consideration of the power-supply and ground-return layout helps to meet the rated performance. DGND is the return path for digital currents and AGND is the power ground for the DAC. For the best ac performance, care should be taken to connect DGND and AGND with very low resistance back to the supply ground. The PCB must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device.

The power-supply traces must be as large as possible to provide low impedance paths and reduce the effects of glitches on the power-supply line. Fast switching signals must never be run near the reference inputs. It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This configuration reduces the effects of feedthrough on the board. A microstrip technique may be considered, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder-side.

Each DAC group has a ground pin, AGND-x, which is the ground of the output from the DACs in the group. It must be connected directly to the corresponding reference ground in low-impedance paths to get the best performance. AGND-A must be connected with REFGND-A and AGND-B must be connected with REFGND-B. AGND-A and AGND-B must be tied together and connected to the analog power ground and DGND.

During single-supply operation, the OFFSET-x pins must be connected to AGND-x with a low-impedance path because these pins carry DAC-code-dependent current. Any resistance from OFFSET-x to AGND-x causes a voltage drop by this code-dependent current. Therefore, it is very important to minimize routing resistance to AGND-x or to any ground plane that AGND-x is connected to.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DAC7718SPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 85	DAC7718S	Samples
DAC7718SPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 85	DAC7718S	Samples
DAC7718SRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7718S	Samples
DAC7718SRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7718S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

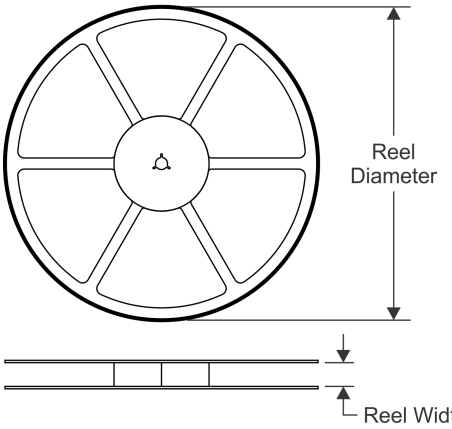
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

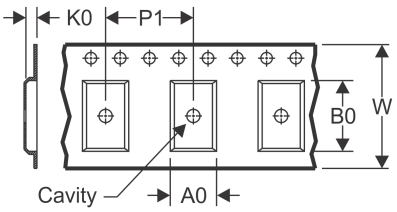
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

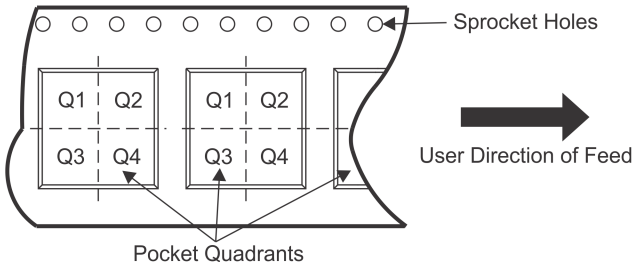


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

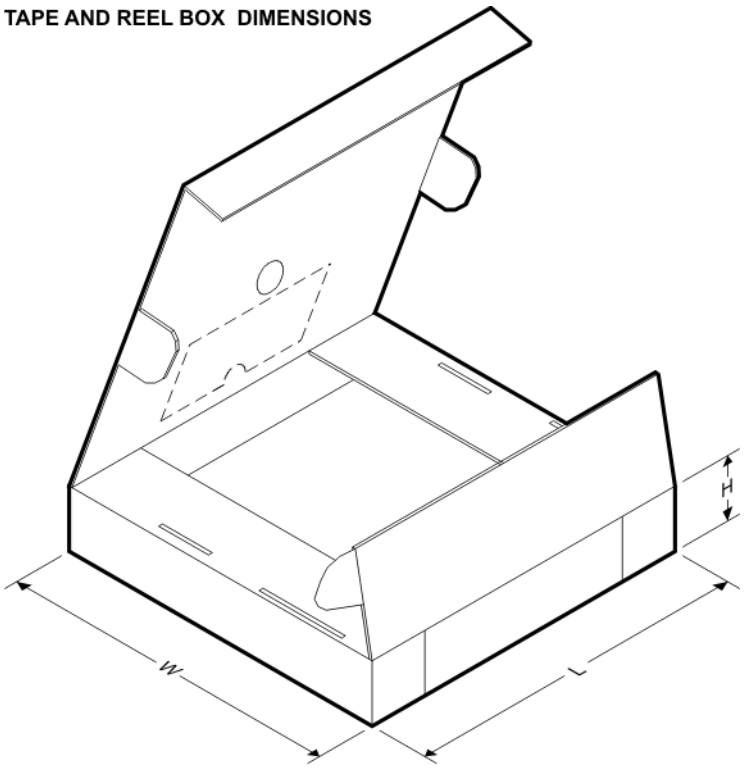
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7718SPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
DAC7718SRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
DAC7718SRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

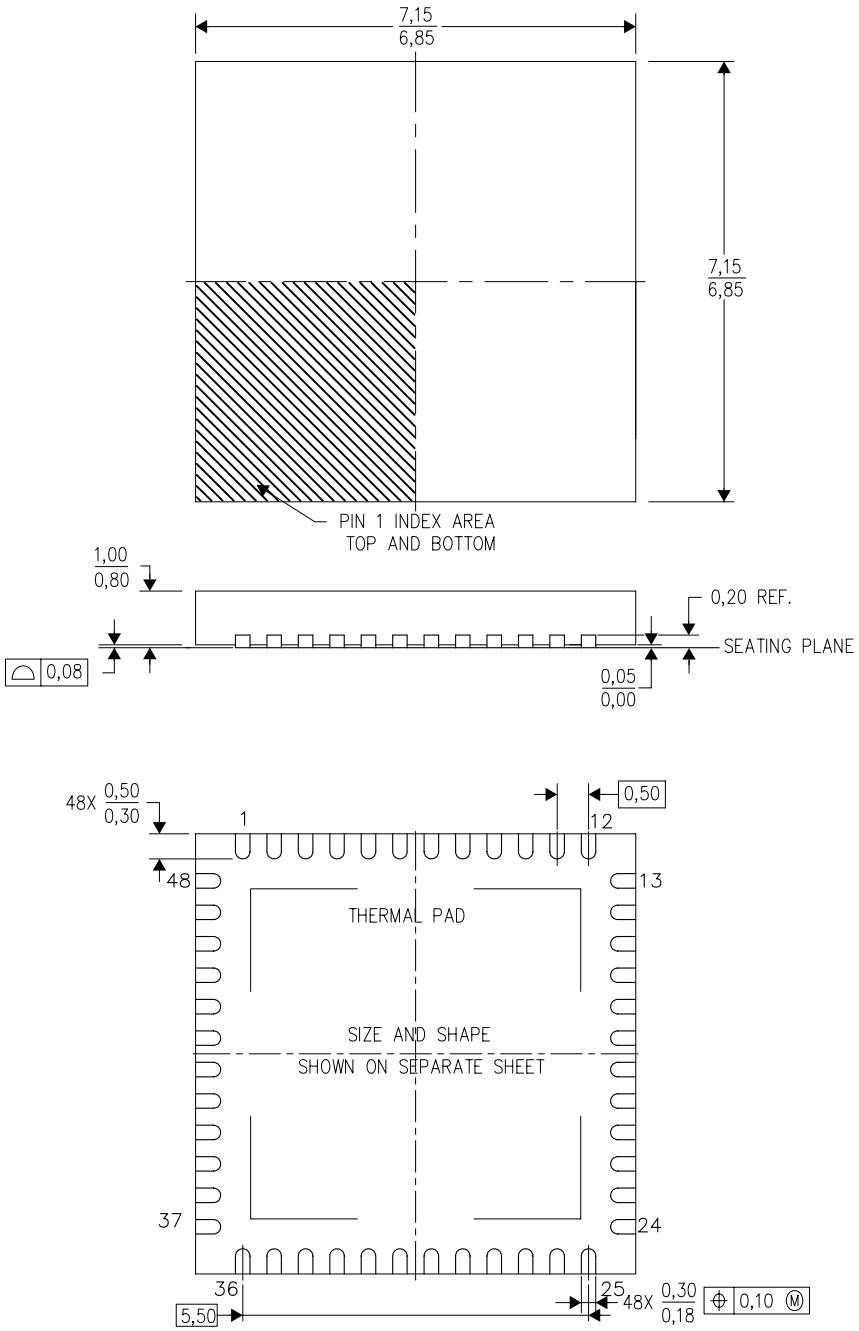
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7718SPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0
DAC7718SRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
DAC7718SRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

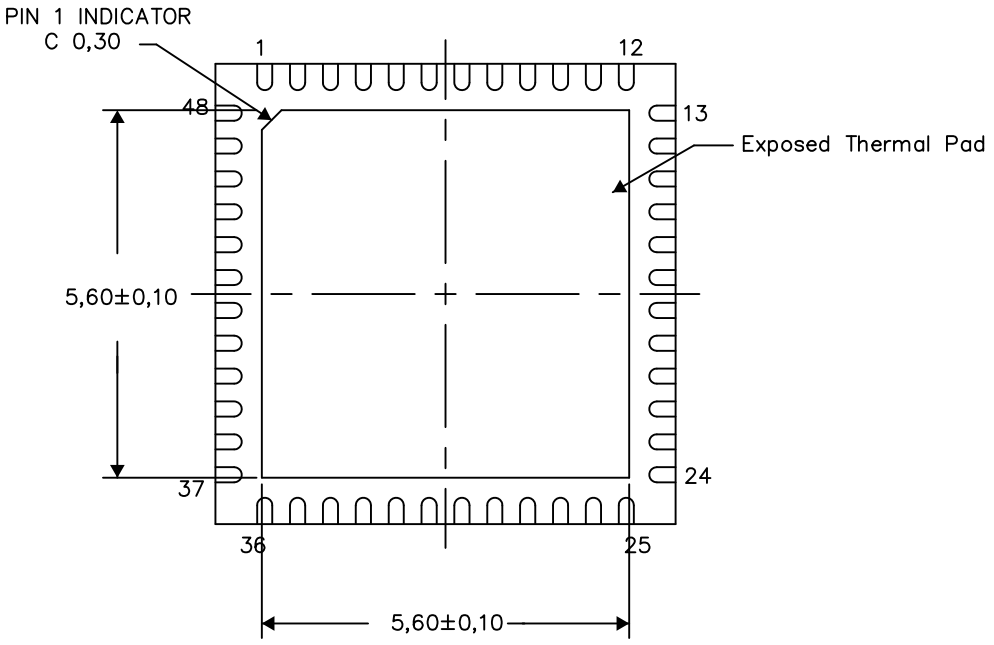
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



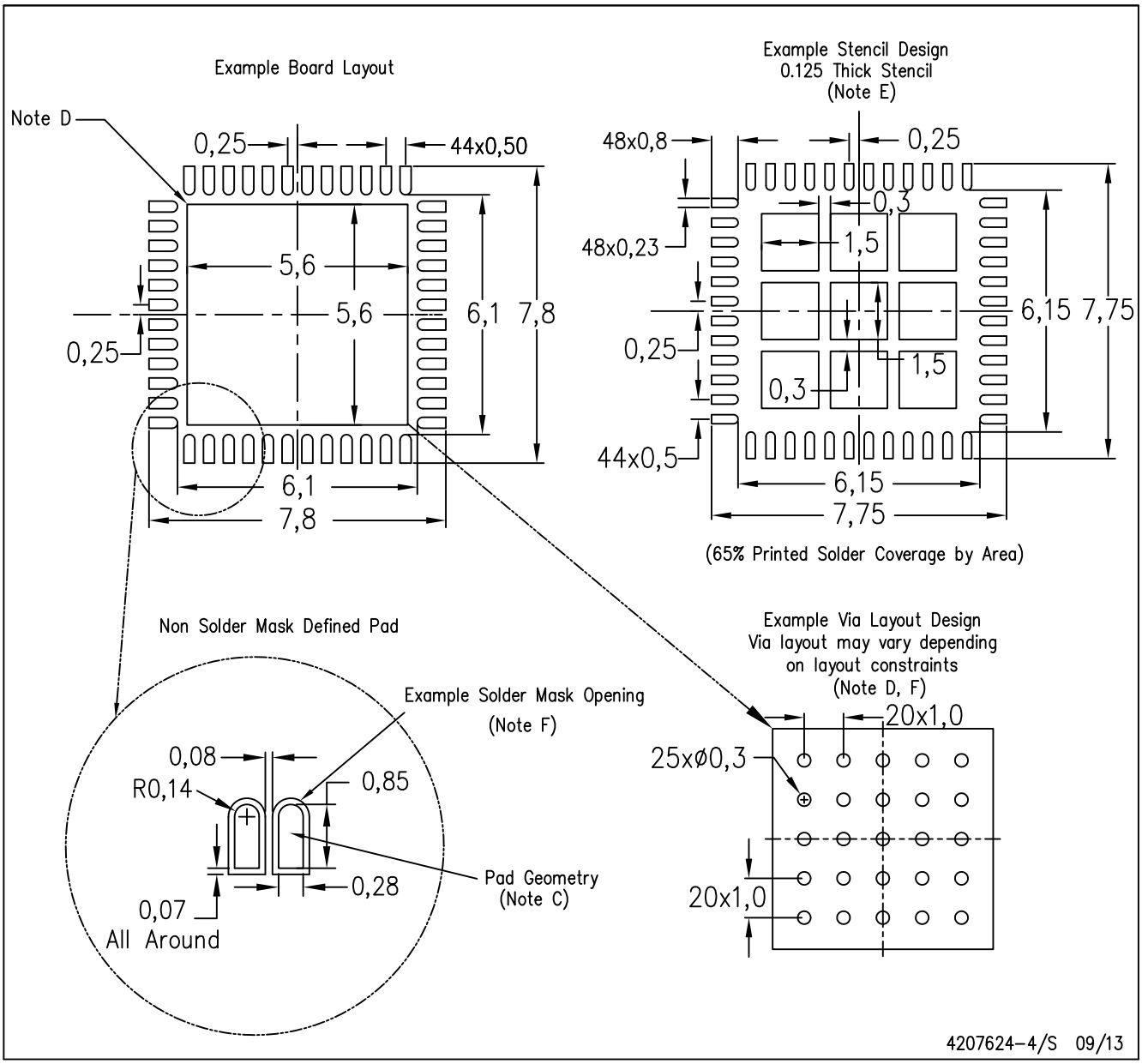
Bottom View

Exposed Thermal Pad Dimensions

4206354–5/X 01/14

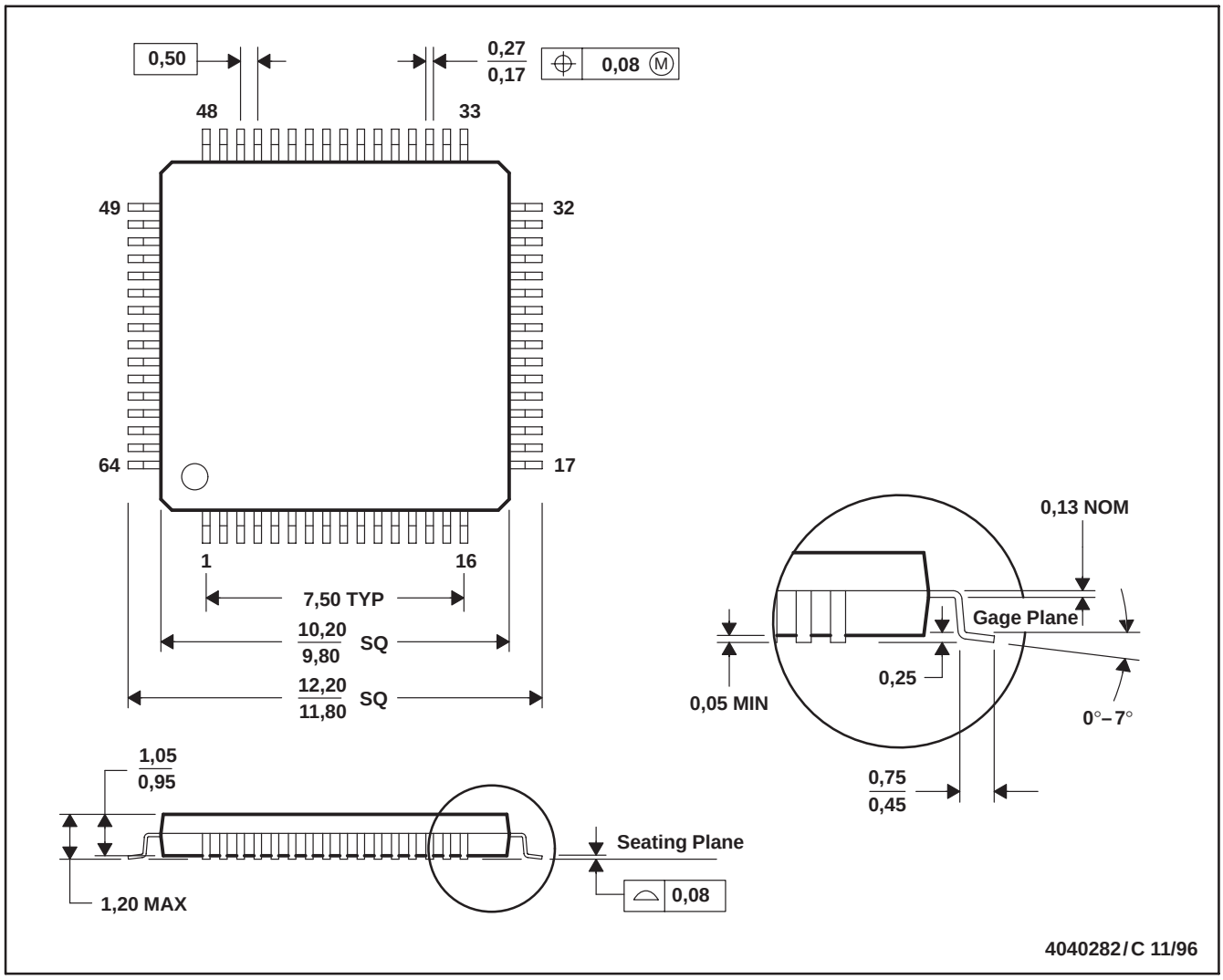
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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