bq2407xT 1.5A USB-Friendly Li-Ion Battery Charger and Power-Path Management IC

1 Features

- Fully Compliant USB Charger
- Selectable 100mA and 500mA Maximum Input Current
- 100mA Maximum Current Limit Ensures Compliance to USB-IF Standard
- Input based Dynamic Power Management (VIN-DPM) for Protection Against Poor USB Sources
- 28V Input Rating with Over-voltage Protection
- Integrated Dynamic Power Path Management (DPPM) Function Simultaneously and Independently Powers the System and Charges the Battery
- System Output Tracks Battery Voltage (bq24072T)
- Supports up to 1.5A Charge Current with Current Monitoring Output (ISET)
- Programmable Input Current Limit up to 1.5A for Wall Adapters
- Battery Disconnect Function with SYSOFF Input
- Reverse Current, Short-Circuit and Thermal Protection
- Flexible Voltage Based NTC Thermistor Input
- Proprietary Start Up Sequence Limits Inrush Current
- Status Indication – Charging/Done, Power Good
- Small 3 mm × 3 mm 16 Lead VQFN Package

2 Applications

- Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

3 Description

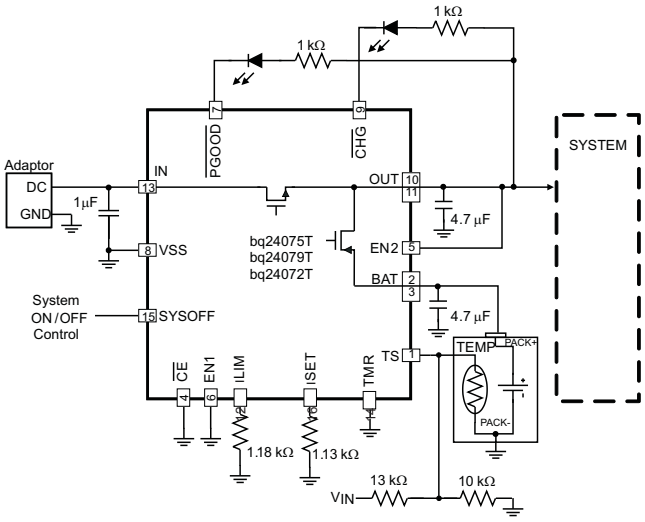
The bq2407xT series of devices are integrated Li-ion linear chargers and system power path management devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter and support charge currents up to 1.5A. The input voltage range with input over-voltage protection supports unregulated adapters. The USB input current limit accuracy and start up sequence allow the bq2407xT to meet USB-IF inrush current specification. Additionally, the input dynamic power management (V_{IN} - DPM) prevents the charger from crashing incorrectly configure USB sources.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24072T	VQFN (16)	3.00 mm x 3.00 mm
bq24075T		
bq24079T		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2010) to Revision B — **Page**

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 1
- Deleted text from the Pin Configuration and Functions section: "Pin out designations are not final. Subject to change." ... 4
- Changed $V_{O(REG)}$ to $V_{BAT(REG)}$ in Min Typ Max columns on the V_{RCH} spec. of Electrical Characteristics table under sub section BATTERY CHARGER ... 8
- Changed I_{OUT} 5.5 V To V_{OUT} 5.5 V in Figure 28 ... 27

Changes from Original (December 2009) to Revision A — **Page**

- Added bq24072T device to data sheet header ... 1
- Added bq24072T feature bullet ... 1
- Added "bq24072T" to graphic entity ... 1
- Added bq24072T spec. to Ordering Info table ... 3
- Added bq24072T Pin Diagram ... 4
- Added bq24072T to $V_{O(REG)}$Elec. Char. spec. ... 7
- Added "bq24072T" to V_{DPPM} in the Electrical Characteristics table ... 8
- Added "bq24072T" to $V_{BAT(REG)}$ the Electrical Characteristics table ... 8
- Added bq24072T Termination Disable (TD) description ... 17
- Added graphic entity for bq24072T DPPM and Battery Supplement Modes ... 23
- Added graphic entity for bq24072T Host Controlled Charger application ... 29
- Added Termination Disable operation procedure. ... 29

5 Description (Continued)

The bq2407xT features dynamic power path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold; thus, supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack.

Additionally, the regulated system input enables instant system turn-on when plugged in even with a totally discharged battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents, enabling the use of a smaller adapter.

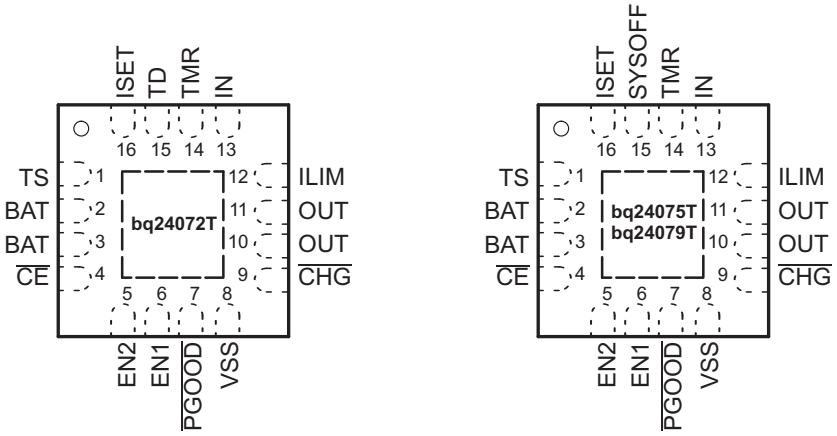
The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

6 Device Comparison

PART NO.	V_{OVP}	$V_{BAT(REG)}$	$V_{OUT(REG)}$	V_{DPPM}	OPTIONAL FUNCTION
bq24072TRGTR	6.6V	4.2 V	V_{BAT} + 225 mV	V_{OREG} –100 mV	TD
bq24072TRGTT	6.6V	4.2 V	V_{BAT} + 225 mV	V_{OREG} –100 mV	TD
bq24075TRGTR	6.6 V	4.2 V	5.5 V	4.3 V	SYSOFF
bq24075TRGTT	6.6 V	4.2 V	5.5 V	4.3 V	SYSOFF
bq24079TRGTR	6.6 V	4.1 V	5.5 V	4.3 V	SYSOFF
bq24079TRGTT	6.6 V	4.1 V	5.5 V	4.3 V	SYSOFF

7 Pin Configuration and Functions

RGT
TOP VIEW



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	bq24072T	bq24075T bq24079T		
TS	1	1	I/O	External NTC Thermistor Input. Connect the TS input to the center tap of a resistor divider from V_{IN} to GND with the NTC in parallel with the bottom resistor to monitor the NTC in the battery pack. For applications that do not utilize the TS function, set the resistor divider to be a 20% ratio. See the Battery Pack Temperature Monitoring section for details on calculating the resistor values.
BAT	2, 3	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7µF to 47µF ceramic capacitor.
$\overline{CE}$	4	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to place the battery charger in standby mode. In standby mode, OUT is active and battery supplement mode is available. Connect /CE to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with ~285kΩ. Do not leave $\overline{CE}$ unconnected to ensure proper operation.
EN2	5	5	I	Input Current Limit Configuration Inputs. Use EN1 and En2 to control the maximum input current and enable USB compliance. See Table 1 for the description of the operation states. EN1 and EN2 are internally pulled down with ~285kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN1	6	6	I	
$\overline{PGOOD}$	7	7	O	Open-Drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 1kΩ to 100kΩ resistor, or use with an LED for visual indication.
VSS	8	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{CHG}$	9	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high-impedance when charging is complete or when the charger is disabled. $\overline{CHG}$ flashes to indicate a timer fault. Connect $\overline{CHG}$ to the desired logic voltage rail using a 1kΩ to 100kΩ resistor, or use with an LED for visual indication.
OUT	10, 11	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to VBAT except when SYSOFF is high. Connect OUT to the system load. Bypass OUT to VSS with a 4.7µF to 47µF ceramic capacitor.
ILIM	12	12	O	Adjustable Current Limit Programming Input. Connect a 1.07kΩ to 7.5kΩ resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging.

Pin Functions (continued)

PIN				
NAME	NUMBER		I/O	DESCRIPTION
	bq24072T	bq24075T bq24079T		
IN	13	13	I	Input Power Connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35V to 6.6V. The input accepts voltages up to 26V without damage, but operation is suspended. Bypass IN to VS with a 1µF to 10µF ceramic capacitor.
TMR	14	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18kΩ to 72kΩ resistor between TMR and VSS to program the timers to a desired length. Leave TMR unconnected to set the timers to the default values.
SYSOFF	–	15	I	System Enable Input. Connect SYSOFF high to turn off the FET connecting the battery to the system output. When an adapter is connected, charge is also disabled. Connect SYSOFF low for normal operation. SYSOFF is internally pulled up to VBAT through a large resistor (~5MΩ). Do not leave SYSOFF unconnected to ensure proper operation.
TD	15	–	I	Termination Disable Input. Connect TD high to disable charger termination. Connect TD to VSS to enable charger termination. TD is checked during startup only and cannot be changed during operation. See the TD section in this datasheet for a description of the behavior when termination is disabled. TD is internally pulled down to VSS with ~285 kΩ. Do not leave TD unconnected to ensure proper operation.
ISET	16	16	I/O	Fast Charge Current Programming Input. Connect a 590 Ω to 3 kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage ISET reflects the actual charging current and can be used to monitor charge current. See the Charge Current Translator section of this datasheet for more details.
Thermal Pad	–	--	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS must be connected to ground at all times.

Table 1. EN1/EN2 Settings

EN2	EN1	MAXIMUM INPUT CURRENT INTO IN
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

8 Specifications

8.1 Absolute Maximum Ratings (1) (2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	–0.3	28	V
	BAT (with respect to VSS)	–0.3	5	V
	OUT, EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, VREF, ITERM, SYSOFF, TD (with respect to VSS)	–0.3	7	V
Input current	IN		1.6	A
Output current (Continuous)	OUT		5	A
	BAT (Discharge mode)		5	A
	BAT (Charging mode)		1.5	A
Output sink current	$\overline{CHG}$, $\overline{PGOOD}$		15	mA
Junction temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.35	26	V
	IN operating voltage range	4.35	6.4	V
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Current, OUT pin		4.5	A
I_{BAT}	Current, BAT pin (Discharging)		4.5	A
I_{CHG}	Current, BAT pin (Charging)		1.5 (1)	A
T_J	Junction Temperature	0	125	°C
R_{ILIM}	Maximum input current programming resistor	1.07	7.5	kΩ
R_{ISET}	Fast-charge current programming resistor (2)	590	3000	Ω
R_{ITERM}	Termination current programming resistor	0	15	kΩ
R_{TMR}	Timer programming resistor	18	72	kΩ

(1) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.
(2) Use a 1% tolerance resistor RISET to avoid issues with the R_{ISET} short test when using the maximum charge current setting.

8.4 Thermal Information

THERMAL METRIC(1)		RGT	UNIT
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	18.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over junction temperature range (0°C < T_J < 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{UVLO}	Under-voltage lock-out	V_{IN}: 0V → 4V	3.2	3.3	3.4	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{IN}: 4V → 0V	200		300	mV
V_{IN-DT}	Input power detection threshold	(Input power detected if V_{IN} > V_{BAT} + V_{IN-DT}) V_{BAT} = 3.6V, V_{IN}: 3.5V → 4V	55	80	140	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT}	V_{BAT} = 3.6V, V_{IN}: 4V → 3.5V	20			mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0V → 5V, 1µs rise-time to $\overline{PGOOD}$ = LO		1.2		ms
V_{OVP}	Input overvoltage protection threshold	VIN: 5V → 7V	6.4	6.6	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	VIN: 7V → 5V		240		mV
$t_{BLK(OVP)}$	Input over-voltage blanking time			50		µs
$t_{REC(OVP)}$	Input over-voltage recovery time	Time measured from V_{IN}: 11V → 5V 1µs fall-time to $\overline{PGOOD}$ = LO		1.2		ms
ILIM, ISET SHORT CIRCUIT TEST						
I_{SC}	Current source			1.3		mA
V_{SC}				520		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, input power not detected, no load on OUT pin			6.5	µA
$I_{IN(STDBY)}$	Standby current into IN pin	EN1= HI, EN2=HI, V_{IN} ≤ 6V			50	µA
		EN1= HI, EN2=HI, V_{IN} > 6V			200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6V, no load on OUT pin, V_{BAT} > $V_{BAT(REG)}$, (EN1,EN2)≠(HI,HI)			1.5	mA
POWER PATH						
$V_{DO(IN-OUT)}$	V_{IN} – V_{OUT}	V_{IN} = 4.3V, I_{IN} = 1A, V_{BAT} = 4.2V		300	475	mV
$V_{DO(BAT-OUT)}$	V_{BAT} – V_{OUT}	I_{OUT} = 1A, V_{IN} = 0V, V_{BAT} > 3V		50	100	mV
$V_{O(REG)}$	OUT pin voltage regulation (bq24072T)	V_{IN} > V_{OUT} + $V_{DO(IN-OUT)}$, V_{BAT}< 3.2 V	3.3	3.4	3.5	V
		V_{IN} > V_{OUT} + $V_{DO(IN-OUT)}$, V_{BAT} ≥ 3.2 V	V_{BAT} + 150 mV	V_{BAT} + 225 mV	V_{BAT} + 270 mV	
	OUT pin voltage regulation (bq24075T, bq24079T)	V_{IN} > V_{OUT} + $V_{DO(IN-OUT)}$	5.4	5.5	5.6	
I_{IN-MAX}	Maximum input current	EN1 = LO, EN2 = LO	90	95	100	mA
		EN1 = HI, EN2 = LO	450	475	500	mA
		EN2 = HI, EN1 = LO		$K_{ILIM}/R_{IL\ IM}$		A
K_{ILIM}	Maximum input current factor	ILIM ≥ 500mA	1500	1600	1700	AΩ
		200mA < ILIM < 500mA	1330	1512	1700	
I_{IN-MAX}	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 8kΩ to 1.1kΩ	200		1500	mA
V_{IN-LOW}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V

Electrical Characteristics (continued)

Over junction temperature range (0°C < T_J < 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DPPM}	Output voltage threshold when charging current is reduced		bq24072T	$V_{O(REG)}$ –180 mV	$V_{O(REG)}$ –100 mV	$V_{O(REG)}$ –30 mV	V
			bq24075T, bq24079T	4.2	4.3	4.4	
V_{BSUP1}	Enter battery supplement mode	VOUT falling, Supplement mode entered when $V_{OUT} < V_{BSUP1}$			V_{BAT} – 40mV		V
V_{BSUP2}	Exit battery supplement mode	VOUT rising, Supplement mode exited when $V_{OUT} > V_{BSUP2}$			V_{BAT} – 20mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on			0.8	0.9	1.0	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} – V_{OUT} > V_{O(SC2)}$ indicates short-circuit			200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit				250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit				60		ms
BATTERY CHARGER							
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection			4	7.5	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold			1.6	1.8	2.0	V
$V_{BAT(REG)}$	Battery charge voltage	bq24072T, bq24075T		4.16	4.20	4.24	V
		bq24079T		4.059	4.100	4.141	
V_{LOWV}	Pre-charge to fast-charge transition threshold			2.9	3	3.1	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition				25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition				25		ms
I_{CHG}	Battery fast charge current range	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$, V_{IN} = 5V, $\overline{CE}$ = LO, EN1= LO, EN2 = HI		300		1500	mA
I_{CHG}	Battery fast charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, $V_{BAT} > V_{LOWV}$, V_{IN} = 5V, $I_{IN-MAX} > I_{CHG}$, no load on OUT pin, thermal loop not active, DPM loop not active			K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor			797	890	975	AΩ
I_{PRECHG}	Pre-charge current				K_{PRECHG}/R_{ISET}		A
k_{PRECHG}	Pre-charge current factor			70	88	106	
I_{TERM}	Charge current value for termination detection threshold	$\overline{CE}$ = LO, (EN1,EN2)≠(LO,LO), $V_{BAT} > V_{RCH}$, $t < t_{MAXCH}$, V_{IN} = 5V, DPM loop not active, thermal loop not active		$0.09\times I_{CHG}$	$0.1\times I_{CHG}$	$0.11\times I_{CHG}$	
		$\overline{CE}$ = LO, (EN1,EN2)=(LO,LO), $V_{BAT} > V_{RCH}$, $t < t_{MAXCH}$, V_{IN} = 5V, DPM loop not active, thermal loop not active		$0.027\times I_{CHG}$	$0.033\times I_{CHG}$	$0.040\times I_{CHG}$	
$t_{DGL(TERM)}$	Deglitch time, termination detected				25		ms
V_{RCH}	Recharge detection threshold			$V_{BAT(REG)}$ –140mV	$V_{BAT(REG)}$ –100mV	$V_{BAT(REG)}$ –60mV	V
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected				62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turn-off	VBAT = 3.6V. Time measured from V_{IN}: 5V → 3.3V 1µs fall-time			20		ms
$I_{BAT(DET)}$	Sink current for battery detection			5	7.5	10	mA
t_{DET}	Battery detection timer				250		ms

Electrical Characteristics (continued)

Over junction temperature range (0°C < T_J < 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGING TIMERS						
t_{PRECHG}	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCH}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Pre-charge safety timer value(externally set)	18kΩ < RTMR < 72kΩ		R_{TMR} x K_{TMR}		s
t_{MAXCH}	Charge safety timer value (externally set)	18kΩ < RTMR < 72kΩ		10 x R_{TMR} x K_{TMR}		s
K_{TMR}	Timer factor		35	45	55	s / kΩ
BATTERY – PACK NTC MONITOR						
V_{HOT}	High temperature trip point	Battery charging	12	12.5	13	% of V_{IN}
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging		1		% of V_{IN}
V_{COLD}	Low temperature trip point	Battery charging	24.5	25	25.5	% of V_{IN}
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging		1		% of V_{IN}
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	Battery charging		50		ms
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, SYSOFF, TD						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6.0	V
I_{IL}					1	µA
I_{IH}					10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

8.6 Typical Characteristics

V_{IN} = 6V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.

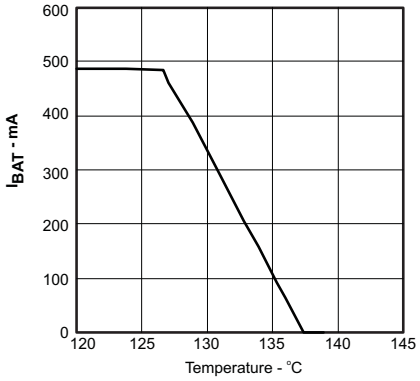


Figure 1. Thermal Regulation

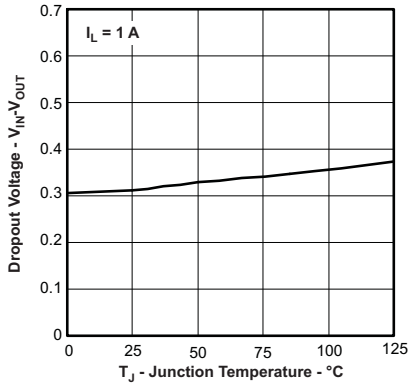


Figure 2. Dropout Voltage vs Temperature

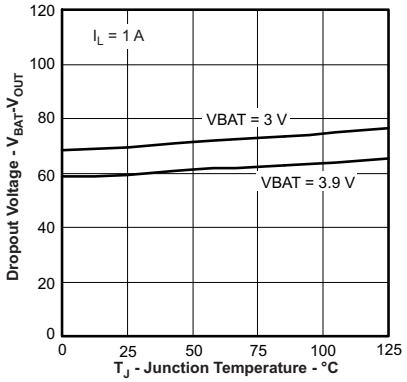


Figure 3. Dropout Voltage vs Temperature

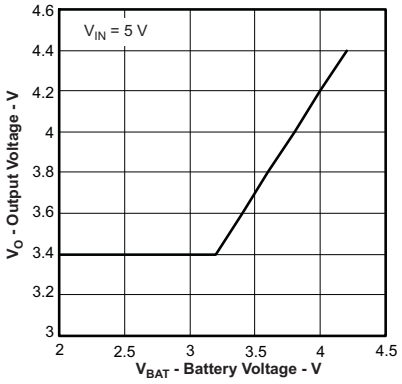


Figure 4. bq24072T Output Regulation Voltage vs Battery Voltage

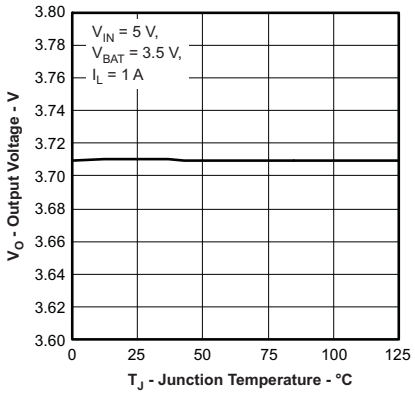


Figure 5. bq24072T Output Regulation Voltage vs Temperature

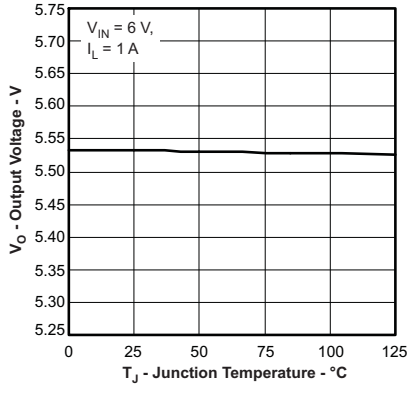


Figure 6. Output Regulation Voltage vs Temperature

Typical Characteristics (continued)

V_{IN} = 6V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.

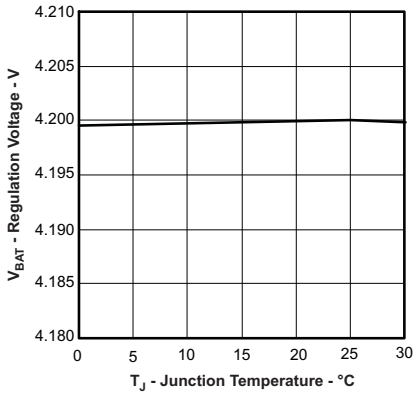


Figure 7. bq24075T BAT Regulation Voltage vs Temperature

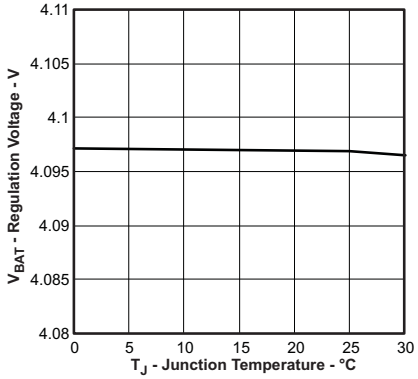


Figure 8. bq24079T Battery Regulation Voltage vs Temperature

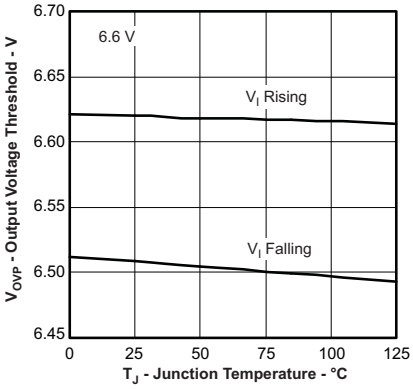


Figure 9. Overvoltage ProtectionThreshold vs Temperature

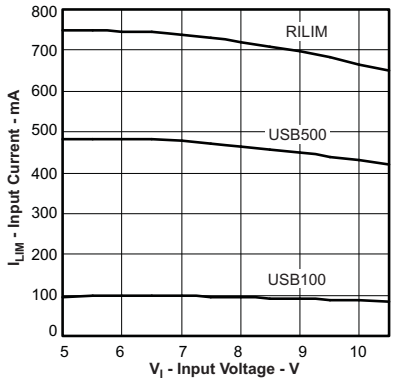


Figure 10. Input Current Limit vs Input Voltage

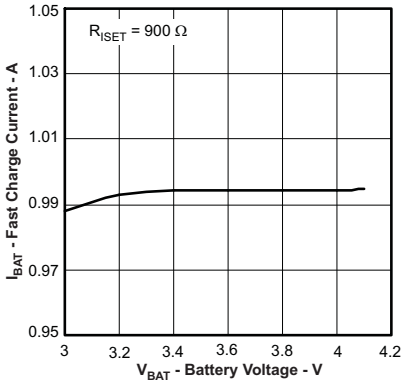


Figure 11. Fastcharge Current vs Battery Voltage

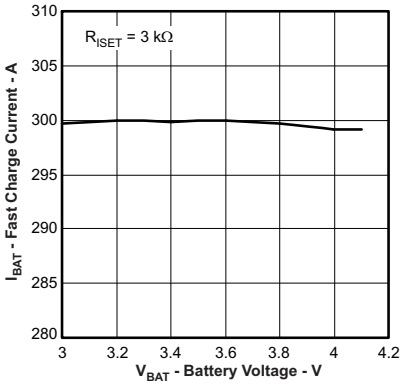


Figure 12. Fastcharge Current vs Battery Voltage

Typical Characteristics (continued)

V_{IN} = 6V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.

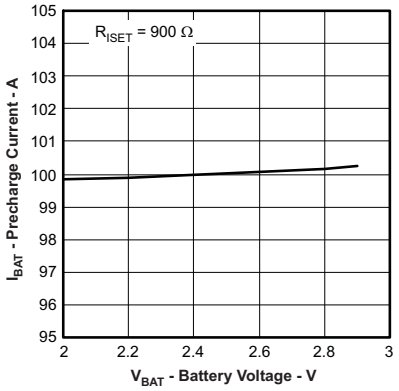


Figure 13. Fastcharge Current vs Battery Voltage

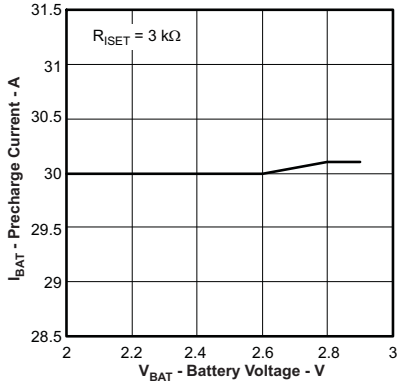


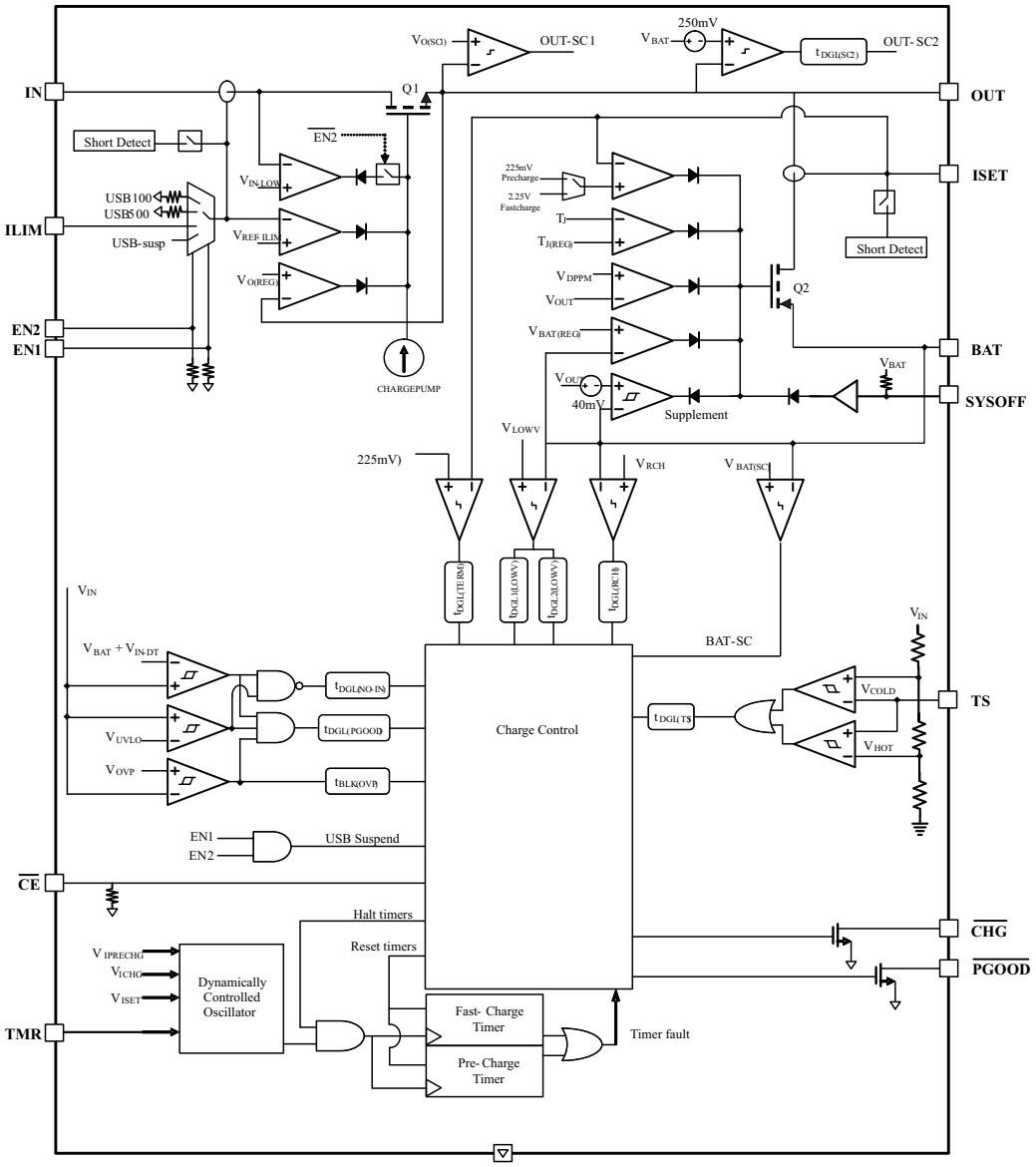
Figure 14. Precharge Current vs Battery Voltage

9 Detailed Description

9.1 Overview

The bq2407x devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature Dynamic Power Path Management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN}-DPM) circuit reduces the input current if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

The bq2407X family remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO). During the power down mode the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs, $\overline{CHG}$ and $\overline{PGOOD}$, are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the VOUT(SC2) circuitry is active and monitors for overload conditions on OUT.

9.3.2 Overvoltage Protection (OVP)

The bq2407xT accepts inputs up to 28V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when $V_{IN} > V_{OVP}$ for a period longer than $t_{DGL(OVP)}$. When in OVP, the system output (OUT) is connected to the battery and $\overline{PGOOD}$ is high impedance. Once the OVP condition is removed, a new power on sequence starts (See the *POWER ON* section). The safety timers are reset and a new charge cycle will be indicated by the $\overline{CHG}$ output.

9.3.3 Dynamic Power-Path Management

The bq2407xT features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

9.3.4 Battery Charging

Set $\overline{CE}$ low to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

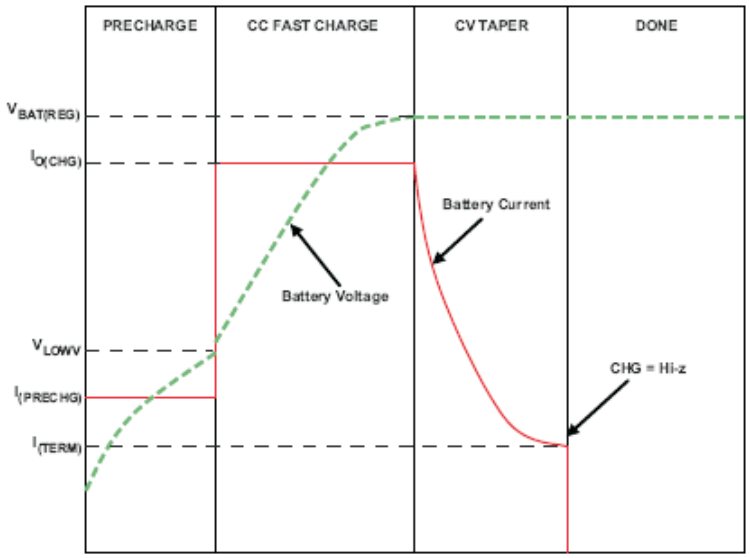


Figure 15. Typical Charging Cycle

Feature Description (continued)

Figure 15 illustrates a normal Li-Ion charge cycle using the bq2407xT. In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop or the V_{IN-DPM} loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by Equation 1.

$$I_{CHG} = K_{ISET} / R_{ISET} \quad (1)$$

The charge current limit is adjustable up to 1.5A. The valid resistor range is 590Ω to 3 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down.

9.3.5 Charge Current Translator

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R_{ISET}, generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET} = I_{CHARGE} / 400 \times R_{ISET} \quad (2)$$

Feature Description (continued)

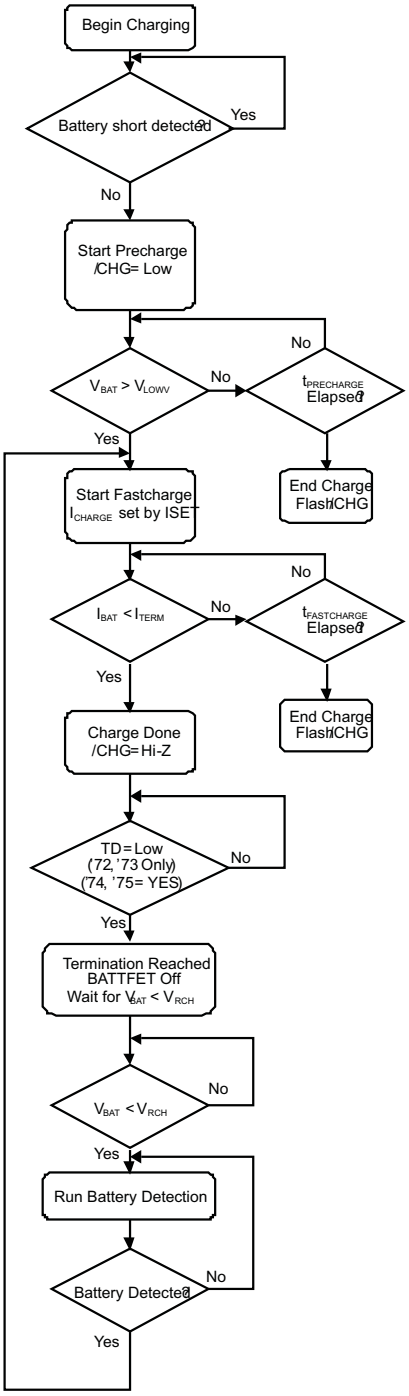


Figure 16. Battery Charging Flow Diagram

Feature Description (continued)

9.3.6 Battery Detection and Recharge

The bq2407xT automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery detection routine is run. During battery detection, current ($I_{BAT(DET)}$) is pulled from the battery for a duration t_{DET} to see if the voltage on BAT falls below V_{LOWV}. If not, charging begins. If it does, then it indicates that the battery is missing or the protector is open. Next, the precharge current is applied for t_{DET} to close the protector if possible. If $V_{BAT} < V_{RCH}$, then the protector is closed and charging is initiated. If $V_{BAT} > V_{RCH}$, then the battery is determined to be missing and the detection routine continues.

9.3.7 Termination Disable (TD Input, bq24072T)

The bq24072T contains a TD input that allows termination to be enabled/ disabled. Connect TD to a logic high to disable charge termination. When termination is disabled, the device goes through the pre-charge, fast-charge and CV phases, then remains in the CV phase. During the CV phase, the charger maintains the output voltage at BAT equal to $V_{BAT(REG)}$, and charging current does not terminate. The charge current is set by I_{CHG} or I_{IN}max, whichever is less. Battery detection is not performed. The $\overline{CHG}$ output is high impedance once the current falls below I_{TERM} and does not go low until the input power or $\overline{CE}$ are toggled. When termination is disabled, the pre-charge and fast-charge safety timers are also disabled.

9.3.8 Battery Disconnect (SYSOFF Input)

The bq24075T and bq24079T feature a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side impedance track fuel gauging, such as bq27500, where the battery open circuit voltage level must be detected before the battery charges or discharges. The $\overline{CHG}$ output remains low when SYSOFF is high. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT through ~5 MΩ resistor.

9.3.9 Dynamic Charge Timers (TMR Input)

The bq2407xT devices contain internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR}$$
$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR}$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation.

1. During the fast charge phase, several events increase the timer durations.
2. The system load current activates the DPPM loop which reduces the available charging current
3. The input current is reduced because the input voltage has fallen to V_{IN-DPM}
4. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half for two minutes, the timer clock is reduced to half the frequency and the counter counts half as fast resulting in only one minute of "counting" time.

If the precharge timer expires before the battery voltage reaches V_{LOWV}, the bq2407xT indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition. The fault condition is cleared by toggling $\overline{CE}$ or the input power, entering/ exiting USB suspend mode, or an OVP event.

Feature Description (continued)

9.3.10 Status Indicators ($\overline{PGOOD}$, $\overline{CHG}$)

The bq2407xT contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when (V_{BAT} + $V_{IN(DT)}$) < V_{IN} < V_{OVP}. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The charge cycle after power-up, $\overline{CE}$ going low, or exiting OVP is indicated with the $\overline{CHG}$ output on (low - LED on), whereas all refresh (subsequent) charges will result in the $\overline{CHG}$ output off (open – LED off). In addition, the $\overline{CHG}$ signals timer faults by flashing at approximately 2Hz.

Table 2. $\overline{PGOOD}$ Status Indicator

INPUT STATE	$\overline{PGOOD}$ OUTPUT
V_{IN} < V_{UVLO}	Hi impedance
V_{UVLO} < V_{IN} < $V_{IN(DT)}$	Hi impedance
$V_{IN(DT)}$ < V_{IN} < V_{OVF}	Low
V_{IN} < V_{OVP}	Hi impedance

Table 3. $\overline{CHG}$ Status Indicator

CHARGE STATE	$\overline{CHG}$ OUTPUT
Charging	Low (for first charge cycle)
Charging suspended by thermal loop, or DPPM loop	
Safety timers expired	Flashing at 2 Hz
Charging done	Hi impedance
Recharging after termination	
IC disabled or no valid input power	
Battery absent	

9.3.11 Thermal Regulation and Thermal Shutdown

The bq2407xT contain a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a "hiccup" mode. During thermal regulation, the safety timers are slowed down proportionately to the reduction in current limit.

Note that this feature monitors the die temperature of the bq2407xT. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in Figure 17. Battery termination is disabled during thermal regulation.

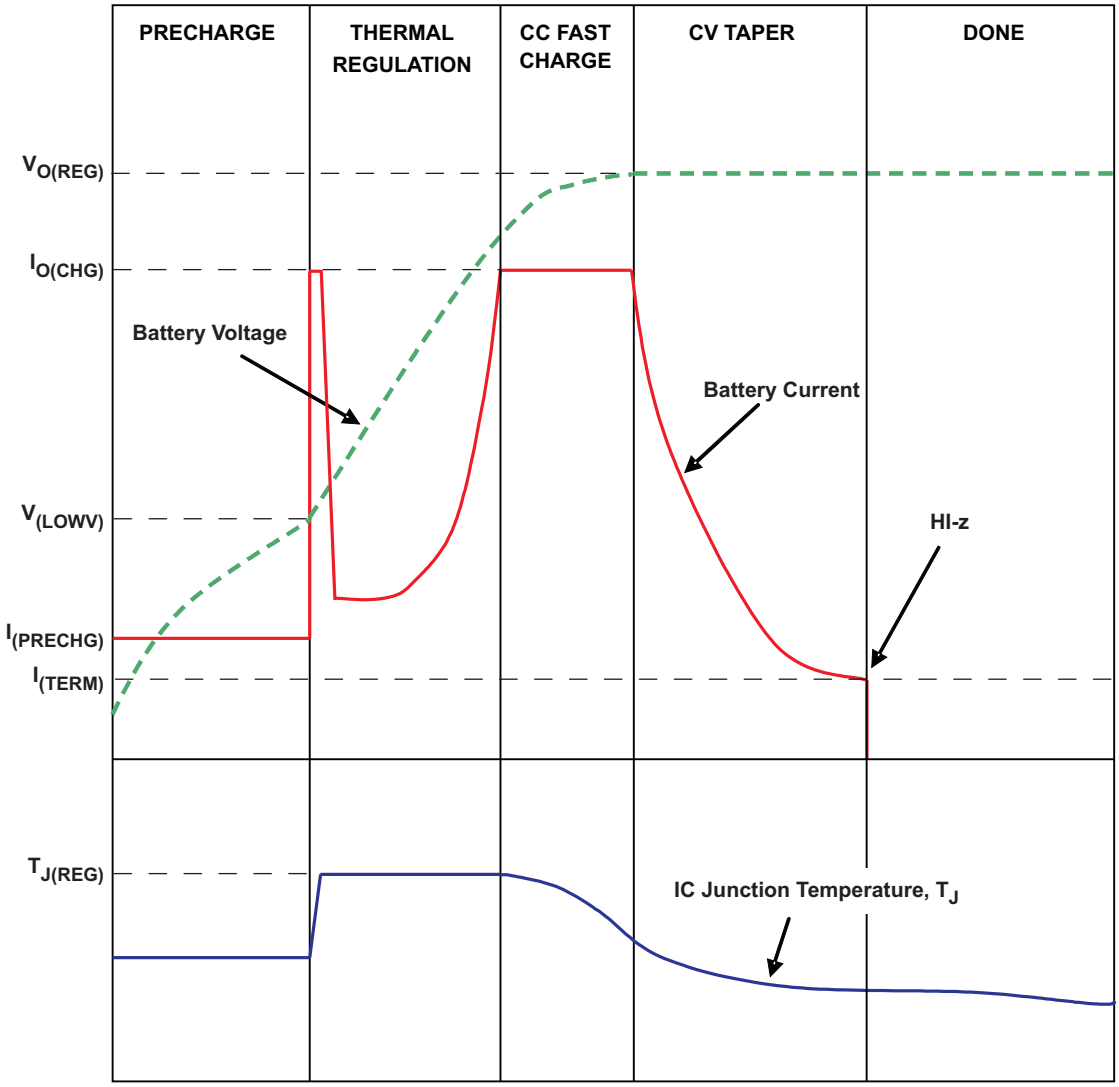


Figure 17. Charge Cycle Modified by Thermal Loop

9.3.12 Battery Pack Temperature Monitoring

The bq2407xT features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ output remains low and continues to indicate charging.

$$R6 = \frac{\frac{V_{IN}}{V_{COLD}} - 1}{\frac{1}{R7} + \frac{1}{RCOLD}} \quad (3)$$

$$R7 = \frac{V_{IN} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{IN}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{IN}}{V_{COLD}} - 1\right]} \quad (4)$$

Where:

$V_{COLD} = 0.25 \times V_{IN}$

$V_{HOT} = 0.125 \times V_{IN}$

RHOT is the expected thermistor resistance at the programmed hot threshold, RCOLD is the expected thermistor resistance at the programmed cold threshold. If the value of R6 is less than 100kΩ, R3 must be added to protect the IC from 28V inputs. If R6 is greater than 100kΩ, R8 does not need to be used.

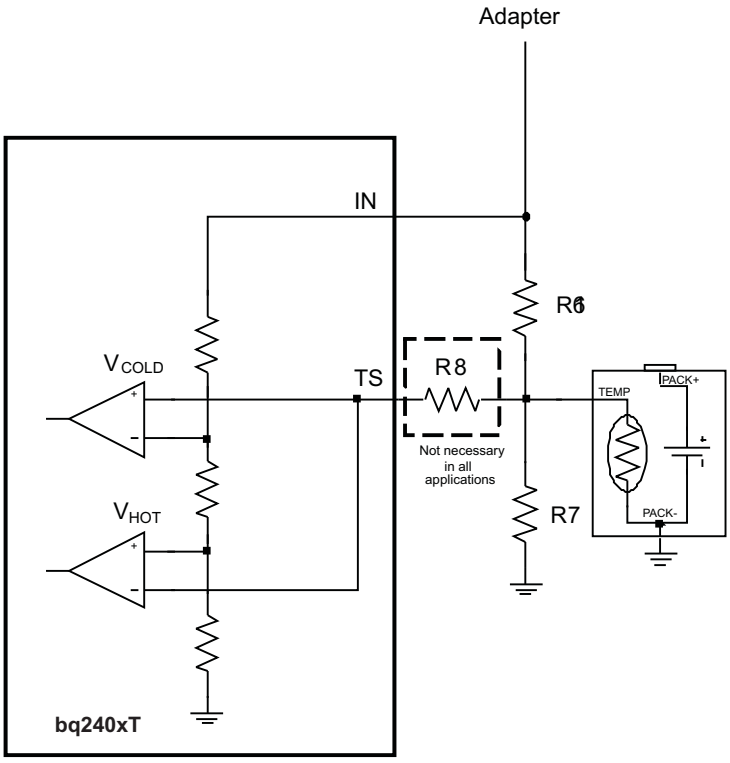


Figure 18. NTC Monitoring Function

For applications that do not require the TS monitoring function, set R6 = 200kΩ and R7 = 49.9kΩ to set the TS voltage at a valid level and maintain charging.

9.4 Device Functional Modes

9.4.1 Input Source Connected (Adapter or USB)

With a source connected, the dynamic power-path management (DPPM) circuitry of the bq2407xT monitors the input current continuously. The OUT output for the bq24075T/ 79T is regulated to a fixed voltage ($V_{O(REG)}$). For the bq24072T, OUT is regulated to 225mV above the voltage at BAT. If the BAT voltage is less than 3.2V, OUT is clamped to 3.4V. This allows for proper startup of the system load even with a discharged battery. The current into IN is shared between charging the battery and powering the system load at OUT. The bq2407xT has internal selectable current limits of 100mA (USB100) and 500mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit.

The bq2407xT is USB IF compliant for the inrush current testing. The USB spec allows up to 10µF to be hard started, which establishes 50µC as the maximum inrush charge value when exceeding 100mA. The input current limit for the bq2407xT prevents the input current from exceeding this limit, even with system capacitances greater than 10µF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10µF), as this current is not limited. Figure 19 demonstrates the startup of the bq2407xT and compares it to the USB-IF specification.

Device Functional Modes (continued)

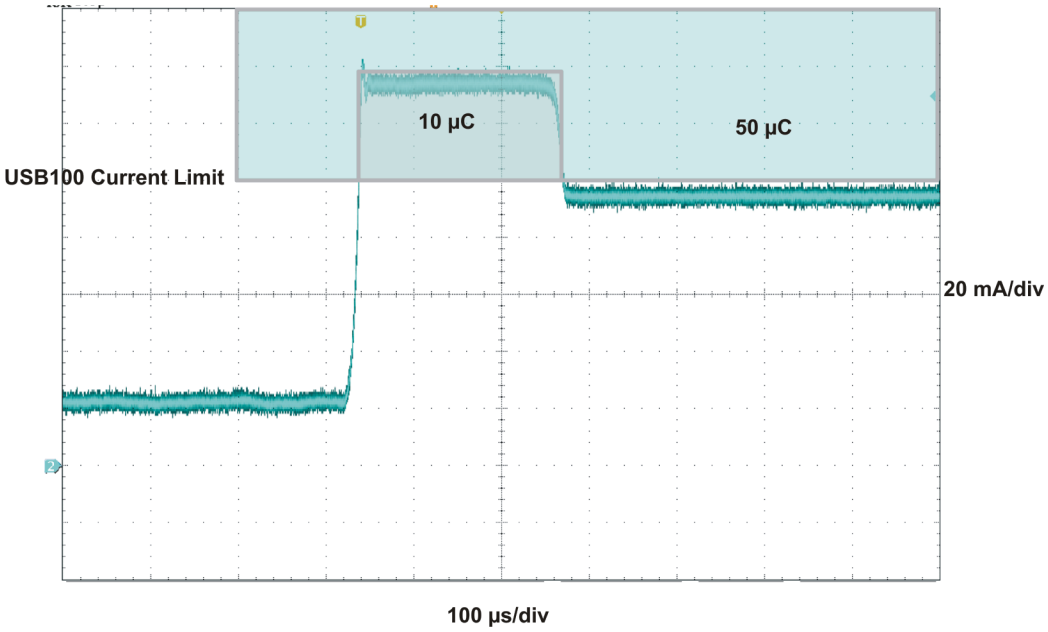


Figure 19. USB-IF Inrush Current Test

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$II_{N\text{-}MAX} = K_{ILIM} / R_{ILIM} \quad (5)$$

The input current limit is adjustable up to 1.5A. The valid resistor range is 1.07 kΩ to 7.5kΩ.

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. Figure 21 illustrates an example of the DPPM and supplement modes. These modes are explained in detail in the following sections.

9.4.1.1 Input DPM Mode (V_{IN}-DPM)

The bq2407xT utilizes the V_{IN}-DPM mode for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2=0, EN1=0) or USB500 (EN2=0, EN2=1) modes, the input voltage is monitored. If V_{IN} falls to $V_{IN\text{-}DPM}$, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq2407xT from crashing poorly designed or incorrectly configured USB sources. Figure 20 shows the V_{IN}-DPM behavior to a current limited source. In this figure, the input source has a 400mA current limit and the device is in USB500 mode (EN1=1, EN2=0).

Device Functional Modes (continued)

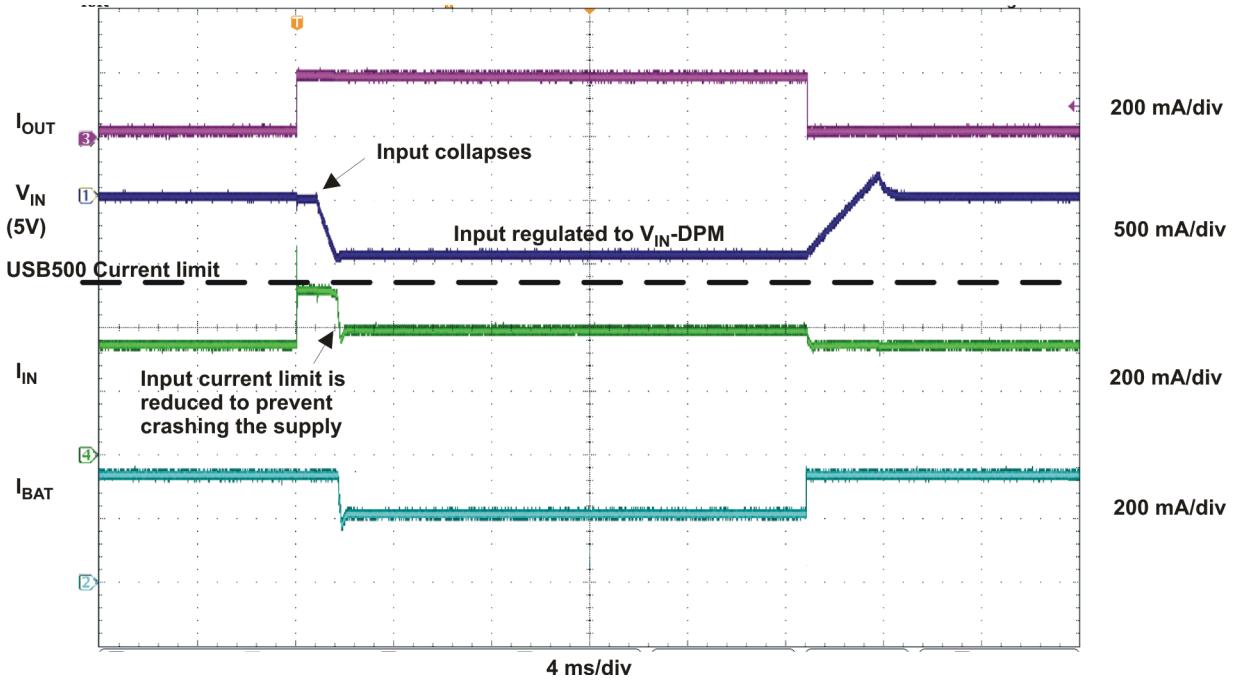


Figure 20. VIN-DPM Mode

9.4.1.2 DPPM Mode

When the sum of the charging and system load currents exceeds the maximum input current (programmed with EN1, EN2 and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPPM}, the bq2407xT enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output. Battery termination is disabled while in DPPM mode.

9.4.1.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the V_{BSUP1} threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the V_{BSUP2} threshold.

During supplement mode, the battery supplement current is not regulated (BAT-FET is fully on), however there is a short circuit protection circuit built in. demonstrate supplement mode. If during battery supplement mode, the voltage at OUT drops $V_{O(SC2)}$ below the BAT voltage, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

Device Functional Modes (continued)

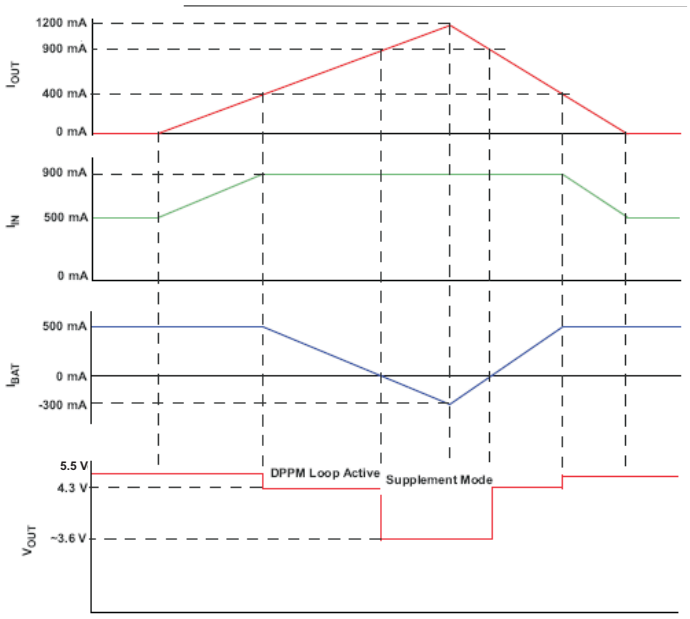


Figure 21. bq24075T, '79T DPPM and Battery Supplement Modes (V_{OREG} = 5.5V, V_{BAT} = 3.6V)

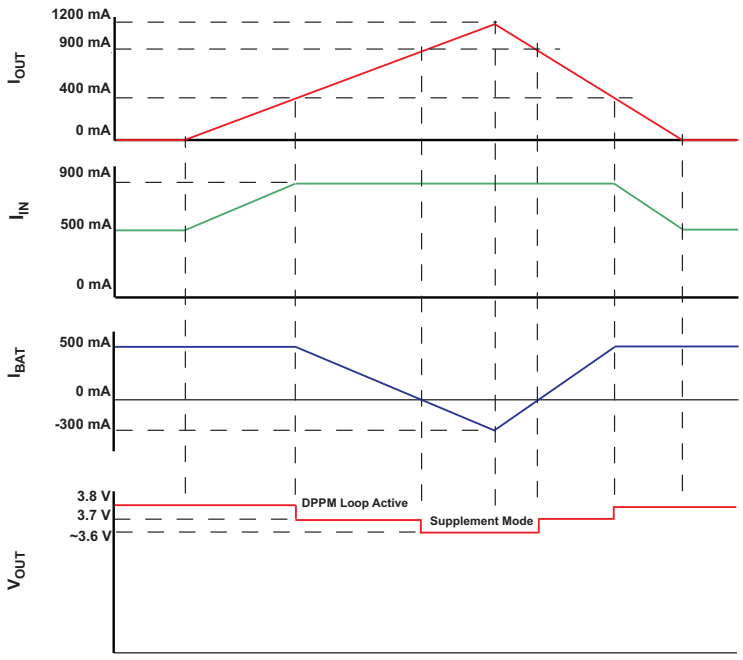


Figure 22. bq24072T DPPM and Battery Supplement Modes (V_{OREG} = V_{BAT} + 225mV, V_{BAT} = 3.6V)

Device Functional Modes (continued)

9.4.2 Input Source Not Connected

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode the current into OUT is not regulated, similar to Battery Supplement Mode, however the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

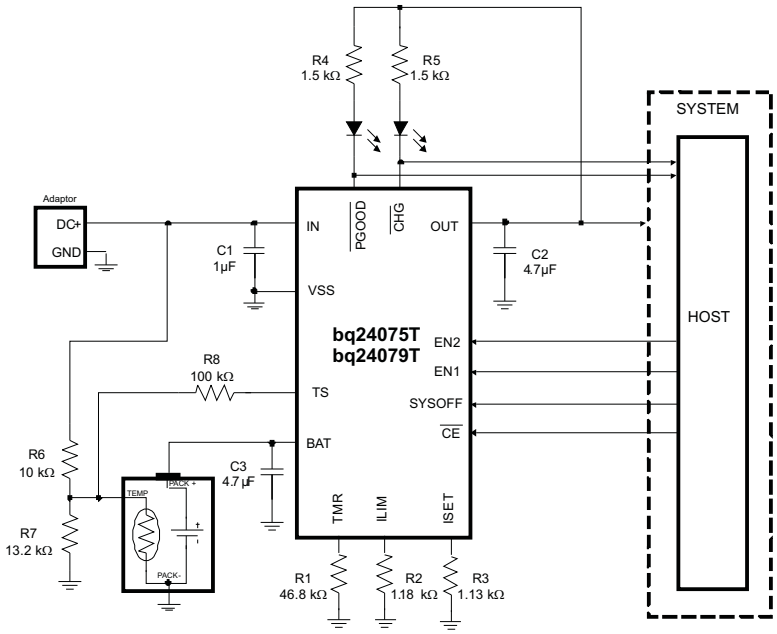
10.1 Application Information

The bq2407xT series of devices are integrated Li-ion linear chargers and system power path management devices targeted at space-limited portable applications

10.2 Typical Applications

10.2.1 Using the bq24075T, bq24079T to Disconnect the Battery from the System

The bq24075T and bq24079T are designed for applications that require the input supply to be passed through to the output (OUT). For these devices, the OUT regulation threshold is set to 5.5V. for applications with a typical regulation on the adapter of 5V, the main LDO in the bq24075T/9T operates in dropout mode so that OUT is as high as possible to supply downstream devices. The input OVP and regulation threshold on OUT protect downstream devices from faulty or incorrect adapters. The bq24075T/9T also contain a SYSOFF input that disconnects the OUT output from the battery to prevent standby loads from draining the battery during long storage intervals. See the "System ON/OFF" section for more details.



NOTE: V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800mA, $I_{IN(MAX)}$ = 1.35A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer

Figure 23. Using the bq24075T, bq24079T to Disconnect the Battery from the System

10.2.1.1 Design Requirements

- Supply voltage = 5V
- Fast charge current of approximately 800 mA; ISET – pin 16
- Input Current Limit =1.35A; ILIM – pin 12
- Safety timer duration, Fast-Charge = 6.25 hours; TMR – pin 14
- Battery Temperature Sense = 10kΩ; NTC (103AT-2), 0°C to 50°C Operation

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Program the Fast Charge Current (ISET):

- $R_{ISET} = K_{ISET} / I_{CHG}$
- K_{ISET} = 890 AΩ; from the *Electrical Characteristics* table
- R_{ISET} = 890AΩ / 0.8A = 1.1125 kΩ
- Select the closest standard value, which for this case is 1.13kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

10.2.1.2.2 Program the Input Current Limit (ILIM):

- $R_{ILIM} = K_{ILIM} / I_{IN(MAX)}$
- K_{ILIM} = 1600 AΩ; from the *Electrical Characteristics* table
- R_{ISET} = 1600AΩ / 1.35A = 1.19 kΩ
- Select the closest standard value, which for this case is 1.18 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

10.2.1.2.3 Program 6.25-hour Fast-Charge Safety Timer (TMR):

- $R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$
- K_{TMR} = 45 s/kΩ from the *Electrical Characteristics* table.
- R_{TMR} = (6.25 hr × 3600 s/hr) / (10 x 45 s/kΩ) = 46.8kΩ;
- Select the closest standard value, which for this case is 46.4 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

10.2.1.2.4 TS Function:

Using a 10kΩ NTC thermistor in the battery pack (103AT-2). Connect a resistor divider from V_{IN} to V_{SS} with the thermistor and TS connected to the center tap (R6 and R7 in Figure 23).

- R_{HOT} = 4.086kΩ; 50°C threshold from NTC data sheet
- R_{COLD} = 28.16 kΩ; 0°C threshold from NTC data sheet
- V_{COLD} = 0.25 x V_{IN} = 0.25 x 5V = 1.25V
- V_{HOT} = 0.125 x V_{IN} = 0.125 x 5V = 0.625V

$$R7 = \frac{V_{IN} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{IN}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{IN}}{V_{COLD}} - 1\right]} = \frac{5 \times 28160 \times 4086 \times \left[\frac{1}{1.25} - \frac{1}{0.625}\right]}{4086 \times \left[\frac{5}{0.625} - 1\right] - 28160 \times \left[\frac{5}{1.25} - 1\right]} = 8.236k\Omega \quad (6)$$

$$R6 = \frac{\frac{V_{IN}}{V_{COLD}} - 1}{\frac{1}{R7} + \frac{1}{RCOLD}} = \frac{\frac{5}{1.25} - 1}{\frac{1}{8250} + \frac{1}{28160}} = 19.14k\Omega \quad (7)$$

Since the calculated values for R6 is less than 100kΩ, a 100kΩ resistor for R8 must be used. Choose the closest standard values, which for this case are R6 = 8.25kΩ and R7 = 19.1kΩ.

For applications that do not require the TS monitoring function, set R6 = 200kΩ and R7 = 49.9kΩ to set the TS voltage at a valid level and maintain charging.

10.2.1.2.5 $\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$ LED Status:

connect a 1.5kΩ resistor in series with a LED between OUT and $\overline{\text{CHG}}$ to indicate charging status. Connect a 1.5kΩ resistor in series with a LED between OUT and $\overline{\text{PGOOD}}$ to indicate when a valid input source is connected.

Typical Applications (continued)

10.2.1.2.6 Processor Monitoring Status:

connect a pullup resistor (on the order of 100 kΩ) between the processor power rail and $\overline{CHG}$ and PGOOD

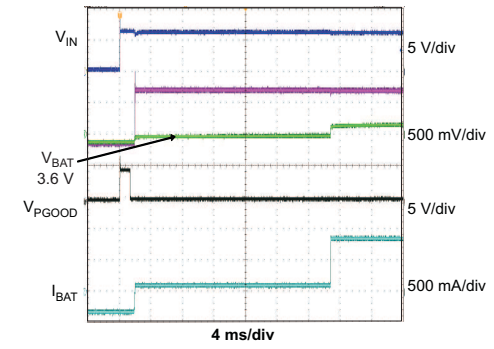
10.2.1.2.7 System ON/OFF (SYSOFF):

Connect SYSOFF high to disconnect the battery from the system load. Connect SYSOFF low for normal operation.

10.2.1.2.8 Selecting IN, OUT and BAT Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output and battery pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed high input voltage sources (bad adapters or wrong adapters), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

10.2.1.3 Application Curves



R_{LOAD} = 10 Ω

Figure 24. Adapter Plug-In Battery Connected

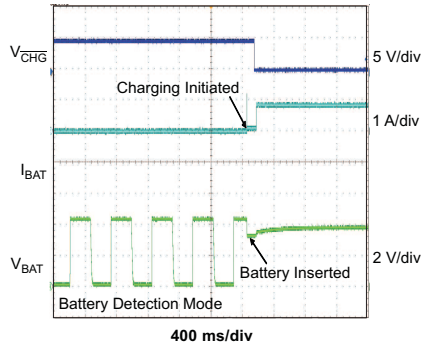


Figure 25. Battery Detection / Battery Inserted

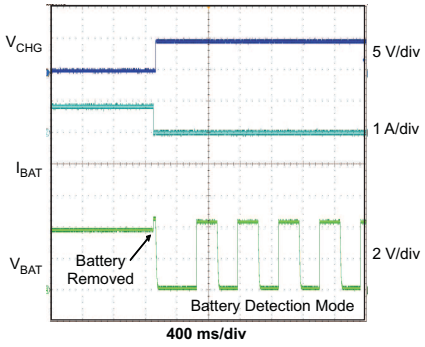
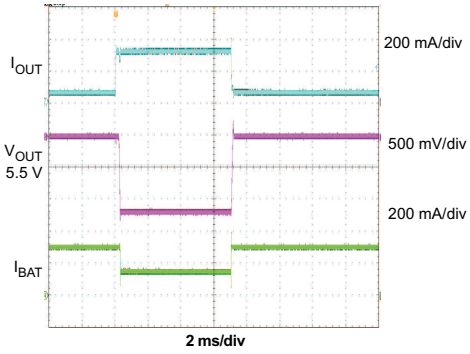


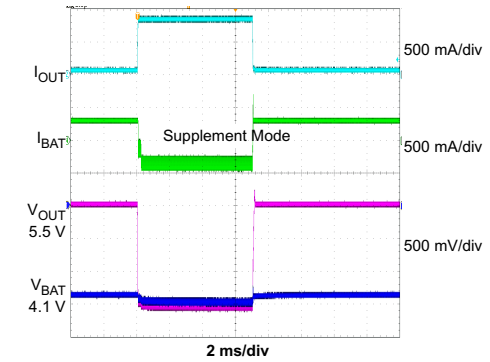
Figure 26. Battery Detection / Battery Removed



I_{LOAD} = 25 mA TO 250 mA

Figure 27. Entering and Exiting, DPPM Mode

Typical Applications (continued)



I_{LOAD} = 25 mA to 750 mA

Figure 28. bq24075T, bq24079T Entering and Exiting Battery, Supplement Mode

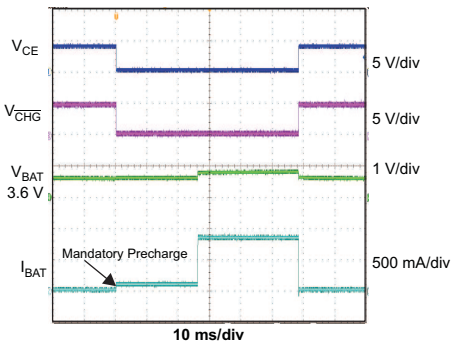
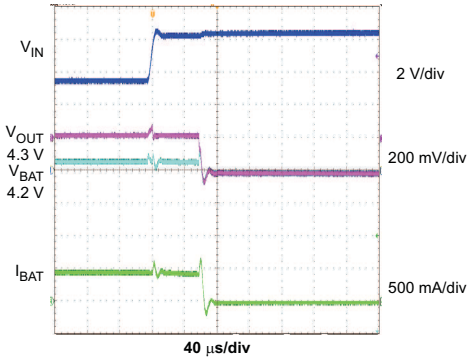
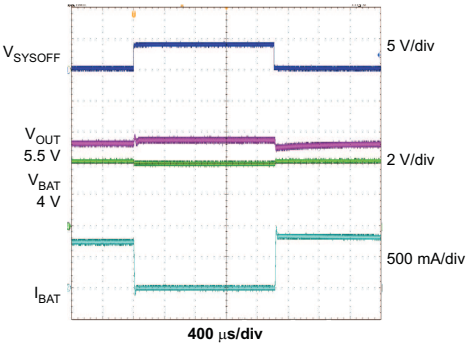


Figure 29. Charger On/Off Using $\overline{CE}$



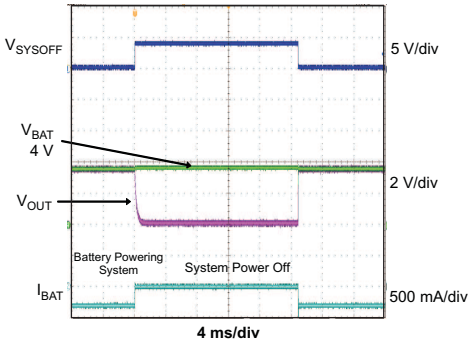
V_{IN} = 5.5 V to 8.5 V

Figure 30. OVP Fault



V_{IN} = 6 V

Figure 31. bq24075T, bq24079T System On/Off With Input Connected



V_{IN} = 0 V

Figure 32. bq24075T, bq24079T System On/Off With Input Not Connected

Typical Applications (continued)

10.2.2 bq24072T in a Host Controlled Charger Application

The bq24072T is designed for applications that require a lower regulation on the system rail. For bq24072T, the OUT regulation threshold is set to VBAT+225mV. The lower regulation point protects downstream devices from the higher voltage on the supply. Additionally, the lower difference between the BAT and OUT outputs decreases the voltage drop during supplement events. The bq24072T also contains a TD input that enables/disables the termination function. See the "Termination Disable" section for more details.

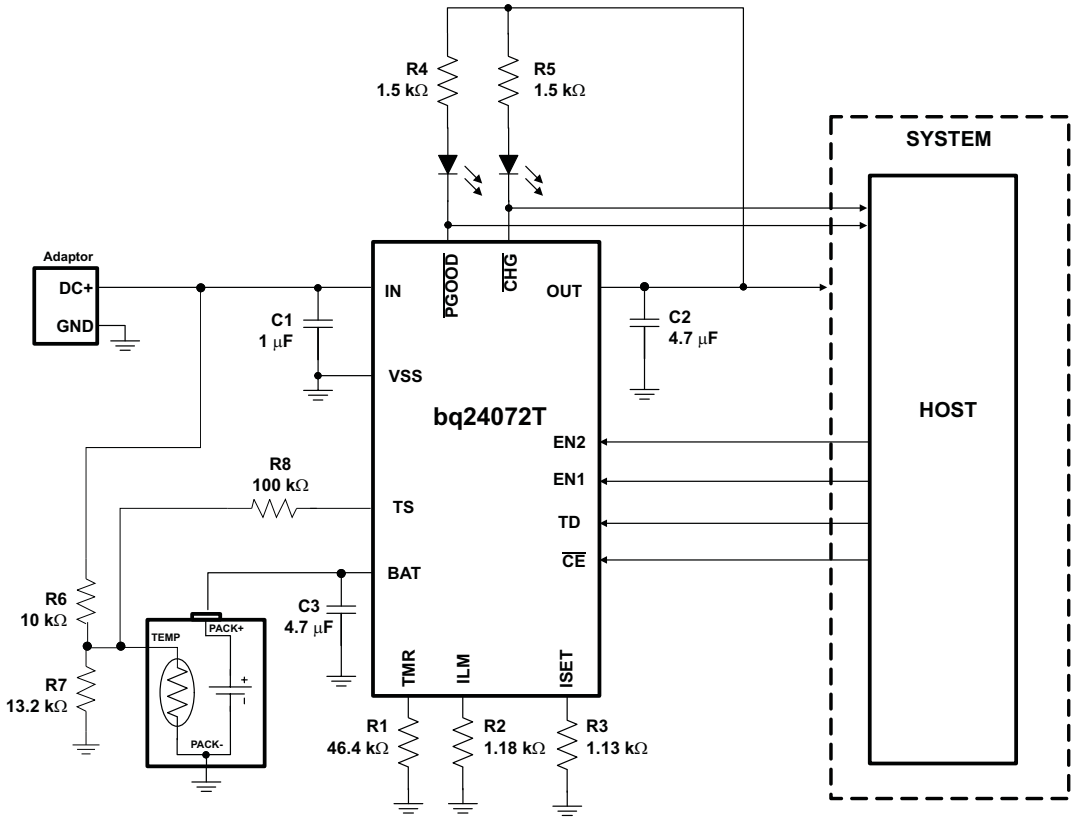


Figure 33. Using bq24072T in a Host Controlled Charger Application

10.2.2.1 Design Requirements

Refer to the *Typical Applications* for the Design Requirements.

10.2.2.2 Detailed Design Procedures

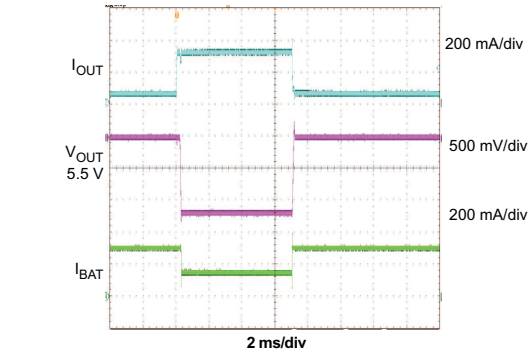
Refer to the *Typical Applications* for the Detailed Design Procedures.

10.2.2.2.1 Termination Disable:

Connect TD high to disable termination. Connect TD low to enable termination.

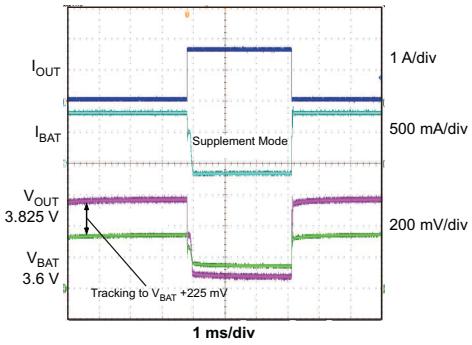
Typical Applications (continued)

10.2.2.3 Application Curves



I_{LOAD} = 25 mA TO 250 mA

Figure 34. Entering and Exiting, DPPM Mode



R_{LOAD} = 20 Ω to 40 Ω

Figure 35. bq2472T Entering and Exiting Battery, Supplement Mode

11 Power Supply Recommendations

11.1 Power On

When VIN exceeds the UVLO threshold, the bq2407xT powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Once V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, $\overline{PGOOD}$ is driven low to indicate the valid power status and the $\overline{CE}$, EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO **AND** V_{IN} > V_{BAT} + $V_{IN(DT)}$ **AND** V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)] all internal timers and other circuit blocks are activated. The device then checks for short-circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. When V_{OUT} is above V_{SC}, the FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of $\overline{CE}$, EN1 and EN2 as well as the input voltage conditions.

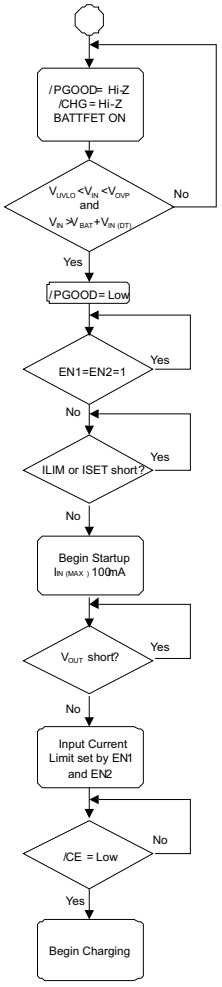


Figure 36. Startup Flow Diagram

Power On (continued)

11.1.1 Half-Wave Adapters

Some adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with adapters under those conditions, the bq2407xT family keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external adapters using 50 Hz networks. The input must not drop below the UVLO voltage for the charger to work properly. Thus, the battery voltage should be above the UVLO to help prevent the input from dropping out. Additional input capacitance may be needed.

When the input is between V_{UVLO} and $V_{IN(DT)}$, the device enters sleep mode. After entering sleep mode for 20ms the internal FET connection between the IN and OUT pin is disabled and pulling the input to ground will not discharge the battery, other than the leakage on the BAT pin. If one has a full 1000mAHr battery and the leakage is 10µA, then it would take 1000mAHr/10µA = 100000 hours (11.4 years) to discharge the battery. The battery ‘s self discharge is typically 5 times higher than this

12 Layout

12.1 Layout Guidelines

1. To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq2407xT, with short trace runs to both IN, OUT and GND (thermal pad).
2. All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
3. The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces

The bq2407xT family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the SLUA271 application note: *QFN/SON PCB Attachment Application*.

12.2 Layout Example

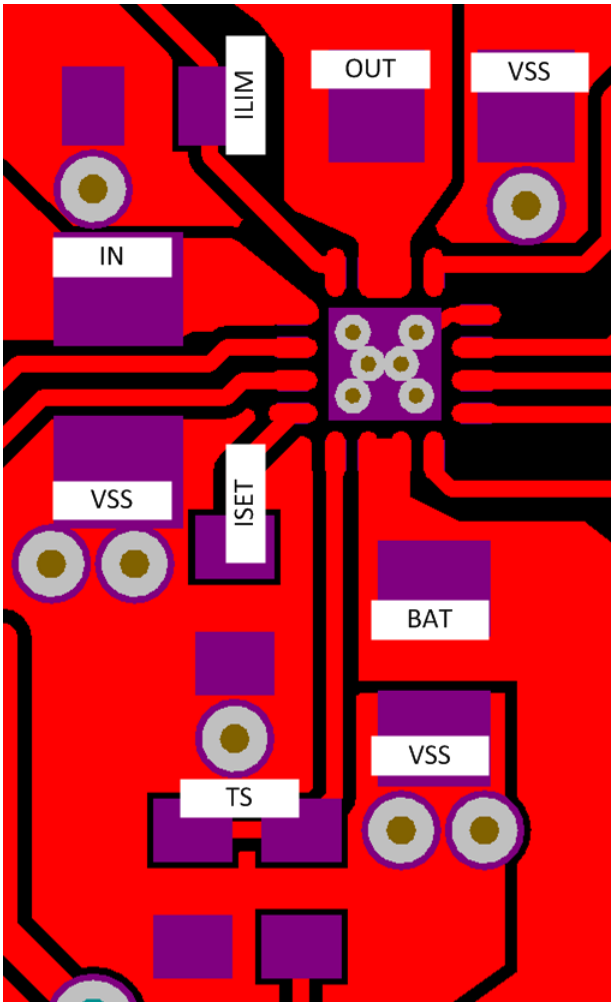


Figure 37. bq2407xT Layout

12.3 Thermal Package

The bq2407xT family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to V_{SS}. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note. The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient).

The mathematical expression for θ_{JA} is: = (T_J – T) / P

Where:

T_J = chip junction temperature
T = ambient temperature
P = device power dissipation
Factors that can influence the measurement and calculation of θ_{JA} include
Whether or not the device is board mounted
Trace size, composition, thickness, and geometry
Orientation of the device (horizontal or vertical)
Volume of the ambient air surrounding the device under test and airflow
Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to 3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from Equation 8 when a battery pack is being charged :

$$P = [V_{IN} – V_{OUT}] \times I_{OUT} + [V_{OUT} – V_{BAT}] \times I_{BAT} \quad (8)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24072T	Click here	Click here	Click here	Click here	Click here
bq24075T	Click here	Click here	Click here	Click here	Click here
bq24079T	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24072TRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PAP	Samples
BQ24072TRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PAP	Samples
BQ24075TRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OEC	Samples
BQ24075TRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OEC	Samples
BQ24079TRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OED	Samples
BQ24079TRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OED	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

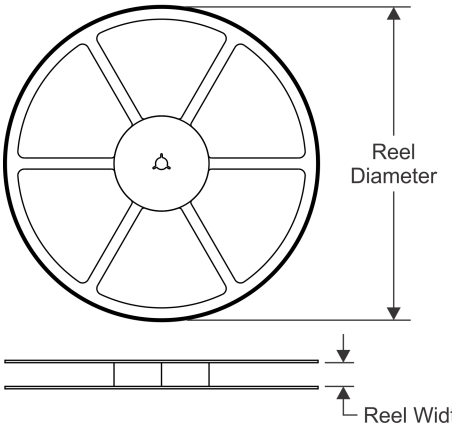
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

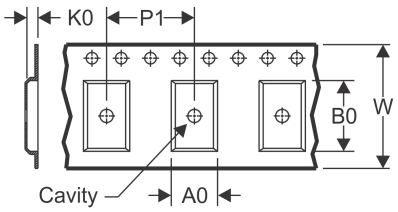
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

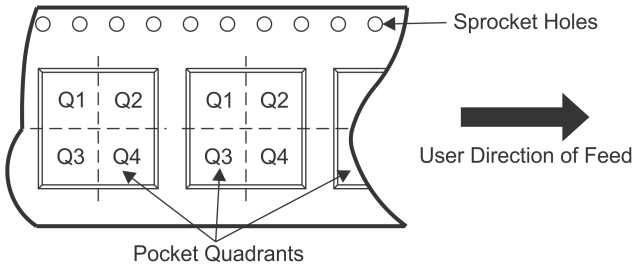


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

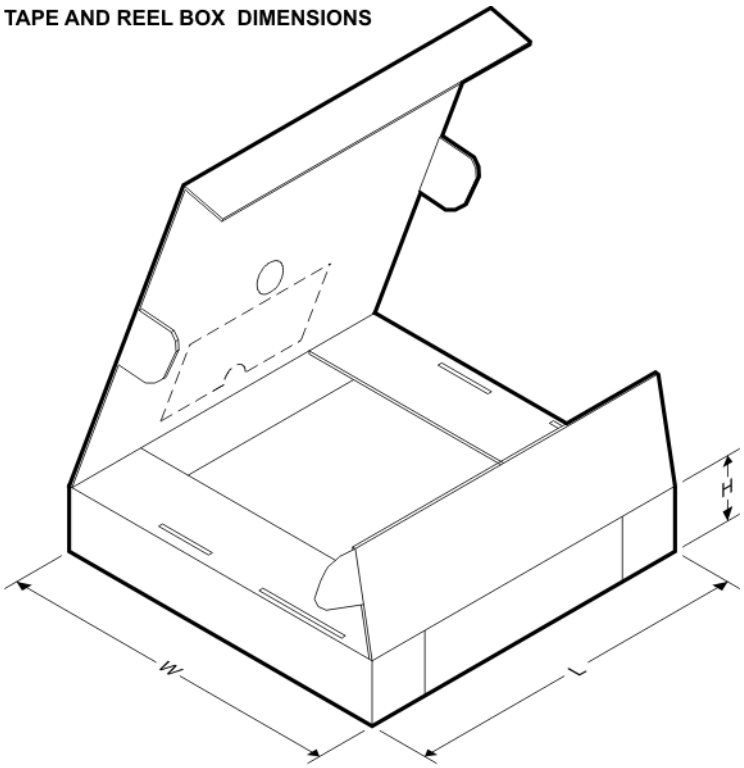
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24072TRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24072TRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24072TRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075TRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075TRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079TRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079TRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079TRGTT	QFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079TRGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

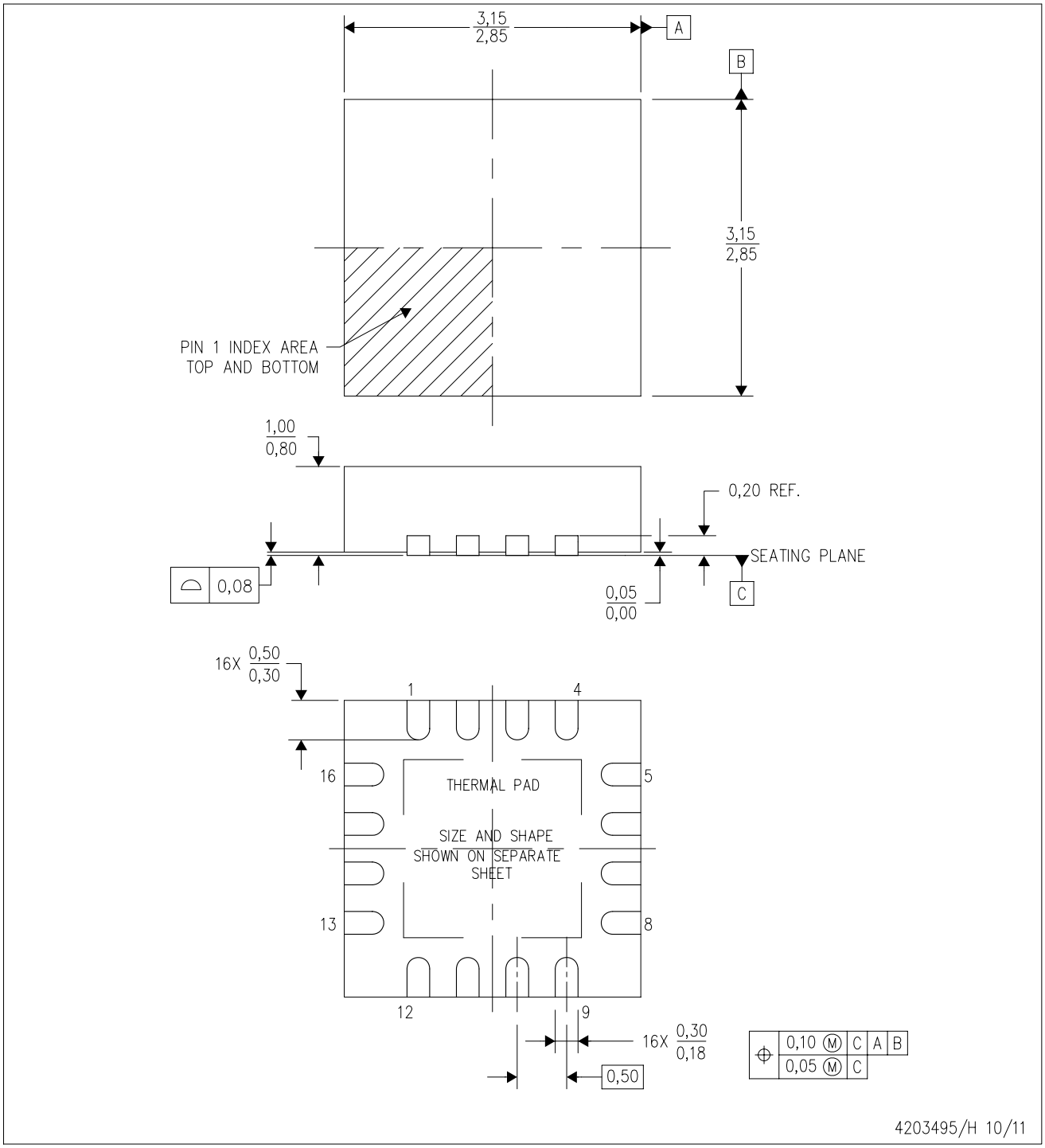
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24072TRGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24072TRGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24072TRGTT	QFN	RGT	16	250	210.0	185.0	35.0
BQ24075TRGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24075TRGTT	QFN	RGT	16	250	210.0	185.0	35.0
BQ24079TRGTR	QFN	RGT	16	3000	338.0	355.0	50.0
BQ24079TRGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ24079TRGTT	QFN	RGT	16	250	338.0	355.0	50.0
BQ24079TRGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

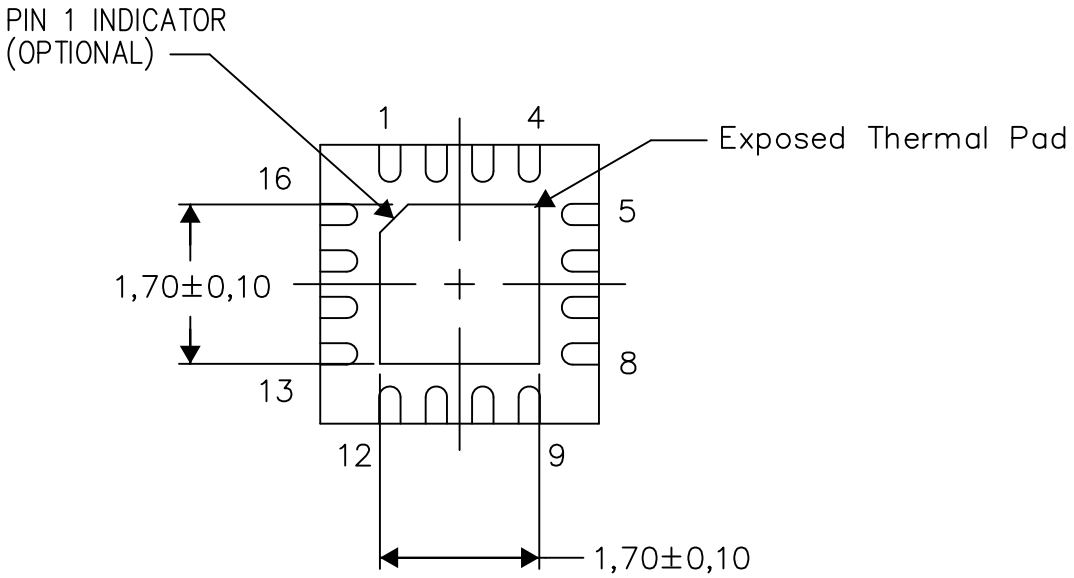
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



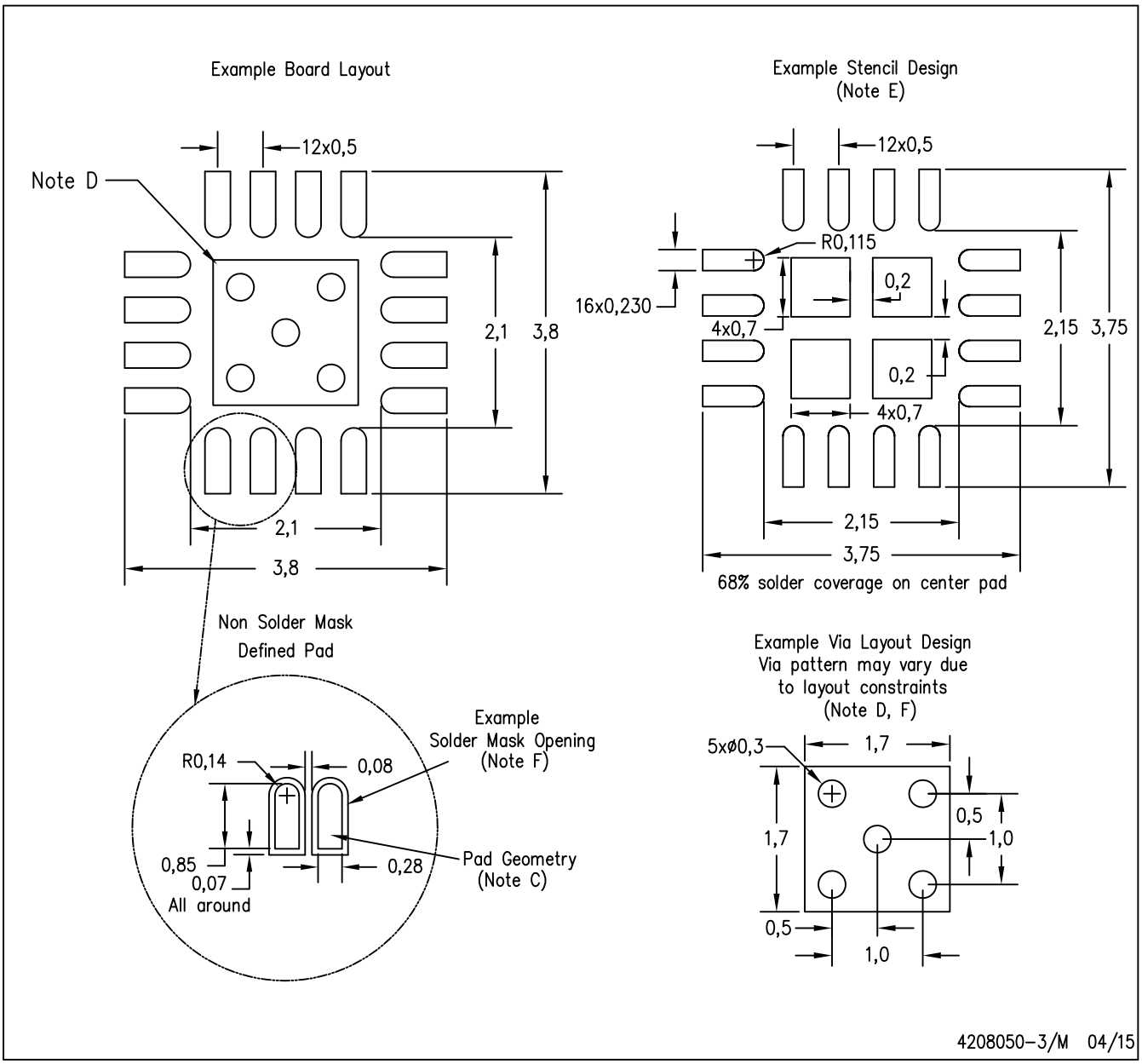
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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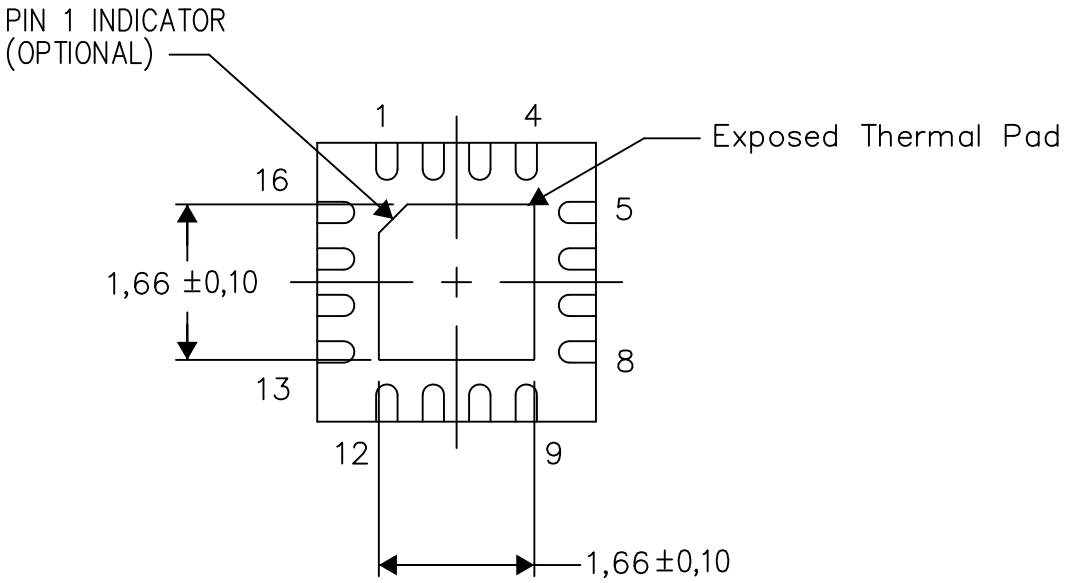
The exposed thermal pad dimensions for this package are shown in the following illustration.



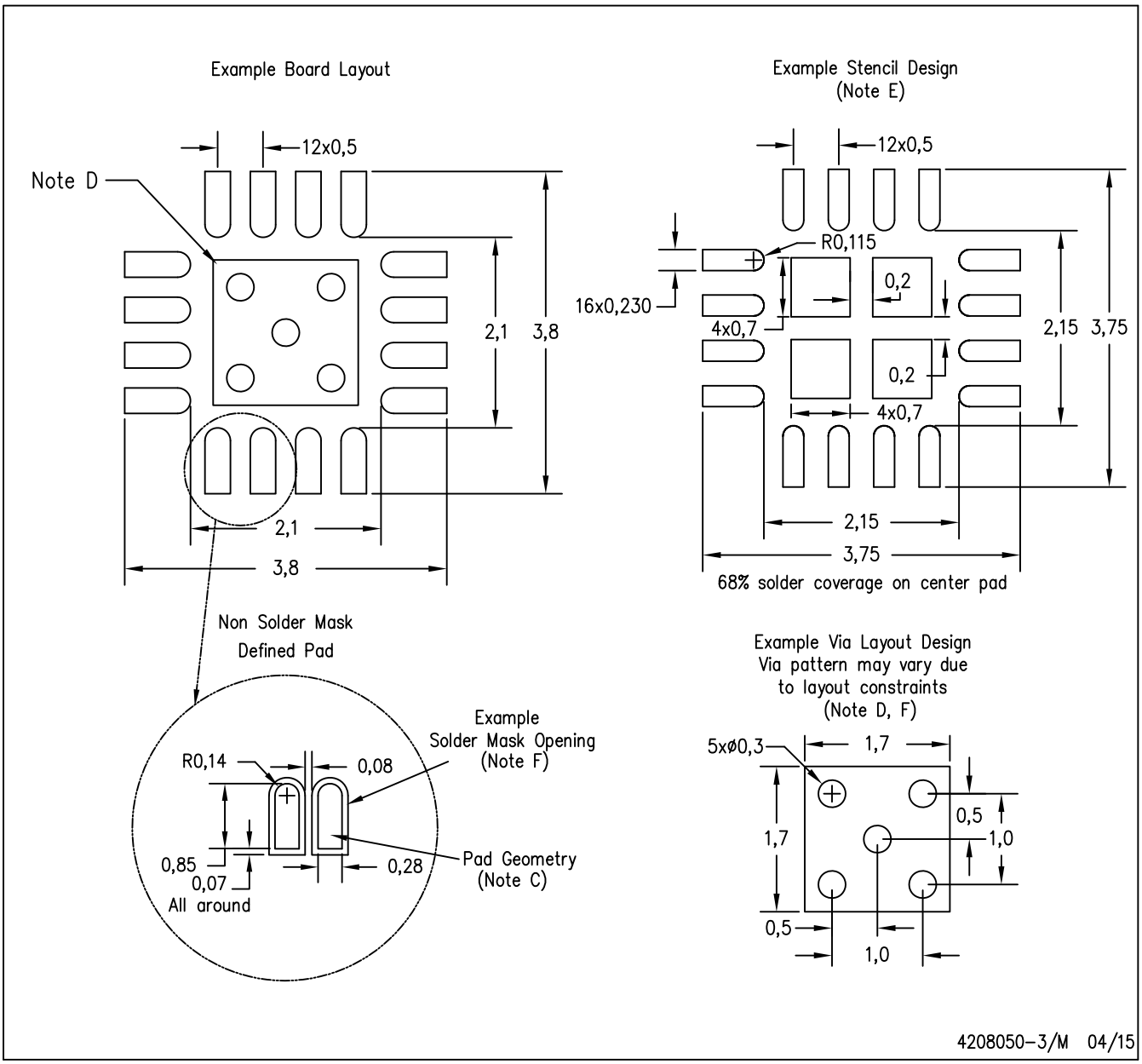
Bottom View

Exposed Thermal Pad Dimensions

4206349–10/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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