![Texas Instruments logo] **TEXAS INSTRUMENTS**
Data sheet acquired from Harris Semiconductor
SCHS105C – Revised October 2003

CD40175B Types

CMOS Quad 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

Features:

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- Noise margin (full package-temperature range) =
    1 V at V_{DD} = 5 V
    2 V at V_{DD} = 10 V
    2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load
- Functional equivalent to TTL 74175
- Standardized symmetrical output characteristics

Applications:
- Shift registers
- Buffer/storage registers
- Pattern generators

CD40175B FUNCTION DIAGRAM

- CD40175B consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and $\overline{Q}$ outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).
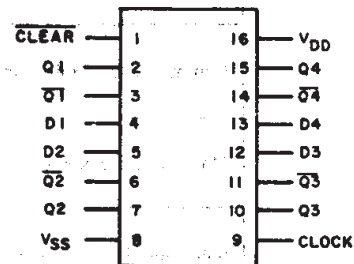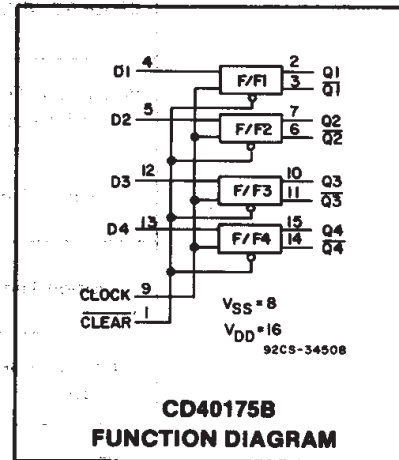
V_{DD} = PIN 16
V_{SS} = PIN 8

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = −55ºC to +100ºC 500mW
  For T_A = +100ºC to +125ºC .... Derate Linearity at 12mW/ºC to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package-Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... −55ºC to +125ºC
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65ºC to +150ºC
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265ºC

CD40175B Types

RECOMMENDED OPERATING CONDITIONS at TA = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		VDD (V)	LIMITS		UNITS
			MIN.	MAX.	
Supply-Voltage Range (For TA = Full Package-Temperature Range)		—	3	18	V
Data Setup Time	tSU	5	120	—	ns
		10	50	—	
		15	40	—	
Data Hold Time	tH	5	80	—	ns
		10	40	—	
		15	30	—	
Clock Input Frequency	fCL	5	—	2	MHz
		10	dc	5	
		15	—	6.5	
Clock Input Rise or Fall Time	trCL, tfCL	5	—	15	µs
		10	—	15	
		15	—	15	
Clock Input Pulse Width	tWL, tWH	5	250	—	ns
		10	100	—	
		15	75	—	
$\overline{\text{Clear}}$ Pulse Width	tWL	5	200	—	ns
		10	80	—	
		15	60	—	
$\overline{\text{Clear}}$ Removal Time	tREM	5	250	—	ns
		10	100	—	
		15	80	—	

* Inputs Protected by CMOS Protection Network

92CM-34509

Fig. 1 – Logic diagram (1 of 4 flip-flops).

CD40175B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				+25			UNITS
		Vo (V)	VIN (V)	VDD (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent		—	0, 5	5	1	1	30	30	—	0.02	1	
Device		—	0, 10	10	2	2	60	60	—	0.02	2	
Current		—	0, 15	15	4	4	120	120	—	0.02	4	µA
Max.	IDD	—	0, 20	20	20	20	600	600	—	0.04	20	
Output Low		0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	
(Sink) Current		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
Min.	IOL	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High		4.6	0, 5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	mA
(Source)		2.5	0, 5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
Current		9.5	0, 10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
Min.	IOH	13.5	0, 15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage:		—	0, 5	5	0.05				—	0	0.05	
Low-Level		—	0, 10	10	0.05				—	0	0.05	
Max.	VOL	—	0, 15	15	0.05				—	0	0.05	V
Output Voltage:		—	0, 5	5	4.95				4.95	5	—	
High-Level		—	0, 10	10	9.95				9.95	10	—	
Min.	VOH	—	0, 15	15	14.95				14.95	15	—	
Input Low		0.5, 4.5	—	5	1.5				—	—	1.5	
Voltage		1, 9	—	10	3				—	—	3	
Max.	VIL	1.5, 13.5	—	15	4				—	—	4	V
Input High		0.5, 4.5	—	5	3.5				3.5	—	—	
Voltage		1, 9	—	10	7				7	—	—	
Min.	VIH	1.5, 13.5	—	15	11				11	—	—	V
Input Current Max.	IIN	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10⁻⁵	±0.1	µA

Fig. 2 – Definition of setup, hold, propagation delay, and removal times.

*(LH) OR (HL) OPTIONAL

92CS-20069R3

TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

INPUTS			OUTPUTS	
CLOCK	DATA	CLEAR	Q	Q̄
⌐	0	1	0	1
⌐	1	1	1	0
⌐	X	1	Q	Q̄
X	X	0	0	1

1=High Level   X=Don't Care   0=Low Level

CD40175B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input tr, tf = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Transition Time	tTHL, tTLH	5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time Clock to Q Output	tPHL, tPLH	5	—	220	400	
		10	—	90	160	
		15	—	70	120	
Propagation Delay Time $\overline{CLEAR}$ to Q Output	tPHL	5	—	325	500	ns
		10	—	130	200	
		15	—	100	150	
Minimum Pulse Width Clock	tWH	5	—	110	250	
		10	—	45	100	
		15	—	35	75	
$\overline{Clear}$	tWL	5	—	100	200	
		10	—	40	80	
		15	—	30	60	
Maximum Clock Frequency	fCL	5	2	4.5	—	
		10	5	11	—	MHz
		15	6.5	14	—	
Maximum Clock Rise or Fall Time	trCL, tfCL	5	15	—	—	
		10	15	—	—	μs
		15	15	—	—	
Minimum Data Setup Time	tSU	5	—	60	120	
		10	—	25	50	
		15	—	20	40	
Minimum Data Hold Time	tH	5	—	40	80	
		10	—	20	40	ns
		15	—	15	30	
Minimum $\overline{Clear}$ Removal Time ‡	tREM	5	—	125	250	
		10	—	50	100	
		15	—	40	80	
Input Capacitance	CIN	—	—	5	7.5	pF

‡ $\overline{CLEAR}$ signal must be high prior to positive-going transition of CLOCK pulse.
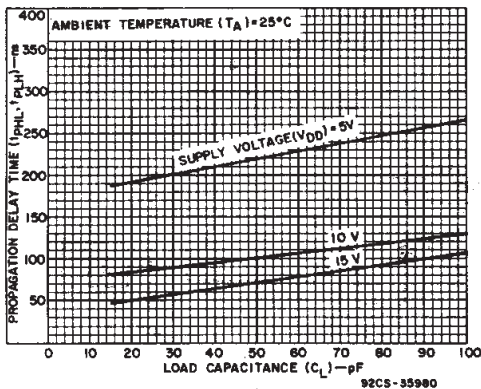
Fig. 3 – Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.
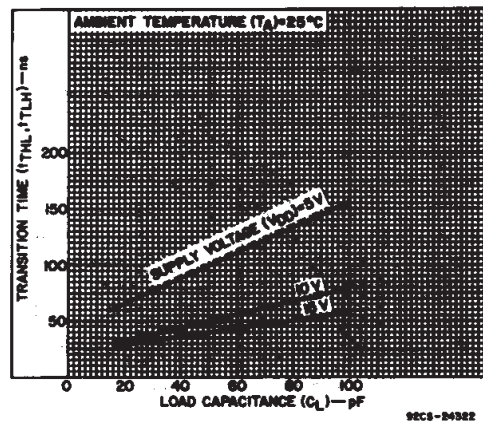
Fig. 4 – Typical transition time as a function of load capacitance.
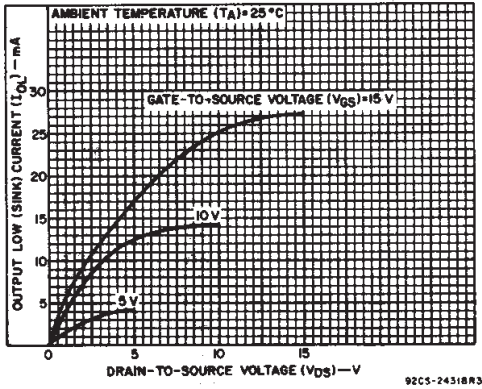
Fig. 5 – Typical output low (sink) current characteristics.
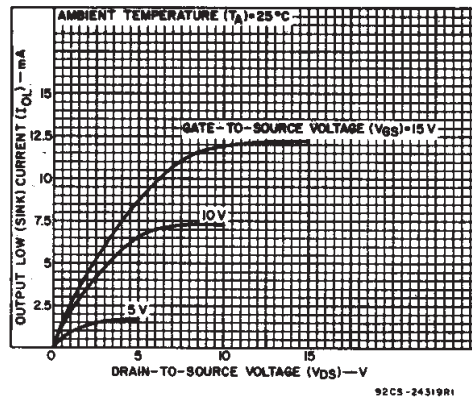
Fig. 6 – Minimum output low (sink) current characteristics.

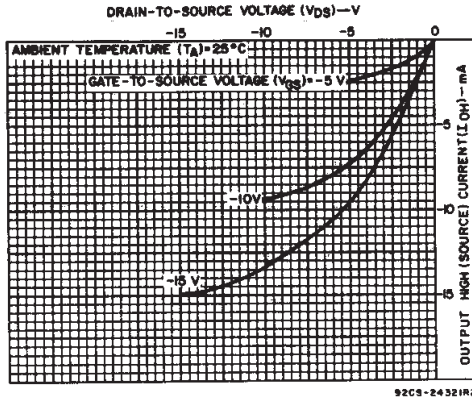Fig. 7 – Typical output high (source) current characteristics.

Fig. 8 – Minimum output high (source) current characteristics.

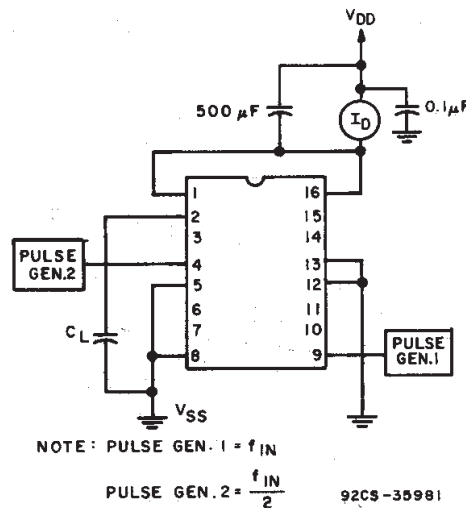Fig. 9 – Typical dynamic power dissipation as a function of CLOCK frequency.

NOTE: PULSE GEN. I = f_{IN}

PULSE GEN. 2 = $\dfrac{f_{IN}}{2}$

92CS-35981

Fig. 10 – Dynamic power dissipation test circuit.

CD40175B Types
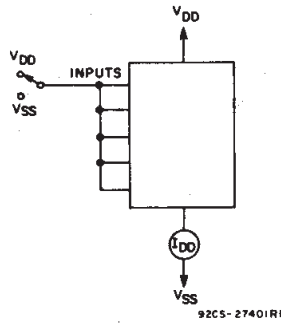
Fig. 11 – Quiescent device current test circuit.
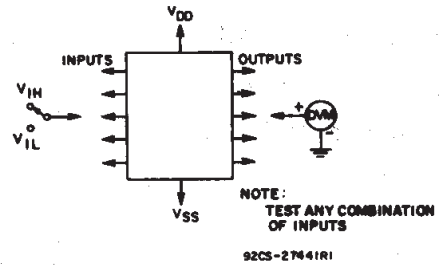
Fig. 12 – Noise immunity test circuit.
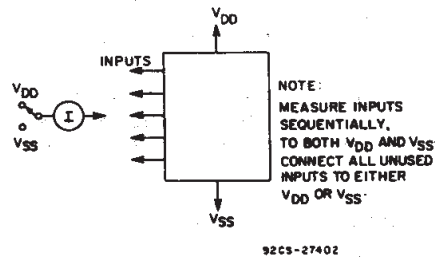
Fig. 13 – Input leakage current test circuit.

92CS-35083
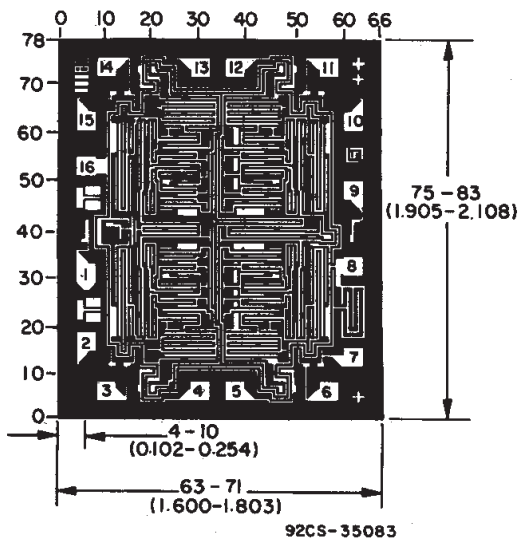
Dimensions and pad layout for CD40175BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40175BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40175BE	Samples
CD40175BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40175BE	Samples
CD40175BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40175BF3A	Samples
CD40175BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM	Samples
CD40175BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM	Samples
CD40175BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM	Samples
CD40175BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM	Samples
CD40175BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175BM	Samples
CD40175BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175B	Samples
CD40175BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40175B	Samples
CD40175BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0175B	Samples
CD40175BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0175B	Samples
CD40175BW	OBSOLETE	WAFERSALE	YS	0		TBD	Call TI	Call TI			

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD40175B, CD40175B-MIL :

● Catalog: CD40175B

● Military: CD40175B-MIL

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40175BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD40175BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40175BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40175BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD40175BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD40175BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)　　　　　PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E   12/2002

NOTES:　A. All linear dimensions are in inches (millimeters).
　　　　B. This drawing is subject to change without notice.
　　　Ⓒ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
　　　Ⓓ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

◁ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
       ⚠C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
       ⚠D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

16x0,55

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

D   4,50
     4,30

6,60
6,20

1   8

5,10
4,90

C

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10

4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

0,35

1,60

0,07
All Around

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211284−3/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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