THREE PLLs BASED CLOCK GENERATOR FOR DIGITAL TV APPLICATIONS

FEATURES

- **High Performance Clock Generator**
- **Clock Input Compatible With LVCMOS/LVTTL**
- **Requires a 54-MHz Input Clock to Generate Multiple Output Frequencies**
- **Low Jitter for Clock Distribution**
- **Generates the Following Clocks:**
  - **VIDCLK 74.175824 MHz/54 MHz (Buffered)**
  - **AUDCLK 16.9344 MHz/12.288 MHz**
  - **CPUCLK 64 MHz**
  - **ASICCLK 32 MHz**
  - **USBCLK 48 MHz**
  - **MCCLK 38.4 MHz/19.2 MHz/12 MHz**
- **Operates From Single 3.3-V Supply**
- **Low Peak-to-Peak Period Jitter (150 ps Max)**
- **PLLs Are Powered Down, if No Valid REF_IN Clock (< 5 MHz) is Detected or the V_{DD} is Below 2 V**
- **PLL Loop Filter Components Integrated**
- **Packaged in TSSOP (PW) 20-Pin Package**
- **Industrial Temperature Range -40°C to 85°C Applications**

APPLICATIONS

- **Digital Television With a Memory Card Interface**

DESCRIPTION

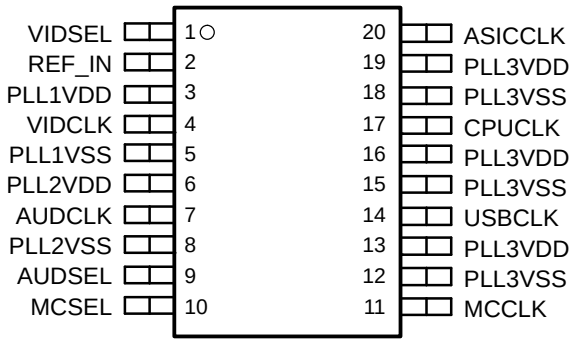
The CDC5806 is a clock generator which synthesizes video clocks, audio clocks, CPU clock, ASIC clock, USB clock, and a memory card clock from a 54-MHz system clock.

Three phase-locked loops (PLLs) are used to generate the different frequencies from the system clock. On-chip loop filters and internal feedback eliminate the need for external components.

Since the CDC5806 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLLs. The PLL stabilization time begins after the reference clock input has a stable phase and frequency.

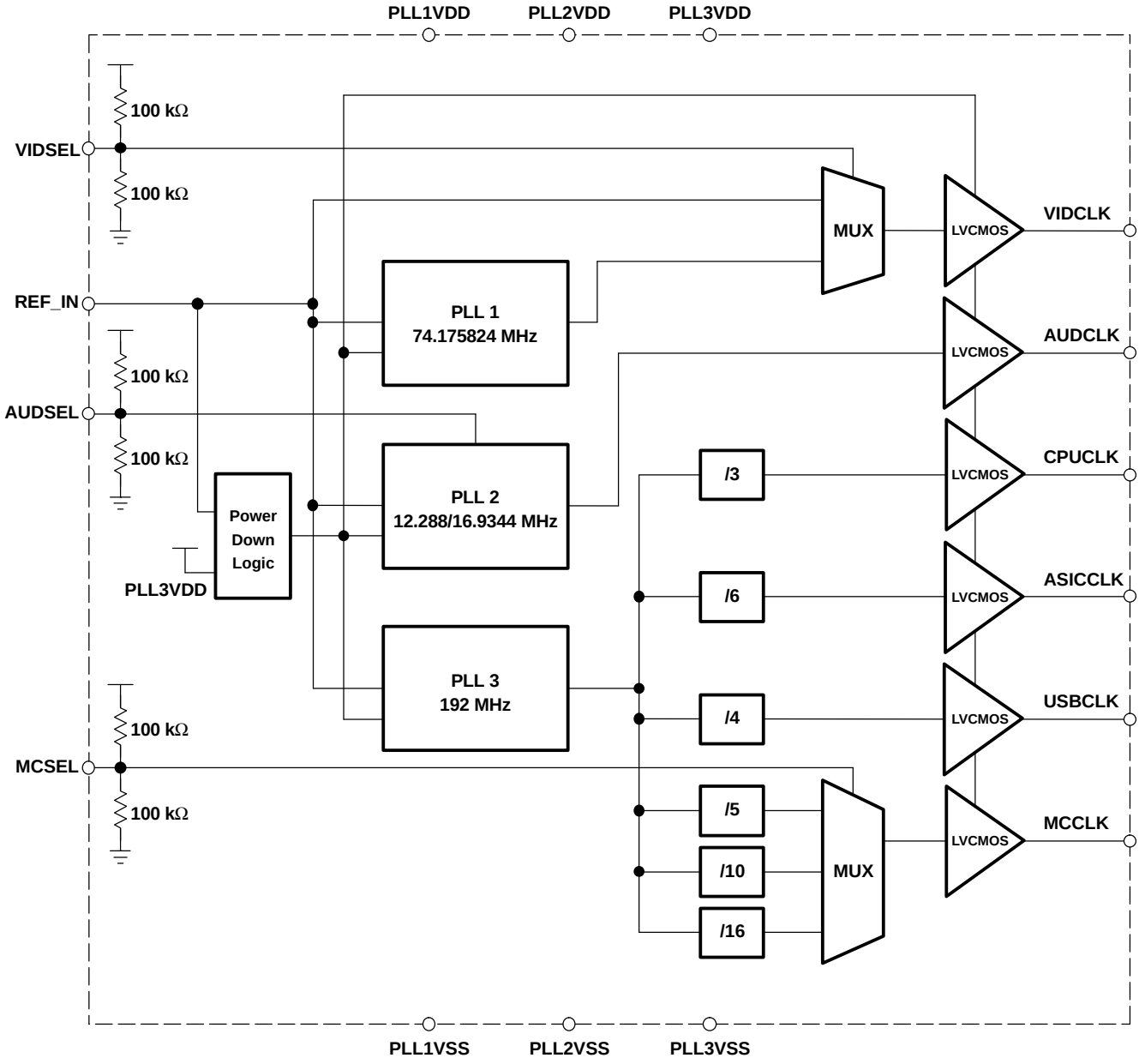
The device operates from a single 3.3-V supply voltage. The CDC5806 device is characterized for operation from -40°C to 85°C.

PW PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO	TYPE	DESCRIPTION
REF_IN	2	I LVCMOS	Reference frequency input
VIDSEL	1	I LVCMOS	VIDSEL select input for VIDCLK. It selects between 74.175824 MHz from PLL1 and buffered input frequency of 54 MHz, 100k||100k pull to mid-level.
AUDSEL	9	I LVCMOS	AUDSEL select input for AUDCLK. It selects between 16.9344 MHz and 12.288 MHz from PLL2, 100k||100k pull to mid level.
MCSEL	10	I LVCMOS	MCSEL select input for MCCLK. It selects from 38.4 MHz, 19.2 MHz, and 12 MHz from PLL3, 100k||100k pull to mid level.
VIDCLK	4	O LVCMOS	VIDCLK output 74.175824 MHz or 54 MHz
AUDCLK	7	O LVCMOS	AUDCLK output 16.9344 MHz or 12.288 MHz
CPUCLK	17	O LVCMOS	CPUCLK output 64 MHz
ASICCLK	20	O LVCMOS	ASICCLK output 32 MHz
USBCLK	14	O LVCMOS	USBCLK output 48 MHz
MCCLK	4	O LVCMOS	MCCLK output 38.4 MHz / 19.2 MHz / 12 MHz
VDD_PLL1	3	Power	3.3-V supply for PLL1 and VIDCLK
VDD_PLL2	6	Power	3.3-V supply for PLL2 and AUDCLK
VDD_PLL3	13, 16, 19	Power	3.3-V supply for PLL3 and CPUCLK, ASICCLK, USBCLK, and MCCLK
VSS_PLL1	5	Ground	Ground for PLL1 and VIDCLK
VSS_PLL2	8	Ground	Ground for PLL2 and AUDCLK
VSS_PLL3	12, 15, 18	Ground	Ground for PLL3 and CPUCLK, ASICCLK, USBCLK, and MCCLK

FUNCTIONAL DESCRIPTION OF THE LOGIC

Table 1. Select Function for Video, Audio, CPU, ASIC, and USB Clocks

VIDSEL	AUDSEL	VIDCLK	AUDCLK	CPUCLK	ASICCLK	USBCLK	Unit
L	L	54 (buffered)	12.288	64	32	48	MHz
L	M	Reserved	Reserved	64	32	48	MHz
L	H	54 (buffered)	16.9344	64	32	48	MHz
M	L	Reserved	Reserved	64	32	48	MHz
M	M	Reserved	Reserved	REFCLK/3	REFCLK/6	REFCLK/4	MHz
M	H	Reserved	Reserved	64	32	48	MHz
H	L	74.175824	12.288	64	32	48	MHz
H	M	Reserved	Reserved	64	32	48	MHz
H	H	74.175824	16.9344	64	32	48	MHz

Table 2. Select Function for MC Clock

MCSEL	MCCLK	MCCLK if VIDSEL = M and AUDSEL = M	UNIT
H	12 MHz	REFCLK/16	MHz
M	38.4 MHz	REFCLK/5	MHz
L	19.2 MHz	REFCLK/10	MHz

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

Supply voltage range, V_{DD}	0.5 V to 4.6 V
Input voltage range, V_I(2)	0.5 V to VDD + 0.5 V
Output voltage range, V_O(2)	0.5 V to VDD + 0.5 V
Input current ($V_I < 0$, $V_I > V_{DD}$)	±20 mA
Continuous output current, I_O	±50 mA
Package thermal impedance, Θ_{JA}(3): TSSOP20 package	104 C/W
Storage temperature range T_{stg}	65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51 (no airflow condition) and JEDEC2S1P (high-k board).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	-40		85	°C
V_{IL}	Low-level input voltage REF_IN			0.3 V_{DD}	V
$V_{I\ thresh}$	Input voltage threshold REF_IN		0.5 V_{DD}		V
V_{IH}	High-level input voltage REF_IN	0.7 V_{DD}			V
$V_{IL(L)}$	Three level input low for control inputs			0.13 V_{DD}	V
$V_{IM(M)}$	Three level input mid for control inputs	0.4 V_{DD}		0.6 V_{DD}	V
$V_{IH(H)}$	Three level input high for control inputs	0.87 V_{DD}			V
I_{OH}	High-level output current LVCMOS			-8	mA
I_{OL}	Low-level output current LVCMOS			8	mA
V_I	Input voltage range LVCMOS	0		3.6	V
C_L	Output load LVCMOS	5		10	pF

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

PARAMETER		MIN	NOM	MAX	UNIT
REF_IN REQUIREMENTS					
f_{CLK_IN}	LVCMOS REF_IN clock input frequency		54		MHz
t_r / t_f	Rise and fall time REF_IN signal (20% to 80%)			4	ns
$duty_{REF}$	Duty cycle of REF_IN (VDD/2)	40%		60%	
AUDSEL, VIDSEL, MCSEL REQUIREMENTS					
t_r / t_f	Rise and fall time (20% to 80%)			4	ns
t_1	Transitional time between AUDSEL and VIDSEL control pins(1)	6			ns

(1) If VIDSEL and AUDSEL are switched from from one state to another state at the same time, then the CPUCLK, ASICCLK, USBCLK, or MCCLK are affected. This is due to the selected reserved mode with VIDSEL = M and AUDSEL = M. This mode causes the PLL3 to be bypassed and the REFCLK will be seen with the appropriate divider ratios at the correspondent outputs.

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL							
I_{CC}	Supply current		Test load		35	45	mA
$I_{CC(ST)}$	Standby current		f_{IN} = 0 MHz, V_{DD} = 3.6 V			1.1	mA
V_{PUC}	Supply voltage threshold for power up control circuit				2		V
LVCMOS							
V_{IK}	LVCMOS input voltage		V_{DD} = 3 V, I_I = –18 mA			–1.2	V
I_I	REF_IN input current		V_I = 0 V or V_{DD}			±5	µA
I_I	SELECT input current		V_I = 0 V or V_{DD}			±55	µA
V_{OH}	High-level output voltage		V_{DD} = MIN to MAX, I_{OH} = –5 mA	V_{DD} – 0.4			V
V_{OL}	Low-level output voltage		V_{DD} = MIN to MAX, I_{OL}= 5 mA			0.4	V
I_{OH}	High-level output current		V_{DD} = 3 V, V_O = V_{DD} – 0.4 V	–5			mA
			V_{DD} = 3.3 V, V_O = 1.65 V		–35		
			V_{DD} = 3.6 V, V_O = 0.4 V			–75	
I_{OL}	Low-level output current		V_{DD} = 3 V, V_O = 0.4 V	5			mA
			V_{DD} = 3.3 V, V_O = 1.65 V		35		
			V_{DD} = 3.6 V, V_O = V_{DD} – 0.4V			75	
AC							
C_I	Input capacitance (Ref_IN)				2		pF
f_{err}	Output accuracy VIDCLK, CPUCLK, ASICCLK, USBCLK, MCCLK (38.4 MHz, 19.2 MHz, 12 MHz)		See Note (1)			±1	ppm
f_{err}	Output accuracy AUDCLK (16.9344 MHz, 12.288 MHz)		See Note (1)			±40	ppm
t_L	PLL start up lock time		See Figure 2			0.5	ms
$t_{L(\omega)}$	PLL lock time after frequency change on AUDCLK		See Figure 2			0.5	ms
odc	Duty cycle for MCCLK		Threshold = VDD/2	47%	50%	53%	
odc	Duty cycle for VIDCLK, AUDCLK, CPUCLK, ASICCLK, USBCLK		Threshold = VDD/2	45%	50%	55%	
t_r/t_f	Rise and fall time of the output		20%–80% of V_O			2	ns
$t_{jit(per)}$	Peak-to-peak period jitter for	VIDCLK (74.175824 MHz)	10,000 cycles		75	150	ps
		CPUCLK (64 MHz)			60	150	
		USBCLK (48 MHz)			65	150	
		MCCLK (38.4 MHz)			65	150	
		ASICCLK (32 MHz)			60	150	
		MCCLK (19.2 MHz)			70	150	
		AUDCLK (16.9344 MHz)			75	150	
		AUDCLK (12.288 MHz)			85	150	
		MCCLK (12 MHz)			65	150	

(1) This parameter is assured by design as a result of the chosen settings of the internal dividers in the PLL's.

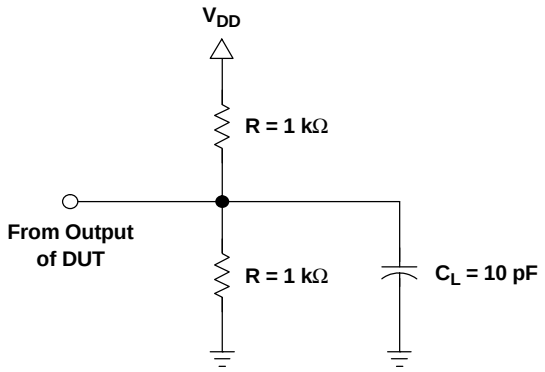


Figure 1. LVCMOS Output Test Load

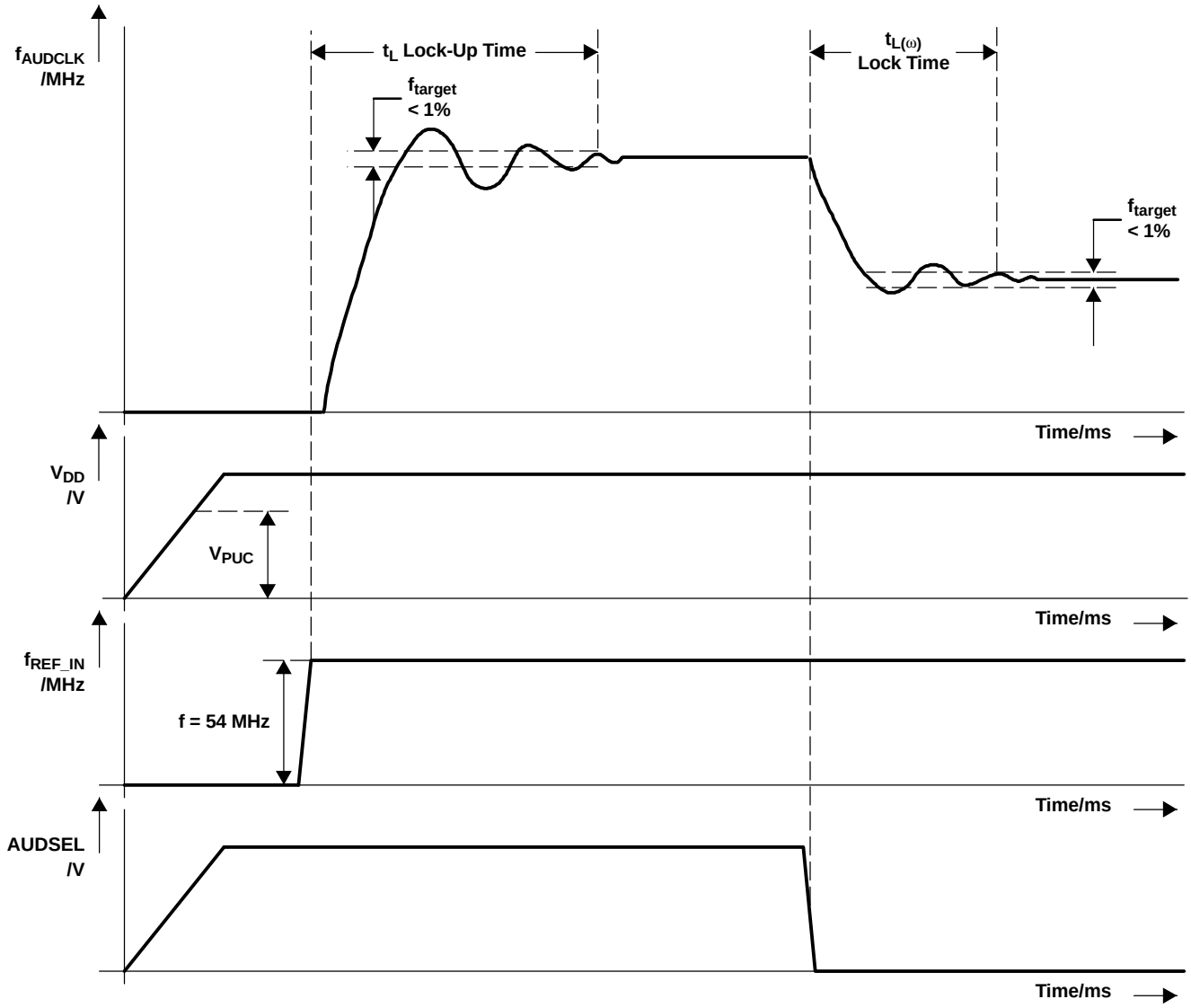


Figure 2. Timing Diagram of PLL Lock Time of Audio Clock

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC5806PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC5806	Samples
CDC5806PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC5806	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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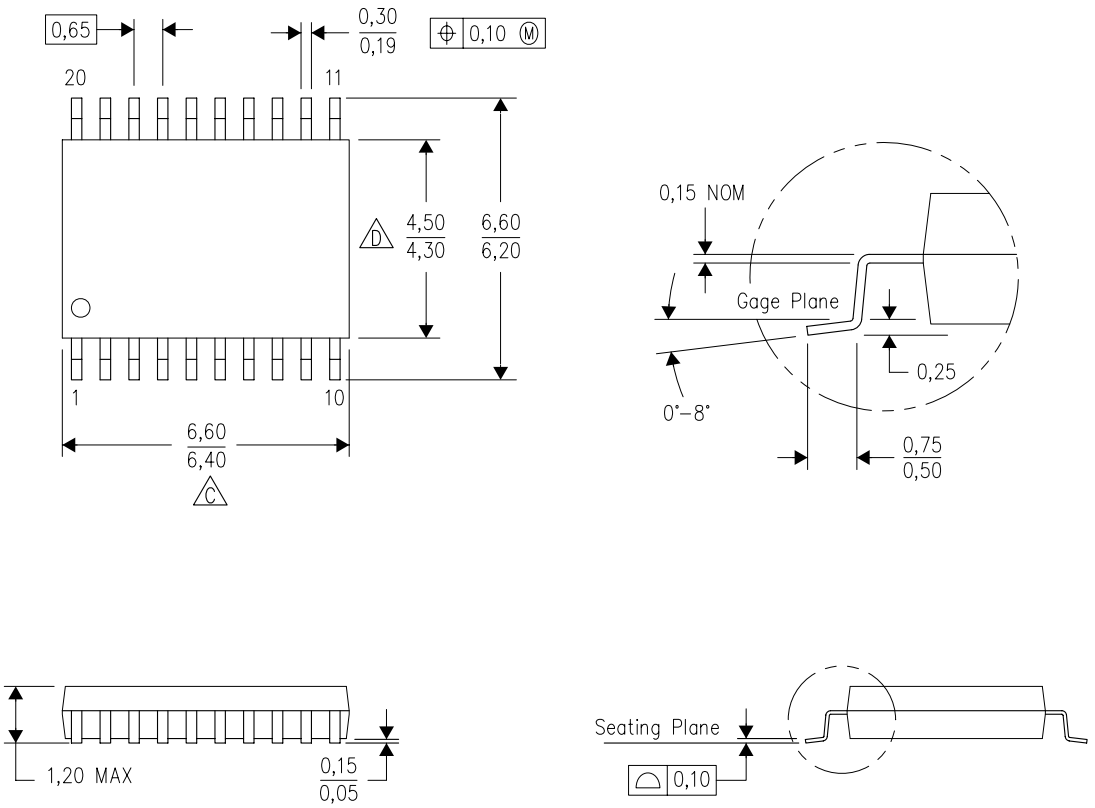
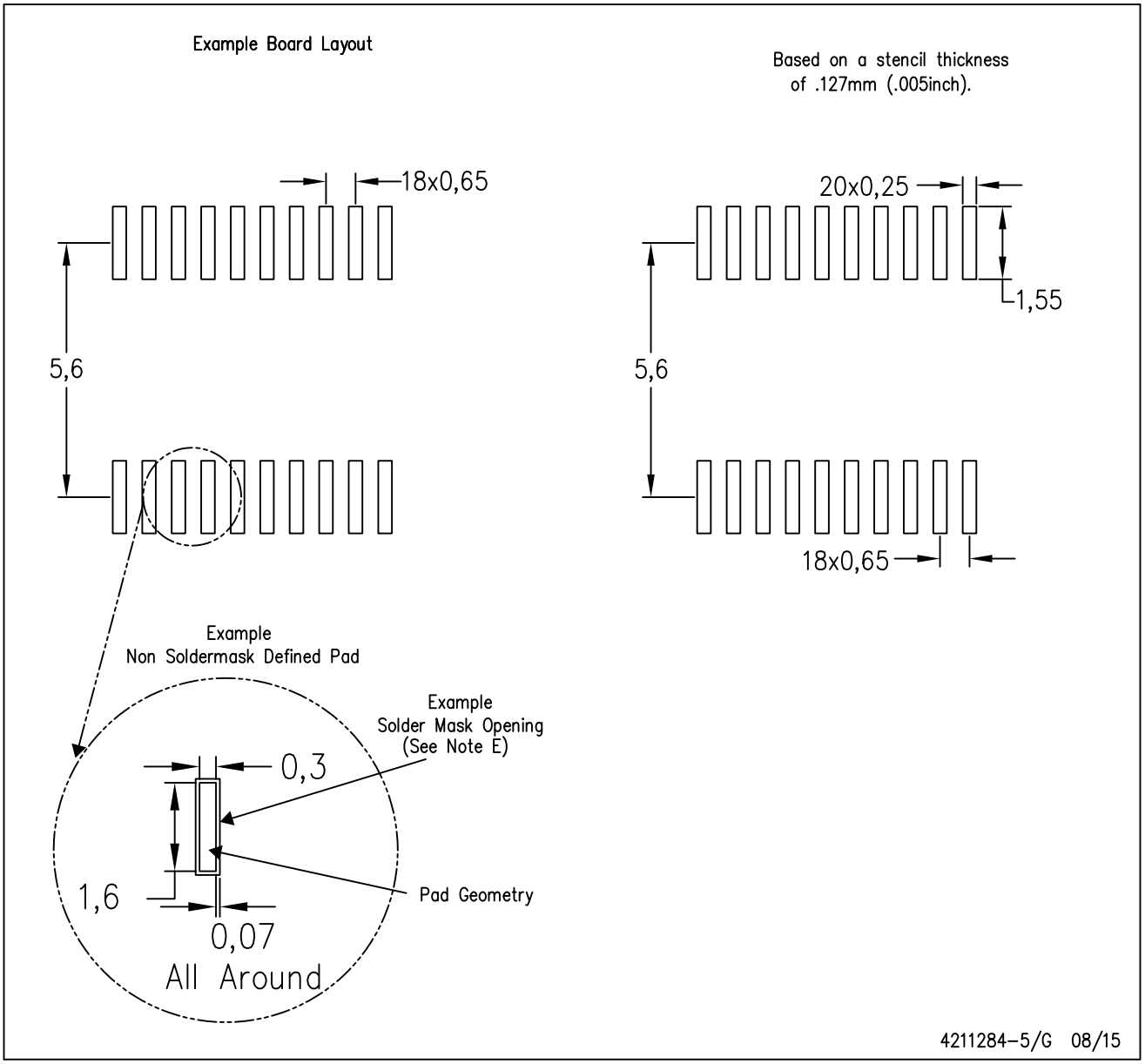
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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