DS92LV1260 Six Channel 10 Bit BLVDS Deserializer

Check for Samples: DS92LV1260

FEATURES

- **Deserializes One to Six BusLVDS Input Serial Data Streams with Embedded Clocks**
- **Seven Selectable Serial Inputs to Support n+1 Redundancy of Deserialized Streams**
- **Seventh Channel has Single Pin Monitor Output That Reflects Input From Seventh Channel Input**
- **Parallel Clock Rate up to 40MHz**
- **On Chip Filtering for PLL**
- **Absolute Maximum Worst Case Power Dissipation = 1.9W at 3.6V**
- **High Impedance Inputs Upon Power Off (V_{cc} = 0V)**
- **Single Power Supply at +3.3V**
- **196-pin NFBGA Package (Low-profile Ball Grid Array) Package**
- **Industrial Temperature Range Operation: −40°C to +85°C**

DESCRIPTION

The DS92LV1260 integrates six deserializer devices into a single chip. The chip uses a 0.25u CMOS process technology. The DS92LV1260 can simultaneously deserialize up to six data streams that have been serialized by the Texas Instruments DS92LV1021 or DS92LV1023 Bus LVDS serializers. The device also includes a seventh serial input channel that serves as a redundant input.

Each deserializer block in the DS92LV1260 operates independently with its own clock recovery circuitry and lock-detect signaling.

The DS92LV1260 uses a single +3.3V power supply with a typical power dissipation of 1.2W at 3.3V with a PRBS-15 pattern. Refer to the Connection Diagrams for packaging information.

Block Diagram

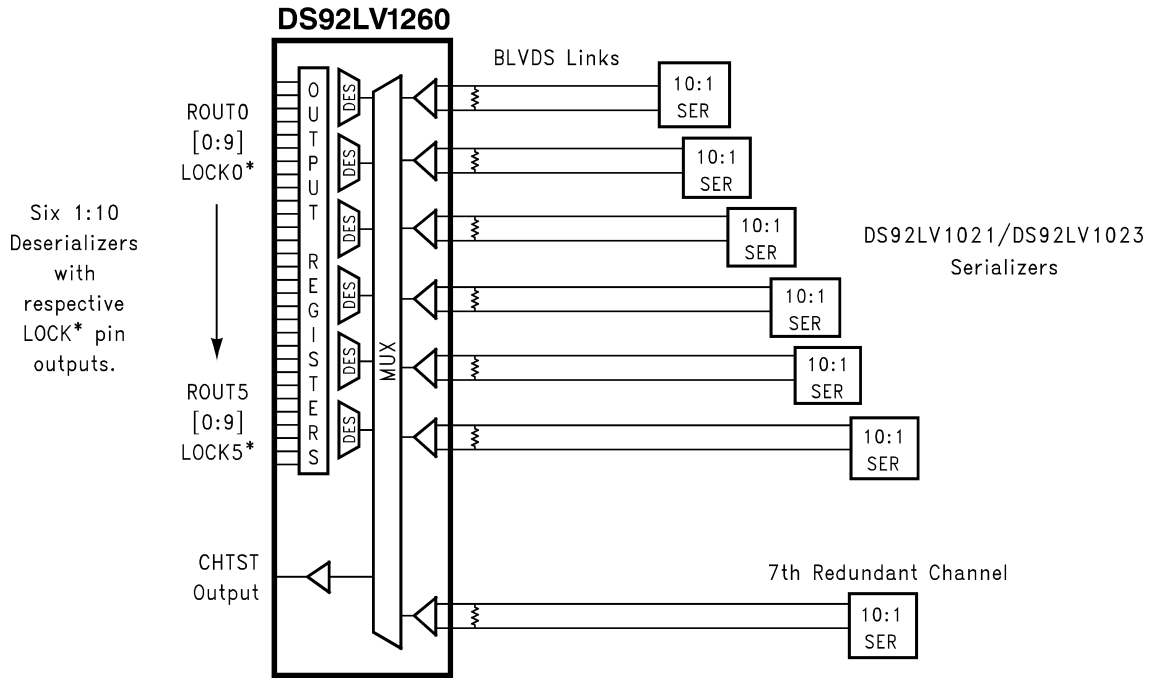


Figure 1. Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{cc})	-0.3 to 4V
Bus LVDS Input Voltage (Rin +/-)	-0.3V to 3.9V
Maximum Package Power Dissipation @25°C	3.7W
Package Thermal Resistance	
θ_{JA} 196 NFBGA:	34°C/W
θ_{JC} 196 NFBGA:	8°C/W
Storage Temp. Range	-65°C to +150°C
Junction Termperature	+150°C
Lead Temperature (Soldering 10 Sec)	+225°C
ESD Rating:	
Human Body Model	>3KV
Machine Model	>750V
Reliability Information	
Transistor Count	35,682

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Operating Free Air Temperature (T_A)	-40°C to +85°C
Operating Frequency	16-40 MHz

Electrical Characteristics (1)

Basic functionality and specifications per deserializer channel will be similar to DS92LV1212A. Over recommended operating supply and termperature ranges unless otherwise specified. (2)

Parameter		Test Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC Specifications:							
V_{IH}	High Level Input Voltage		REN,REFCLK,$\overline{PWRDWN}$, SEL (0:2),R_{OUT}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage				-0.87	-1.5	V
I_{IN}	Input Current	V_{in} = 0 or 3.6V		-10		+10	uA
V_{OH}	High Level Output Voltage	I_{OH} = -6mA	R_{out}, $\overline{RCLK}$, $\overline{LOCK}$	2	3	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 6mA		GND	0.18	0.4	V
I_{OS}	Output short Circuit Current	V_{out} = 0V, (3)		-15	-46	-85	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWRDWN}$ or REN = 0.8V, V_{out} = 0V or V_{CC}		-10	+/-0.2	+10	uA

(1) Current into the device pins is defined as positive. Current out of device pins is defined as negative. Voltage are referenced to ground except VTH and VTL which are differential voltages.
(2) Typical values are given for Vcc = 3.3V and TA =25°C
(3) Only one output should be shorted at a time. Do not exceed maximum package power dissipation capacity.

Electrical Characteristics[1] (continued)

Basic functionality and specifications per deserializer channel will be similar to DS92LV1212A. Over recommended operating supply and termperature ranges unless otherwise specified.[2]

Parameter		Test Conditions	Pin/Freq.	Min	Typ	Max	Units
Bus LVDS DC specifications							
V_{TH}	Differential Threshold High Voltage	VCM = 1.1V (V_{RI+}-V_{RI-})	RI+, RI-		+3	+50	mV
V_{TL}	Differential Threshold Low Voltage			-50	-2		mV
I_{IN}	Input Current	V_{in} = +2.4V, V_{cc} = 3.6 or 0V		-10	+/- 1	+10	uA
		V_{in} =0V, V_{cc} = 3.6 or 0V		-10	+/- 1	+10	uA
Supply Current							
I_{CCR}	Worst Case Supply Current	3.6V, 40 MHz, Checker Board Pattern, CL=15pF			460	530	mA
I_{CCXR}	Supply Current when Powered Down	$\overline{PWRDN}$= 0.8V REN = 0.8V			0.36	1	mA
Timing Requirements for REFCLK							
t_{RFCP}	REFCLK Period			25		62.5	ns
t_{RFDC}	REFCLK Duty Cycle			40	50	60	%
t_{RFCP}/t_{TCP}	Ratio of REFCLK to TCLK			0.95		1.05	
t_{RFTT}	REFCLK Transition Time					8	ns
Deserializer Switching Characteristics							
t_{RCP}	RCLK Period		RCLK	25		62.5	ns
t_{RDC}	RCLK Duty Cycle			43	50	55	%
t_{CHTST}	Period of Bus LVDS signal when CHTST is selected by MUX	See [4]	CHTST	25			ns
t_{CLH}	CMOS/TTL Low-to-High Transition Time		Rout, $\overline{LOCK}$, RCLK		1.7	6	ns
t_{CHL}	CMOS/TTL High-to-Low Transition Time				1.6	6	ns
t_{ROS}	Rout Data Valid before RCLK	See Figure 3		$0.4*t_{RCP}$			ns
t_{ROH}	Rout Data Valid after RCLK	See Figure 3		$-0.4*t_{RCP}$			ns
t_{HZR}	High to TRI-STATE Delay					10	ns
t_{LZR}	Low to TRI-STATE Delay					10	ns
t_{ZHR}	TRI-STATE to High Delay					12	ns
t_{ZLR}	TRI-STATE to Low Delay					12	ns
t_{DD}	Deserializer Delay	See Figure 2	RCLK	$1.75*t_{RCP}+5$	$1.75*t_{RCP}+7$	$1.75*t_{RCP}+10$	ns
		Room Temp 3.3V 40MHz		$1.75*t_{RCP}+6$	$1.75*t_{RCP}+7$	$1.75*t_{RCP}+9$	ns
t_{DSR1}	Deserializer PLL LOCK Time from PWRDN (with SYNCPAT)	See Figure 4 See [5]	40MHz			3	us
			20MHz			10	us

(4) Because the Bus LVDS serial data stream is not decoded, the maximum frequency of the CHTST output driver could be exceeded if the data stream were switched to CHTST. The maximum frequency of the BUS LVDS input should not exceed the parallel clock rate.

(5) For the purpose of specifying deserializer PLL performance t_{DSR1} and t_{DSR2} are specified with the REFCLK running and stable, and specific conditions of the incoming data stream (SYNCPATs). t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI−) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). The time to lock to random data is dependent upon the incoming data.

Electrical Characteristics[1] (continued)

Basic functionality and specifications per deserializer channel will be similar to DS92LV1212A. Over recommended operating supply and termperature ranges unless otherwise specified.[2]

Parameter		Test Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DSR2}	Deserializer PLL Lock Time from SYNCPAT	See Figure 5 See [5]	40MHz			2	us
			20MHz			5	us
t_{RNM}	Deserializer Noise Margin	See [6]	40MHz	450	920		ps
			20MHz	1200	1960		ps

(6) t_{RNM} is a measure of how much phase noise (jitter)the deserializer can tolerate in the incoming data stream before bit errors occur. The Deserializer Noise Margin is Specified By Design (GBD) using statistical analysis.

AC Timing Diagrams and Test Circuits

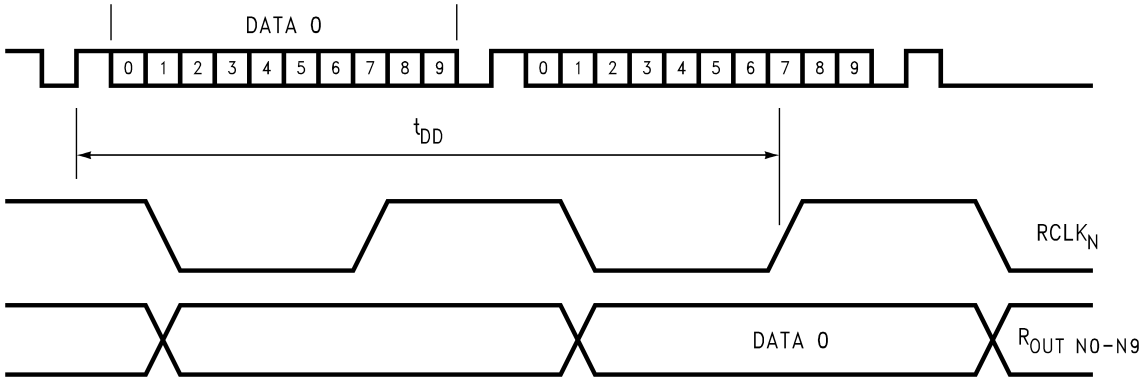


Figure 2. Deserializer Delay t_{DD}

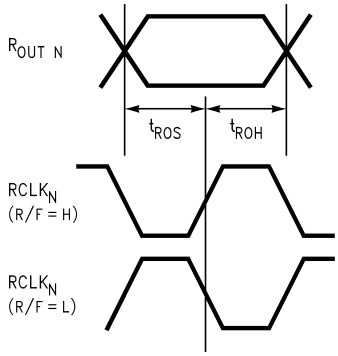


Figure 3. Output Timing t_{ROS} and t_{ROH}

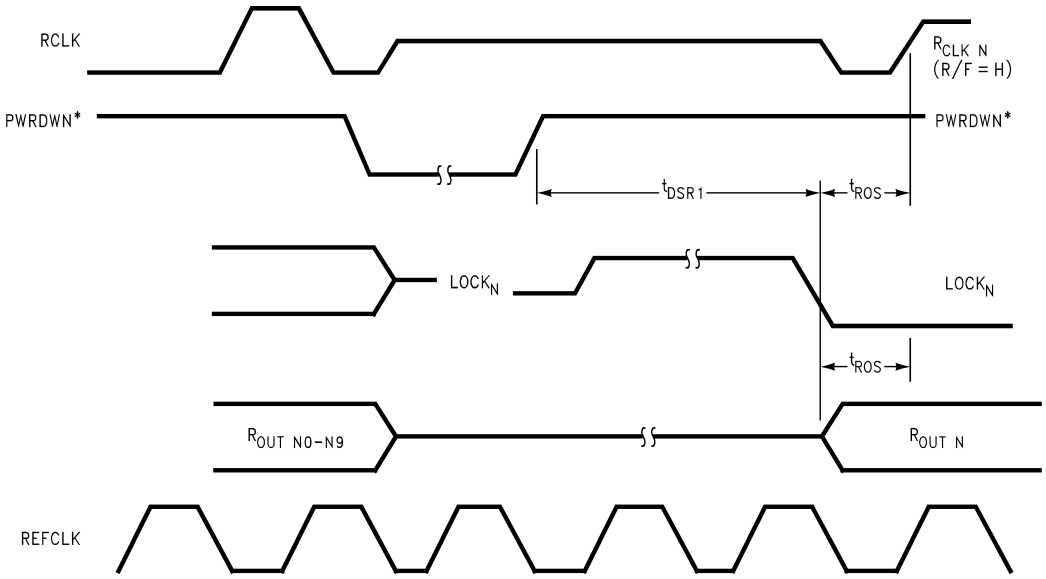


Figure 4. Locktime from PWRDN* t_{DSR1}

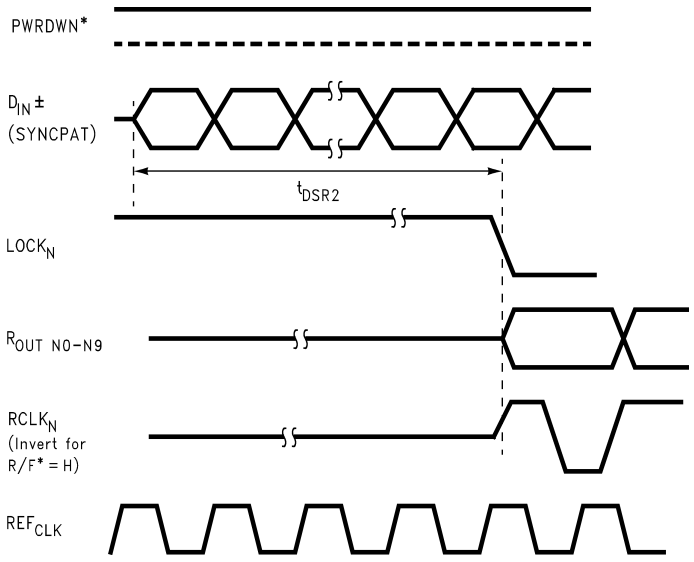


Figure 5. Locktime to SYNCPAT t_{DSR2}

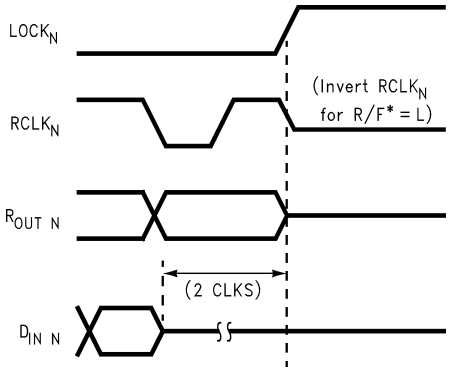


Figure 6. Unlock

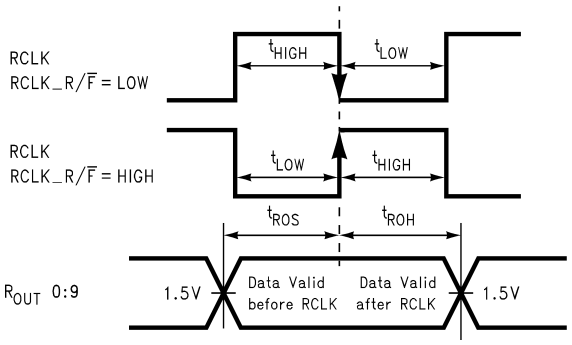


Figure 7. Deserializer Data Valid Out Times

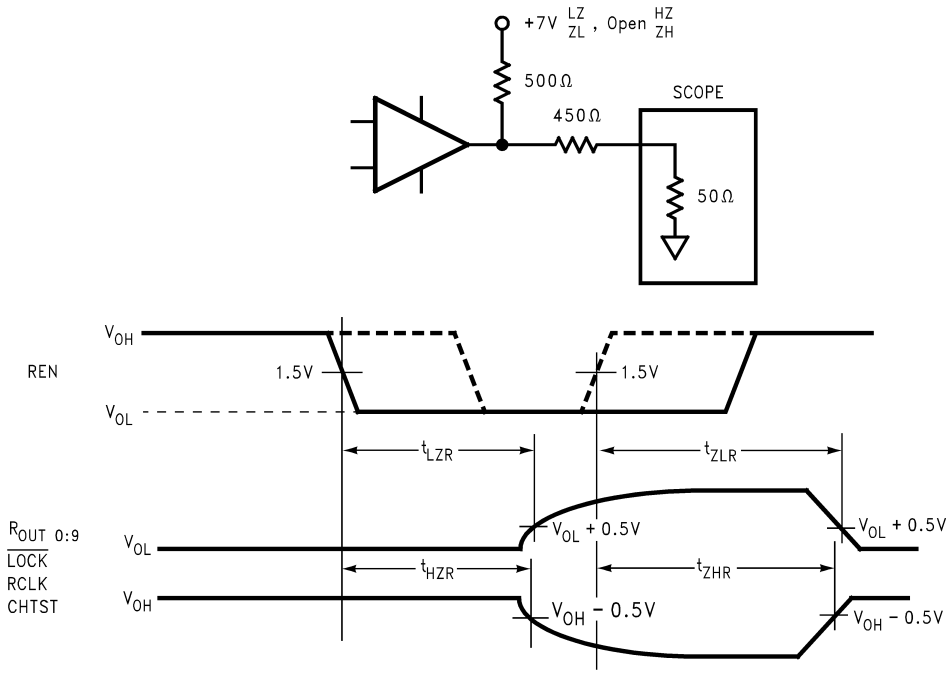
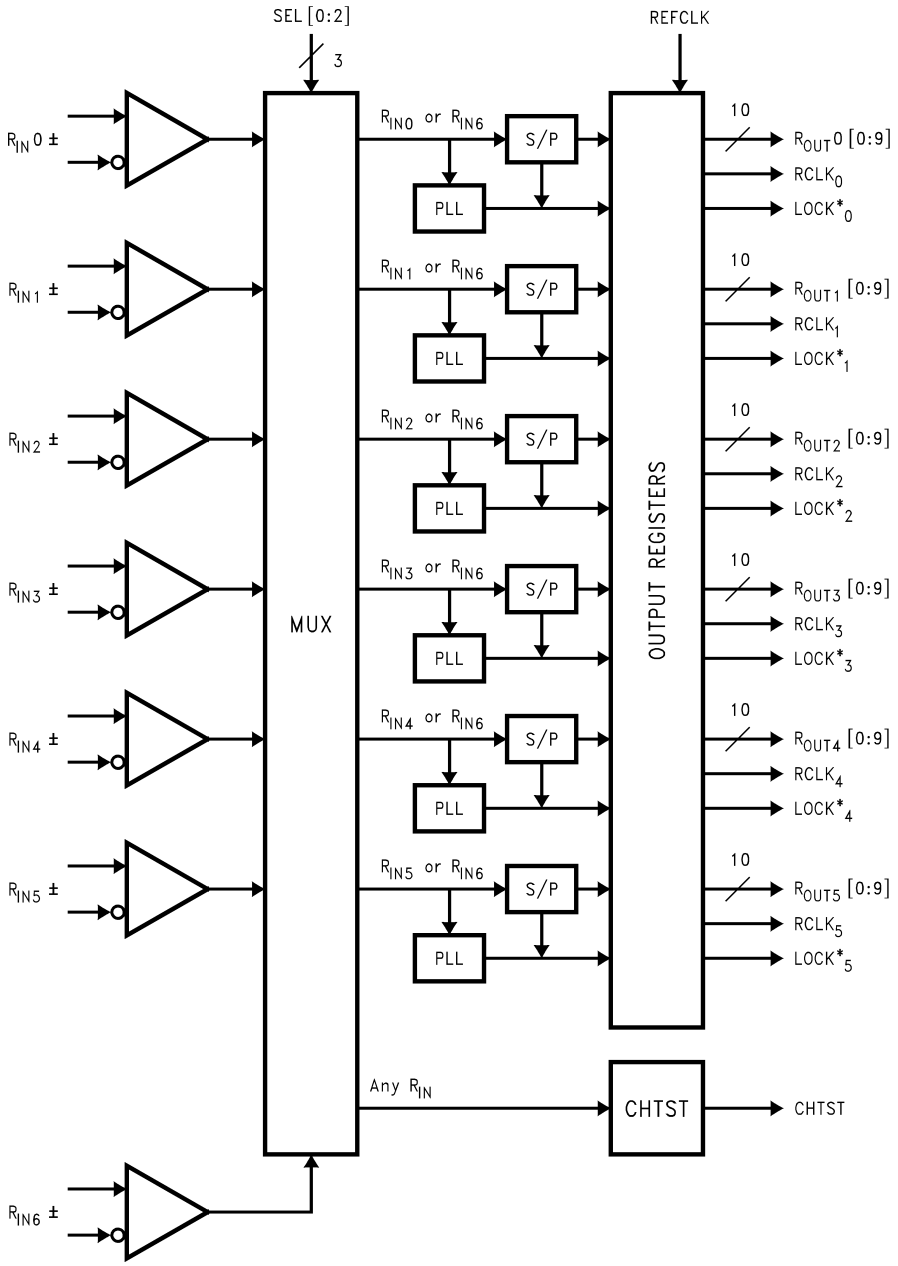


Figure 8. Deserializer TRI-STATE Test Circuit and Timing

Block Diagram



Control Pins Truth Table(1)

PWRDN	REN	SEL2	SEL1	SEL0	Rout	CHTST	LOCK[0:5]	RCLK[0:5]
H	H	L	L	L	Din6 Decoded to Rout 0 (0:9)(2)	Din0 (not decoded)	Active(3)	Active(4) (2)
H	H	L	L	H	Din6 Decoded to Rout 1 (0:9)(2)	Din1 (not decoded)	Active(3)	Active(4) (2)
H	H	L	H	L	Din6 Decoded to Rout 2 (0:9)(2)	Din2 (not decoded)	Active(3)	Active(4) (2)
H	H	L	H	H	Din6 Decoded to Rout 3 (0:9)(2)	Din3 (not decoded)	Active(3)	Active(4) (2)
H	H	H	L	L	Din6 Decoded to Rout 4 (0:9)(2)	Din4 (not decoded)	Active(3)	Active(4) (2)
H	H	H	L	H	Din6 Decoded to Rout 5 (0:9)(2)	Din5 (not decoded)	Active(3)	Active(4) (2)
H	H	H	H	L	Din6 is not Decoded	Z	Active(3)	Active(4) (2)
H	H	H	H	H	Din6 is not Decoded	Din6 (not decoded)	Active(3)	Active(4) (2)
L	X	X	X	X	Z	Z	Z	Z
H	L	X	X	X	Z	Z	Active(3)	Z

(1) The routing of the Din inputs to the Deserializers and to the CHTST outputs are dependent on the states of SEL [0:2].
(2) Rout n[0:9] and RCLK [0:5] are Tri-Stated when $\overline{\text{LOCK}}$n[0:5] is High.
(3) $\overline{\text{LOCK}}$ Active indicates that the $\overline{\text{LOCK}}$ output will reflect the state of it's respective Deserializer with regard to the selected data stream.
(4) RCLK Active indicates that the RCLK will be running if the Deserializer is locked. The timing of RCLK [0:5] with respect to Rout [0:5][0:9] is determined by RCLK_R/$\overline{\text{F}}$ Figure 6

FUNCTIONAL DESCRIPTION

The DS92LV1260 combines six 1:10 deserializers into a single chip. Each of the six deserializers accepts a BusLVDS data stream from Texas Instruments' DS92LV1021 or DS92LV1023 Serializer. The deserializers then recover the clock and data to deliver the resulting 10-bit wide words to the outputs. A seventh serial data input provides n+1 redundancy capability. The user can program the seventh input to be an alternative input to any of the six deserializers. Whichever input is replaced by the seventh input is then routed to the CHANNEL TEST (CHTST) pin on receiver output port.

Each of the 6 channels acts completely independent of each other. Each independent channel has outputs for a 10-bit wide data word, the recovered clock out, and the lock-detect output.

The DS92LV1260 has three operating states: Initialization, Data Transfer, and Resynchronization. In addition, there are two passive states: Powerdown and TRI-STATE.

The following sections describe each operating mode and passive state.

Initialization

Before the DS92LV1260 receives and deserializes data, it and the transmitting serializer devices must initialize the link. Initialization refers to synchronizing the Serializer's and the Deserializer's PLL's to local clocks. The local clocks must be the same frequency or within a specified range if from different sources. After all devices synchronize to local clocks, the Deserializers synchronize to the Serializers as the second and final initialization step.

Step 1: After applying power to the Deserializer, the outputs are held in TRI-STATE and the on-chip power-sequencing circuitry disables the internal circuits. When V_{cc} reaches V_{cc}OK (2.1V), the PLL in each deserializer begins locking to the local clock (REFCLK). A local on-board oscillator or other source provides the specified clock input to the REFCLK pin.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. Refer to the Serializer data sheet for the proper operation during this step of the Initialization State. The Deserializer identifies the rising clock edge in a synchronization pattern or random data and after 80 clock cycles will synchronize to the data stream from the serializer. At the point where the Deserializer's PLL locks to the embedded clock, the LOCKn pin goes low and valid data appears on the output. Note that this differs from pervious deserializers where the LOCKn signal was not synchronous to valid data appearing on the outputs.

Data Transfer

After initialization, the serializer transfers data to the deserializers. The serial data stream includes a start and stop bit appended by the serializer, which frame the ten data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

The Serializer transmits the data and clock bits (10+2 bits) at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 X 12 = 480 Mbps. Since only 10 bits are from input data, the serial 'payload' rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data is 40 X 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 20 MHz to 40 MHz nominal.

When one of six Deserializer channels synchronizes to the input from a Serializer, it drives its LOCKn pin low and synchronously delivers valid data on the output. The Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and drives the embedded clock to the RCLKn pin. The RCLKn is synchronous to the data on the ROUT[n0:n9] pins. While LOCKn is low, data on ROUT [n0:n9] is valid. Otherwise, ROUT[n0:n9] is invalid.

All ROUT, LOCK, and RCLK signals will drive a minimum of three CMOS input gates (15pF load) with a 40 MHz clock. This amount of drive allows bussing outputs of two Deserializers and a destination ASIC. REN controls TRI-STATE of all the outputs.

The Deserializer input pins are high impedance during Powerdown (PWRDN low) and power-off (V_{cc} = 0V).

Resynchronization

Whenever one of the six Deserializers loses lock, it will automatically try to resynchronize. For example, if the embedded clock edge is not detected two times in succession, the PLL loses lock and the LOCKn pin is driven high. The system must monitor the LOCKn pin to determine when data is valid.

The user has the choice of allowing the deserializer to re-synch to the data stream or to force synchronization by pulsing the Serializer SYNC1 or SYNC2 pin. This scheme is left up to the user discretion. One recommendation is to provide a feedback loop using the LOCKn pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are given for multiple control in a multi-drop application.

Powerdown

The Powerdown state is a low power sleep mode that the Serializer and Deserializer typically occupy while waiting for initialization, or to reduce power consumption when no data is transfers. The Deserializer enters Powerdown when PWRDN is driven low. In Powerdown, the PLL stops and the outputs go into TRI-STATE, which reduces supply current to the microamp range. To exit Powerdown, the system drives PWRDN high.

Upon exiting Powerdown, the Deserializer enters the Initialization state. The system must then allow time to Initialize before data transfer can begin.

TRI-STATE

When the system drives REN pin low, the Deserializer enters TRI-STATE. This will TRI-STATE the receiver output pins (ROUT[00:59]) and RCLK[0:5]. When the system drives REN high, the Deserializer will return to the previous state as long as all other control pins remain static (PWRDN, RCLK_R/F).

USING THE DS92LV1021 AND DS92LV1260

The DS92LV1260 combines six 1:10 deserializers into a single chip. Each of the six deserializers accepts a BusLVDS data stream up to 480 Mbps from Texas Instruments' DS92LV1021 or DS92LV1023 Serializer. The deserializers then recover the embedded two clock bits and data to deliver the resulting 10-bit wide words to the output. A seventh serial data input provides n+1 redundancy capability. The user can program the seventh input to be an alternative input to any of the six deserializers. Whichever input is replaced by the seventh input is then routed to the CHANNEL TEST (CHTST) pin on receiver output port. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the LOCKn output high when loss of lock occurs.

POWER CONSIDERATIONS

An all CMOS design of the Deserializer makes it an inherently low power device.

POWERING UP THE DESERIALIZER

The DS92LV1260 can be powered up at any time by following the proper sequence. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

TRANSMITTING DATA

Once you power up the Deserializer, it must be phase locked to the transmitter to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends sync patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The LOCKn output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the LOCKn output of the Deserializer to one of the SYNC inputs of the Serializer will ensure that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the “random lock” circuitry to find and lock to the data stream.

NOISE MARGIN

While the Deserializer LOCKn output is low, data at the Deserializer outputs (ROUT0-9) are valid, except for the specific case of loss of lock during transmission which is further discussed in the RECOVERING FROM LOCK LOSS section below.

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)

Media: ISI, Large V_{CM} shifts

Deserializer: V_{CC} noise

RECOVERING FROM LOCK LOSS

In the case where the Deserializer loses lock during data transmission, up to 1 cycle of data that was previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 2 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the Deserializer relocks to the incoming data stream and the Deserializer LOCKn pin goes low, at least one previous data cycle should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by random locking, which can take more time, depending on the data patterns being received.

HOT INSERTION

All the BusLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in Figure 12.

TRANSMISSION MEDIA

The Serializer and Deserializer can also be used in point-to-point configurations, through PCB trace, or through twisted pair cable. In point-to-point configurations, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configurations, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a +/− 1V common mode range at the receiver inputs.

FAILSAFE BIASING FOR THE DS92LV1260

The DS92LV1260 has internal failsafe biasing and an improved input threshold sensitivity of +/− 50mV versus +/− 100mV for the DS92LV1210 or DS92LV1212. This allows for greater differential noise margin in the DS92LV1260. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the DS92LV1260 can pickup noise as a signal and cause unintentional locking . For example, this can occur when the input cable is disconnected.

External resistors can be added to the receiver circuit board to prevent noise pick-up. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors (R_1 and R_2) provide a current path through the termination resistor (R_L) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a +15mV drop across the termination resistor. Please see Figure 10 for the Failsafe Biasing Setup.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the DS92LV1260 should be designed to provide noise-free power to the device. Good layout practice will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. There are a few common practices which should be followed when designing PCB's for Bus LVDS Signaling. Recommended layout practices are:

- Use at least 4 PCB board layers (Bus LVDS signals, ground, power, and TTL signals).
  - Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical.
- Keep Serializers and Deserializers as close to the (Bus LVDS port side) connector as possible.
  - Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes.
  - Surface mount capacitors placed close to power and ground pins work best. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the

range 0.001 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. Randomly distributed by-pass capacitors should also be used.

  - Package and pin layout permitting, it is also recommended to use two vias at each power pin as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance between layers by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.
  - The outer layers of the PCB may be flooded with additional ground planes. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement improves signal integrity on signal transmission lines by providing short paths for image currents, which reduces signal distortion. Depending on which is greater, the planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s). Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.
- Use a termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating).
  - Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals.
- Use controlled impedance media.
  - The backplane and connectors should have a matched differential impedance.

For a typical application circuit, please see Figure 9.

There are more common practices which should be followed when designing PCBs for LVDS signaling. General application guidelines and hints may be found in the following application notes: AN-808 (SNLA028), AN-903 (SNLA034), AN-971 (SNLA165), AN-977 (SNLA166), and AN-1108 (SNLA008). For packaging information on BGA's, please see AN-1126 (SNOA021).

USING T_{DJIT} AND T_{RNM} TO VALIDATE SIGNAL QUALITY

The parameter t_{RNM} is calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the ideal bit that is available for external sources of noise is called t_{RNM}.

The vertical limits of the mask are determined by the DS92LV1260 receiver input threshold of +/− 50mV.

Please refer to the eye mask pattern of Figure 11 for a graphic representation of t_{DJIT} and t_{RNM}.

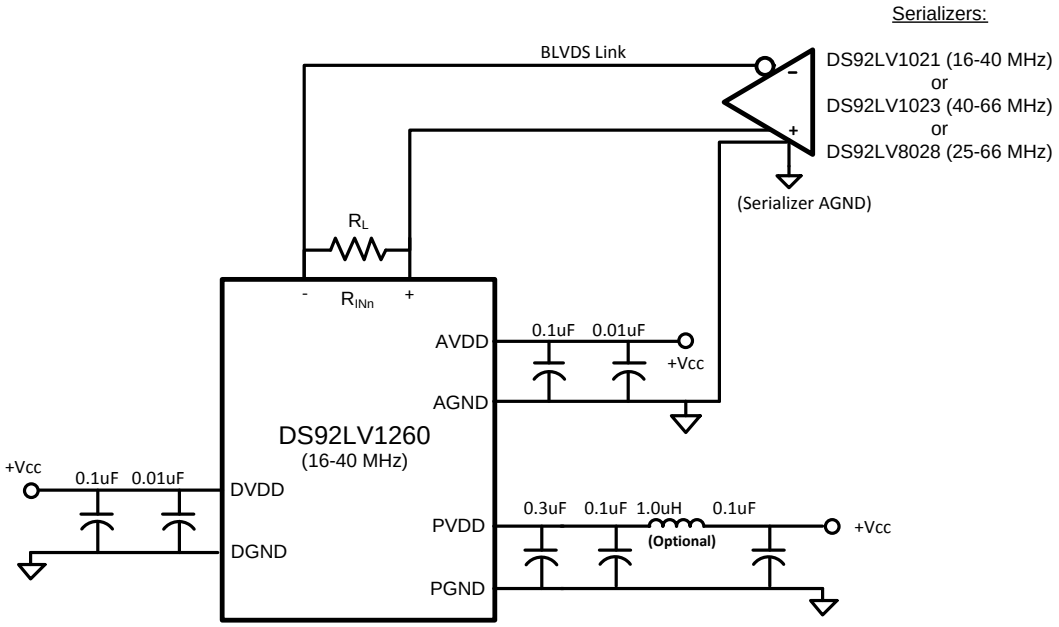


Figure 9. Typical Applications Circuit

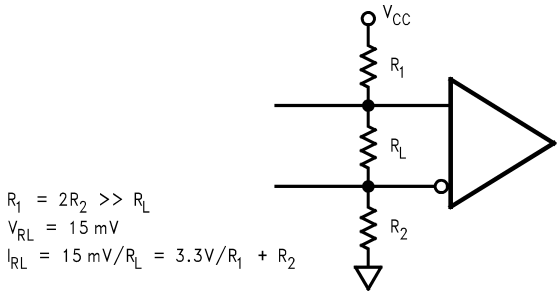


Figure 10. Failsafe Biasing Setup

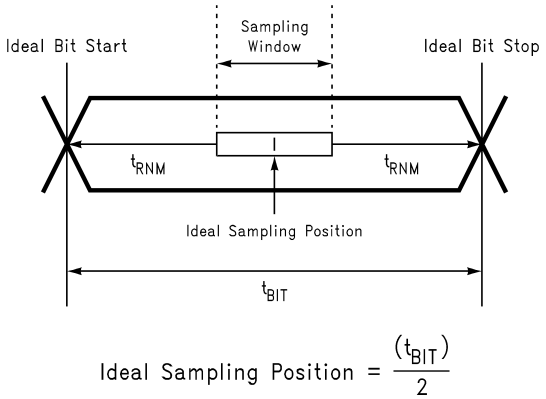


Figure 11. Using t_{DJIT} and t_{RNM} to Generate an Eye Pattern Mask and Validate Signal Quality

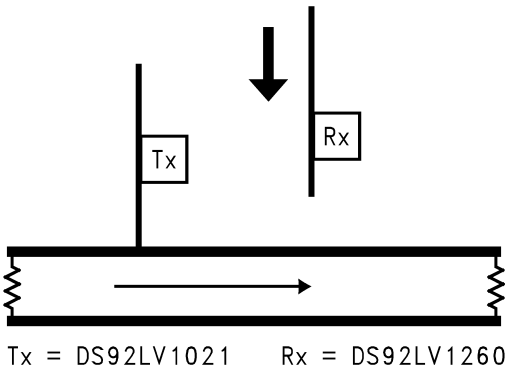


Figure 12. Random Lock Hot Insertion

Pin Diagram

A1 DGND	A2 REN	A3 $R_{IN0}-$	A4 $R_{IN0}+$	A5 AGND	A6 $R_{IN2}-$	A7 $R_{IN2}+$	A8 AGND	A9 $R_{IN4}-$	A10 $R_{IN4}+$	A11 AV_{DD}	A12 $R_{IN6}-$	A13 $R_{IN6}+$	A14 PGND
B1 N/C	B2 DGND	B3 DV_{DD}	B4 REF_{CLK}	B5 PWRDN*	B6 AV_{DD}	B7 AGND	B8 AGND	B9 AV_{DD}	B10 N/C	B11 AGND	B12 PGND	B13 SEL2	B14 DGND
C1 JTL2	C2 JTL1	C3 CHTST	C4 RCLK_R/F*	C5 $R_{IN1}-$	C6 $R_{IN1}+$	C7 AV_{DD}	C8 $R_{IN3}-$	C9 $R_{IN3}+$	C10 $R_{IN5}-$	C11 $R_{IN5}+$	C12 SEL0	C13 SEL1	C14 N/C
D1 JTL3	D2 JTL4	D3 JTL5	D4 N/C	D5 DGND	D6 DV_{DD}	D7 DGND	D8 N/C	D9 N/C	D10 PGND	D11 N/C	D12 PV_{DD}	D13 $LOCK_5$*	D14 N/C
E1 PV_{DD}	E2 R_{OUT09}	E3 N/C	E4 R_{OUT08}	E5 DGND	E6 DV_{DD}	E7 DV_{DD}	E8 DGND	E9 DV_{DD}	E10 DV_{DD}	E11 N/C	E12 R_{OUT57}	E13 R_{OUT58}	E14 R_{OUT59}
F1 PV_{DD}	F2 $RCLK_0$	F3 $LOCK_0$*	F4 R_{OUT07}	F5 DGND	F6 DGND	F7 DV_{DD}	F8 DGND	F9 DGND	F10 DV_{DD}	F11 N/C	F12 AV_{DD}	F13 $RCLK_5$	F14 PV_{DD}
G1 PGND	G2 PGND	G3 R_{OUT06}	G4 R_{OUT05}	G5 DGND	G6 DV_{DD}	G7 DGND	G8 DGND	G9 DGND	G10 DV_{DD}	G11 R_{OUT55}	G12 R_{OUT56}	G13 PGND	G14 PV_{DD}
H1 PGND	H2 R_{OUT04}	H3 R_{OUT02}	H4 R_{OUT03}	H5 DGND	H6 DV_{DD}	H7 DGND	H8 DGND	H9 DGND	H10 DV_{DD}	H11 R_{OUT54}	H12 R_{OUT53}	H13 PGND	H14 PGND
J1 PV_{DD}	J2 R_{OUT12}	J3 R_{OUT10}	J4 PGND	J5 DV_{DD}	J6 DGND	J7 DGND	J8 DV_{DD}	J9 DV_{DD}	J10 DV_{DD}	J11 R_{OUT52}	J12 R_{OUT51}	J13 PGND	J14 PV_{DD}
K1 PV_{DD}	K2 R_{OUT14}	K3 R_{OUT00}	K4 R_{OUT01}	K5 DV_{DD}	K6 DV_{DD}	K7 DV_{DD}	K8 DGND	K9 DGND	K10 DV_{DD}	K11 N/C	K12 R_{OUT50}	K13 R_{OUT40}	K14 PV_{DD}
L1 R_{OUT13}	L2 $RCLK_1$	L3 R_{OUT11}	L4 N/C	L5 N/C	L6 R_{OUT21}	L7 N/C	L8 R_{OUT31}	L9 R_{OUT34}	L10 N/C	L11 R_{OUT45}	L12 R_{OUT41}	L13 R_{OUT44}	L14 R_{OUT42}
M1 R_{OUT15}	M2 R_{OUT18}	M3 R_{OUT19}	M4 R_{OUT29}	M5 R_{OUT25}	M6 R_{OUT23}	M7 R_{OUT20}	M8 R_{OUT30}	M9 R_{OUT33}	M10 R_{OUT35}	M11 R_{OUT36}	M12 R_{OUT46}	M13 $RCLK_4$	M14 R_{OUT43}
N1 R_{OUT16}	N2 R_{OUT17}	N3 $LOCK_2$*	N4 R_{OUT27}	N5 $RCLK_2$	N6 R_{OUT22}	N7 PGND	N8 PGND	N9 R_{OUT32}	N10 $RCLK_3$	N11 R_{OUT37}	N12 R_{OUT39}	N13 R_{OUT47}	N14 R_{OUT48}
P1 $LOCK_1$*	P2 R_{OUT28}	P3 R_{OUT26}	P4 R_{OUT24}	P5 PV_{DD}	P6 PV_{DD}	P7 PGND	P8 PGND	P9 PV_{DD}	P10 PV_{DD}	P11 R_{OUT38}	P12 $LOCK_3$*	P13 $LOCK_4$*	P14 R_{OUT49}

Figure 13. Top View of DS92LV1260 (196-pin NFBGA package, see Package Number NZH0196A)

PIN DESCRIPTIONS

Pin No.	Pin Name	Type	Description
B2,B14	GND	GND	GND pins for ESD structures
C12,C13,B13	SEL (0:2)	3.3V CMOS I	These pins control which Bus LVDS input is steered to the CHTST output
A4-A3, C6-C5, A7-A6, C9-C8, A10-A9, C11-C10, A13-A12	Rin(n) +/-	Bus LVDS I	Bus LVDS differential input pins
D12	PVdd		Supply voltage for PLL circuitry
F12	AVdd		Supply voltage for input buffer circuitry
B12,A14,D10	PGND		GND pin for PLL circuitry
B11	AGND		GND pin for input buffer circuitry
C7	AVdd		Supply voltage for LVDS REC.
B9	AVdd		Supply voltage for LVDS REC.
A11	AVdd		Supply voltage for Band Gap reference.
B7	AGND		GND pin for AVDD.
A8	AGND		GND pin for AVDD1.
B8	AGND		GND pin for BGVDD.
A5	AGND		GND pin for VDDI.
B6	AVdd		Supply voltage for input logic circuitry.
D7	DGND		Tie to digital ground.
B5	$\overline{\text{PWRDN}}$	3.3V CMOS I	Controls whether the device is active or in 'sleep' mode
C4	RCLK_R/$\overline{\text{F}}$	3.3V CMOS I	Controls the relation of Rout data to RCLK edge: RCLK_R/$\overline{\text{F}}$ = H setup and hold times are referred to the rising RCLK edge; RCLK_R/$\overline{\text{F}}$ = L setup and hold times are referenced to the falling RCLK edge.
A2	REN	3.3V CMOS I	Enables the Routn, RCLKn, and SYNCCLK outputs.
B4	REFCLK	3.3V CMOS I	Frequency reference clock input.
D5	DGND		GND pin for VDDO
A1	DGND		GND for digital section.
B1	N/C		Do not connect.
D6	DVdd		Supply voltage for digital section.
B3	DVdd		Supply voltage for digital section.
C3	CHTST	3.3V CMOS O	Allows low speed testing of the Rin inputs under control of the SEL (0:2) pins.
F3,P1,N3,P12,P13,D13	$\overline{\text{LOCK}}$ (0:5)	3.3V CMOS O	Indicates the status of the PLLs for the individual deserializers: $\overline{\text{LOCK}}$= L indicates locked, $\overline{\text{LOCK}}$= H indicates unlicked.
E6,J5,K5,K10,J10,E9	DVdd		Supply voltage for the logic circuitry.
K3, K4, H3, H4, H2, G4, G3, F4, E4, E2, J3, L3, J2 ,L1 ,K2 ,M1 ,N1 ,N2 ,M2 ,M3 ,M7 ,L6 ,N6 ,M6 ,P4, M5, P3, N4, P2, M4, M8, L8, N9, M9, L9, M10, M11, N11, P11, N12, K13, L12, L14, M14, L13, L11, M12, N13, N14, P14, K12, J12, J11, H12, H11, G11, G12, E12, E13, E14	Rout nx	3.3V CMOS O	Outputs for the ten bit deserializers, n = deserializer number, x = bit number
E5,G5,J6,K8,H9,F8	DGND		GND pins for digital section.

PIN DESCRIPTIONS (continued)

Pin No.	Pin Name	Type	Description
F2,L2,N5,N10,M13,F13	RCLK (0:5)	3.3V CMOS O	Recovered clock for each deserializer's output data.
D6, F7, E7, G6, H6, K7, K6, J8, J9, G10, H10, F10, E10	DVdd		Supply voltage for output buffers.
D5, F6, F5, G7, H5, J7, H7, H8, K9, G9, G8, F9, E8	DGND		GND pins for output buffers.
F1, E1, J1, K1, P6, P5, P9, P10, J14, K14, G14, F14	PVdd		Supply voltages for PLL circuitry.
G2, G1, H1, J4, N7, P7, P8, N8, J13, H14, H13, G13	PGND		GND pins for PLL circuitry.
C2,C1,D1,D2,D3,	JTL (1:5)		Reserved pins for JTAG access port.
L4, L5, L7, L10, K11, D11, B10, D9, E3, D4, E11, F11, D8, D14, C14	N/C		Unused solder ball location. Do not connect.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV1260TUJB	NRND	NFBGA	NZH	196	119	TBD	Call TI	Call TI	-40 to 85	DS92LV1260T UJB >B	
DS92LV1260TUJB/NOPB	ACTIVE	NFBGA	NZH	196	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS92LV1260T UJB >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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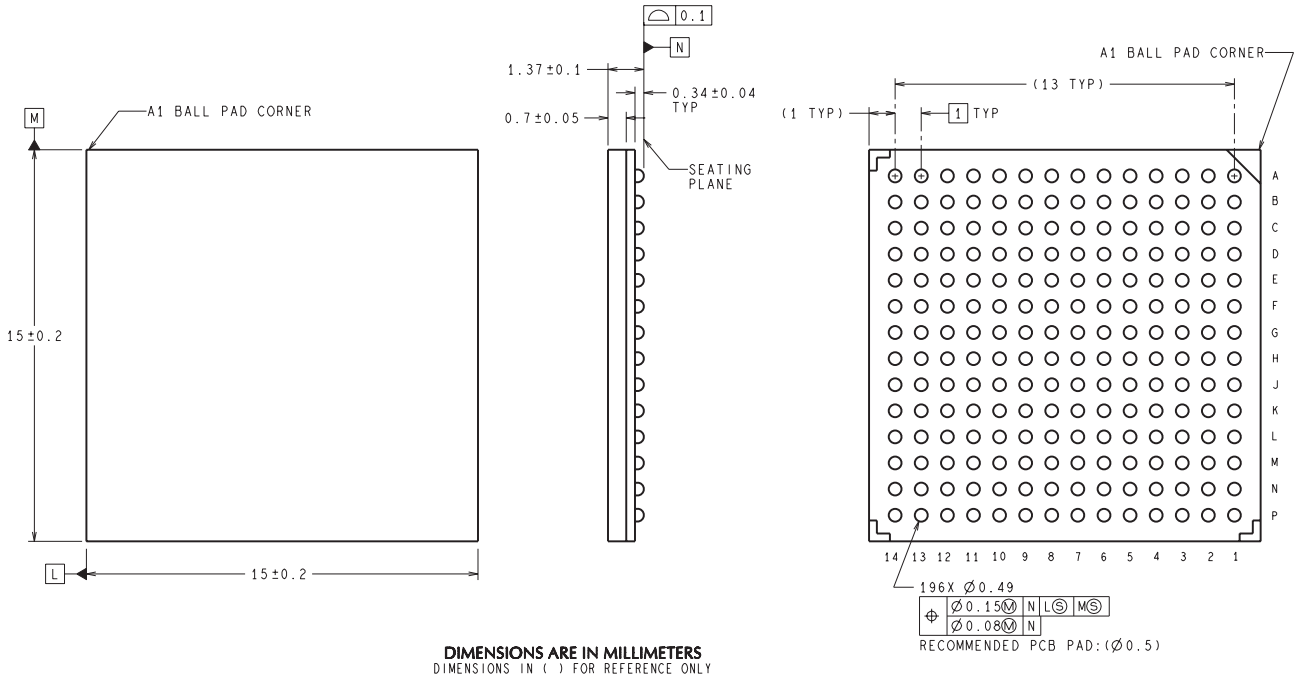

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