LM3550 5-A Super-Capacitor Flash LED Driver

1 Features

- Up to 5 A Flash Current
- 4 Selectable Super-Capacitor Charge Voltage Levels (4.5 V, 5 V, 5.3 V, Optimized)
- Adjustable Torch Current (60 mA to 200 mA)
- Ambient Light or LED Thermal Sensing With Current Scaleback
- Dedicated Indicator LED Current Source
- No Inductor Required
- Programmable Flash Pulse Duration, and Torch and Flash Currents via I^2C-Compatible Interface
- True Shutdown (LED Disconnect)
- Flash Timeout Protection
- Low Profile 20-Pin UQFN Package (3 mm × 2.5 mm × 0.8 mm)

2 Applications

- Digital Still Camera
- Voltage Rail Management
- Fire Alarm Notification
- Emergency Strobe Lighting
- Intruder Alert Notification
- Barcode Scanner
- Handheld Data Terminal

3 Description

The LM3550 device is a low-noise, switched-capacitor DC-DC converter designed to operate as a current-limited and adjustable (up to 5.3 V) super-capacitor charger. The LM3550 features user-selectable termination voltages and provides one adjustable constant current output (up to 200 mA) and one NFET controller ideal for driving one or more high-current LEDs in a high-power flash mode or a low-power torch mode.

The LED current and flash pulse duration of the LM3550 can be programmed via an I^2C-compatible interface. The STROBE pin allows the flash to be toggled via a flash-enable signal from a controller or camera module. The $\overline{EOC}$ pin sinks current when the output voltage reaches 95% of the final value.

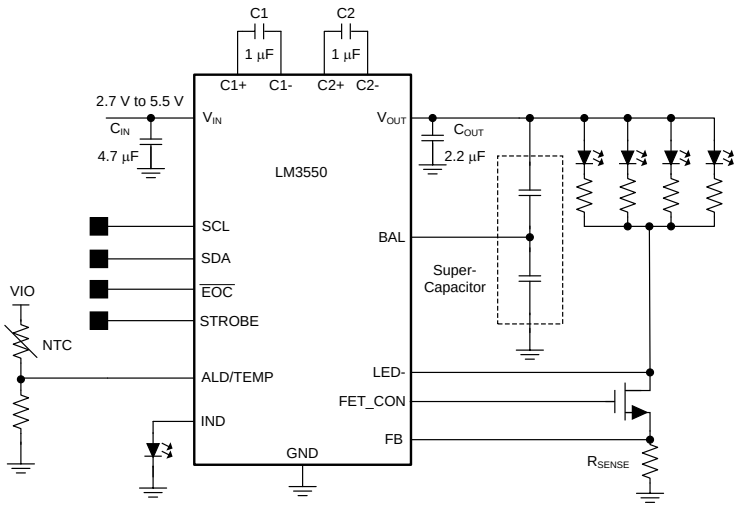
The ALD/TEMP input pin allows either a light sensor to adjust the flash-current level based on the ambient light conditions, or it allows for overtemperature detection and protection of the LED during high-power operation or high ambient-temperature conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3550	UQFN (16)	3.00 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



C1 = C2 = 1 µF, C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF
10 V X5R or X7R

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C — **Page**

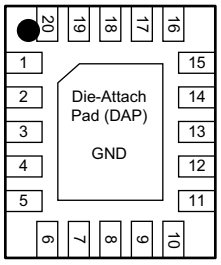
- Changed title from "5-A Flash LED Driver With Automatic V_{LED} and ESR Detection for Mobile Camera Systems" to " 5-A Super-Capacitor Flash LED Driver"; add top nav icon for reference design ... 1
- Added new *Applications: delete 'camera phones"* ... 1
- Deleted redundant text from "Features" and "Description" so required content fits on page 1 ... 1
- Added "controller or" ... 1
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted footnotes 1, 3, 4 from *ROC* table rows - no longer necessary ... 4
- Changed value for $R_{\theta JA}$ from "57°C/W" to "60.1°C/W"; add additional thermal values ... 4
- Added "a controller" ... 13
- Deleted "in the microcontroller/microprocessor." ... 13

Changes from Revision A (May 2013) to Revision B — **Page**

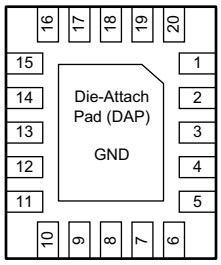
- Changed layout of National Semiconductor data sheet to TI format ... 32

5 Pin Configuration and Functions

NHU Package
16-Pin UQFN
Top View



NHU Package
16-Pin UQFN
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
ALD/TEMP	12	Input	Ambient light sensor or temperature monitoring pin. For ambient light sensing, connect a light sensor or photo-diode and a resistor to this pin. For temperature monitoring, connect a NTC thermistor from VCC to the NTC pin and a resistor from the NTC pin to ground.
BAL	2	Power	Super-capacitor active balance pin
C1+	20	Power	Flying capacitor pins. Connect a 1-µF ceramic capacitor from C1+ to C1− and C2+ to C2−.
C1–	18		
C2+	15		
C2–	16		
$\overline{EOC}$	6	Output	End-of-charge output/ flash ready. The $\overline{EOC}$ pin transitions from high to low when an end of charge flash ready. The $\overline{EOC}$ pin transitions from high to low when an end of charge state has been reached
FB	5	Input	Programmable feedback voltage pin
FET_CON	4	Output	External FET controller. Connect gate of flash NFET to this pin.
IND	13	Output	Indicator LED current source. Drives one red LED with a 5-mA current
LED-	3	Input	Regulated current sink input for torch mode
SCL	10	Input	I^2C serial clock pin
SDA	8	Input/Output	I^2C serial data I/O pin
STROBE	11	Input	Manual flash enable pin. The STROBE pin can be configured to be rising-edge sensitive with the flash timing controlled internally, or level sensitive with the flash timing being controlled externally.
V_{IN}	14	Input	Input voltage connection. A 1-µF ceramic capacitor is required from VIN to GND.
V_{OUT}	1	Output	Charge pump output. A 1-µF ceramic capacitor is required from VOUT to GND. Connect the flash LED anodes and super-capacitor to this pin.
GND	7,9,17,19, DAP	Ground	Ground pins – these pins should be connected directly to a low-impedance ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V_{IN} to GND	–0.3	6	V
V_{OUT}, LED−, FB to GND	–0.3	6	V
SDA, SCL, STROBE, FET_CON, $\overline{EOC}$, ALD/TEMP, IND to GND	–0.3	6	V
Continuous power dissipation(4)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 145°C (typical) and disengages at T_J = 125°C (typical). The thermal shutdown is specified by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The LED pin has a machine model ESD rating of 150 V.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage	2.7		5.5	V
Junction temperature, T_J	–30		125	°C
Ambient temperature, T_A	–30		85	°C

(1) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC(1)		LM3550 NHU (UQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical imits are for T_J = 25°C; minimum and maximum limits apply over the full ambient junction temperature range (−30°C ≤ T_A ≤ 85°C). Unless otherwise noted, specifications apply to *Typical Application* with: : V_{IN} = 3.6 V, C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C_1 = C_2 = 1 µF.(1)(2)

PARAMETER		TEST CONDITION		MIN(3)	TYP	MAX(3)	UNIT
I_{LED-}	Current sink accuracy	2.7 V ≤ V_{IN} ≤ 5.5 V 3 V ≤ V_{IN} ≤ 5.5 V		54	60	66	mA
				90	100	110	
				180	200	220	
V_{OVP}	Output overvoltage protection	2.7 V ≤ V_{IN} ≤ 5.5 V	Going into OVP		5.3	5.479	V
			Hysteresis		0.2		
V_{OUT}	Output voltage regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 mA		4.275	4.5	4.666	V
				4.75	5	5169	
				5.035	5.3	5.479	
V_{BAL}	BAL pin voltage regulation	2.7 V ≤ V_{IN} ≤ 5.5 V			V_{OUT} / 2		
I_{IND}	IND pin current regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, V_{IND} = 2 V		3.3	4.8	6.3	mA
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5.5 V		0.882	1	1.153	MHz
V_{FB}	FEEDBACK pin regulation voltage	2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} = 4.6 V		94	100	106	mV
$V_{ALD/TEMP}$	ALD/TEMP pin reference voltage	2.7 V ≤ V_{IN} ≤ 5.5 V		095	1	1.05	V
$V_{\overline{EOC}}$	$\overline{EOC}$ pin output logic load	I_{LOAD} = 3 mA				400	mV
I_{IN-CL}	Input current limit	V_{OUT} = 0 V			534	610	mA
I_{SD}	Shutdown supply current	Device disabled, 2.7 V ≤ V_{IN} ≤ 5.5 V			1.8	4	µA
I_Q	Quiescent supply current	2.7 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 mA 5-V charge mode, non switching			168	240	µA
V_{STROBE}	STROBE logic thresholds	2.7 V ≤ V_{IN} ≤ 5.5 V	High	1.23		V_{IN}	V
			Low	0		0.7	
I²C-COMPATIBLE VOLTAGE SPECIFICATIONS (SCL, SDA)							
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V		1.23		V_{IN}	V
V_{OL}	Output logic low	I_{LOAD} = 3 mA				400	mV

(1) All voltages are with respect to the potential at the GND pin.
(2) Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm × 76 mm × 1.6 mm with a 2 × 1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1 W.
(3) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for TYP specifications are: V_{IN} = 3.6 V and T_A = 25°C.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t1	SCK (clock period)	294			ns
t2	Data in setup time to SCL high, f_{SCL} = 400 kHz	100			ns
t3	Data out stable after SCL low, f_{SCL} = 400 kHz	0			ns
t4	SDA low setup time to SCL low (start), f_{SCL} = 400 kHz	100			ns
t5	SDA igh hold time after SCL high (stop), f_{SCL} = 400 kHz	100			ns

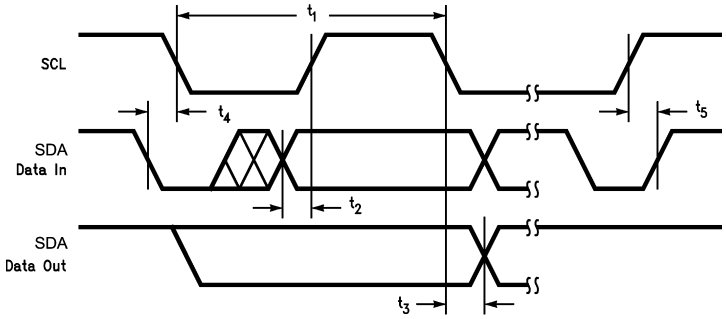
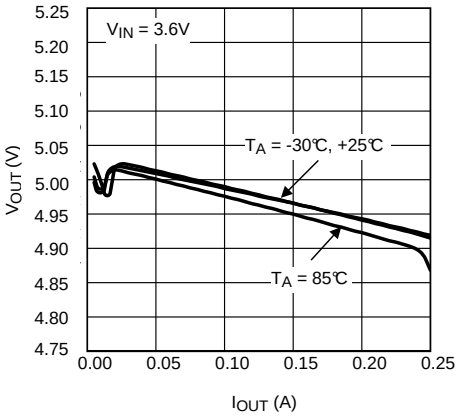


Figure 1. LM3550 Timing

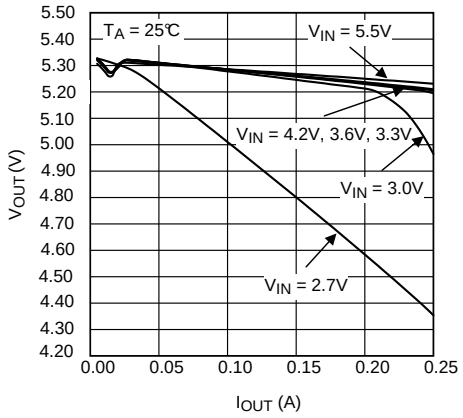
6.7 Typical Characteristics

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.



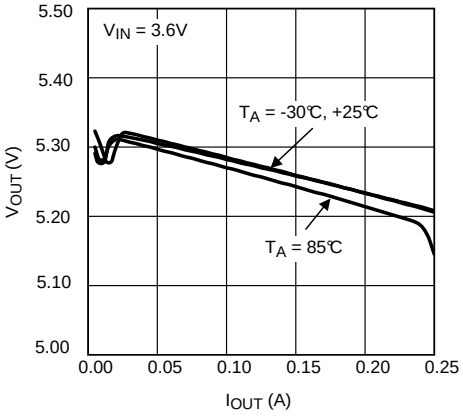
5-V Mode, Tri-Temp

Figure 2. Output Voltage vs Output Current



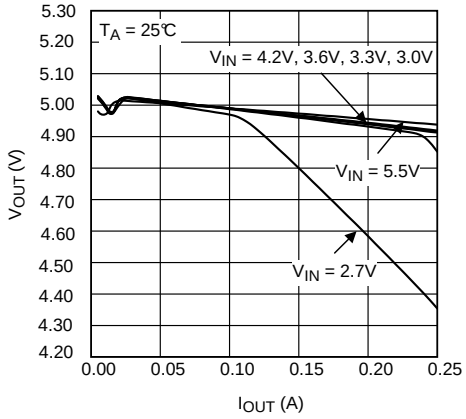
5.3-V Mode

Figure 3. Output Voltage vs Output Current



5.3-V Mode, Tri-Temp

Figure 4. Output Voltage vs Output Current

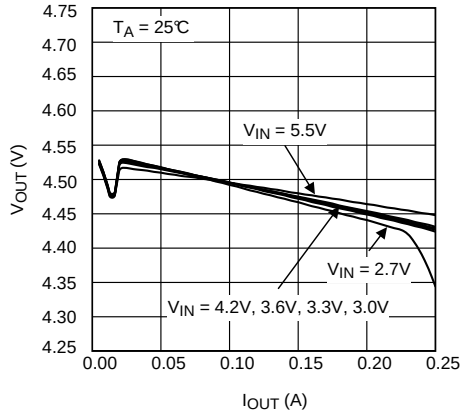


5-V Mode

Figure 5. Output Voltage vs Output Current

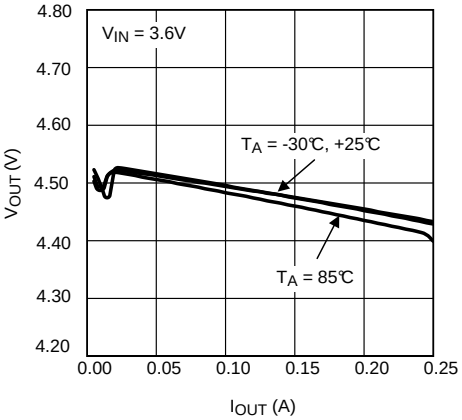
Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.



4.5-V Mode

Figure 6. Output Voltage vs Output Current



4.5-V Mode, Tri-Temp

Figure 7. Output Voltage vs Output Current

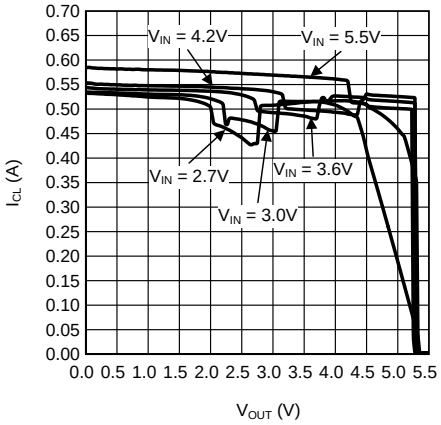


Figure 8. Input Current Limit vs Output Voltage

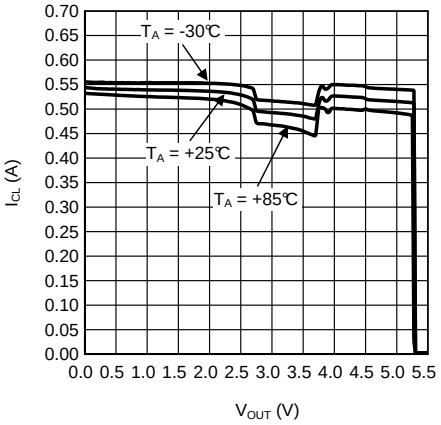
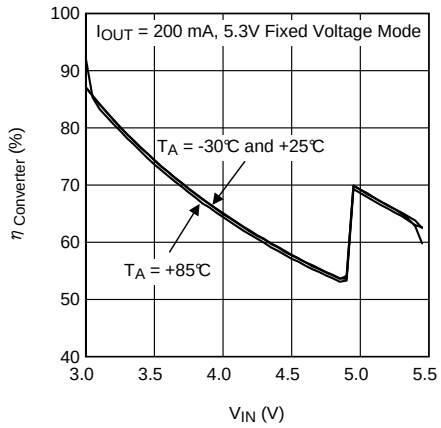


Figure 9. Input Current Limit vs Output Voltage Tri-Temp



5.3-V Mode

Figure 10. Converter Efficiency vs Input Voltage

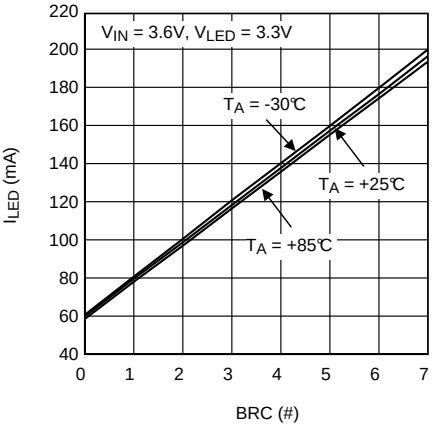


Figure 11. Torch Current vs Brightness Code

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.

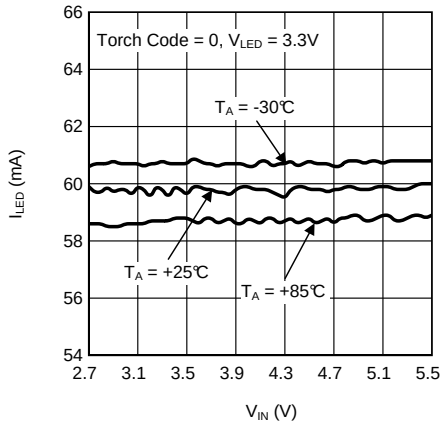


Figure 12. Torch Current vs Input Voltage Code = 0

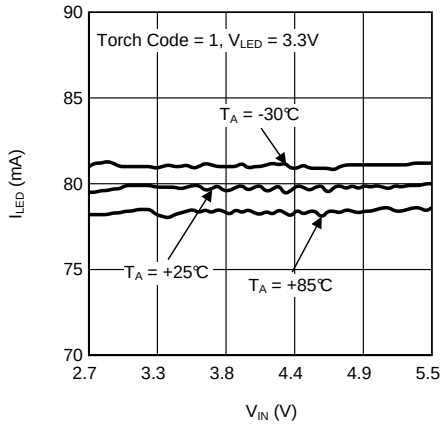


Figure 13. Torch Current vs Input Voltage Code = 1

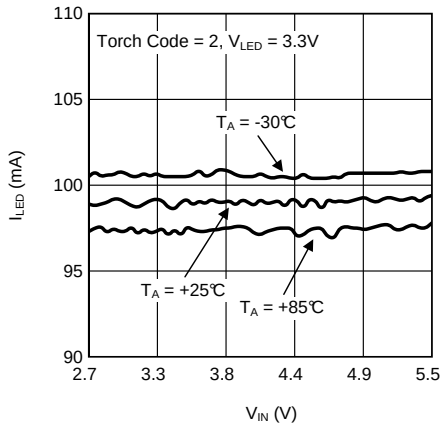


Figure 14. Torch Current vs Input Voltage Code = 2

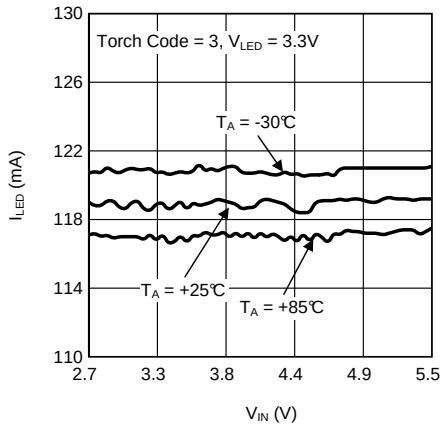


Figure 15. Torch Current vs Input Voltage Code = 3

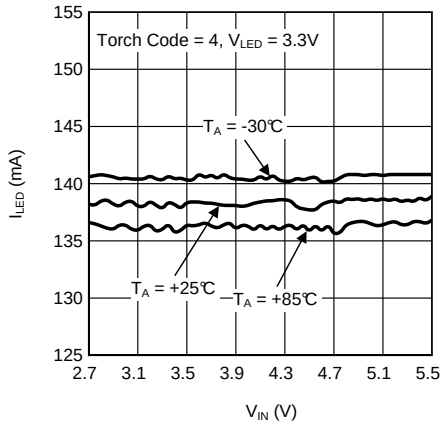


Figure 16. Torch Current vs Input Voltage Code = 4

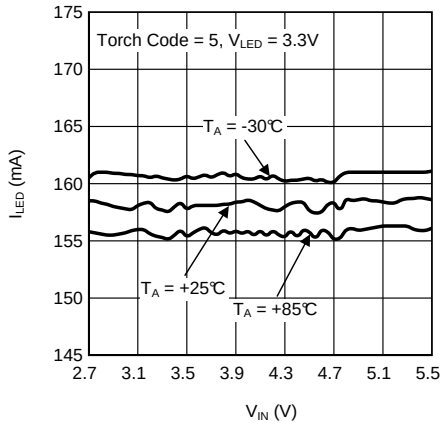


Figure 17. Torch Current vs Input Voltage Code = 5

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.

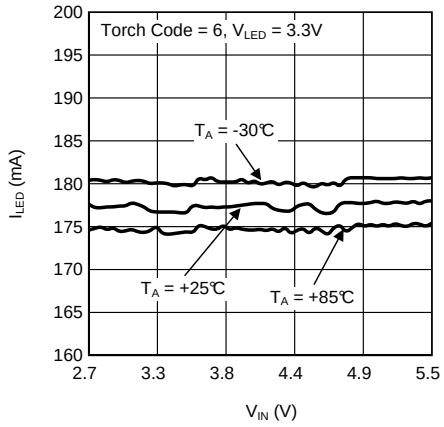


Figure 18. Torch Current vs Input Voltage Code = 6

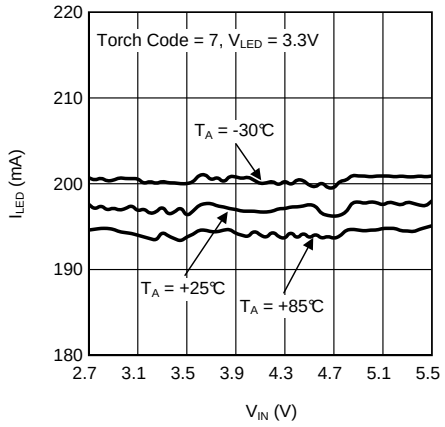


Figure 19. Torch Current vs Input Voltage Code = 7

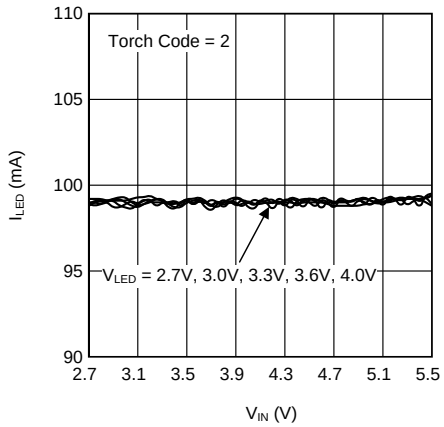


Figure 20. Torch Current vs Input Voltage Different V_{LED}

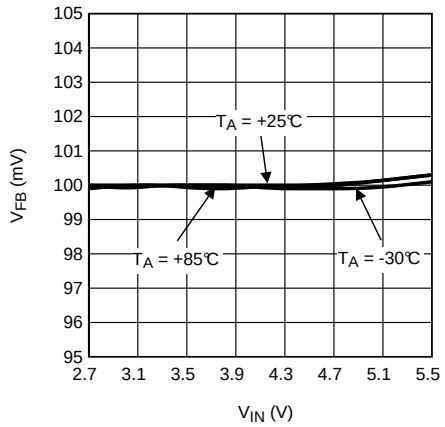


Figure 21. Feedback Voltage vs Input Voltage

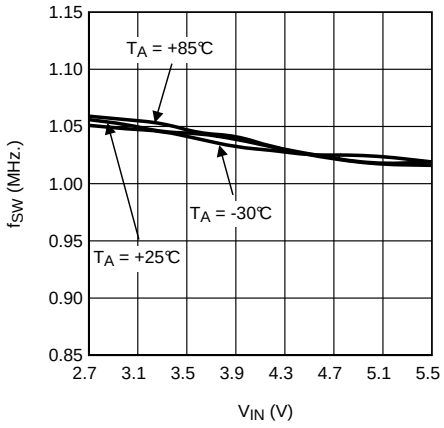


Figure 22. Oscillator Frequency vs Input Voltage

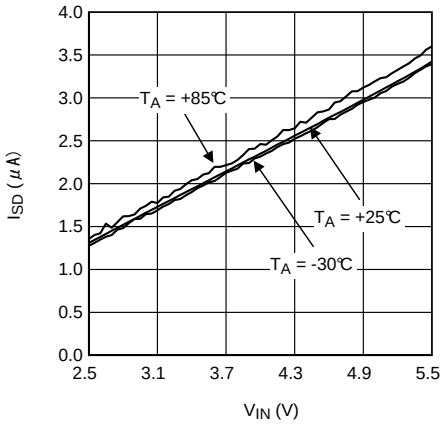


Figure 23. Shutdown Current vs Input Voltage

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.

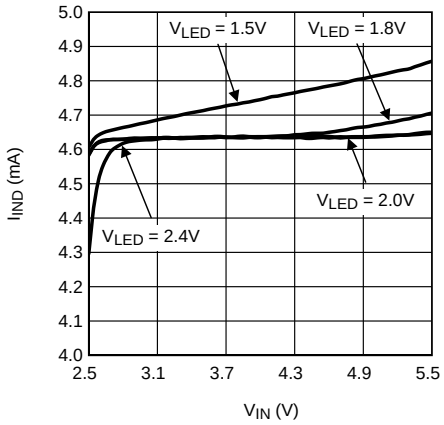


Figure 24. Indicator Current vs Input Voltage Different V_{LED}

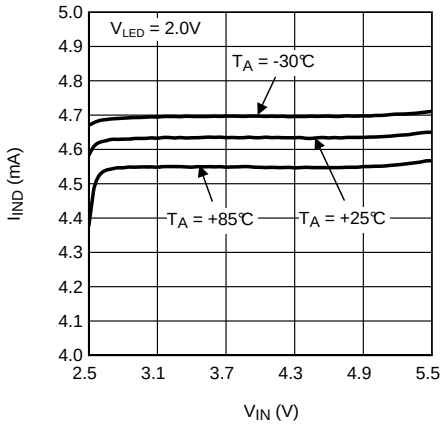


Figure 25. Indicator Current vs Input Voltage Tri-Temp

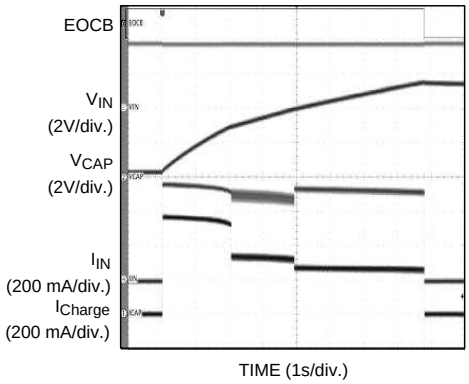


Figure 26. 5.3-V Mode Super Capacitor Charge

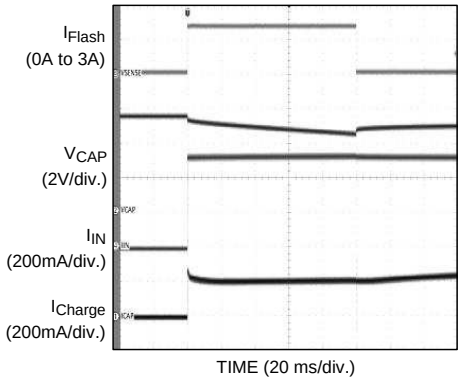


Figure 27. 2 LED, 3-A Flash (1.5 A Each)

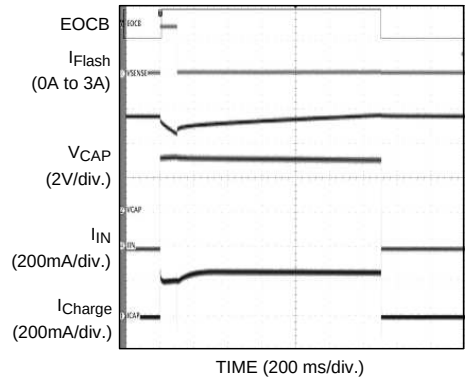


Figure 28. 5.3-V Mode Super Capacitor Recharge

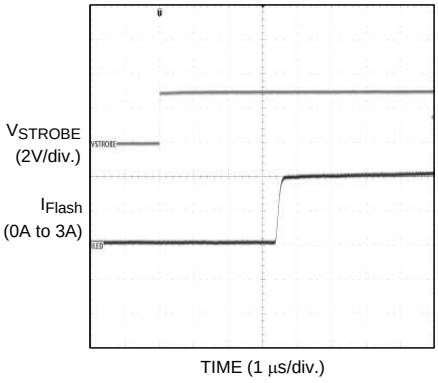


Figure 29. Strobe-to-Flash Delay

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.

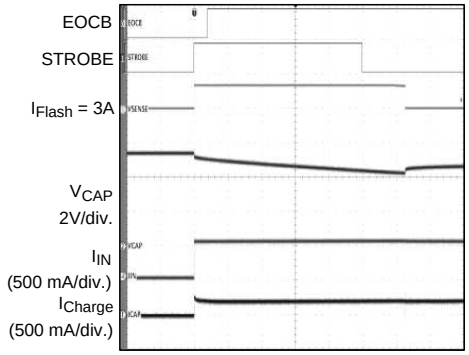


Figure 30. Edge-Sensitive Strobe

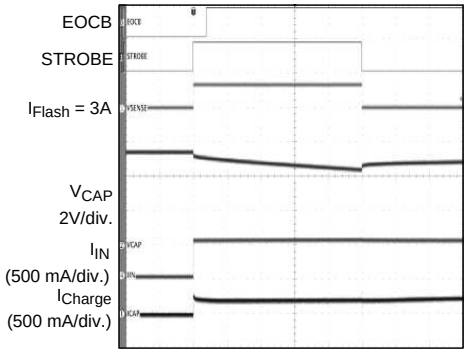


Figure 31. Level-Sensitive Strobe

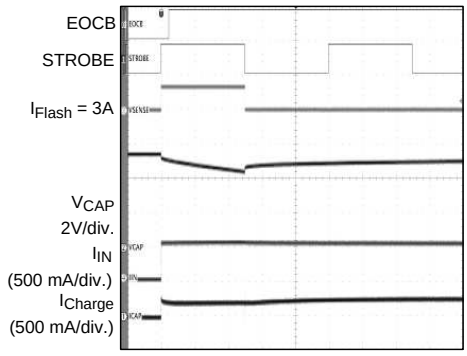


Figure 32. Flash With $\overline{\text{FGATE}}$ = 0

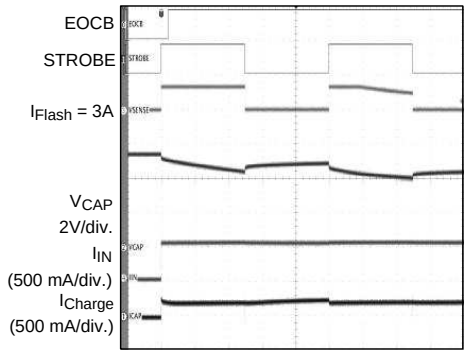
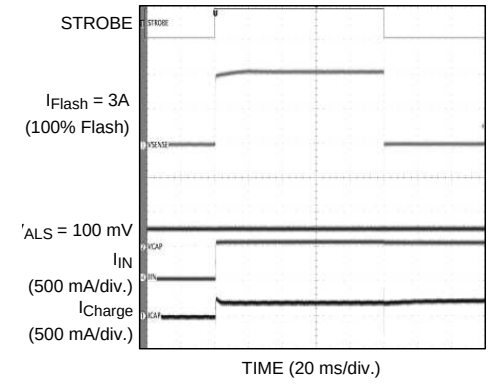
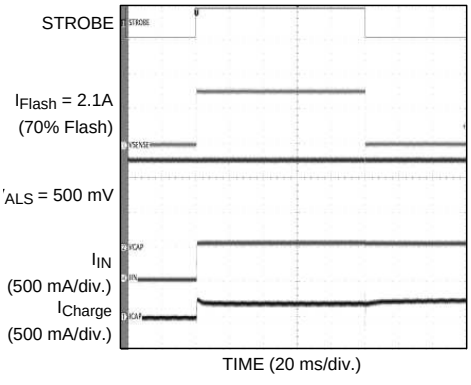


Figure 33. Flash With $\overline{\text{FGATE}}$ = 1



V_{ALS} = 100 mV

Figure 34. ALS Detect Zone 0

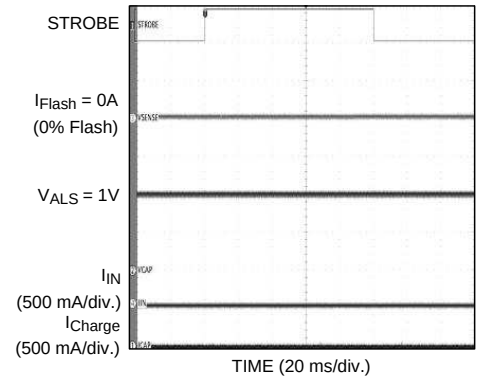


V_{ALS} = 500 mV

Figure 35. ALS Detect Zone 1

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6 V; C_{IN} = 4.7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super capacitor = 0.5 F TDK EDLC272020-501-2F-50.



V_{ALS} = 1 V

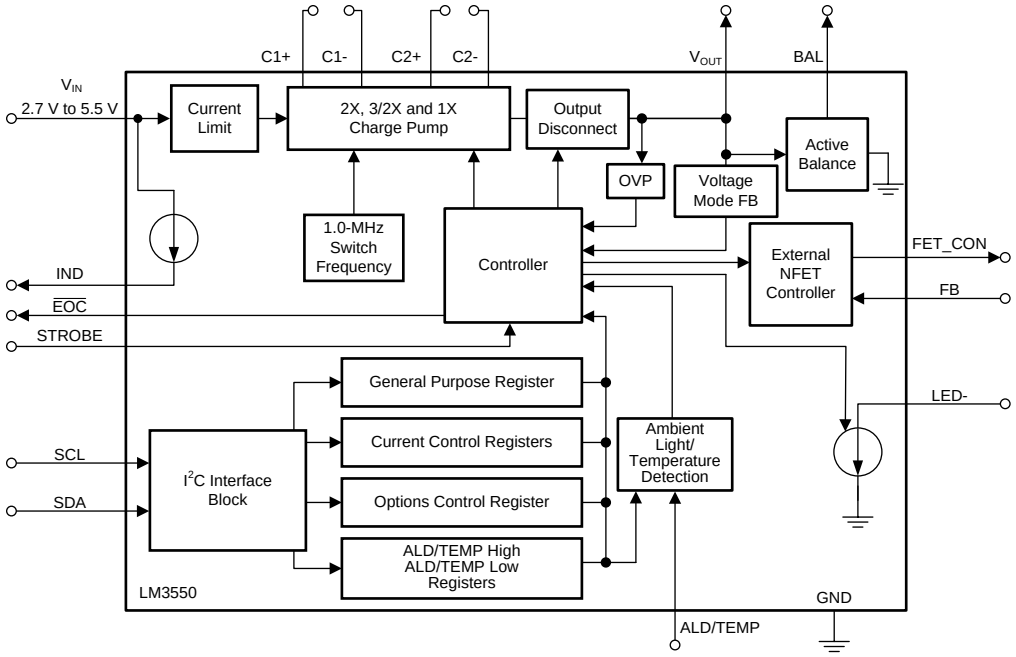
Figure 36. ALS Detect Zone 2

7 Detailed Description

7.1 Overview

The LM3550 is a super-capacitor charger and high-current-flash controller based upon a switched-capacitor boost converter. On the charging end of the application, the LM3550 has a 534 mA (typical) input current limit that prevents the part from drawing an excessive current when the super-capacitor voltage is below the target charge voltage. During the charge phase the LM3550 runs in current limit and adaptively change gains (1×, 1.5×, 2×) until the super-capacitor reaches its target charge voltage. Integrated into the LM3550 is an external NFET controller that allows the flash current drawn from the super-capacitor to remain regulated throughout the flash cycle. Flash timing and current level can be changed through the I^2C-compatible interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 STROBE Pin

The STROBE pin on the LM3550 provides an external method of flash triggering. This means a direct connection between a controller or camera/imager and the LM3550 device can be made, avoiding any latency added due to communication delays. The STROBE pin can be configured to be rising-edge sensitive (default) or level sensitive. In the rising-edge sensitive mode, the flash duration is controlled internally and uses the value stored in the FLASH duration bits (Options Control Register bits 3:0) to determine the pulse length. If level sensitive mode is selected (Options Control Register bit 7 = 1), the flash-pulse duration can be controlled externally. In this mode, when the STROBE pin is high, the flash remains on as long as the duration does not exceed the value stored in the FLASH duration control bits. If the timing does exceed the internal flash-duration value, the LM3550 automatically disables the flash current.

Feature Description (continued)

7.3.2 End-of-Charge Pin ($\overline{EOC}$)

The $\overline{EOC}$ pin provides an external flag alerting the microcontroller/microprocessor that the super-capacitor has reached the end of charging. When the super-capacitor has reached the desired end-of-charge level, the $\overline{EOC}$ pin transitions from its default state (logic 1) to the EOC state (logic 0). The $\overline{EOC}$ pin utilizes an open-drain driver that allows the $\overline{EOC}$ logic levels to be compatible with many of the common controller input/output (I/O) levels. Connecting a resistor between the system I/O supply and the $\overline{EOC}$ pin on the LM3550 ensures the proper voltage levels are utilized.

The state of the $\overline{EOC}$ pin can change during a flash event, or any other event whenever the super-capacitor voltage drops below 95% of the target charge voltage.

7.3.3 ALD/TEMP Pin

The ALD/TEMP pin allows the LM3550 to monitor the ambient light or ambient temperature and adjust the flash current through the LED/LEDs without requiring the microcontroller/microprocessor to issue commands through the control interface.

For ambient light detection, a reverse-biased photosensor/diode and a resistor are required. For ambient temperature sensing, a negative temperature coefficient (NTC) thermistor and a resistor are required. Internal to the LM3550 are two comparators (based on a 1-V reference) connected to the ALD/TEMP pin that provide three user-selectable regions of flash current adjustment. The trip-point thresholds are selectable in the ALD/TEMP Sense High and Low Registers.

If the ambient light or ambient temperature are sufficiently low (LM3550 in low region) the full-scale flash current is allowed. As the lighting conditions or temperature increase, the LM3550 ALD/TEMP detection circuit transitions to the second level that limits the flash current to 70% or the full-scale value. For conditions where a flash is not required (ambient detection) or if the ambient temperature is too high to flash safely, placing the ALD/TEMP circuit in the high-detection level, the LM3550 prevents a flash event from occurring. The functionality of the ALD/TEMP pin can be enabled or disabled through General Purpose Register (bit 6). These macro-functions, when enabled, off-load the microcontroller/microprocessor and provide significant system-power savings.

To help filter out the 50 to 60 Hz noise caused by indoor lighting, TI recommends a 1-µF ceramic capacitor tied between the ALD/TEMP pin and GND.

7.3.4 IND Pin

The Indicator pin (IND) consists of a current source that is capable of driving a red indicator LED with 5 mA of drive current. This indicator LED can be turned on and off by toggling bit 7 in the General Purpose Register.

7.3.5 BAL Pin

The Balance pin (BAL), when connected to a super-capacitor (if needed), regulates the two sections of the super-capacitor so that voltage on either cell is equal to ½ the output voltage. This ensures that an overvoltage condition on either capacitor section does not occur.

7.3.6 Super-Capacitor Charging Time

The time it takes the LM3550 to charge a super-capacitor from 0 V to the target voltage is highly dependent on the input voltage, output-voltage target, and super-capacitor capacitance value.

- The LM3550 up a capacitor faster if the target output voltage is lower and slower if the target output voltage is higher. For a given charge profile, a up a capacitor faster with higher input voltage and slower with lower input voltages. This is due to the LM3550 staying in the lower gains for longer periods of time.
- The LM3550 charges up a capacitor faster if the target output voltage is lower and slower if the target output voltage is higher. For a given charge profile, a lower capacitor voltage is reached faster than a higher voltage level.
- The LM3550 charges up a capacitor having a lower capacitance value faster than a capacitor having a higher capacitance level.

Feature Description (continued)

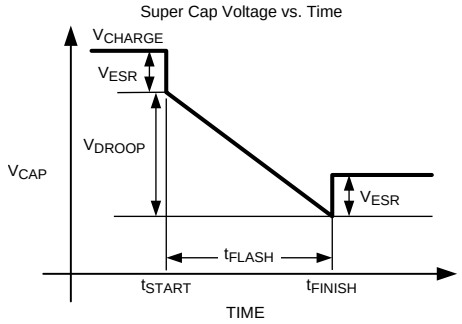
Table 1. Super-Capacitor Charging Times 0.5-F Capacitor, 0 V To Target

	OPTIMAL MODE(1)	FIXED VOLTAGE MODE		
VIN	**4.38 V**	**4.5 V**	**5 V**	**5.3 V**
4.2 V	4.565 s	5.087 s	6.314 s	7.014 s
3.6 V	5.207 s	5.765 s	6.978 s	7.832 s
3 V	6.090 s	6.446 s	7.870 s	8.904 s

(1) Optimal Mode Flash = 2 LEDs at 3 A (1.5 A each) for 48 ms. Super-capacitor part number: TDK EDLC272020-501-2F-50.

7.3.7 Super-Capacitor Voltage Profile

When a constant load current is drawn from the charged super-capacitor, the voltage on the capacitor changes. The capacitor ESR and capacitance both affect the discharge profile.



At the beginning of the flash (t_{START}), the super-capacitor voltage drops due to the ESR of the super-capacitor. The magnitude of the drop is equal to the flash current (I_{FLASH}) multiplied by the ESR (R_{ESR}).

$$V_{ESR} = I_{FLASH} \times R_{ESR} \quad (1)$$

Once the initial voltage drop occurs (V_{ESR}) the super-capacitor voltage decays at a constant rate until the flash ends (t_{FINISH}). The voltage droop (V_{DROOP}) during the flash event is equal to flash current (I_{FLASH}) multiplied by the flash duration (t_{FLASH}) divided by the capacitance value of the super-capacitor (C_{SC}).

$$V_{DROOP} = (I_{FLASH} \times t_{FLASH}) / C_{SC} \quad (2)$$

After the flash event has finished, the voltage on the super-capacitor increases due to the absence of current flowing through the ESR of the super-capacitor. This step-up is equal to

$$V_{ESR} = I_{FLASH} \times R_{ESR} \quad (3)$$

7.3.8 Peak Flash Current

To set the peak flash current controlled by the LM3550, a current setting resistor must be placed between the source of the current source and ground (FB to GND). The LM3550 regulates the voltage across the resistor to a value between 100 mV and 30 mV depending on the setting in the Current Control Register. Using the 100 mV setting, the peak flash current can be found using Equation 4:

$$I_{FLASH} = V_{FB} / R_{SENSE} \quad (4)$$

The LM3550 provides eight feedback voltage levels allowing eight different current settings. The current ranges from 100% of full-scale (100 mV setting) down to 30% of full-scale (30 mV setting) in 10% steps.

7.3.9 Maximum Flash Duration

Several factors determine the maximum achievable flash pulse duration. The flash current magnitude, feedback voltage, R_{DSON} of the current source FET, super-capacitor capacitance (C_{SC}), super-capacitor ESR (R_{ESR}) and super-capacitor charge voltage (V_{CAP}) determine the ability of the device to regulate the flash current for a given amount of time.

$$t_{FLASH}\ (\text{maximum}) = (C_{SC} \times V_{DROOP}) / I_{FLASH} \quad (5)$$

where

- $V_{DROOP} = V_{CAP} - V_{LED} - [I_{FLASH} \times (R_{ESR} + R_{DSON} + \{R_{BAL}/N)\}] - V_{FB}$
- N = number of flash LEDs

Example:

If V_{CAP} = 5.3 V, V_{LED} = 4 V (at 1.5 A), I_{FLASH} (total) = 3 A, C_{SC} = 0.5 F, R_{ESR} = 50 mΩ, R_{DSON} = 40 mΩ, V_{FB} = 100 mV, and R_{BAL} = 75 mΩ, then V_{DROOP} = 0.82 V and t_{FLASH} (maximum) = 136 ms.

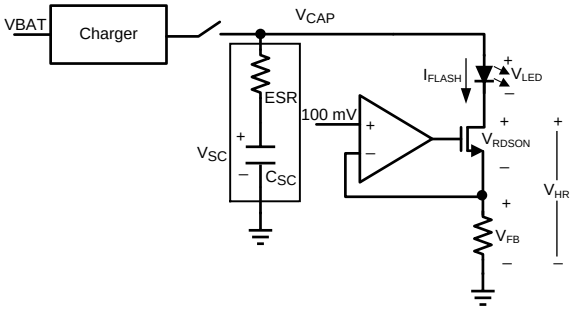


Figure 37. Power Loss Model

7.4 Device Functional Modes

7.4.1 State Machine Description

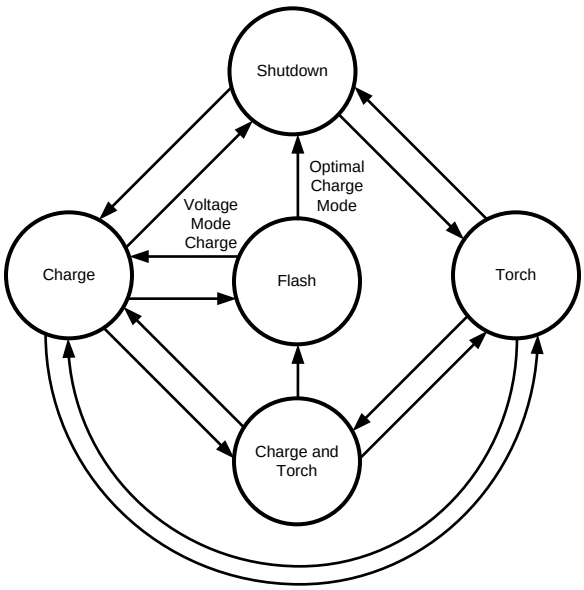


Figure 38. Default State Diagram

Device Functional Modes (continued)

7.4.1.1 Basic Description

The state machine for the LM3550 involves five different states: shutdown, torch, charge, charge and torch, and flash.

The shutdown state, or standby state, places the LM3550 in a low-power mode that typically draws 1.8 µA of current from the power supply.

The torch state charges the super-capacitor up to V_{LED} + V_{TREG} (V_{TREG} ≈ 300 mV) and utilizes the internal current sink to drive the flash LEDs with a current up to 200 mA.

The charge state places the LM3550 into a dedicated charge mode that provides the fastest means of charging the super-capacitor up to the target level (4.5 V, 5 V, 5.3 V or optimal).

The charge and torch state combines the functionality of both the torch state and charge state. This state allows the flash LEDs to be on during the charging of the super-capacitor. During the initial charging, the torch current is limited to 60 mA to allow the majority of the output current to be utilized in the super-capacitor charging. Once the target capacitor voltage is reached, the torch-current levels become fully adjustable.

The Flash state is responsible for driving the flash LEDs at the desired flash current. This state can be entered either through I^2C-controlled event or through an external strobe event.

7.4.1.2 Shutdown State

The shutdown state is the default power-up state. The LM3550 enters the shutdown state when the STROBE pin is held low without a flash event occurring, and when the flash, torch, and charge bits in the General Purpose Register are equal to 0.

7.4.1.3 Torch State

The torch state of the LM3550 provides the flash LED / LEDs with a constant current level that is safe for continuous operation. This state is useful in low light conditions when an imager is placed in movie or video mode. The torch state is enabled when the torch bit in the General Purpose Register is set to a 1 and the flash and charge bits are set to 0. The desired torch current level (8 total levels between 60 mA and 200 mA) is set in the Current Control Register.

Enabling the torch bit starts up the LM3550 and begin charging the capacitor. Before a torch event can occur, the super-capacitor must be charged to a voltage greater than 3 V. Once the super-capacitor reaches a voltage of 3 V, the LED− pin begins sinking current. In order for the torch current to be properly regulated, the super-capacitor must be charged up to a value that is greater than V_{LED} + V_{TREG} (V_{TREG} ≈ 300 mV).

When in the torch state, the LM3550 regulates the proper output voltage (either 3 V or V_{LED} + V_{REG}) utilizing a pulsed regulation scheme (PFM). During this mode, the device operate in current limit until the output voltage reaches the target level. At that point, the charge-pump turns off, and the super-capacitor supplies the load. Once the super-capacitor voltage drops below the turnon threshold due to the loading caused by the torch current, the charge-pump turns on again and re-charges the super-capacitor.

7.4.1.4 Charge State

The charge state of the LM3550 provides the fastest charge time when compared to the other states of operation. In this state, the user has the option of charging the super-capacitor to a voltage equal to 4.5 V, 5 V, 5.3 V or to an optimal voltage. The charge state is enabled through the I^2C interface by setting the charge bit to a 1 and setting the flash and torch Bits to a 0 in the General Purpose Register. The charge voltage is selectable by setting the two charge-mode bits (CM1 and CM0) also found in the General Purpose Register.

Depending on the input voltage and output voltage conditions, the LM3550 delivers different charge currents to the super-capacitor. Charge current is dependent on the charge-pump gain.

Device Functional Modes (continued)

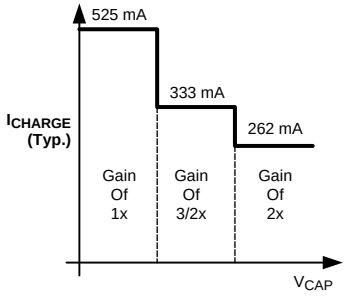


Figure 39. Charge Current vs Output Voltage

7.4.1.4.1 Fixed-Voltage-Charge Mode

During the charge state, the LM3550 operates in current limit until the target voltage is reached. For the 4.5 V, 5 V and 5.3 V charge modes, the LM3550 operates in a constant-frequency mode once the target voltage is reached for load currents greater than 60 mA. This allows the LM3550 to draw only the required current from the power source when the load current is less than the maximum. When the average output current exceeds the maximum of the LM3550, the device returns to the current limited operation until the target voltage is reached. If the output current is less than 60 mA, the LM3550 operates in a PFM-burst mode.

7.4.1.4.2 Optimal Charge Mode

For the optimal charge mode, the current-limited, pulsed-regulation scheme (PFM) is used to maintain the target voltage. In optimal charge mode, the LM3550 charges the super-capacitor to a level that is required to sustain a flash for a given period of time. optimal charge mode compensates for variations in LED forward voltage and super-capacitor ESR by charging the capacitor to an optimal voltage that minimizes the power dissipated in the external current source during the flash. The user must calculate the required overhead voltage and select this value in the Options Control Register. For more information regarding the optimal charge mode, see the *Application and Implementation* description.

NOTE

When the LM3550 is placed into optimal charge mode, the flash LEDs begin to glow once the super-capacitor voltage exceeds 3 V. The LEDs continue to glow until the device is placed into shutdown, into the flash state, or into one of the fixed-voltage charge modes.

7.4.1.5 Torch and Charge State

The torch and charge state provides the ability to utilize the torch functionality while charging to the selected target voltage. The torch and charge state is entered by setting the torch bit and charge bit to a 1 and by setting the flash bit to a 0 in the General Purpose Register. Additionally, the CM1 and CM0 bits can be configured to define the target charge voltage.

During the initial charging of the super-capacitor, the torch functionality is enabled until the capacitor voltage reaches 3 V. Additionally, the torch current is limited to 60 mA until the target voltage is reached. Once the output reaches the target, the current level specified in the Current Control Register is allowed.

In the event that the total output current exceeds the capacitor charge current ($I_{CHARGE} = I_{MAX} - I_{TORCH} - I_{EXTERNAL}$), causing the super-capacitor to drop below the target voltage, the LM3550 automatically sets the T2 bit in the Current Control Register to a 0, decreasing the torch current.

Device Functional Modes (continued)

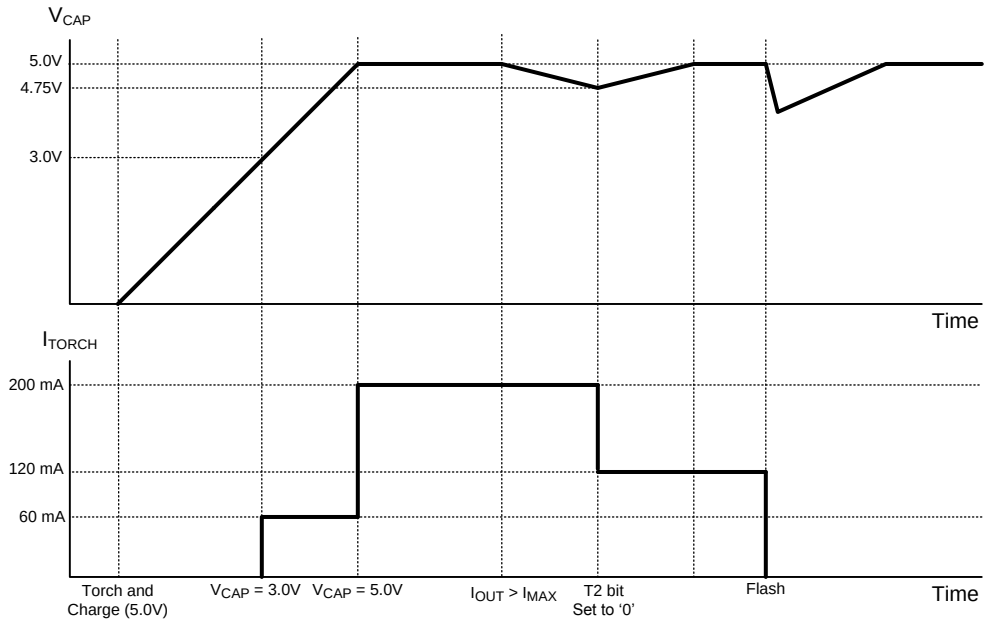


Figure 40. Torch Current Diagram

7.4.1.6 Flash State

When entered, the flash state of the LM3550 device delivers a high-current burst of current to the flash LEDs. To enter the flash state, the flash bit in the General Purpose Register must be set to a 1 or the STROBE pin must be pulled high (edge or level sensitive). The flash duration and current level are user adjustable via the I^2C interface (F2-F0 in current control and FD3-FD0 in options).

By default, a flash does not occur if the super-capacitor is not fully charged (that is, the end-of-charge flag ($\overline{EOC}$ pin) must transition low). If the flash state was entered via the I^2C interface (flash bit = 1), the LM3550 automatically resets the flash bit and the torch bit to 0 upon completion of the flash. Additionally, after the flash event has occurred, the LM3550 returns to the charge state/mode that was in operation before the flash event with the exception of optimal charge mode. (If optimal charge mode was used before a flash, all charging is halted after the flash.)

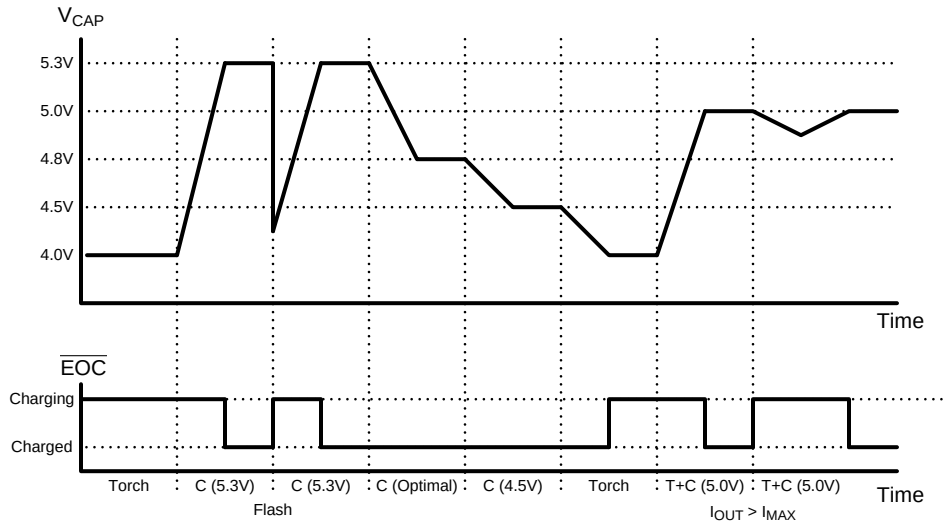
7.4.1.7 $\overline{EOC}$ Functionality

The $\overline{EOC}$ pin of the device provides an indicator alerting the controller that the super-capacitor has reached its target voltage. The $\overline{EOC}$ pin transitions low once the capacitor reaches 95% of the target voltage for the 4.5 V, 5 V and 5.3 V modes or once the capacitor has reached the optimal charge voltage in optimal charge mode.

During operation, the LM3550 continues to monitor the voltage on the super-capacitor and updates the $\overline{EOC}$ pin when needed. Any time a mode transition occurs during charge mode or charge and torch mode, the EOC state is re-evaluated.

During torch mode, the $\overline{EOC}$ always indicates a charging state ($\overline{EOC}$ = 1) .

Device Functional Modes (continued)



Device Functional Modes (continued)

7.4.1.8 State Diagram $\overline{FGATE}$ = 1

By default, the LM3550 prevents a flash event from occurring if the super-capacitor has not reached the target voltage ($\overline{EOC}$ = 0). In the event that this restriction is not desired, the flash gate bit ($\overline{FGATE}$ in the General Purpose Register) can be set to a 1 disabling the end-of-charge requirement. Setting $\overline{FGATE}$ to a 1 allows the flash state to be entered at anytime. If the super-capacitor is not charged to the proper voltage before the $\overline{EOC}$ pin indicates a full charge, the perceived duration and flash level could be lower than desired.

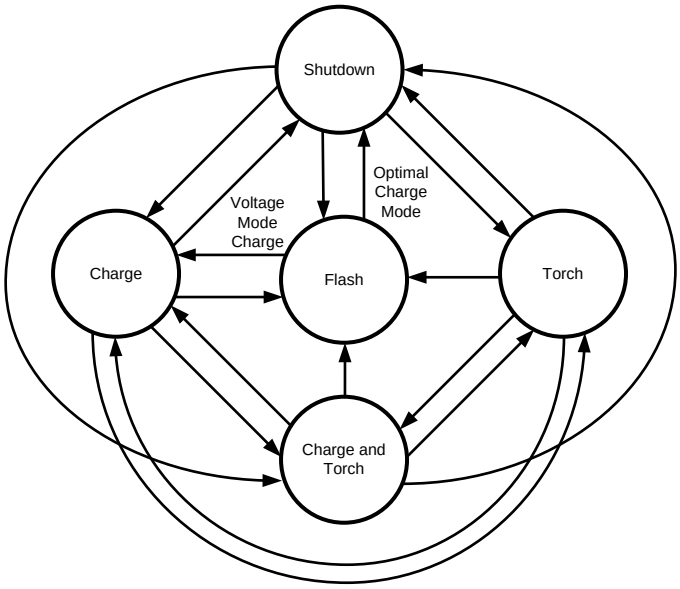


Figure 41. $\overline{FGATE}$ = 1 State Diagram

7.4.1.9 Optimal Charge Mode vs Fixed Voltage Mode

The LM3550 provides two types of super-capacitor charging modes: fixed voltage and optimal charge.

In fixed voltage mode, the LM3550 charges and regulate the super-capacitor to either 4.5 V, 5 V, or 5.3 V. This mode is useful if the LM3550 is going to be used for both flash and fixed-rail applications (power supply for audio or PA sub-systems).

If the LM3550 is only going to be used as a super-capacitor charger and flash controller, the optimal charge mode provides many advantages over the fixed voltage mode. optimal charge mode charges the super-capacitor to the minimum voltage that is required to sustain a flash pulse compensating for variations in super-capacitor ESR and LED forward voltage due to temperature and process. To properly use the optimal charge mode, the overhead voltage (V_{OH}) must be determined. The overhead voltage is equal to the voltage required to maintain current source regulation (V_{HR}) plus the voltage droop (V_{DROOP}) on the super-capacitor due to the flash event.

$$V_{OH} = V_{DROOP} + V_{HR} = (I_{FLASH} \times t_{FLASH} / C_{SC}) + V_{FB} + (I_{FLASH} \times R_{DSDON}) \quad (6)$$

and

$$V_{CAP} = V_{OH} + V_{LED} + [I_{FLASH} \times (R_{ESR} + R_{BAL} / N)] \quad (7)$$

where

- N = Number of flash LEDs

Device Functional Modes (continued)

Example:

If V_{LED} (peak)= 4.1 V (at 1.5 A), I_{FLASH} (total) = 3 A, C_{SC} = 0.5 F, R_{ESR} = 50 mΩ, R_{DSON} = 40 mΩ, V_{FB} = 100 mV, R_{BAL} = 75 mΩ, and t_{FLASH} = 64 ms, then V_{OH} = 0.604 V and V_{CAP} = 4.97 V.

NOTE

V_{LED} (peak) is equal to the LED voltage before self-heating occurs. Once current flows through the LED, the LED heats up, and the forward voltage decreases until it reaches a steady-state level. This voltage drop is dependent on the LED and the PCB layout.

Based on this calculation, setting the overhead voltage to 600 mV in the Current Control Register should ensure a regulated 3-A flash pulse over the entire flash duration.

Unlike fixed voltage mode, optimal charge mode adjusts the super-capacitor voltage upon changes in LED forward voltage and variation in super-capacitor ESR, ensuring that the super-capacitor does not charge to a voltage higher than needed. By charging optimally, the LM3550 can potentially charge the super-capacitor to its EOC state faster due to the target voltage being lower, and it helps ease the thermal loading on the current source FET during the flash.

7.4.1.9.1 Optimal Charge Mode vs Fixed Voltage Mode

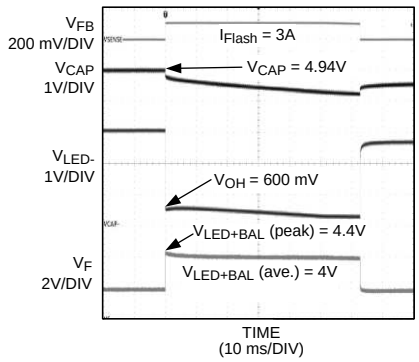


Figure 42. Optimal Charge Mode

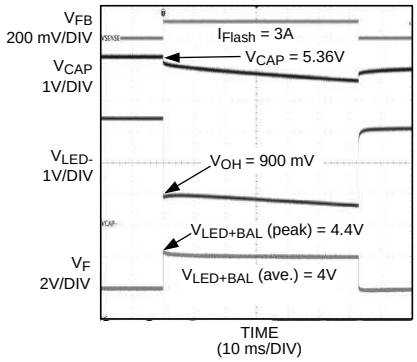


Figure 43. 5.3-V Fixed Voltage Charge Mode

Peak power dissipation across current source FET

$$P_{NFET}\ (\text{maximum}) = I_{FLASH} \times (V_{OH} - V_{FB}) \quad (8)$$

where

- Optimal mode = 1.5 W, fixed voltage mode (5.3 V) = 2.4 W

Average power dissipation across current source FET (64 ms pulse)

$$P_{NFET}\ (\text{average}) = I_{FLASH} \times [V_{OH} - (V_{DROOP} \div 2) - V_{FB}] \quad (9)$$

where

- Optimal mode = 936 mW, fixed voltage mode (5.3 V) = 1.824 W

7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

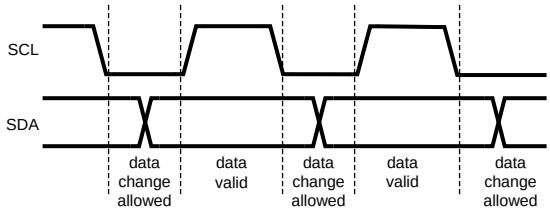


Figure 44. Data Validity Diagram

A pullup resistor between VIO (logic power supply) and SDA must be greater than [(VIO − V_{OL}) / 3 mA] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup resistor results in higher switching currents with faster edges.

7.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

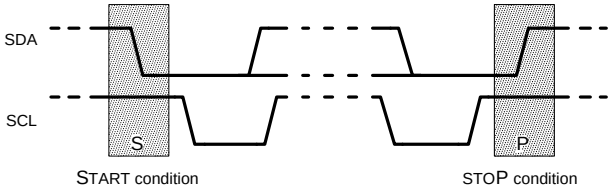


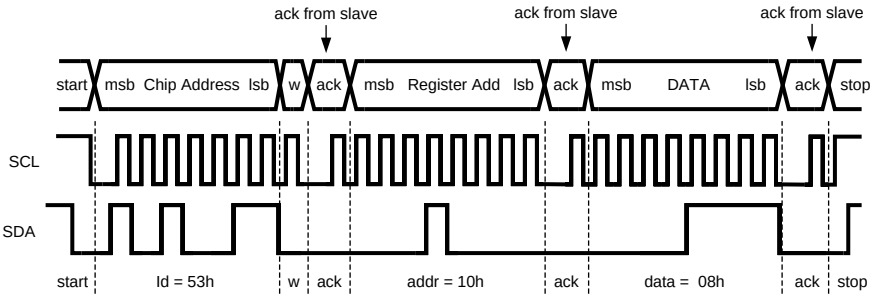
Figure 45. Start and Stop Conditions

Programming (continued)

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3550 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3550 generates an acknowledge after each byte has been received.

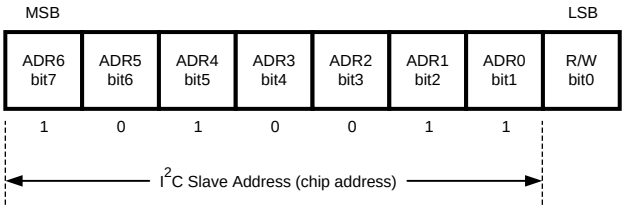
After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3550 address is 53h. For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



w = write (SDA = 0)
ack = acknowledge (SDA pulled down by the slave)
id = chip address, 53h for LM3550

Figure 46. Write Cycle

7.5.1.4 I^2C-Compatible Child Address: 0x53



7.6 Register Maps

7.6.1 Internal Registers

Register	Internal Hex Address	Power On Value
General Purpose	0x10	0000 0000
Current Control	0xA0	1111 1000
Options	0xB0	1000 0000
ALD/TEMP Sense High	0xC0	1111 1001
ALD/TEMP Sense Low	0xD0	1100 0110

7.6.1.1 General Purpose Register Description

General Purpose Register
Register Address: 0x10

MSB							LSB
IND EN bit7	A/T EN bit6	$\overline{\text{FGATE}}$ bit5	CM1 bit4	CM0 bit3	FLASH bit2	CHARGE bit1	TORCH bit0

FLASH, CHARGE, and TORCH: Mode Bits (see Table 2).

CM0–CM1: Capacitor Charge Mode (see Table 3).

$\overline{\text{FGATE}}$: Flash Gate Bit. If $\overline{\text{FGATE}}$ is a 0, then an end-of-charge condition must occur before a flash can take place. If $\overline{\text{FGATE}}$ is a 1, then an end-of-charge condition does not have to occur before a flash can take place.

A/T EN: ALD/TEMP Enable Bit

IND EN: Enable Indicator Current Source (0 = Indicator Off, 1 = Indicator On)

Table 2. Control Modes

Flash	Charge	Torch	Mode
0	0	0	Disabled
0	0	1	Torch
0	1	0	Charge
0	1	1	Charge and Torch
1	x	x	Flash

Table 3. Capacitor Charge Level

CM1	CM0	Level
0	0	Optimal Charge Mode
0	1	4.5
1	0	5.0V
1	1	5.3V

Table 4. Gated Flash Control

$\overline{\text{FGATE}}$ Bit	Result
0	Flash only allowed after EOC reached
1	Flash allowed without EOC reached

Table 5. ALD/TEMP Control

A/T EN Bit	Result
0	ALD MODE DISABLED
1	ALD MODE ENABLED

7.6.1.2 Current Control Register Description

Current Control Register
Register Address: 0xA0

MSB							LSB
1 bit7	1 bit6	F2 bit5	F1 bit4	F0 bit3	T2 bit2	T1 bit1	T0 bit0

Table 6. Torch Level Table

T2	T1	T0	Level
0	0	0	60 mA
0	0	1	80 mA
0	1	0	100 mA
0	1	1	120 mA
1	0	0	140 mA
1	0	1	160 mA
1	1	0	180 mA
1	1	1	200 mA

Table 7. Flash Level Table

F2	F1	F0	FB Voltage Level
0	0	0	30 mV
0	0	1	40 mV
0	1	0	50 mV
0	1	1	60 mV
1	0	0	70 mV
1	0	1	80 mV
1	1	0	90 mV
1	1	1	100 mV

7.6.1.3 Options Control Register Description

Options Register
Register Address: 0xB0

MSB							LSB
SLE bit7	OH2 bit6	OH1 bit5	OH0 bit4	FD3 bit3	FD2 bit2	FD1 bit1	FD0 bit0

SLE: Strobe Level or Edge Sensitivity. 0 = Edge Sensitive, 1 = Level Sensitive

FD0-FD3: Flash Duration control bits (see Table 8).

OH0-OH2: Overhead Charge Voltage control bits (see Table 9).

Table 8. Time-out Duration Table

FD3	FD2	FD1	FD0	Time (msec)
0	0	0	0	16
0	0	0	1	32
0	0	1	0	48
0	0	1	1	64
0	1	0	0	80
0	1	0	1	96
0	1	1	0	112
0	1	1	1	128
1	0	0	0	144

Table 8. Time-out Duration Table (continued)

FD3	FD2	FD1	FD0	Time (msec)
1	0	0	1	160
1	0	1	0	176
1	0	1	1	192
1	1	0	0	208
1	1	0	1	224
1	1	1	0	240
1	1	1	1	512

Table 9. Overhead Charge Voltage Table

OH2	OH1	OH0	Level
0	0	0	300 mV
0	0	1	400 mV
0	1	0	500 mV
0	1	1	600 mV
1	0	0	700 mV
1	0	1	800 mV
1	1	0	900 mV
1	1	1	1V

7.6.1.4 ALD/TEMP Sense High/Low Registers

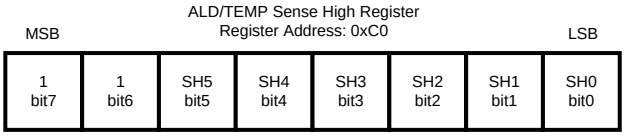


Figure 47. ALD/TEMP Sense High Register

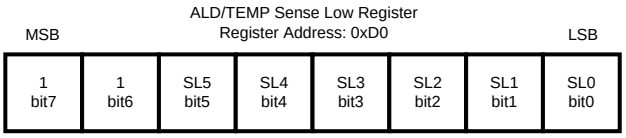


Figure 48. ALD/TEMP Sense Low Register

For ALD/TEMP Sense High and ALD/TEMP sense low, the trip levels are set by Equation 10:

$$\text{Sense High/Low} = 1\ \text{V} \times N / (2^6 - 1) \quad (10)$$

where

- N is the decimal equivalent of the value stored in the ALD/TEMP Sense High/Low registers

$N_{SENSEHIGH}$ must be greater than $N_{SENSELOW}$.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3550 can drive multiple flash LEDs at currents up to 5 A total. The switched-capacitor boost on the LM3550 eliminates the need of an inductor in the application.

8.2 Typical Application

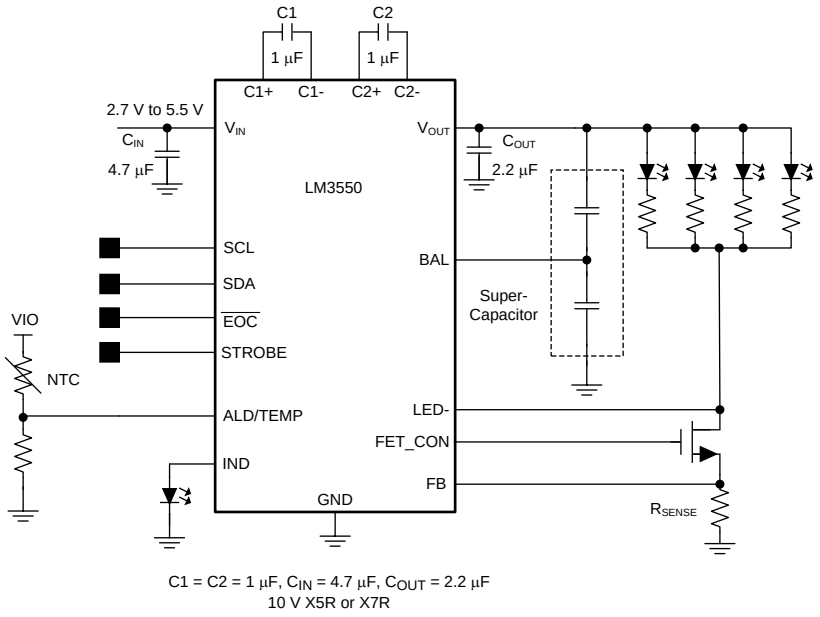


Figure 49. LM3550 Typical Application

8.2.1 Design Requirements

For LM3550, use the parameters listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	5.3 V (maximum)
Torch current	0 to 200 mA (maximum)

8.2.2 Detailed Design Procedure

8.2.2.1 Component Selection

8.2.2.1.1 Super-Capacitor

Super-capacitors, or electrochemical double-layer capacitors (EDLC's), have a very high energy density compared to other capacitor types. Most super-capacitors aimed at applications requiring voltages higher than 3V are three-terminal devices (two super-capacitor cells stacked in series). Special care must be taken to ensure that the voltage on each cell of the super-capacitor does not exceed the maximum rating (typically 2.75 V to 2.85 V, depending on the manufacturer). The LM3550 is capable of safely charging super-capacitors of many different capacitances up to a V_{OUT}(maximum) = 5.3 V typical.

The capacitor balance pin (BAL) on the LM3550 ensures that the voltage on each cell is equal to half of the output voltage to prevent an overvoltage condition on either cell. If either cell fails as a short, the BAL pin does not prevent the second cell from being damaged.

NOTE

The LM3550 is not designed to work with low-voltage, single-cell super-capacitors.

8.2.2.1.2 Boost Capacitors

The LM3550 requires 4 external capacitors for proper operation (C_1 = C_2 = 1 µF; C_{IN} = 4.7 µF; C_{OUT} = 2.2 µF); TI recommends surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR < 20 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM3550 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM3550. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over −55°C to +125°C; X5R: ±15% over −55°C to +85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM3550. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, −20%) and vary significantly over temperature (Y5V: 22%, −82% over −30°C to +85°C range; Z5U: 22%, −56% over 10°C to 85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM3550.

The recommended voltage rating for the capacitors is 10 V to account for DC bias capacitance losses.

8.2.2.1.3 Current Source FET

Choose the proper current source MOSFET to ensure accurate flash current delivery. N-channel MOSFETs (NFET) with allowed drain-to-source voltages (V_{DS}) greater than 5.5 V are required. In order to prevent damage to the current source NFET, special attention must be given to the pulsed-current rating of the MOSFET. The NFET must be sized appropriately to handle the desired flash current and flash duration. Most MOSFET manufacturers provide curves showing the pulsed performance of the NFET in the electrical characteristics section of their data sheets. The performance of the MOSFET rating at temperature, primarily temperatures greater than 40°C, must also be investigated to ensure NFET does not become thermally damaged during a flash pulse. An NFET possessing low R_{DSON} values helps improve the efficiency of the flash pulse.

8.2.2.1.4 ALD/TEMP Components

8.2.2.1.4.1 NTC Selection

NTC thermistors have a temperature-to-resistance relationship of:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T°C+273} - \frac{1}{298}\right)\right]}$$

where

- β is given in the thermistor data sheet
- $R_{25°C}$ is the thermistor's value at 25°C

(11)

R1 in is chosen so that it is equal to:

$$R1 = \frac{V_{TRIP} R_{T(TRIP)}}{(V_{BIAS} - V_{TRIP})}$$

where

- $R_{T(TRIP)}$ is the thermistors value at the temperature trip point
- V_{BIAS} is shown in Figure 50
- V_{TRIP} = 800 mV (typical)

(12)

Choosing R1 here gives a more linear response around the temperature trip voltage. For example, with V_{BIAS} = 1.8 V, a thermistor whose nominal value at 25°C is 100 kΩ, and a β = 4500 K, the trip point is chosen to be 85°C. The value of R(T) at 85°C is:

$$R(T) = 100\ k\Omega \times e^{\left[\beta\left(\frac{1}{85+273} - \frac{1}{298}\right)\right]} = 7.959\ k\Omega$$

$$R1 \text{ is then: } \frac{0.8V \times 7.959\ k\Omega}{1.8V - 0.8V} = 6.367\ k\Omega$$

(13)

Setting the ALD/TEMP Sense High Register to N = 50 or hex 0x32 places the upper trip point to approximately 800 mV. Voltages higher than 800 mV prevent the flash LED from turning on. Based on Figure 50, the Sense Low Register can be set to a lower code to give a second LED current threshold (70% flash). Voltages lower than the value stored in the Sense Low Register allow a full current flash.

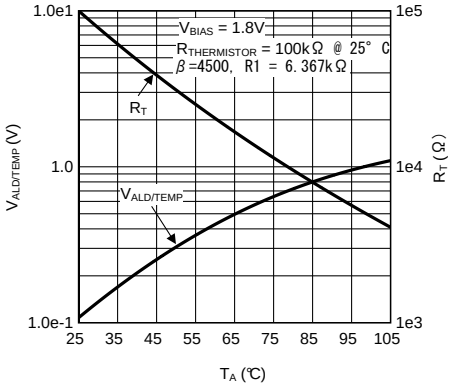


Figure 50. Thermistor Resistive Divider Response vs Temperature

If the temperature changes during a flash event, meaning $V_{ALS/TEMP}$ crosses the sense high and/or sense low values, the current scales to the appropriate zone current.

Place the thermistor as close as possible to the flash LEDs. This provides the best thermal coupling (lowest thermal resistance).

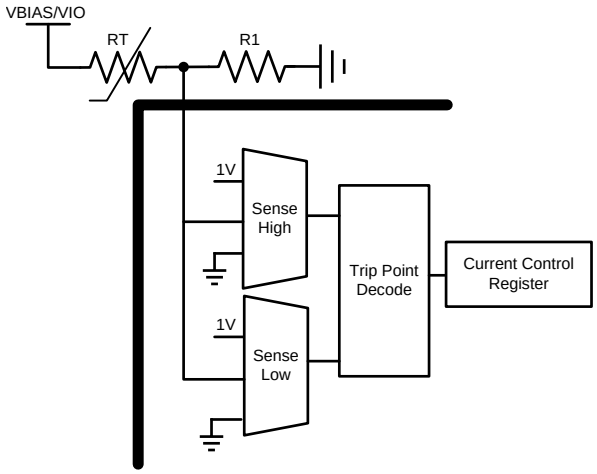
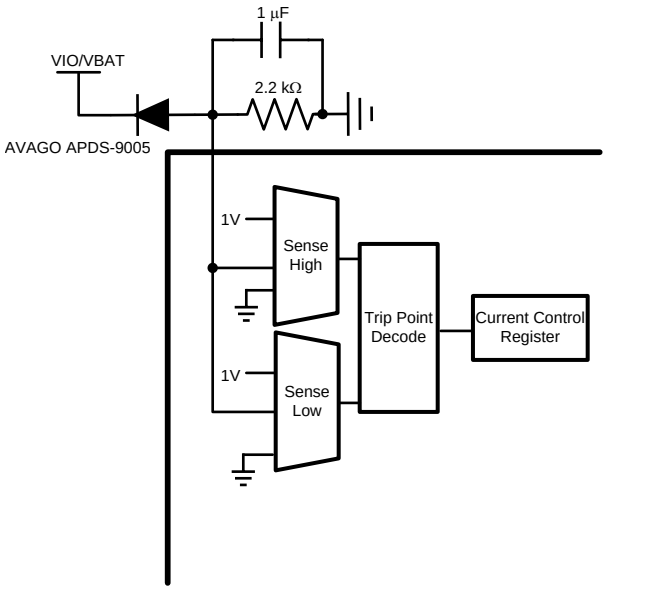


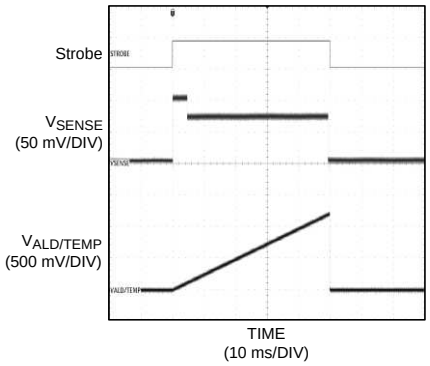
Figure 51. Thermistor Voltage Divider and Sensing Circuit

8.2.2.1.4.2 Ambient Light Sensor

If the ALD/TEMP pin is not used for ambient/LED temperature monitoring, it can be used for ambient light detection. The LM3550 provides three regions of current control based upon ambient conditions. The three regions are defined using the Sense High and Sense Low Registers to set the zone boundaries (user-configurable from 0 to 1 V). Most ambient light sensors are reverse-biased diodes that leak current proportional to the amount of ambient light reaching the sensor. This current is then translated into a voltage by using a resistor in series with the light sensor. The voltage-setting resistor varies based upon the desired ambient detection range and manufacturer.

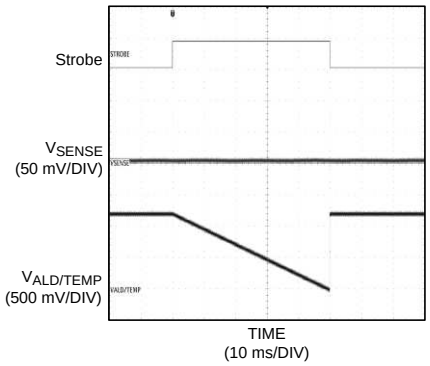


Most ambient light sensors suggest placing a capacitor in parallel with the voltage-setting resistor in order to help filter the 50-, 60-Hz noise generated by fluorescent overhead lighting. This capacitor can range from no capacitor up to 10 µF. The key is to filter the noise so that the peak-to-peak voltage is less than 16 mV (LSB size of the ALD/TEMP sense high and sense low settings). Refer to the data sheet of the ambient light sensor for the recommended capacitor value.



The flash current drops to 70% of the peak once the voltage on the ALD/TEMP pin exceeds the sense low trip point.

Figure 52. Effect of ALD/TEMP Voltage Rising During a Flash



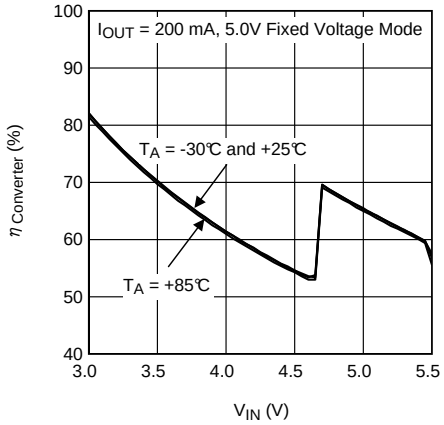
The flash event is not allowed to start if the voltage on ALD/TEMP is higher that the sense high trip point.

Figure 53. Effect of ALD/TEMP Voltage Dropping During a Flash

8.2.2.1.5 Thermal Protection

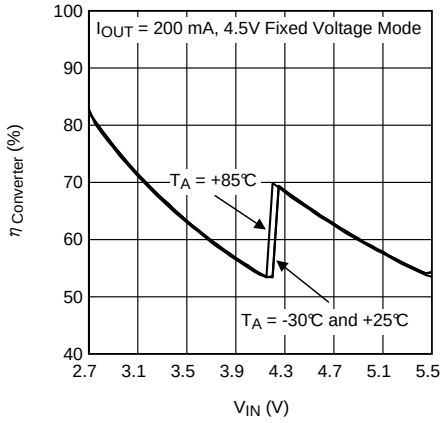
Internal thermal protection circuitry disables the LM3550 when the junction temperature exceeds 145°C (typical). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device recovers and operates normally when the junction temperature falls below 125°C (typical). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

8.2.3 Application Curves



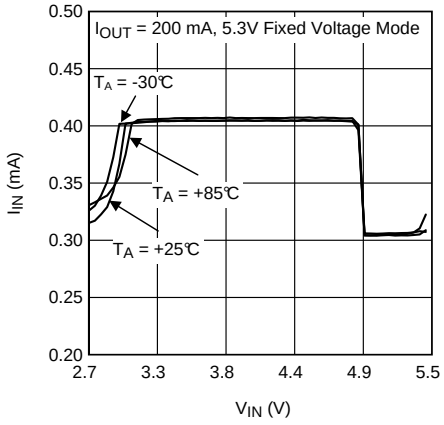
5-V Mode

Figure 54. Converter Efficiency vs Input Voltage



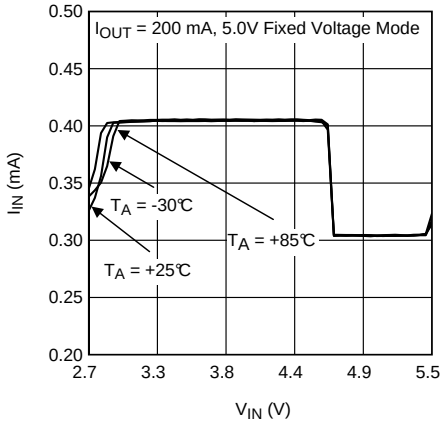
4.5-V Mode

Figure 55. Converter Efficiency vs Input Voltage



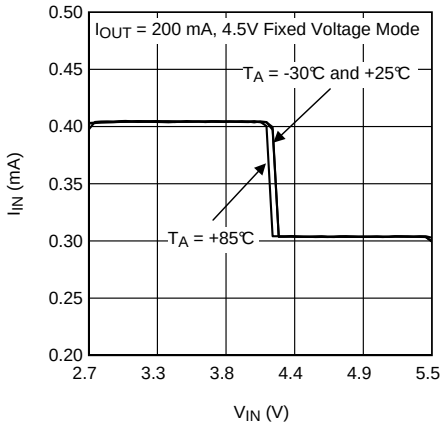
5.3-V Mode

Figure 56. Input Current vs Input Voltage



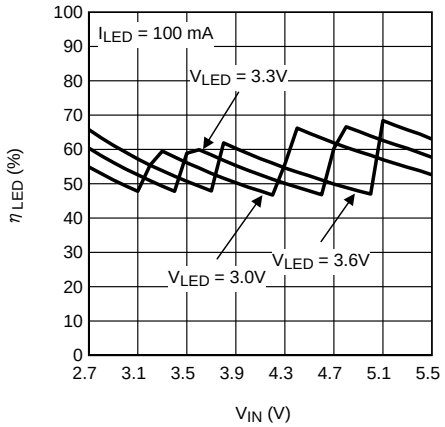
5-V Mode

Figure 57. Input Current vs Input Voltage



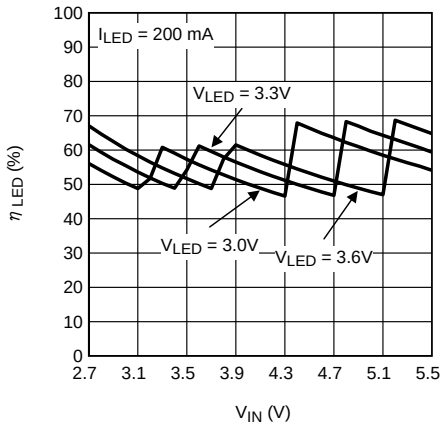
4.5-V Mode

Figure 58. Input Current vs Input Voltage



100 mA

Figure 59. LED Efficiency vs Input Voltage Torch Mode



200 mA

Figure 60. LED Efficiency vs Input Voltage Torch Mode

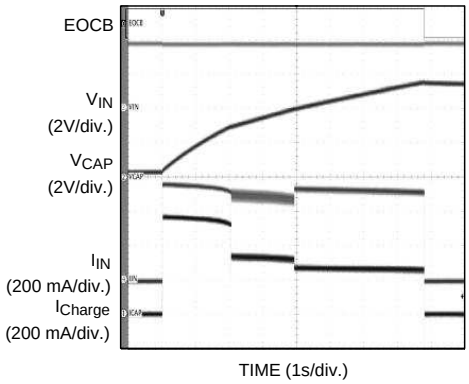


Figure 61. 5.3-V Mode Super Capacitor Charge

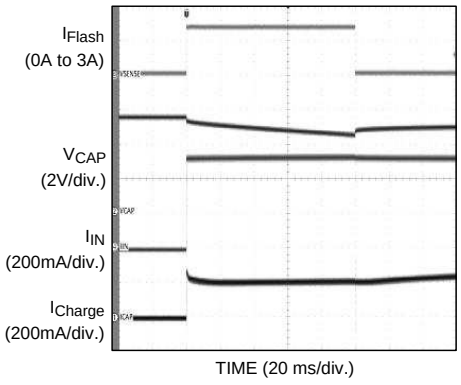


Figure 62. 2 LED, 3-A Flash (1.5 A Each)

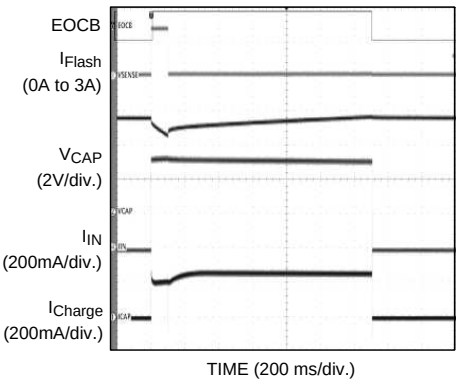


Figure 63. 5.3-V Mode Super Capacitor Recharge

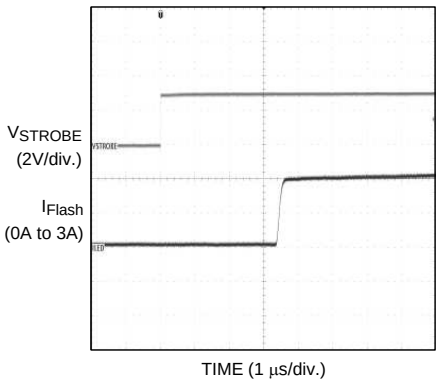


Figure 64. Strobe-to-Flash Delay

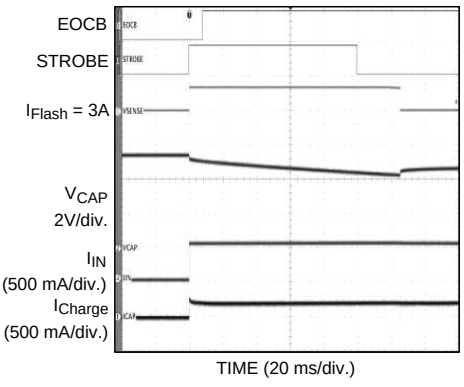


Figure 65. Edge-Sensitive Strobe

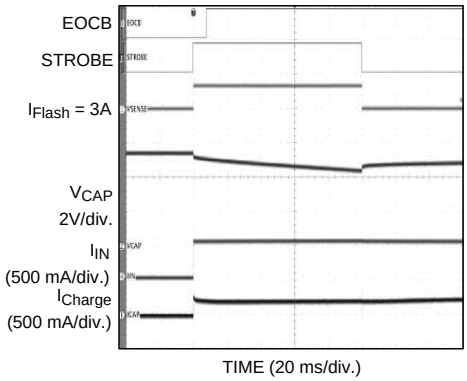


Figure 66. Level-Sensitive Strobe

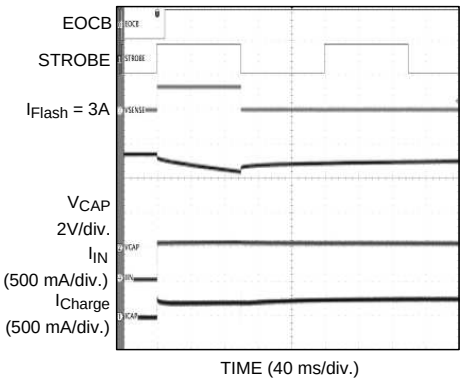


Figure 67. Flash With $\overline{\text{FGATE}}$ = 0

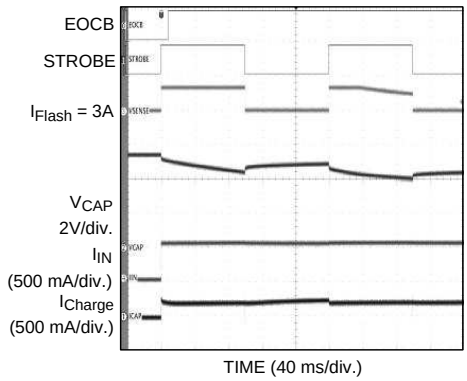
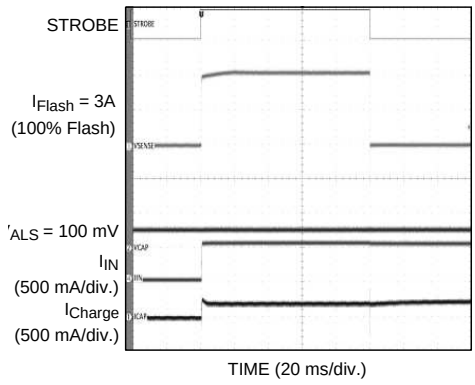
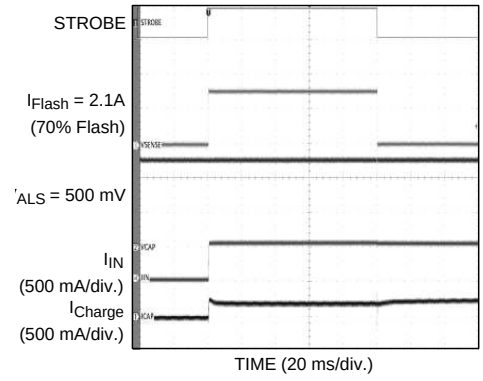


Figure 68. Flash With $\overline{\text{FGATE}}$ = 1



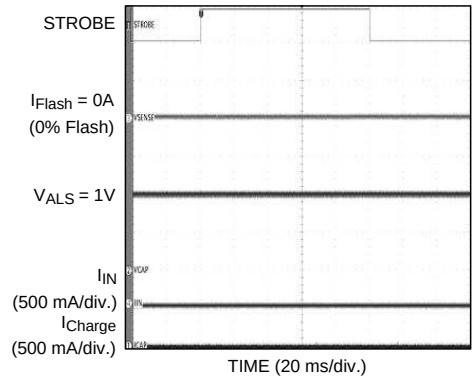
V_{ALS} = 100 mV

Figure 69. ALS Detect Zone 0



V_{ALS} = 500 mV

Figure 70. ALS Detect Zone 1



V_{ALS} = 1 V

Figure 71. ALS Detect Zone 2

9 Power Supply Recommendations

The LM3550 is designed to operate from an input supply range of 2.7 V to 5.5 V. This input supply must be well regulated and provide the peak current required by the LED configuration.

10 Layout

10.1 Layout Guidelines

The UQFN is a leadless package with very good thermal properties. This package has an exposed DAP (die attach pad) at the underside center of the package measuring 1.86 mm × 2.2 mm. The main advantage of this exposed DAP is to offer low thermal resistance when soldered to the thermal ground pad on the PCB. For good PCB layout TI recommends a 1:1 ratio between the package and the PCB thermal land. To further enhance thermal conductivity, the PCB thermal ground pad may include vias to a 2nd layer ground plane. For more detailed instructions on mounting UQFN packages, refer to *AN-1187 Leadless Leadframe Package (LLP)*.

The proceeding steps must be followed to ensure stable operation and proper current source regulation.

1. Bypass V_{IN} with at least a 4.7-µF ceramic capacitor. Connect the positive terminal of this capacitor as close as possible to V_{IN}.
2. Connect C_{OUT} as close as possible to the VOUT pin with at least a 2.2-µF capacitor.
3. Connect the return terminals of the input capacitor and the output capacitor as close as possible to the exposed DAP and GND pins through low impedance traces.
4. Place the two 1-µF flying capacitors (C1 and C2) as close as possible to the LM3550 C1+, C1− and C2+, C2− pins.
5. To minimize losses during the flash pulse, TI recommends that the flash LEDs, the current source NFET, and current-setting resistor be placed as close as possible to the super capacitor.

10.2 Layout Example

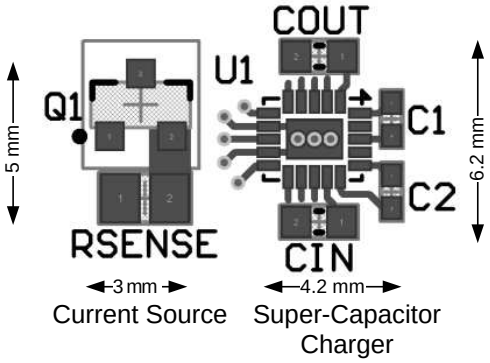


Figure 72. LM3550 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

V_{BATT} Voltage supplying charger circuit.

V_{CAP} Super-capacitor voltage at the end of the charge cycle and before a flash.

I_{CL} Maximum current allowed to be drawn from the battery.

I_{FLASH} LED current during the flash event.

t_{FLASH} Desired flash duration.

C_{SC} Super capacitor value.

V_{LED} Flash diode forward voltage at I_{FLASH}.

V_{HR} The headroom required across the FET and the Sense resistor to maintain current sink regulation.

V_{FB} The degeneration resistor R_{SENSE} regulation voltage that in part sets I_{FLASH}.

R_{DSON} On-Resistance of NFET.

V_{RDSON} The voltage drop across the current source FET.

V_{PUMP} The initial SC voltage required for the Flash.

R_{SENSE} Current set resistor.

V_{DROOP} Voltage droop on the super-capacitor during a flash of duration t_{FLASH}.
$= I_{FLASH} \times t_{FLASH} / C_{SC}$

R_{ESR} Super-capacitor ESR value.

V_{ESR} Voltage drop due to SC ESR.

V_{BAL} Voltage drop due to LED ballast resistors

V_{OH} Overhead charge voltage required for constant current regulation during the entire flash duration.

V_{PUMP} $V_{OH} + V_{LED} + V_{ESR} = V_{FB} + V_{RDSON} + V_{ESR} + V_{LED} + V_{DROOP} + V_{BAL}$

V_{HR} $V_{FB} + V_{RDSON}$

11.2 Related Documentation

For additional information, see the following:

AN-1187 Leadless Leadframe Package (LLP)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3550SP/NOPB	ACTIVE	UQFN	NHU	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-30 to 85	3550	Samples
LM3550SPX/NOPB	ACTIVE	UQFN	NHU	20	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-30 to 85	3550	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

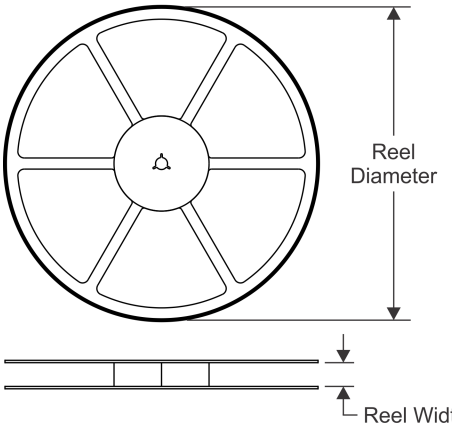
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

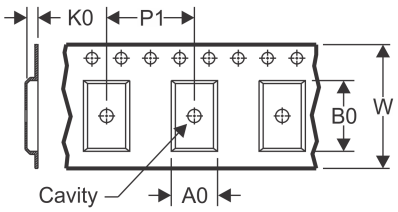
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

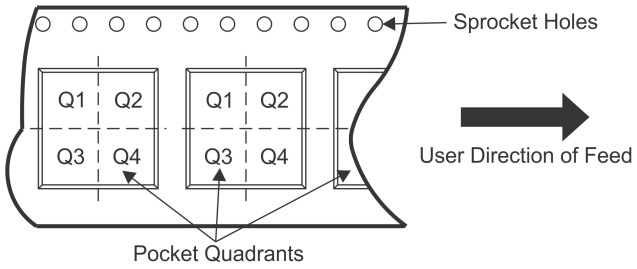


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

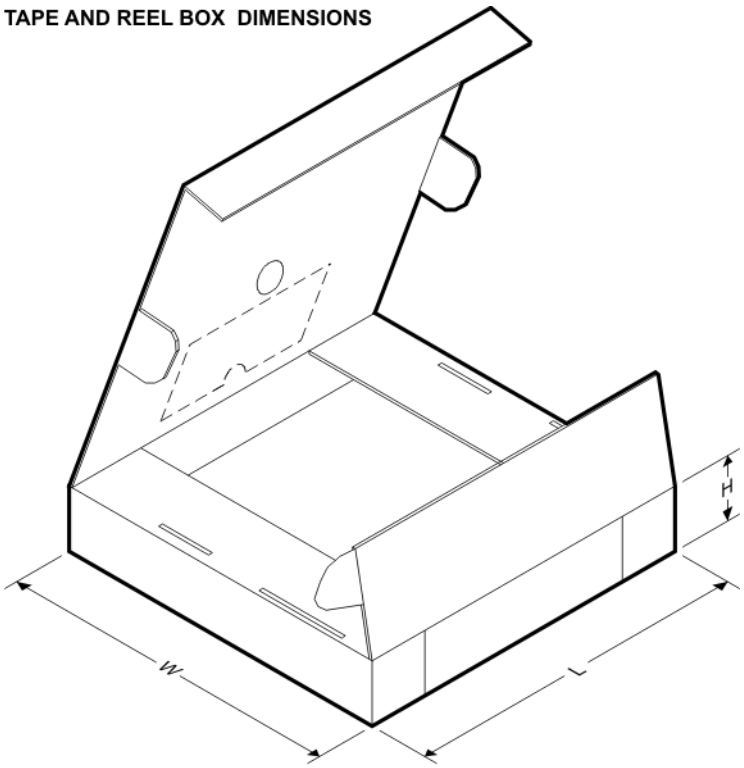
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3550SP/NOPB	UQFN	NHU	20	1000	178.0	12.4	2.7	3.2	0.8	8.0	12.0	Q1
LM3550SPX/NOPB	UQFN	NHU	20	4500	330.0	12.4	2.7	3.2	0.8	8.0	12.0	Q1

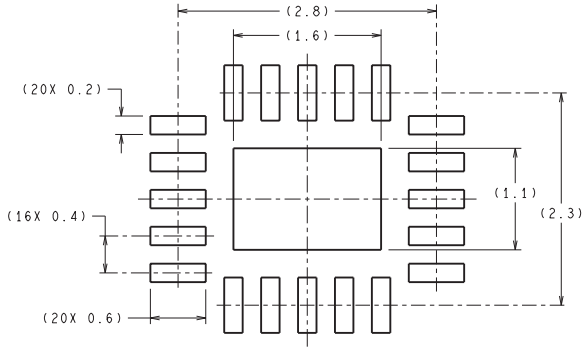
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3550SP/NOPB	UQFN	NHU	20	1000	210.0	185.0	35.0
LM3550SPX/NOPB	UQFN	NHU	20	4500	367.0	367.0	35.0

NHU0020A



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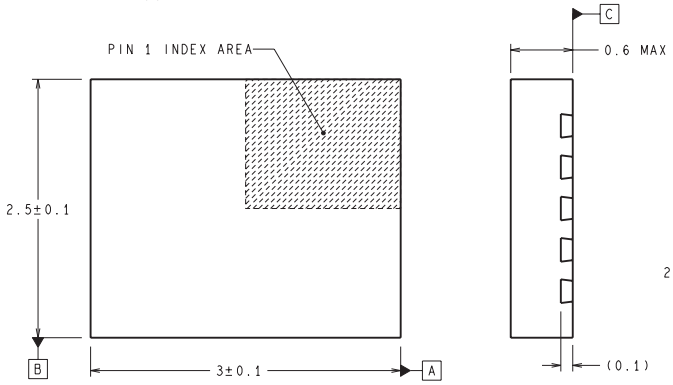

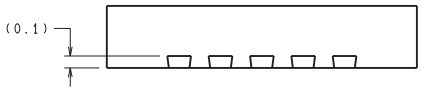

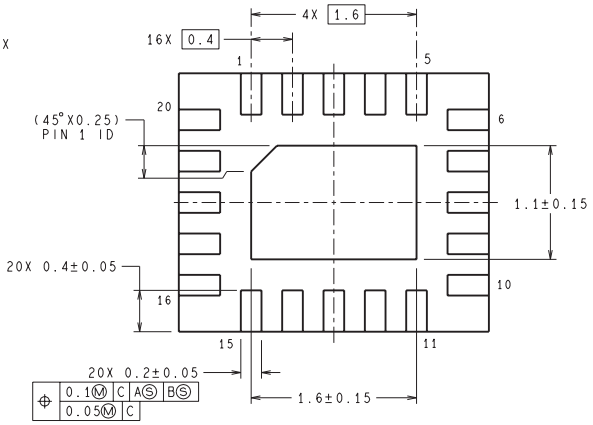

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