INA28x High-Accuracy, Wide Common-Mode Range, Bidirectional Current Shunt Monitors, Zero-Drift Series

1 Features

- Wide Common-Mode Range: –14 V to +80 V
- Offset Voltage: ±20 µV
- CMRR: 140 dB
- Accuracy:
  - ±1.4% Gain Error (Max)
  - 0.3 µV/°C Offset Drift
  - 0.005%/°C Gain Drift (Max)
- Available Gains:
  - 50 V/V: INA282
  - 100 V/V: INA286
  - 200 V/V: INA283
  - 500 V/V: INA284
  - 1000 V/V: INA285
- Quiescent Current: 900 µA (Max)

2 Applications

- Telecom Equipment
- Automotive
- Power Management
- Solar Inverters

3 Description

The INA28x family includes the INA282, INA283, INA284, INA285, and INA286 devices. These devices are voltage output current shunt monitors that can sense drops across shunts at common-mode voltages from –14 V to +80 V, independent of the supply voltage. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10 mV full-scale.

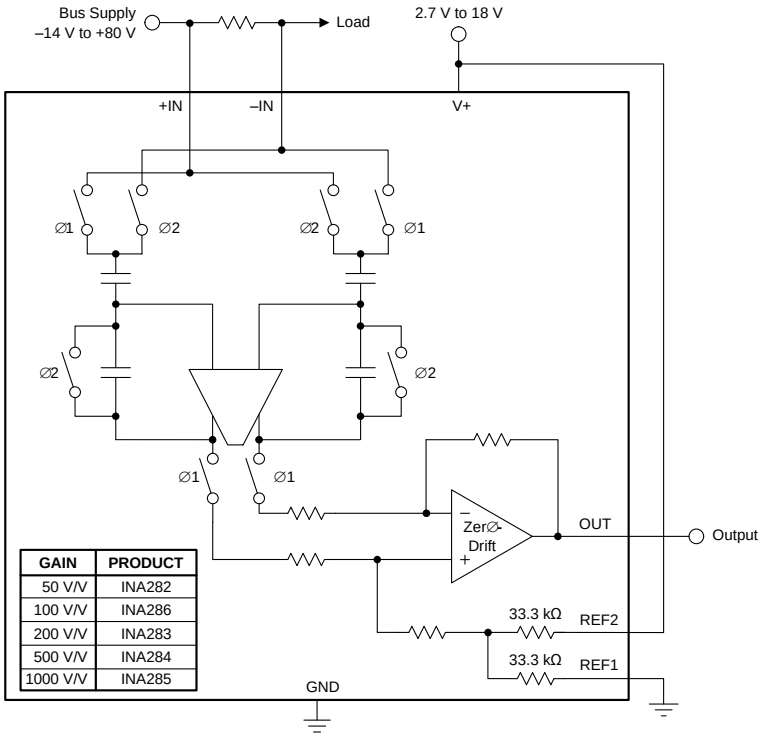
These current sense amplifiers operate from a single +2.7-V to +18-V supply, drawing a maximum of 900 µA of supply current. These devices are specified over the extended operating temperature range of –40°C to +125°C, and offered in SOIC-8 and VSSOP-8 packages.

Device Information(1)

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
INA28x	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Detailed Block Diagram



GAIN	PRODUCT
50 V/V	INA282
100 V/V	INA286
200 V/V	INA283
500 V/V	INA284
1000 V/V	INA285

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2012) to Revision C — **Page**

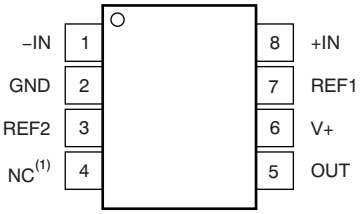
- Added DGK (VSSOP) package to data sheet ... 1
- Changed front page diagram ... 1
- Added ESD Ratings and Recommended Operating Conditions tables, and *Feature Description*, *Application and Implementation*, *Power Supply Recommendations* ,*Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 4
- Deleted Machine Model ESD rating ... 4
- Changed HBM ESD rating from ±3000 V to ±2000 V ... 4
- Added RVRR as symbol for reference voltage rejection ratio ... 5
- Changed order of figures in *Typical Characteristics* section ... 7
- Changed Figure 16 ... 8
- Changed V_{DRIVE} condition in Figure 19 and Figure 20 ... 9
- Added functional block diagram ... 13
- Changed Figure 32 and Figure 33 ... 15
- Changed Figure 34 and Figure 35 ... 16
- Changed Figure 36 and Figure 37 ... 17
- Changed Figure 38 ... 18
- Changed *Reference Common-Mode Rejection* to *Reference Voltage Rejection Ratio* ... 18
- Changed R_{CMR} to RVRR in Table 1 and Table 2 ... 19
- Changed Figure 39 ... 20
- Changed Figure 40 ... 21
- Changed Figure 42 ... 23

Changes from Revision A (July 2010) to Revision B — **Page**

- Changed devices from product preview to production data. ... 1

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



(1) NC: This pin is not internally connected. Leave the NC pin floating or connect this pin to GND.

Pin Descriptions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	–IN	Analog input	Connect this pin to load side of shunt resistor.
2	GND	Analog	Ground
3	REF2	Analog input	Reference voltage, 0 V to V+. See *Reference Pin Connection Options* section for connection options.
4	NC	—	This pin is not internally connected. Either float or connect this pin to GND.
5	OUT	Analog output	Output voltage
6	V+	Analog	Power supply, 2.7 V to 18 V
7	REF1	Analog input	Reference voltage, 0 V to V+. See *Reference Pin Connection Options* section for connection options.
8	+IN	Analog input	Connect this pin to supply side of shunt resistor.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V+			18	V
Analog inputs, V_{+IN}, $V_{–IN}$ (2)	Differential (V_{+IN}) – ($V_{–IN}$)(3)	–5	+5	V
	Common-mode	–14	+80	V
REF1, REF2, OUT		GND – 0.3	(V+) + 0.3	V
Input current into any pin			5	mA
Junction temperature			150	°C
Storage temperature range, T_{stg}		–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{+IN} and $V_{–IN}$ are the voltages at the +IN and –IN pins, respectively.
(3) Input voltages must not exceed common-mode rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V+	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		+125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA28x		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.9	164.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.9	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	85.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.9	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	83.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, RTI(1)	V_{SENSE} = 0 mV			±20	±70	µV
dV_{OS}/dT	vs temperature	V_{SENSE} = 0 mV, T_A = –40°C to +125°C			±0.3	±1.5	µV/°C
PSRR	vs power supply	V+ = +2.7 V to +18 V, V_{SENSE} = 0 mV			3		µV/V
V_{CM}	Common-mode input range	T_A = –40°C to +125°C		–14		+80	V
CMRR	Common-mode rejection ratio	V_{+IN} = –14 V to +80 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C		120	140		dB
I_B	Input bias current per pin(2)	V_{SENSE} = 0 mV			25		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV			1		µA
	Differential input impedance				6		kΩ
REFERENCE INPUTS							
	Reference input gain				1		V/V
	Reference input voltage range(3)			0		V_{GND} + 9	V
	Divider accuracy(4)				±0.2%	±0.5%	
RVRR	Reference voltage rejection ratio ($V_{REF}1$ = $V_{REF}2$ = 40 mV to 9 V, V+ = 18 V)	INA282			±25	±75	µV/V
			T_A = –40°C to +125°C		0.055		µV/V/°C
		INA283			±13	±30	µV/V
			T_A = –40°C to +125°C		0.040		µV/V/°C
		INA284			±6	±25	µV/V
			T_A = –40°C to +125°C		0.015		µV/V/°C
		INA285			±4	±10	µV/V
			T_A = –40°C to +125°C		0.010		µV/V/°C
		INA286			±17	±45	µV/V
			T_A = –40°C to +125°C		0.040		µV/V/°C
GAIN(5) (GND + 0.5 V ≤ V_{OUT} ≤ (V+) – 0.5 V; V_{REF1} = V_{REF2} = (V+) / 2 for all devices)							
G	Gain	INA282, V+ = 5 V			50		V/V
		INA283, V+ = 5 V			200		V/V
		INA284, V+ = 12 V			500		V/V
		INA285, V+ = 12 V			1000		V/V
		INA286, V+ = 5 V			100		V/V
	Gain error	INA282, INA283, INA286			±0.4%	±1.4%	
		INA284, INA285			±0.4%	±1.6%	
		T_A = –40°C to +125°C			0.0008	0.005	%/°C

(1) RTI = referred-to-input.
(2) See typical characteristic graph Figure 7.
(3) The average of the voltage on pins REF1 and REF2 must be between V_{GND} and the lesser of (V_{GND} + 9 V) and V+.
(4) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 36.
(5) See typical characteristic graph Figure 12.

Electrical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Nonlinearity error			±0.01%		
	Output impedance			1.5		Ω
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(6)						
	Swing to V+ power-supply rail	V+ = 5 V, R_{LOAD} = 10 kΩ to GND, T_A = –40°C to +125°C		(V+) – 0.17	(V+) – 0.4	V
	Swing to GND	R_{LOAD} = 10 kΩ to GND, T_A = –40°C to +125°C		GND + 0.015	GND + 0.04	V
FREQUENCY RESPONSE						
BW	Effective bandwidth(7)	INA282		10		kHz
		INA283		10		kHz
		INA284		4		kHz
		INA285		2		kHz
		INA286		10		kHz
NOISE, RTI(1)						
	Voltage noise density	1 kHz		110		nV/√Hz
POWER SUPPLY						
V_S	Specified voltage range	T_A = –40°C to +125°C	2.7		18	V
I_Q	Quiescent current			600	900	µA

(6) See typical characteristic graphs Figure 16 through Figure 18.
(7) See typical characteristic graph Figure 1 and the *Effective Bandwidth* section.

6.6 Typical Characteristics

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

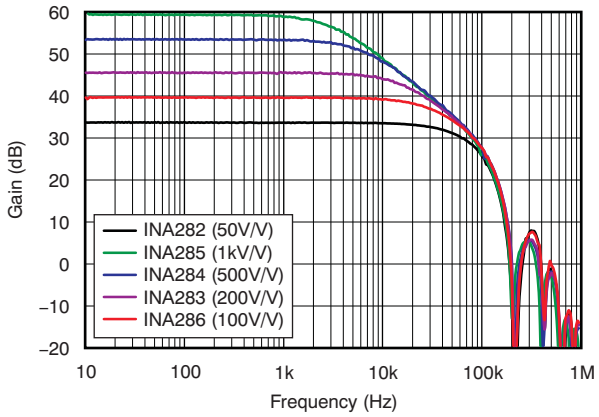


Figure 1. Gain vs Frequency

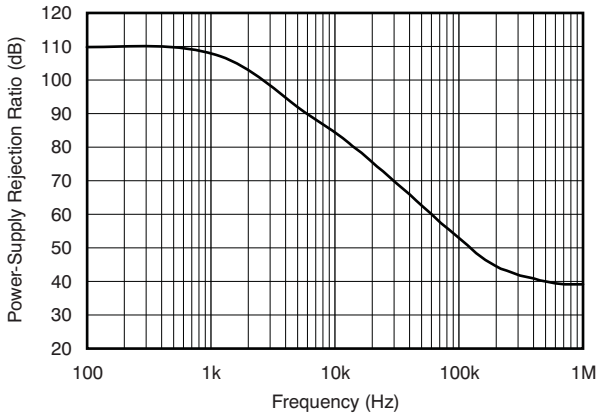


Figure 2. INA282 PSRR (RTI) vs Frequency

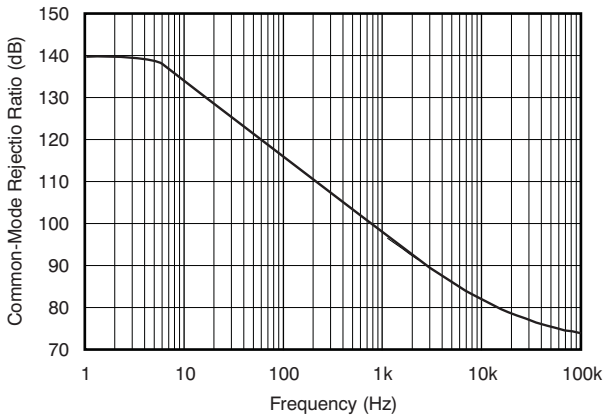


Figure 3. INA284 Common-Mode Rejection Ratio (RTI)

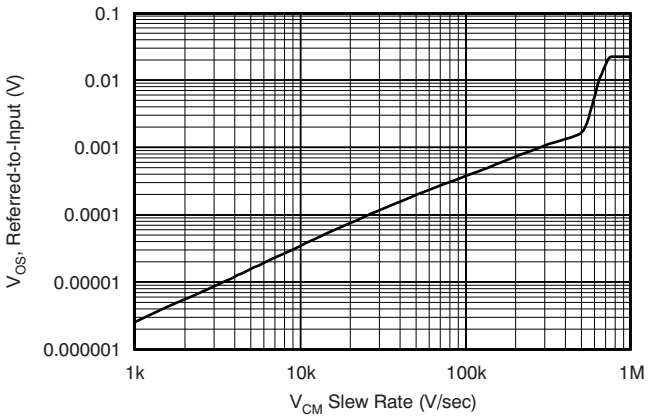


Figure 4. INA282 Common-Mode Slew Rate Induced Offset

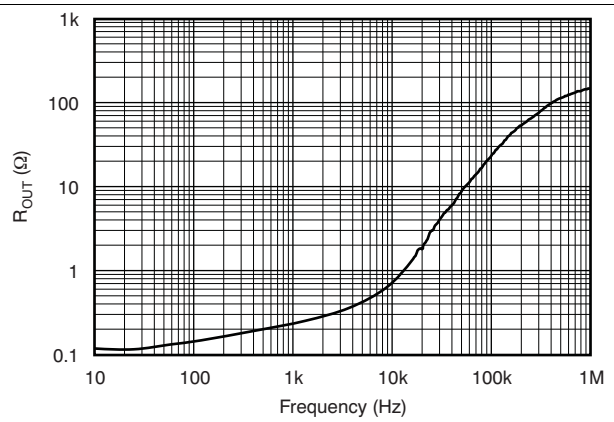


Figure 5. INA286 Output Impedance vs Frequency

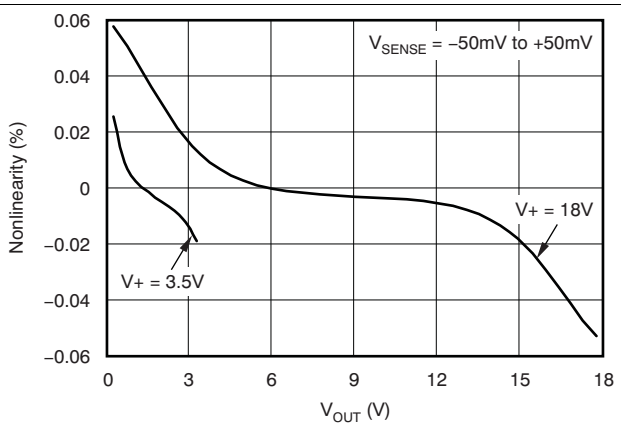


Figure 6. INA282 Typical Nonlinearity vs Output Voltage

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

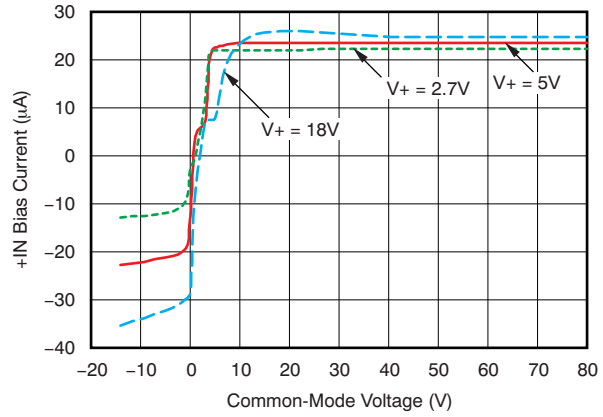


Figure 7. INA283 +IN Bias Current vs Common-Mode Voltage

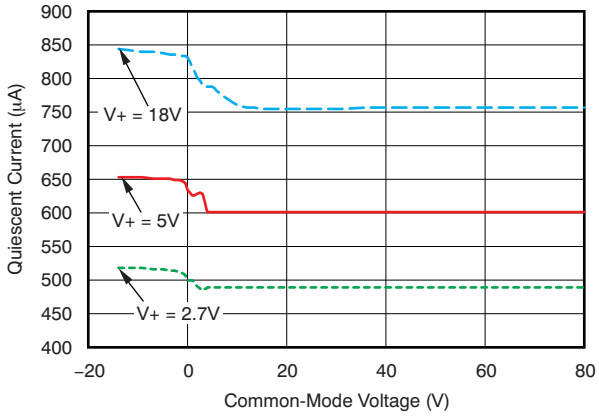


Figure 8. INA283 Quiescent Current vs Common-Mode Voltage

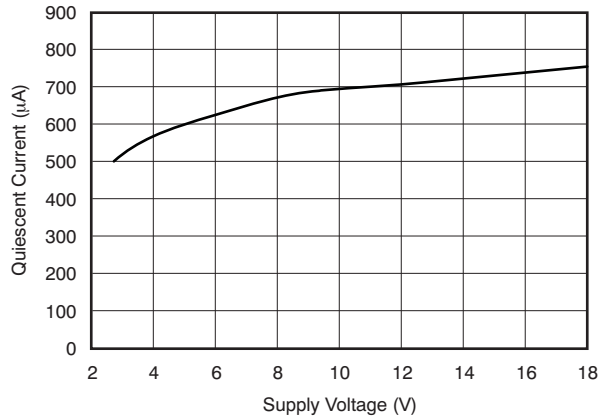


Figure 9. Quiescent Current vs Supply Voltage

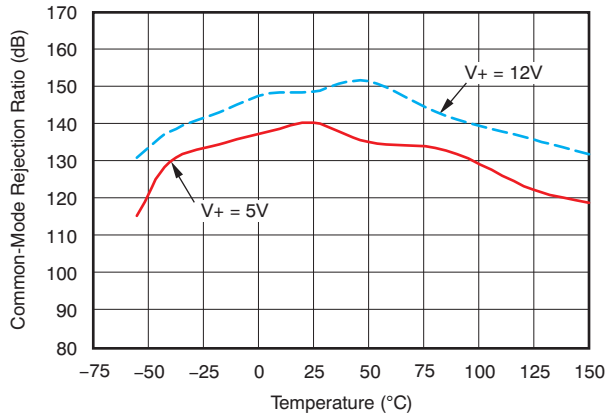


Figure 10. Common-Mode Rejection Ratio vs Temperature

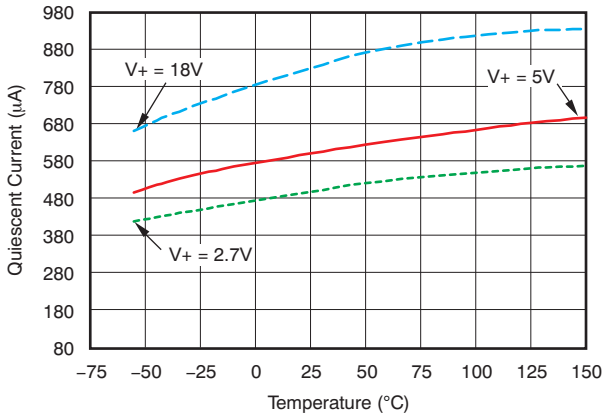


Figure 11. Quiescent Current vs Temperature

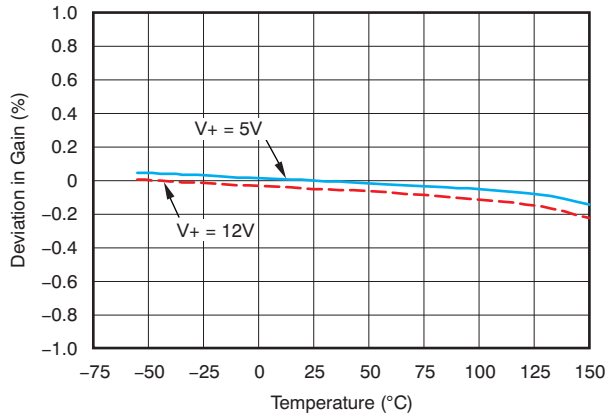


Figure 12. Deviation in Gain vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

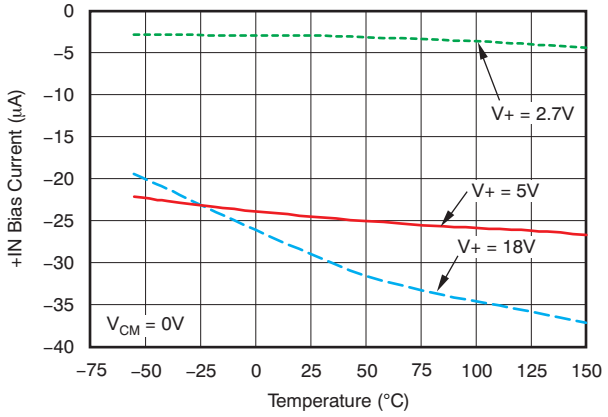


Figure 13. +IN Bias Current vs Temperature

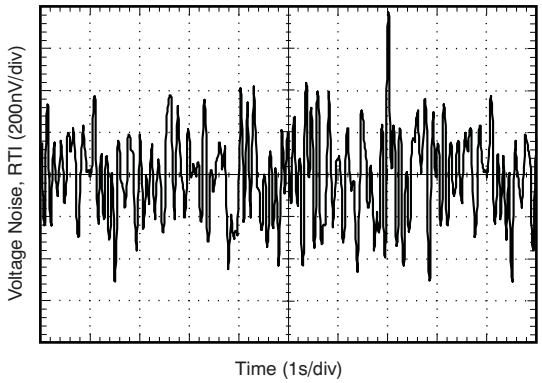


Figure 14. INA282 0.1-Hz to 10-Hz Voltage Noise, RTI

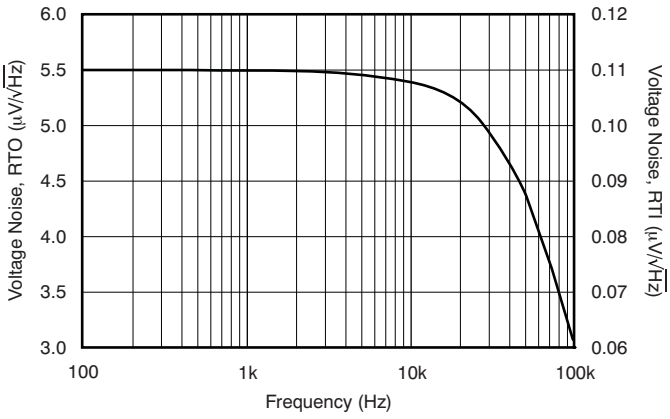


Figure 15. INA282 Voltage Noise vs Frequency

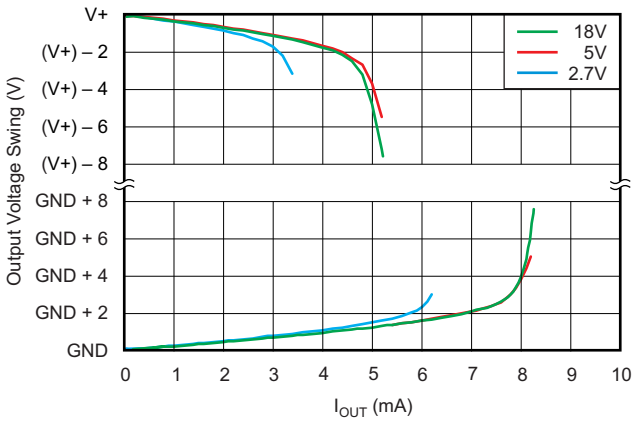


Figure 16. INA284 Output Voltage Swing vs Output Current

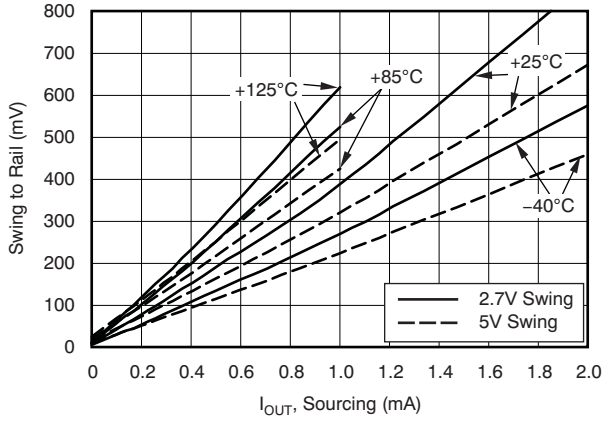


Figure 17. INA283 Swing to Rail vs Output Current

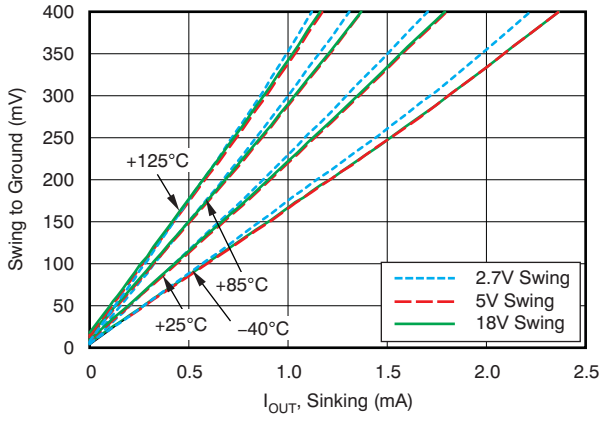


Figure 18. INA283 Swing to Ground vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

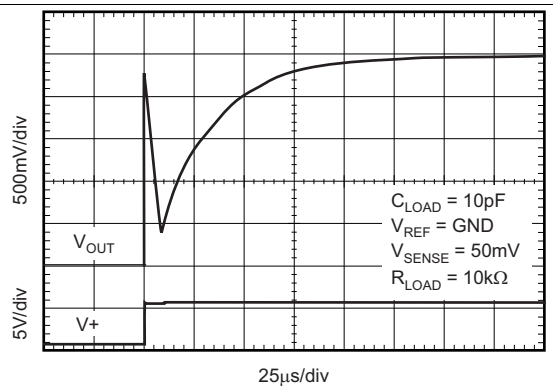


Figure 19. Start-Up Transient Response

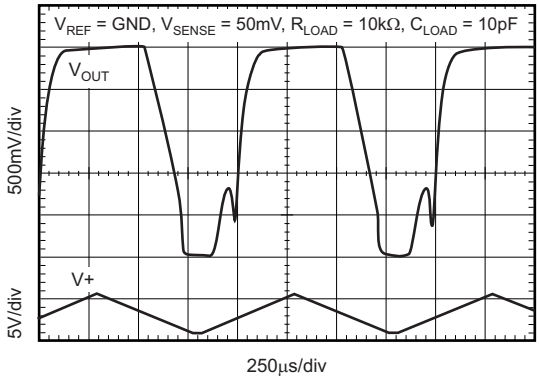


Figure 20. Start-Up Transient Response

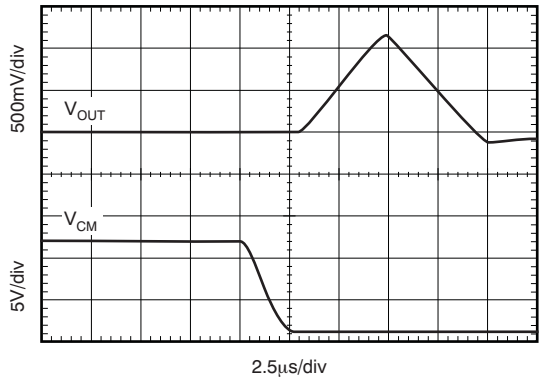


Figure 21. 12-V Common-Mode Step Response

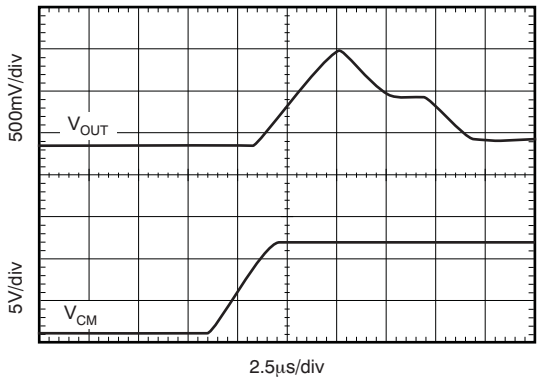


Figure 22. 12-V Common-Mode Step Response

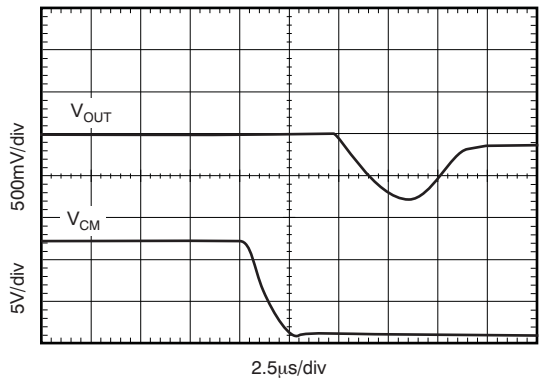


Figure 23. 12-V Common-Mode Step Response

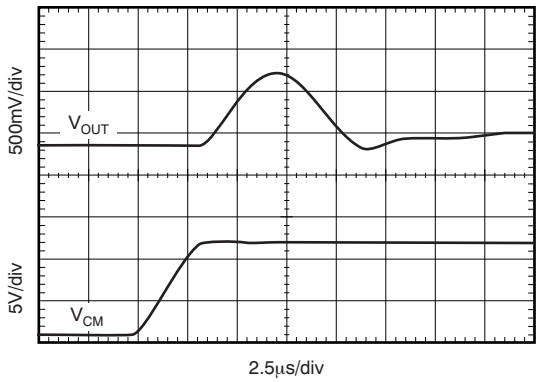


Figure 24. 12-V Common-Mode Step Response

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

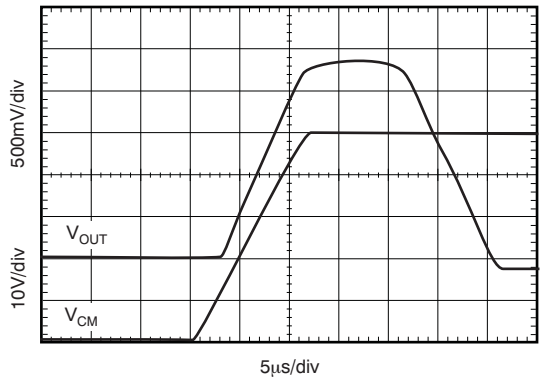


Figure 25. 50-V Common-Mode Step Response

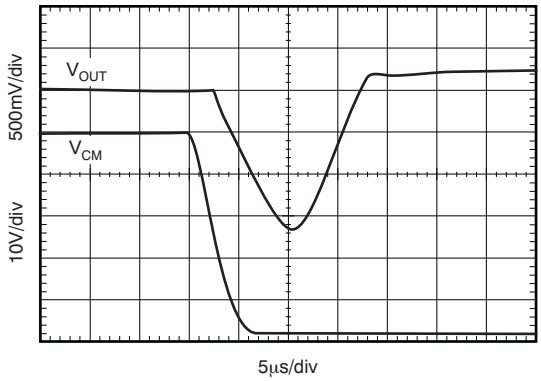


Figure 26. 50-V Common-Mode Step Response

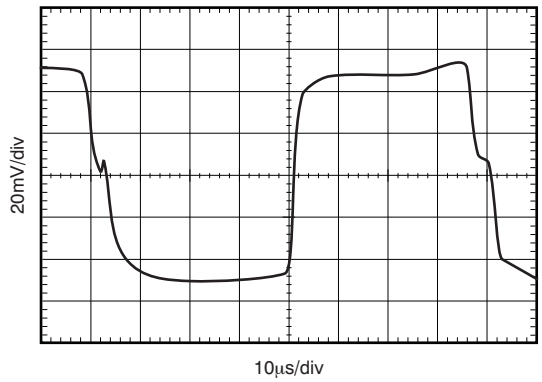


Figure 27. 100-mV Step Response

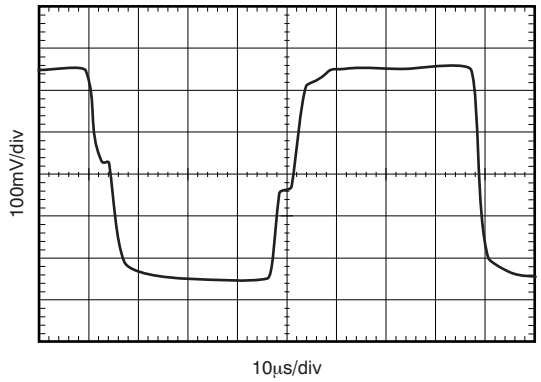


Figure 28. 500-mV Step Response

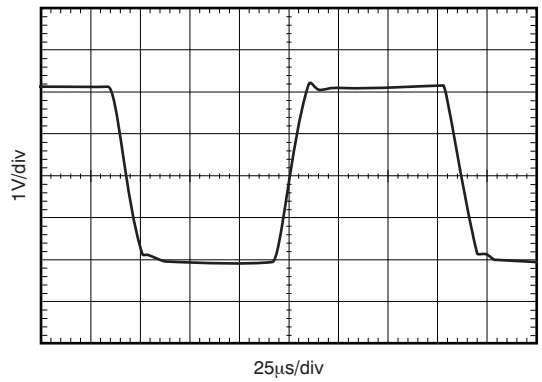


Figure 29. 4-V Step Response

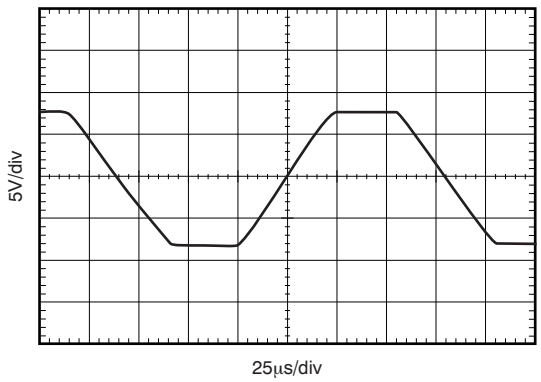


Figure 30. 17-V Step Response

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V_{+IN} = 12 V, V_{REF1} = V_{REF2} = 2.048 V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$ (unless otherwise noted)

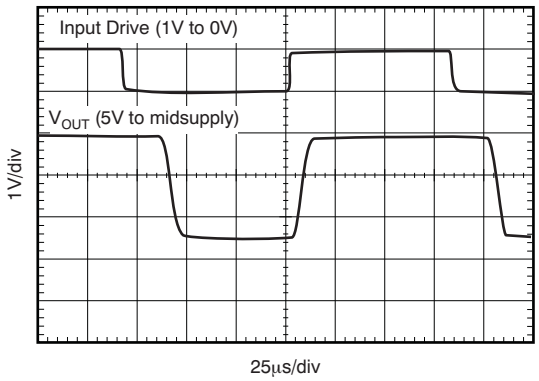


Figure 31. Input Overload

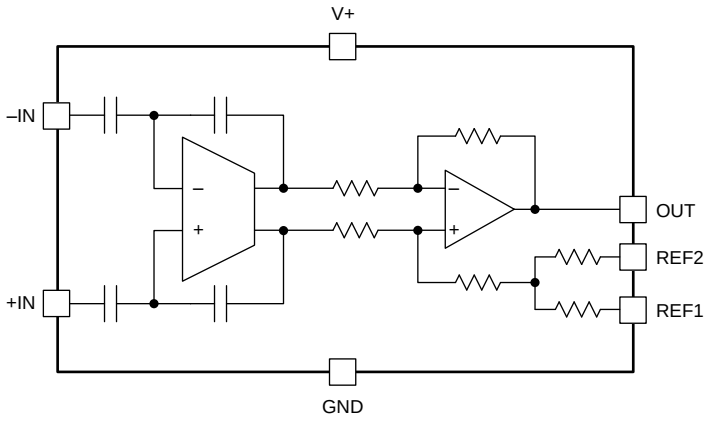
7 Detailed Description

7.1 Overview

The INA28x family of voltage output current-sensing amplifiers are specifically designed to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the devices. This family features a common-mode range that extends 14 V below the negative supply rail, as well as up to 80 V, allowing for either low-side or high-side current sensing while the device is powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 70 µV with a maximum temperature contribution of 1.5 µV/°C over the full temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Selecting R_S

The zero-drift offset performance of the INA28x family offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift, current-shunt monitors typically require a full-scale range of 100 mV. The INA28x family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude, with many additional benefits. Alternatively, applications that must measure current over a wide dynamic range can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA282, INA286, or INA283 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA282 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 55 mV, with only 70 µV of offset.

7.3.2 Effective Bandwidth

The extremely high dc CMRR of the INA28x family results from the switched-capacitor input structure. Because of this architecture, the INA28x exhibits discrete time-system behaviors, as illustrated in the *Gain vs Frequency* curve of Figure 1 and the *Step Response* curves of Figure 21 through Figure 28. The response to a step input depends in part on the phase of the internal INA28x clock when the input step occurs. It is possible to overload the input amplifier with a rapid change in input common-mode voltage (see Figure 4). Errors as a result of common-mode voltage steps or overload situations typically disappear within 15 µs after the disturbance is removed.

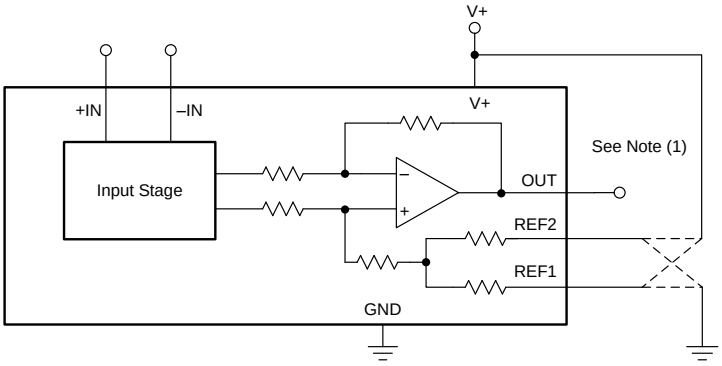
7.3.3 Transient Protection

The –14-V to +80-V common-mode range of the INA28x family is ideal for withstanding automotive fault conditions that range from 12-V battery reversal up to 80-V transients; no additional protective components are needed up to those levels. In the event that the INA28x family is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (Zener diodes or transorbs) are required. Use of metal-oxide varistors (MOVs) or voltage-dependent resistors (VDRs) is not recommended except when they are used in addition to a semiconductor transient absorber. Select a transient absorber that does not allow the INA28x family to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage as a result of transient absorber dynamic impedance). Despite the use of internal zener-type electrostatic discharge (ESD) protection, the INA28x family does not lend itself to using external resistors in series with the inputs without degrading gain accuracy.

7.4 Device Functional Modes

7.4.1 Reference Pin Connection Options

Figure 32 illustrates a test circuit for reference-divider accuracy. The output of the INA28x family can be connected for unidirectional or bidirectional operation. Do not connect the REF1 pin or the REF2 pin to any voltage source lower than GND or higher than V+. The effective reference voltage (REF1 + REF2) / 2 must be 9 V or less. This parameter means that the V+ reference output connection shown in Figure 34 is not allowed for a V+ value greater than 9 V. However, the split-supply reference connection shown in Figure 36 is allowed for all values of V+ up to 18 V.



(1) Reference divider accuracy is determined by measuring the output with the reference voltage applied to alternate reference resistors, and calculating a result where the amplifier offset is cancelled in the final measurement.

Figure 32. Test Circuit For Reference Divider Accuracy

7.4.1.1 Unidirectional Operation

Unidirectional operation allows the INA28x family to measure currents through a resistive shunt in one direction. In the case of unidirectional operation, set the output at the negative rail (near ground, and the most common connection) or at the positive rail (near V+) when the differential input is 0 V. The output moves to the opposite rail when a correct polarity differential input voltage is applied.

The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to move the output down. If the output is set at ground, the polarity is positive to move the output up.

The following sections describe how to configure the output for unidirectional operation.

7.4.1.1.1 Ground Referenced Output

When using the INA28x family in ground referenced output mode, both reference inputs are connected to ground; this configuration takes the output to the negative rail when there is 0 V differential at the input (as Figure 33 shows).

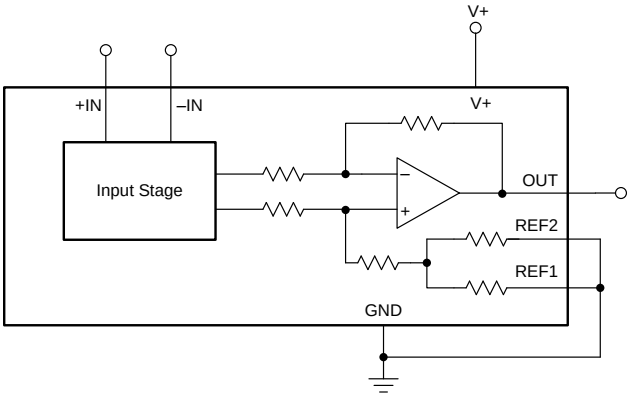


Figure 33. Ground Referenced Output

Device Functional Modes (continued)

7.4.1.1.2 V+ Referenced Output

V+ referenced output mode is set when both reference pins are connected to the positive supply. This mode is typically used when a diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (as shown in Figure 34).

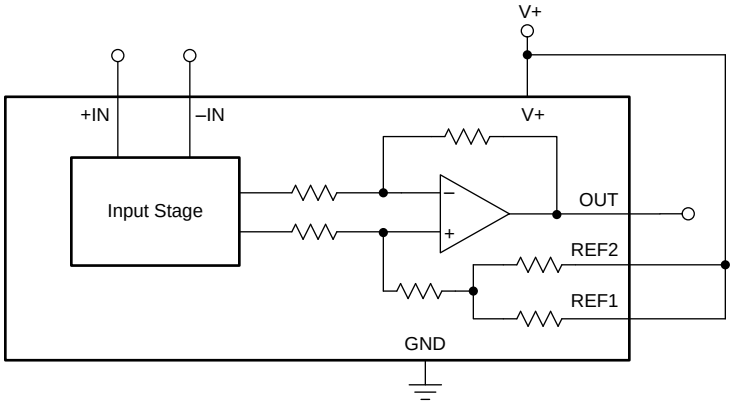


Figure 34. V+ Referenced Output

7.4.1.2 Bidirectional Operation

Bidirectional operation allows the INA28x family to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, between 0 V to 9 V, but never to exceed the supply voltage). Typically, the reference inputs are set at half-scale for equal range in both directions. In some cases, however, the reference inputs are set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage or voltages to the reference inputs. REF1 and REF2 are connected to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

7.4.1.2.1 External Reference Output

Connecting both pins together and to a reference produces an output at the reference voltage when there is no differential input; this configuration is illustrated in Figure 35. The output moves down from the reference voltage when the input is negative relative to the –IN pin and up when the input is positive relative to the –IN pin. Note that this technique is the most accurate way to bias the output to a precise voltage.

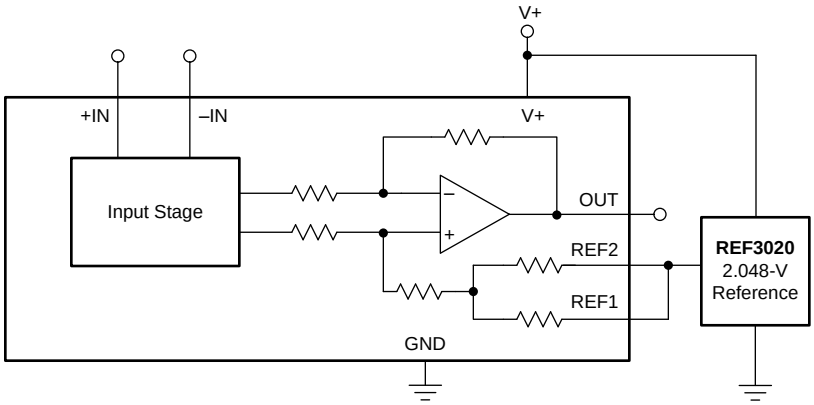


Figure 35. External Reference Output

Device Functional Modes (continued)

7.4.1.2.2 Splitting The Supply

By connecting one reference pin to V+ and the other to the ground pin, the output is set at half of the supply when there is no differential input, as shown in Figure 36. This method creates a midscale offset that is ratiometric to the supply voltage; thus, if the supply increases or decreases, the output remains at half the supply.

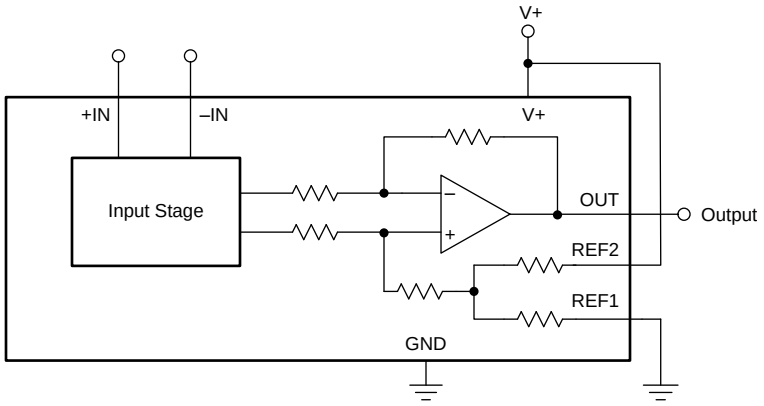


Figure 36. Split-Supply Output

7.4.1.2.3 Splitting an External Reference

In this case, an external reference is divided by two with an accuracy of approximately 0.5% by connecting one REF pin to ground and the other REF pin to the reference (as Figure 37 illustrates).

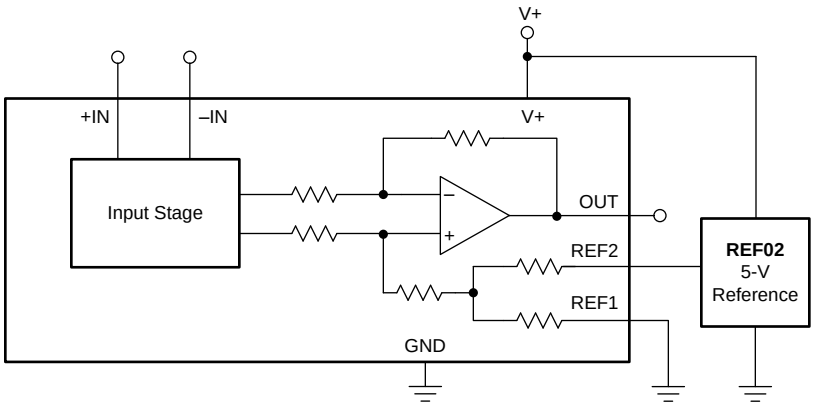


Figure 37. Split Reference Output

7.4.2 Shutdown

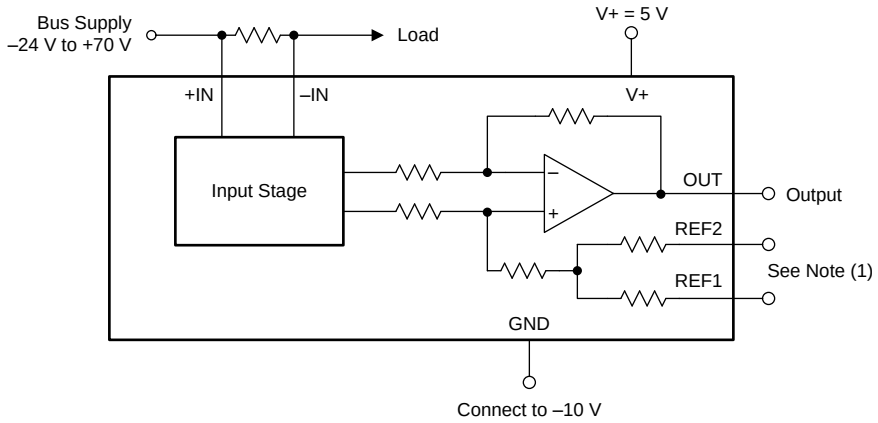
While the INA28x family does not provide a shutdown pin, the quiescent current of 600 µA enables the device to be powered from the output of a logic gate. Take the gate low to shut down the INA28x family devices.

7.4.3 Extended Negative Common-Mode Range

Using a negative power supply can extend the common-mode range 14 V more negative than the supply used. For instance, a –10-V supply allows up to a –24-V negative common-mode. Remember to keep the total voltage between the GND pin and V+ pin to less than 18 V. The positive common-mode decreases by the same amount.

The reference input simplifies this type of operation because the output quiescent bias point is always based on the reference connections. Figure 38 shows a circuit configuration for common-mode ranges from –24 V to +70 V.

Device Functional Modes (continued)



(1) Connect the REF pins as desired; however, they cannot exceed 9 V above the GND pin voltage.

Figure 38. Circuit Configuration for Common-Mode Ranges from –24 V to +70 V

7.4.4 Calculating Total Error

The electrical specifications for the INA28x family of devices include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in the *Electrical Characteristics* table. In order to accurately calculate the expected error of the device, the operating conditions of the device must first be known. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them in order to calculate the total error value for the device under any normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode rejection ratio, gain error, and nonlinearity error. For the INA28x, an additional error source referred to as *reference voltage rejection ratio* is also included in the total error value.

The nonlinearity error of the INA28x is relatively low compared to the gain error specification. This low error results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA28x decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal resulting in an increase in error in the measurement. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The relatively low input offset voltages present in the INA28x devices limit the amount of contribution the offset voltage has on the total error term.

The term *reference voltage rejection ratio* refers to the amount of error induced by applying a reference voltage to the INA28x device that deviates from the inherent bias voltage present at the output of the first stage of the device. The output of the switched-capacitor network and first-stage amplifier has an inherent bias voltage of approximately 2.048 V. Applying a reference voltage of 2.048 V to the INA28x reference pins results in no additional error term contribution. Applying a voltage to the reference pins that differs from 2.048 V creates a voltage potential in the internal difference amplifier, resulting in additional current flowing through the resistor network. As a result of resistor tolerances, this additional current flow causes additional error at the output because of resistor mismatches. Additionally, as a result of resistor tolerances, this additional current flow causes additional error at the output based on the common-mode rejection ratio of the output stage amplifier. This error term is referred back to the input of the device as additional input offset voltage. Increasing the difference between the 2.048 V internal bias and the external reference voltage results in a higher input offset voltage. Also, as the error at the output is referred back to the input, there is a larger impact on the input-referred offset, V_{OS}, for the lower-gain versions of the device.

Device Functional Modes (continued)

Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well, to provide the user more information on how much error variance is present from device to device.

7.4.4.1 Example 1

INA282; V+ = 5 V; V_{CM} = 12 V; V_{REF1} = V_{REF2} = 2.048 V; V_{SENSE} = 10 mV

Table 1. Example 1

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	V_{OS}	—	20 µV	70 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	0 µV	0 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times (2.048\ V - V_{REF})$	0 µV	0 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	20 µV	70 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.20%	0.70%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error	—	$\sqrt{(Error\_V_{OS})^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.45%	1.56%

7.4.4.2 Example 2

INA286; V+ = 5 V; V_{CM} = 24 V; V_{REF1} = V_{REF2} = 0 V; V_{SENSE} = 10 mV

Table 2. Example 2

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	V_{OS}	—	20 µV	70 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	1.2 µV	12 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times (2.048\ V - V_{REF})$	34.8 µV	92.2 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	40.2 µV	116.4 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.40%	1.16%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error	—	$\sqrt{(Error\_V_{OS})^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.57%	1.82%

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA28x family of devices measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pins to adjust the functionality of the output signal is shown in multiple configurations.

8.1.1 Basic Connections

Figure 39 shows the basic connection of an INA28x family device. Connect the input pins, +IN and –IN, as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

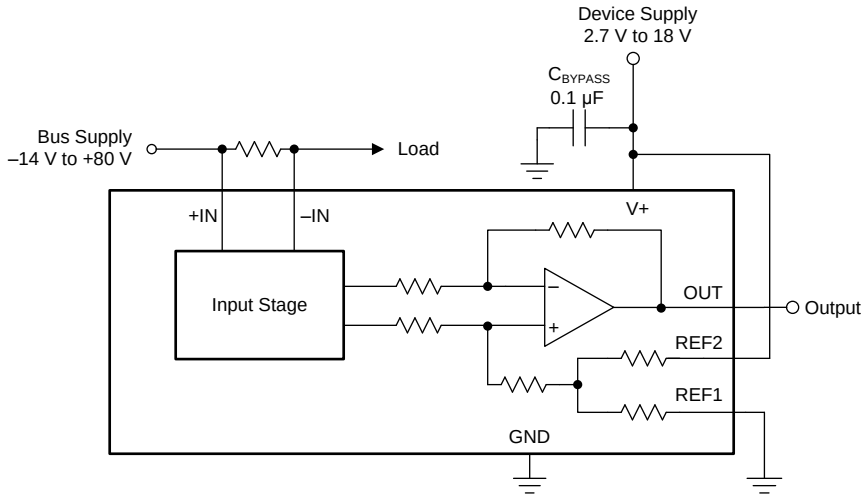


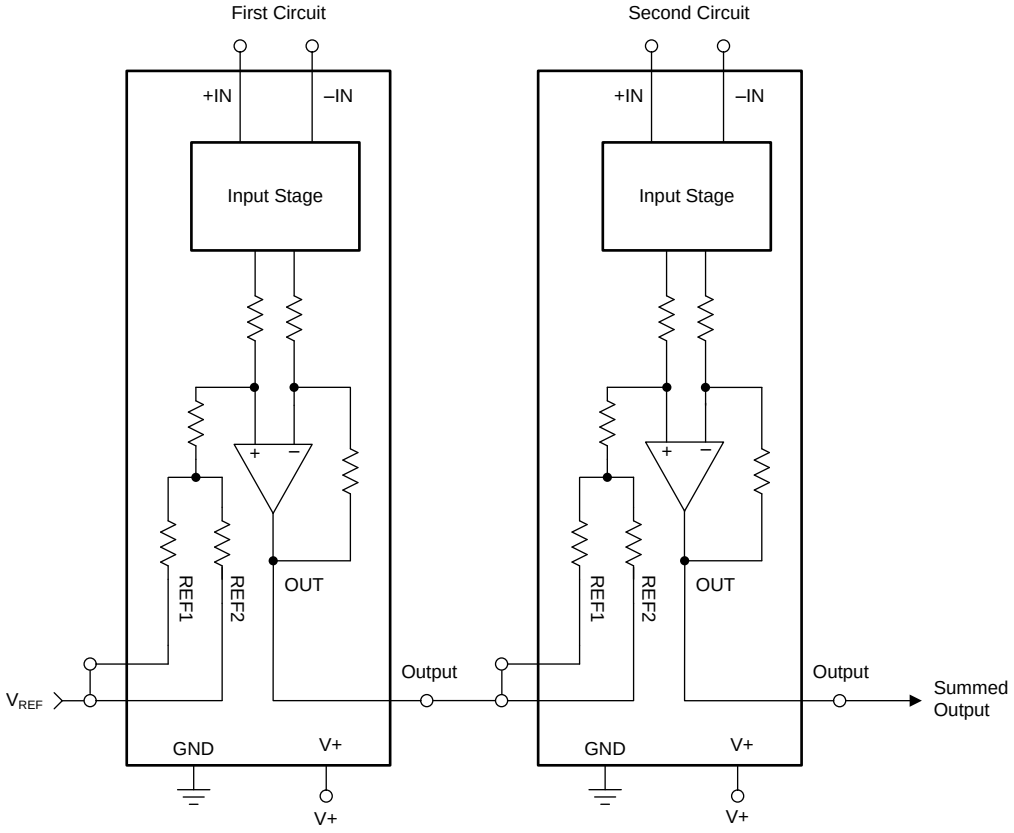
Figure 39. Basic Connections

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

8.2 Typical Applications

8.2.1 Current Summing

The outputs of multiple INA28x family devices are easily summed by connecting the output of one INA28x family device to the reference input of a second INA28x family device. The circuit configuration shown in Figure 40 is an easy way to achieve current summing.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

Figure 40. Summing the Outputs of Multiple INA28x Family Devices

Typical Applications (continued)

8.2.1.1 Design Requirements

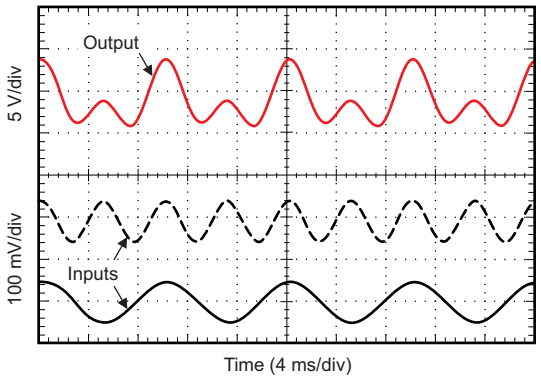
In order to sum multiple load currents, multiple INA28x devices must be connected. Figure 40 shows summing for two devices. Summing beyond two devices is possible by repeating this connection. The reference input of the first INA28x family device sets the output quiescent level for all the devices in the string.

8.2.1.2 Detailed Design Procedure

Connect the output of one INA28x family device to the reference input of the next INA28x family device in the chain. Use the reference input of the first circuit to set the reference of the final summed output. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

8.2.1.3 Application Curves

An example output response of a summing configuration is shown in Figure 41. The reference pins of the first circuit are connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.



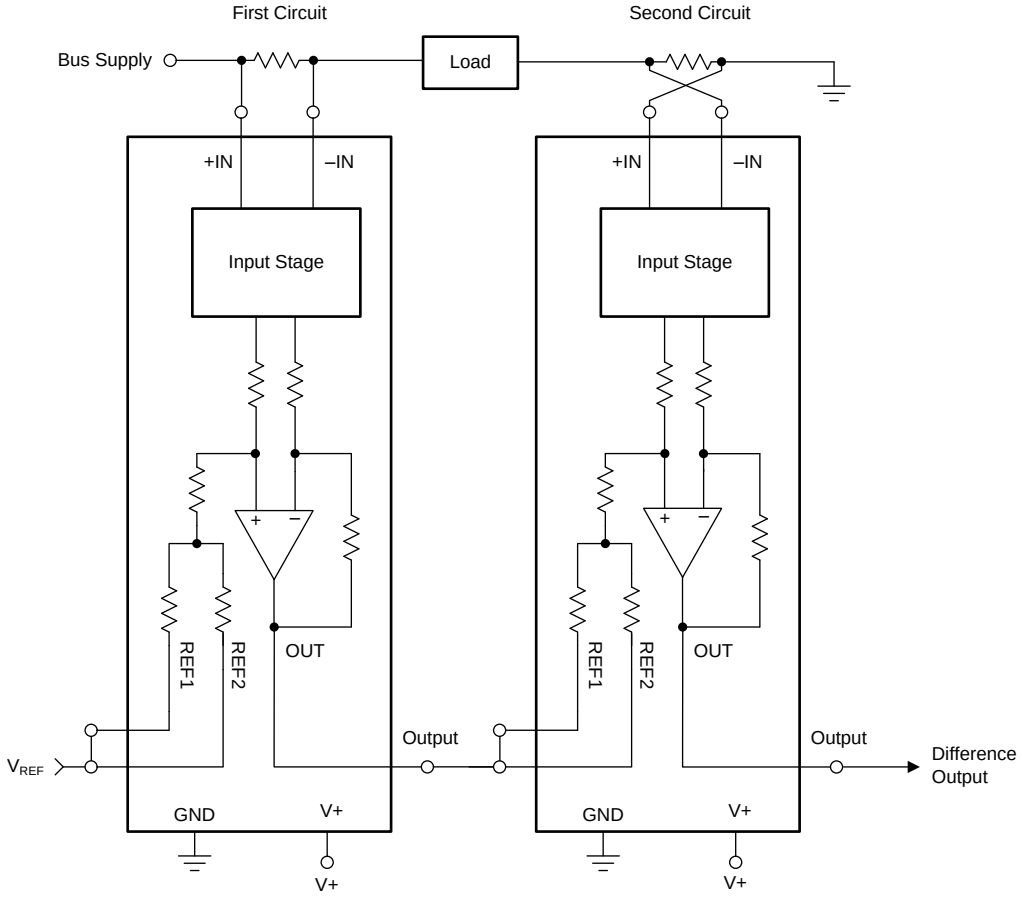
V_{REF} = 0 V

Figure 41. Current Summing Application Output Response

Typical Applications (continued)

8.2.2 Current Differencing

Occasionally, the need arises to confirm that the current into a load is identical to the current out of a load, usually as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing except that the two amplifiers have the inputs connected opposite of each other.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

Figure 42. Current Differencing Using an INA28x Family Device

Typical Applications (continued)

8.2.2.1 Design Requirements

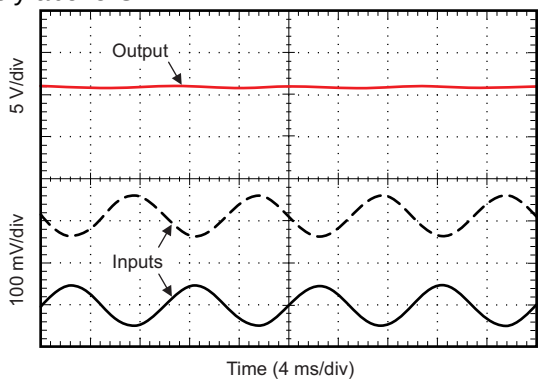
For current differencing, connect two INA28x devices, and have the inputs connected opposite to each other, as shown in Figure 42. The reference input of the first INA28x family device sets the output quiescent level for all the devices in the string.

8.2.2.2 Detailed Design Procedure

Connect the output of one INA28x family device to the reference input of the second INA28x family device. The reference input of the first circuit sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current in to and out of a load do not match.

8.2.2.3 Application Curves

An example output response of a difference configuration is shown in Figure 43. The reference pins of the first circuit are connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out of phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.



V_{REF} = 2.048 V

Figure 43. Current Differencing Application Output Response

9 Power Supply Recommendations

The INA28x family makes accurate measurements well outside of its own power-supply voltage (V+) because the inputs (+IN and –IN) operate anywhere between –14 V and +80 V independent of V+. For example, the V+ power supply can be 5 V while the common-mode voltage being monitored by the shunt may be as high as 80 V. Of course, the output voltage range of the INA28x family is constrained by the V+ supply voltage. Note that when the power to the INA28x family is off (that is, no voltage is supplied to the V+ pin), the input pins (+IN and –IN) are high impedance with respect to ground and typically leak less than ±1 µA over the full common-mode range of –14 V to +80 V

10 Layout

10.1 Layout Guidelines

Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

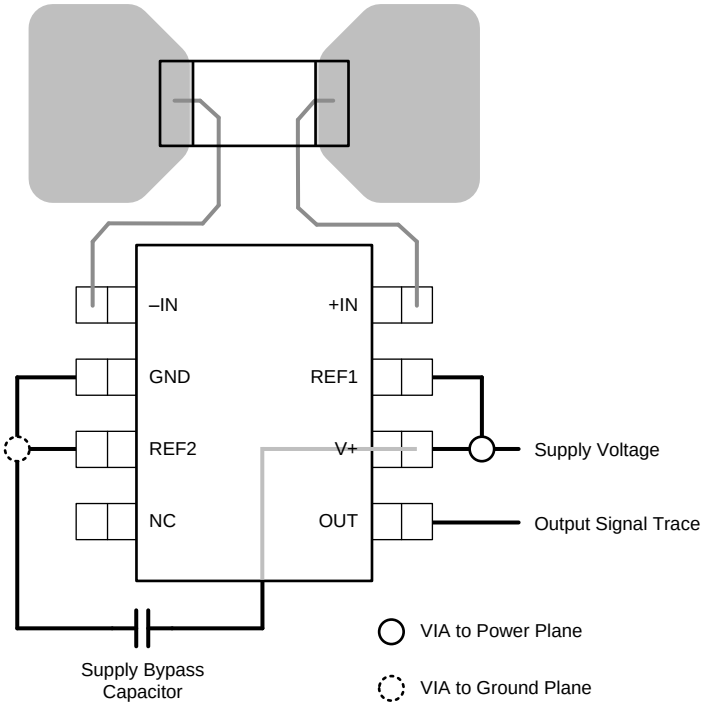


Figure 44. Layout Example

11 Device and Documentation Support

11.1 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA282	Click here	Click here	Click here	Click here	Click here
INA283	Click here	Click here	Click here	Click here	Click here
INA284	Click here	Click here	Click here	Click here	Click here
INA285	Click here	Click here	Click here	Click here	Click here
INA286	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided *AS IS* by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA282AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I282A	Samples
INA282AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFI ~ CFIF)	Samples
INA282AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFI ~ CFIF)	Samples
INA282AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I282A	Samples
INA283AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I283A	Samples
INA283AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFJ ~ CFJF)	Samples
INA283AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFJ ~ CFJF)	Samples
INA283AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I283A	Samples
INA284AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I284A	Samples
INA284AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFK ~ CFKF)	Samples
INA284AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFK ~ CFKF)	Samples
INA284AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I284A	Samples
INA285AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I285A	Samples
INA285AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFL ~ CFLF)	Samples
INA285AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(CFL ~ CFLF)	Samples
INA285AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I285A	Samples
INA286AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I286A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA286AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(ODY ~ ODYF)	Samples
INA286AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(ODY ~ ODYF)	Samples
INA286AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I286A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA282 :

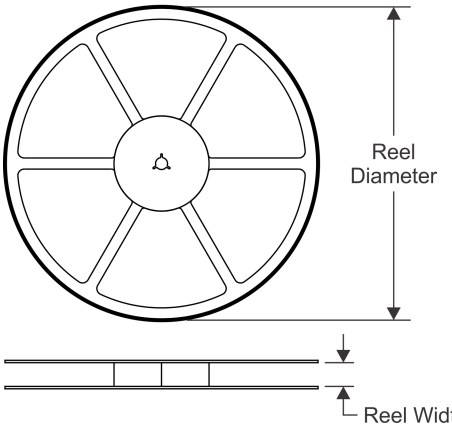
- Automotive: INA282-Q1

NOTE: Qualified Version Definitions:

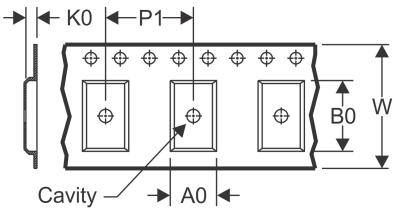
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

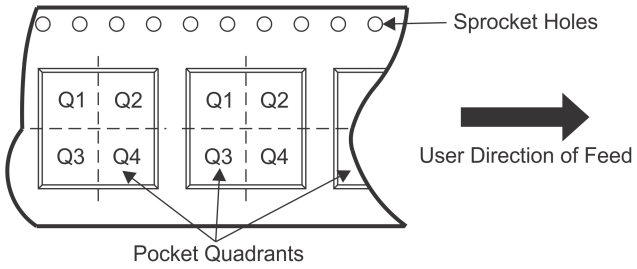


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

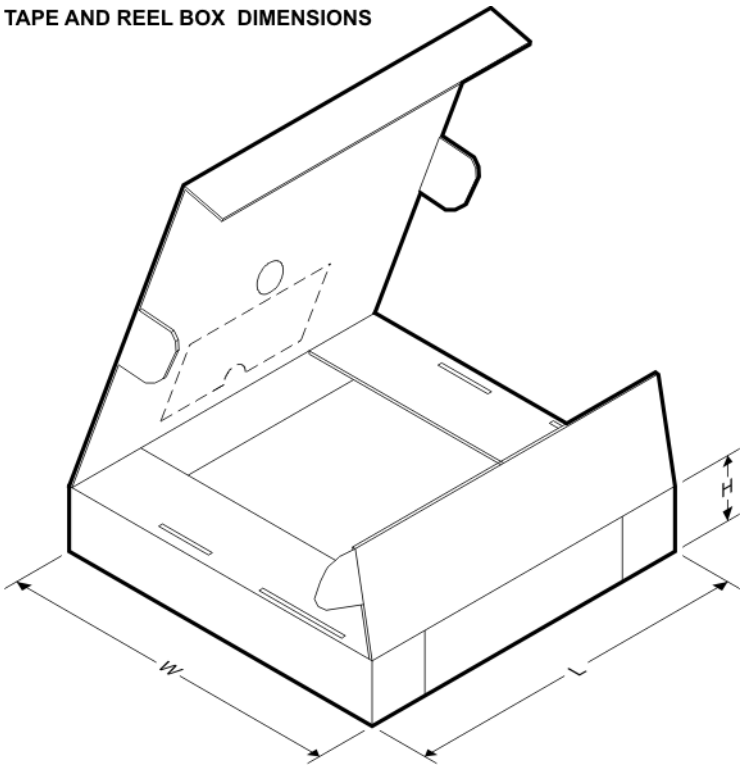
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA282AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA282AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA282AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA283AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA283AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA283AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA284AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA284AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA284AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA285AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA285AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA285AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA286AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA286AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA286AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

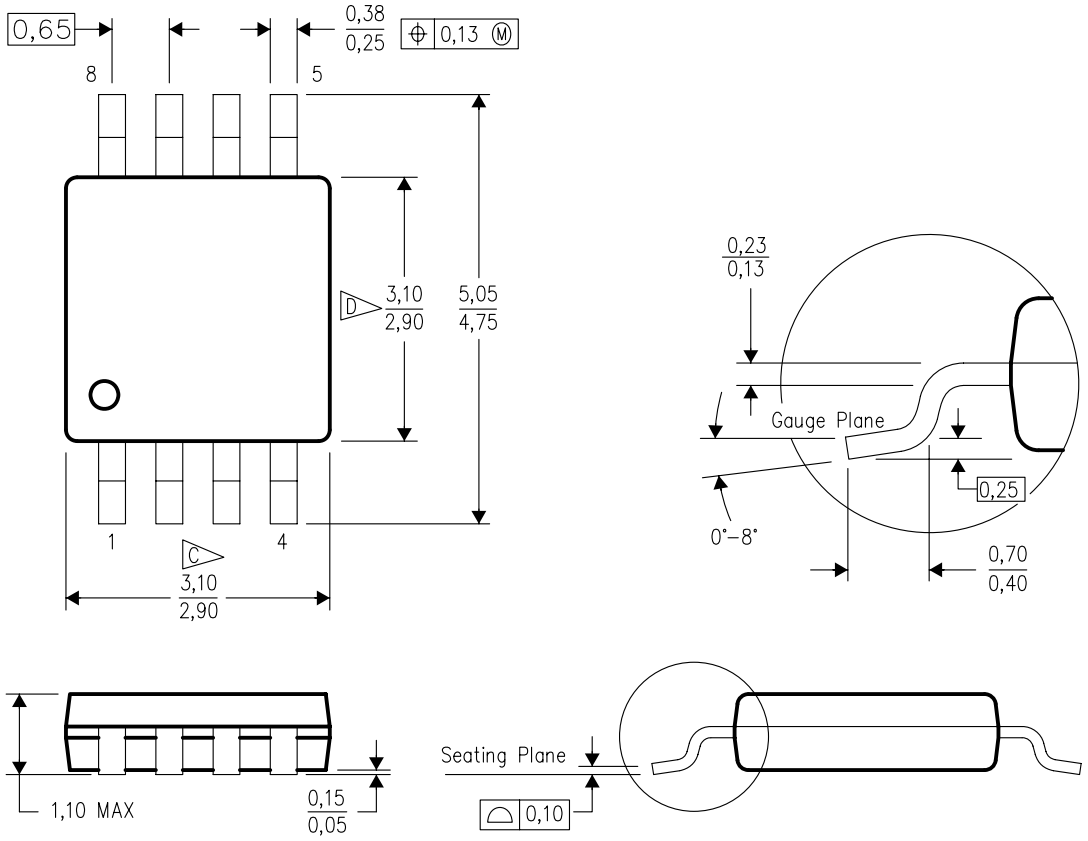
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA282AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA282AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA282AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA283AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA283AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA283AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA284AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA284AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA284AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA285AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA285AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA285AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA286AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA286AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA286AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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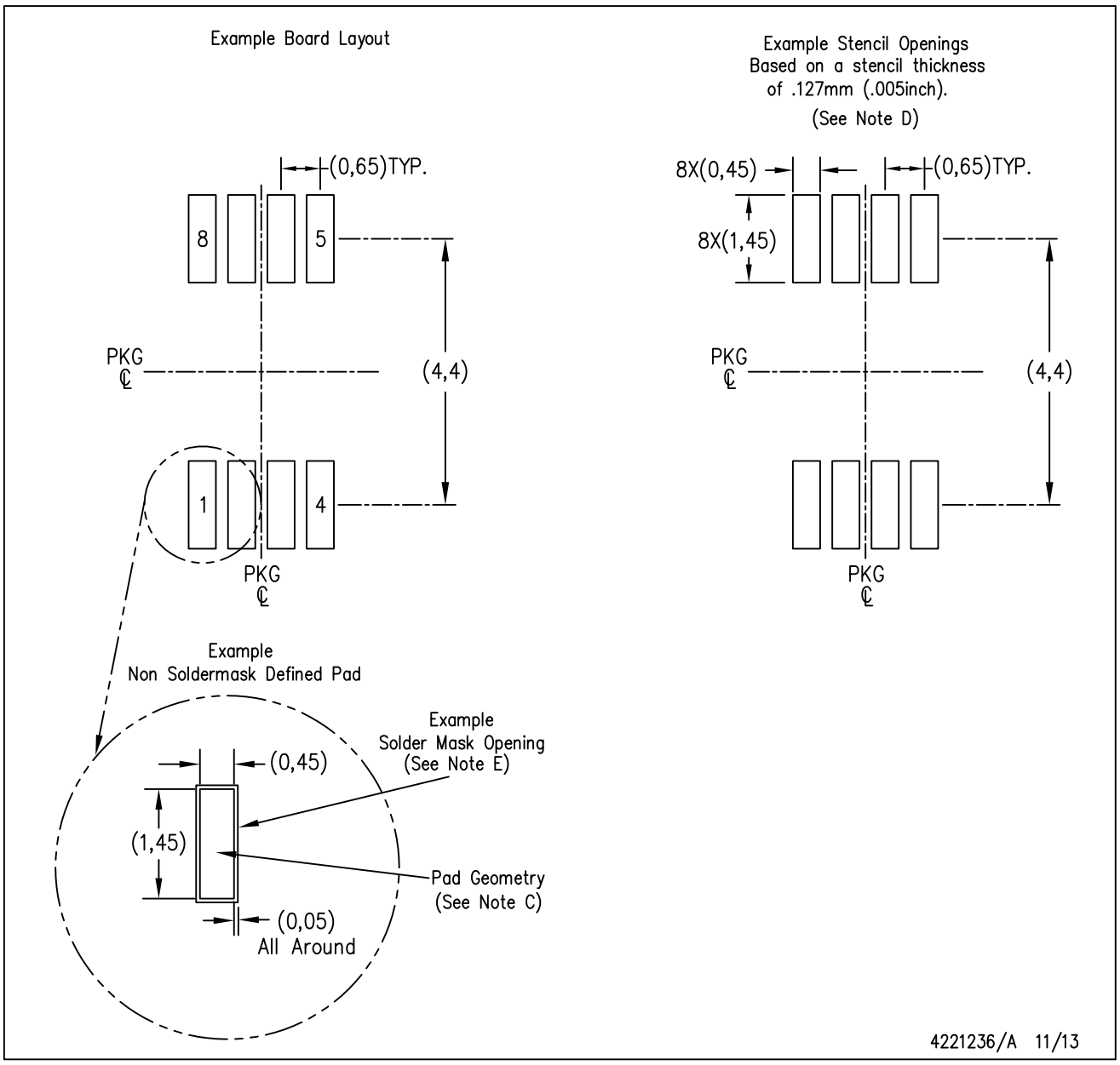
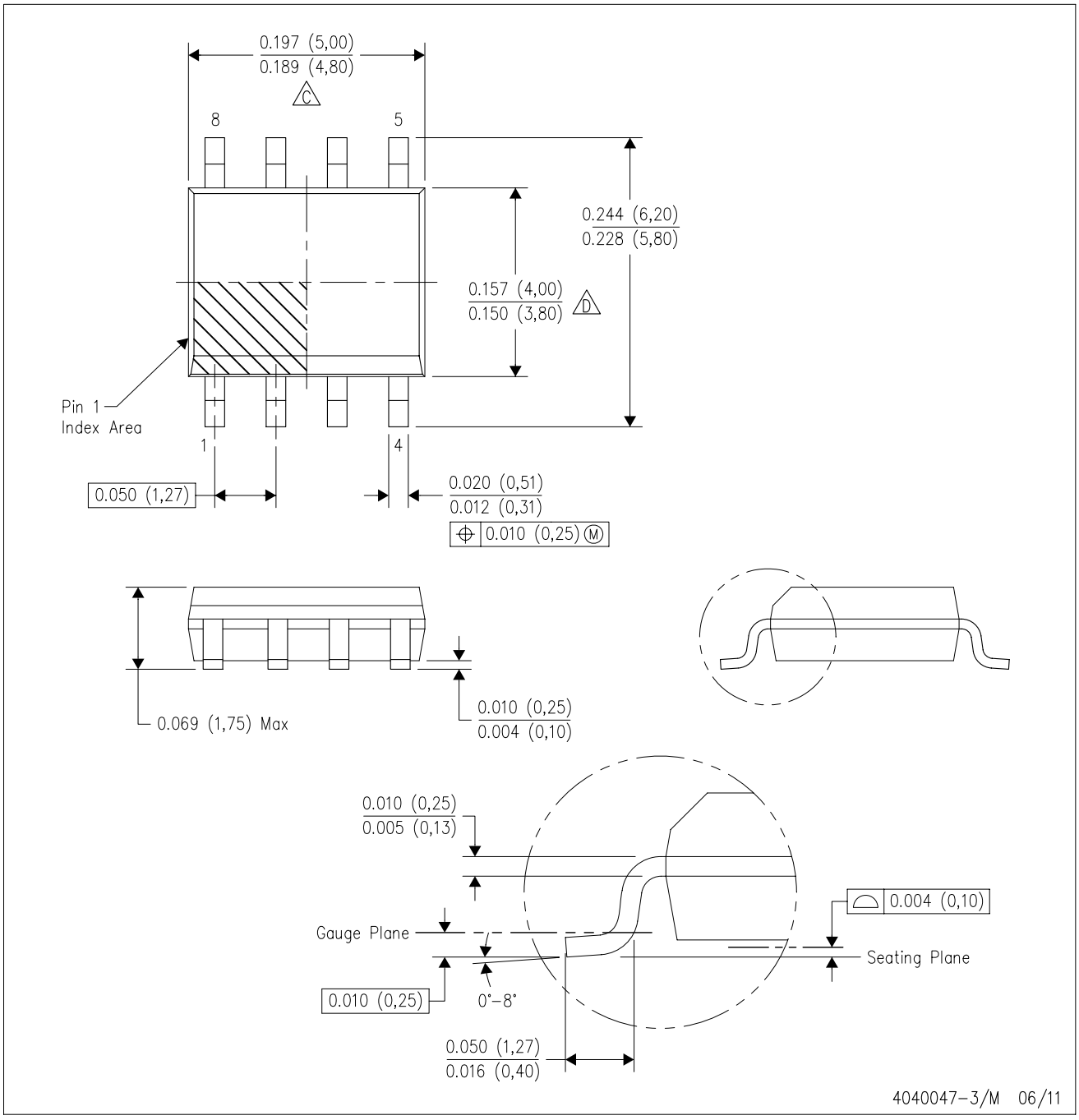
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



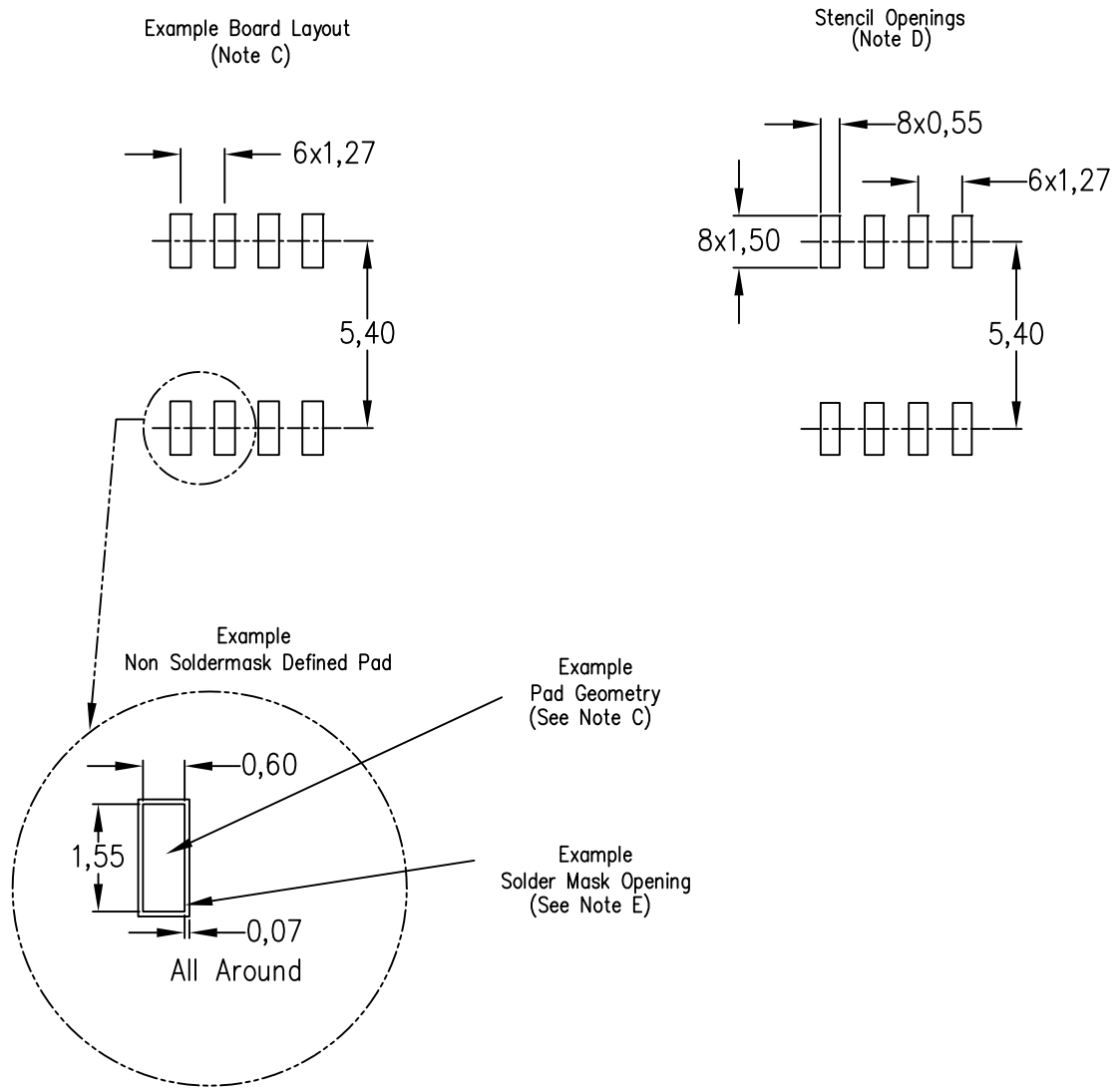
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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