LM9061/-Q1 High-Side Protection Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Withstands 60-V Supply Transients
- Overvoltage Shut-OFF With V_{CC} > 30V
- Lossless Overcurrent Protection Latch-OFF
  - Current Sense Resistor is Not Required
  - Minimizes Power Loss With High Current Loads
- Programmable Delay of Protection Latch-OFF
- Gradual turn-OFF to Minimize Inductive Load Transient Voltages
- CMOS Logic Compatible ON/OFF Control Input

2 Applications

- Transmission Control Unit (TCU)
- Engine Control Unit (ECU)
- Valve, Relay and Solenoid Drivers
- Lamp Drivers
- DC Motor PWM Drivers
- Logic-Controlled Power Supply Distribution Switch
- Electronic Circuit Breaker
- High-Power Audio Speakers

3 Description

The LM9061 is a charge-pump device which provides the gate drive to an external power MOSFET of any size configured as a high-side driver or switch. This includes multiple parallel connected MOSFETs for very high current applications. A CMOS logic compatible ON/OFF input controls the output gate drive voltage. In the ON state, the charge pump voltage, which is well above the available V_{CC} supply, is directly applied to the gate of the MOSFET. A built-in 15-V Zener clamps the maximum gate to source voltage of the MOSFET. When commanded OFF a 110-µA current sink discharges the gate capacitances of the MOSFET for a gradual turn-OFF characteristic to minimize the duration of inductive load transient voltages and further protect the power MOSFET.

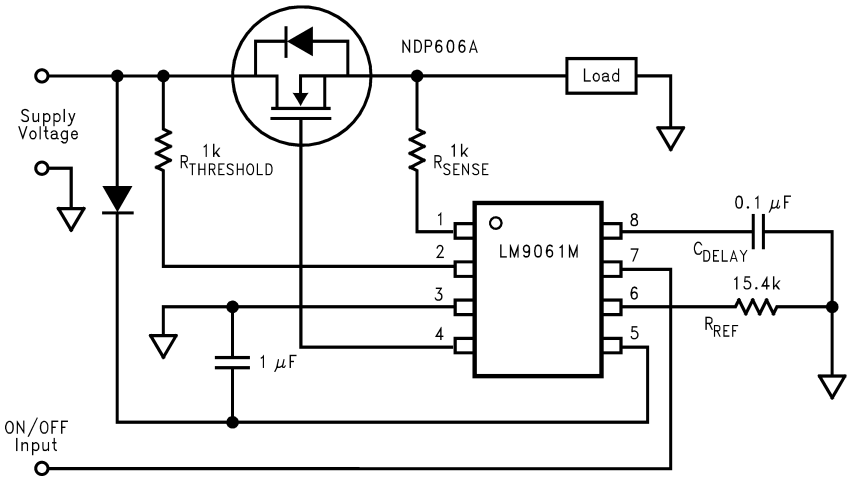
Lossless protection of the power MOSFET is a key feature of the LM9061. The voltage drop (V_{DS}) across the power device is continually monitored and compared against an externally programmable threshold voltage. A small current sensing resistor in series with the load, which causes a loss of available energy, is not required for the protection circuitry. If the V_{DS} voltage, due to excessive load current, exceeds the threshold voltage, the output is latched OFF in a more gradual fashion (through a 10-µA output current sink) after a programmable delay time interval.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM9061/-Q1	SOIC (8)	4.9 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

High-Side Driving and Protection to a Connected Load



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Changed *Handling Ratings* to *ESD Ratings* ... 4
- Added content to *Application and Implementation* section ... 21
- Changed Layout Example figure ... 23

Changes from Revision F (April 1995) to Revision G — **Page**

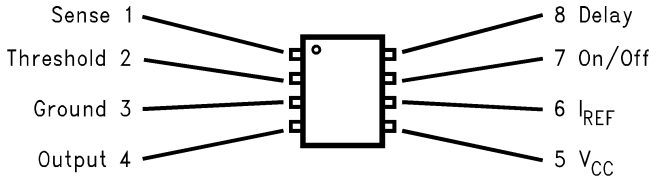
- Added AEC-Q100 Qualification ... 1
- Added Handling Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 4

Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

SOIC
See Package Number D0008A
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Sense	1	I	The inverting input to the protection comparator, connected to the external MOSFET source pin and the load.
Threshold	2	I	The noninverting input to the protection comparator, and a current sink for the threshold resistor to set the allowed voltage drop across the external MOSFET.
Ground	3	—	Ground
Output	4	O	The gate drive connection. Charges, and discharges, the MOSFET gate.
V_{CC}	5	I	The voltage supply pin. The V_{CC} operating range has a minimum value of 7 V, and a maximum value of 26 V.
I_{REF}	6	O	A resistor on this pin to ground sets the current through the threshold resistor, which sets the allowed voltage drop across the external MOSFET.
On/Off	7	I	The control pin. A low voltage, $V_{IN}(0)$, will disable device operation, while a high voltage, $V_{IN}(1)$, will enable device operation.
Delay	8	O	A capacitor on this pin to ground will provide a delay time between when the protection comparator detects excessive V_{GS} across the MOSFET and when the gate drive circuitry is latched-OFF.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply Voltage		60	V
Output Voltage		V_{CC} + 15	V
Voltage at Sense and Threshold (through 1 kΩ)	−25	60	V
ON/OFF Input Voltage	−0.3	V_{CC} + 0.3	V
Reverse Supply Current		20	mA
Junction Temperature		150	°C
Lead Temperature Soldering, 10 seconds		260	°C
Storage temperature, T_{stg}	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*(). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings: LM9061

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM9061-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins (1, 4, 5, and 8)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage	7		26	V
ON/OFF Input Voltage	−0.3		V_{CC}	V
Ambient Temperature Range: LM9061	−40		125	°C
Junction Temperature Range: LM9061-Q1	−40		125	°C

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but may not meet the ensured specific performance limits. For ensured specifications and test conditions see the *Typical Characteristics*.

6.5 Thermal Information

THERMAL METRIC(1)		LM9061/-Q1 SOIC 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	
ψ_{JT}	Junction-to-top characterization parameter	6.2	
ψ_{JB}	Junction-to-board characterization parameter	48.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
$7V \le V_{CC} \le 20V$, R_{REF} = 15.4 kΩ, $-40°C \le T_J \le +125°C$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent Supply Current	ON/OFF = "0"			5	mA
I_{CC}	Operating Supply Current	ON/OFF = "1", C_{LOAD} = 0.025 µF, Includes Turn-ON Transient Output Current			40	mA
ON/OFF CONTROL INPUT						
$V_{IN}(0)$	ON/OFF Input Logic "0"	V_{OUT} = OFF			1.5	V
$V_{IN}(1)$	ON/OFF Input Logic "1"	V_{OUT} = ON	3.5			V
V_{HYST}	ON/OFF Input Hysteresis	Peak to Peak	0.8		2	V
I_{IN}	ON/OFF Input Pull-Down Current	VON/OFF = 5 V	50		250	µA
GATE DRIVE OUTPUT						
V_{OH}	Charge Pump Output Voltage	ON/OFF = "1"	V_{CC} + 7		V_{CC} + 15	V
V_{OL}	OFF Output Voltage	ON/OFF = "0", I_{SINK} = 110 µA			0.9	V
V_{CLAMP}	Sense to Output Clamp Voltage	ON/OFF = "1, $V_{SENSE} = V_{THRESHOLD}$	11		15	V
$I_{SINK(Normal-OFF)}$	Output Sink Current Normal Operation	ON/OFF = "0", V_{DELAY} = 0 V, $V_{SENSE} = V_{THRESHOLD}$	75		145	µA
$I_{SINK(Latch-OFF)}$	Output Sink Current with Protection Comparator Tripped	V_{DELAY} = 7 V, $V_{SENSE} < V_{THRESHOLD}$	5		15	µA
PROTECTION CIRCUITRY						
V_{REF}	Reference Voltage		1.15		1.35	V
I_{REF}	Threshold Pin Reference Current	$V_{SENSE} = V_{THRESHOLD}$	75		88	µA
$I_{THR(LEAKAGE)}$	Threshold Pin Leakage Current	V_{CC} = Open, 7 V ≤ $V_{THRESHOLD}$ ≤ 20 V			10	µA
I_{SENSE}	Sense Pin Input Bias Current	$V_{SENSE} = V_{THRESHOLD}$			10	µA
DELAY TIMER						
V_{TIMER}	Delay Timer Threshold Voltage		5		6.2	V
V_{SAT}	Discharge Transistor Saturation Voltage	I_{DIS} = 1 mA			0.4	V
I_{DIS}	Delay Capacitor Discharge Current	V_{DELAY} = 5 V	2		10	mA
I_{DELAY}	Delay Pin Source Current		6.74		15.44	µA

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

$7V \le V_{CC} \le 20V$, R_{REF} = 15.4 kΩ, $-40°C \le T_J \le +125°C$, C_{LOAD} = 0.025 µF, C_{DELAY} = 0.022 µF, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Output Turn-ON Time	C_{LOAD} = 0.025 µF $7V \le V_{CC} \le 10$ V, $V_{OUT} \ge V_{CC} + 7$ V $10V \le V_{CC} \le 20$ V, $V_{OUT} \ge V_{CC} + 11$ V			1.5 1.5	ms ms
$T_{OFF(NORMAL)}$	Output Turn-OFF Time, Normal Operation(1)	C_{LOAD} = 0.025 µF V_{CC} = 14 V, $V_{OUT} \ge 25$ V $V_{SENSE} = V_{THRESHOLD}$	4		10	ms
$T_{OFF(Latch-OFF)}$	Output Turn-OFF Time, Protection Comparator Tripped(1)	C_{LOAD} = 0.025 µF V_{CC} = 14 V, $V_{OUT} \ge 25$ V $V_{SENSE} = V_{THRESHOLD}$	45		140	ms
T_{DELAY}	Delay Timer Interval	C_{DELAY} = 0.022 µF	8		18	ms

(1) The AC Timing specifications for T_{OFF} are not production tested, and therefore are not specifically ensured. Limits are provided for reference purposes only. Smaller load capacitances will have proportionally faster turn-ON and turn-OFF times.

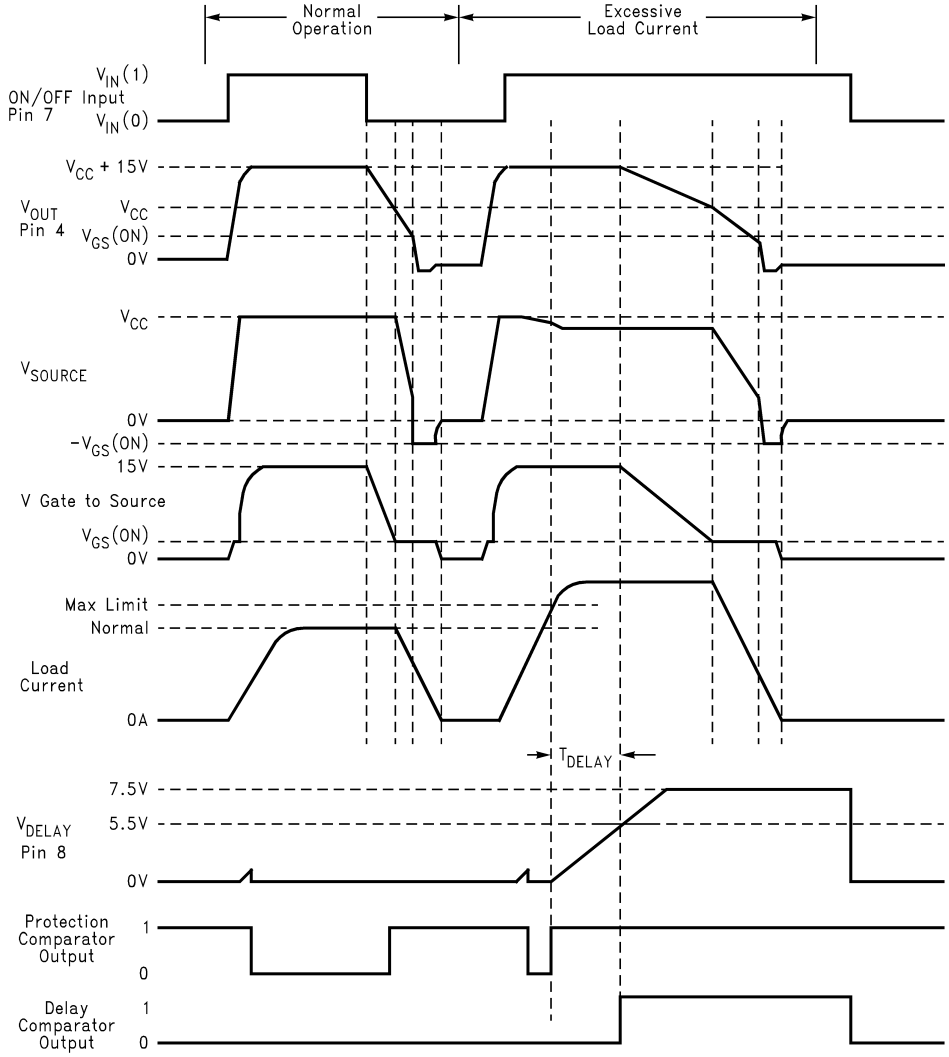


Figure 1. Typical Operating Waveforms

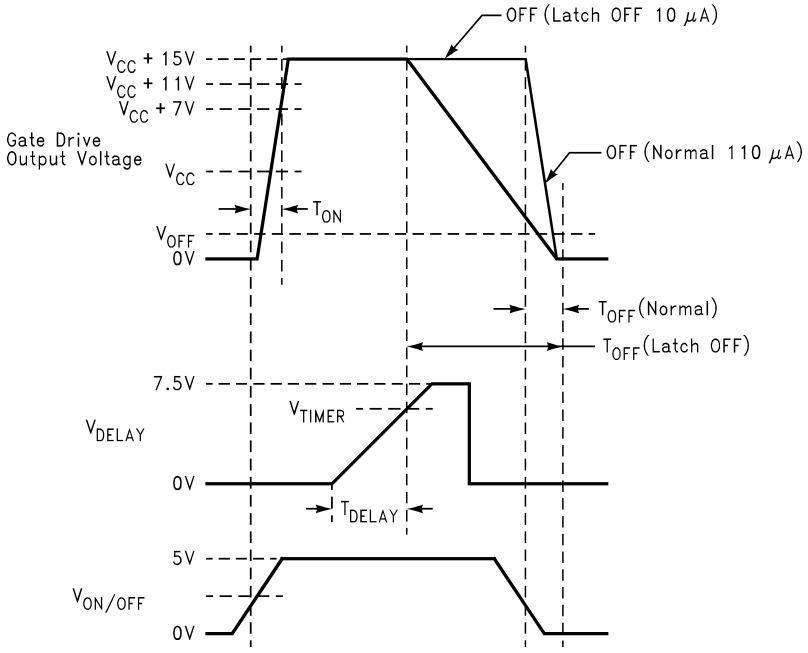


Figure 2. Timing Definitions

6.8 Typical Characteristics

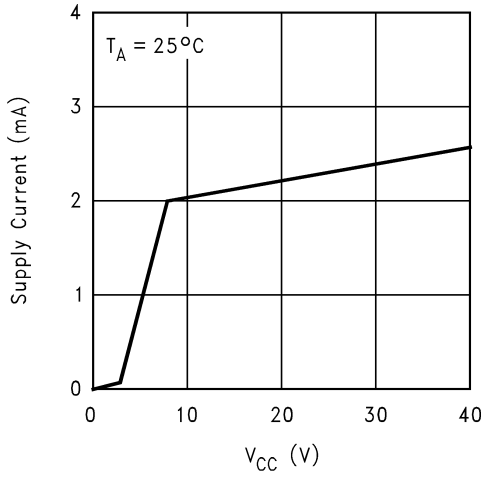


Figure 3. Standby Supply Current vs V_{CC}

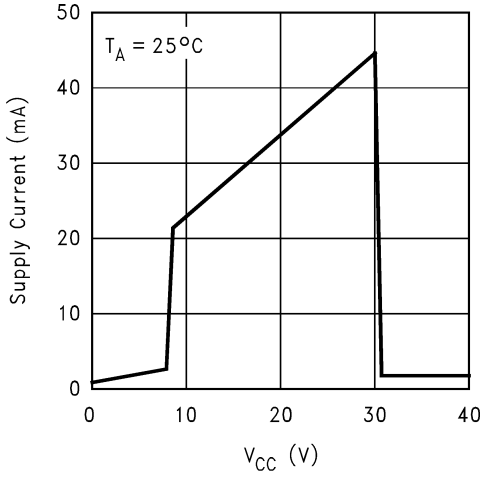


Figure 4. Operating Supply Current vs V_{CC}

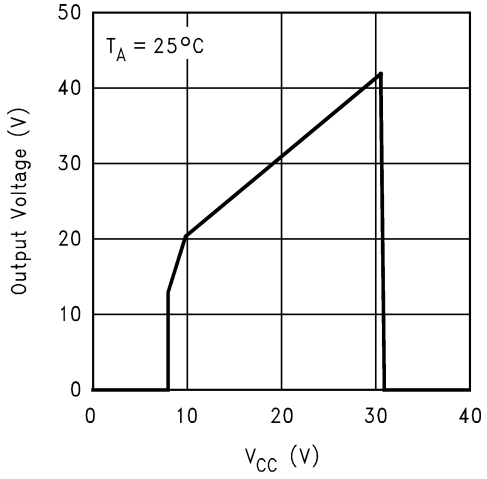


Figure 5. Output Voltage vs V_{CC}

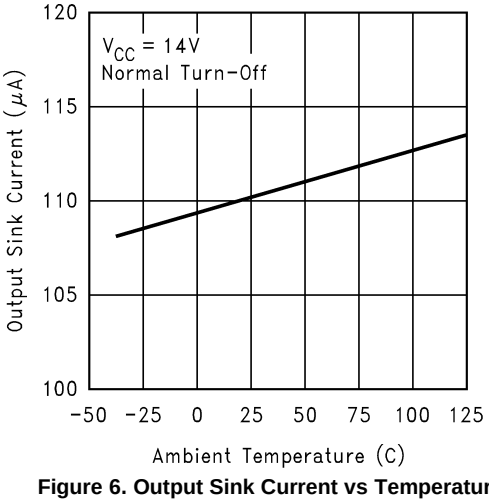


Figure 6. Output Sink Current vs Temperature

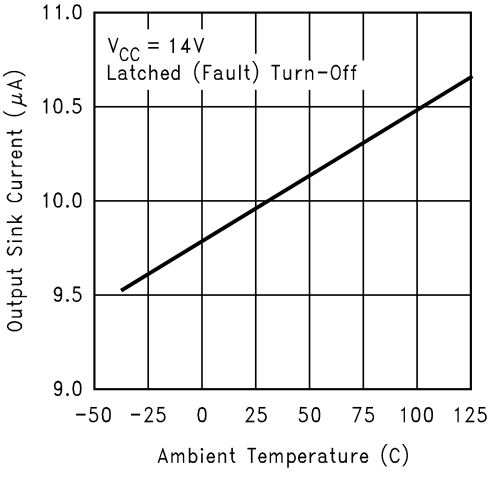


Figure 7. Output Sink Current vs Temperature

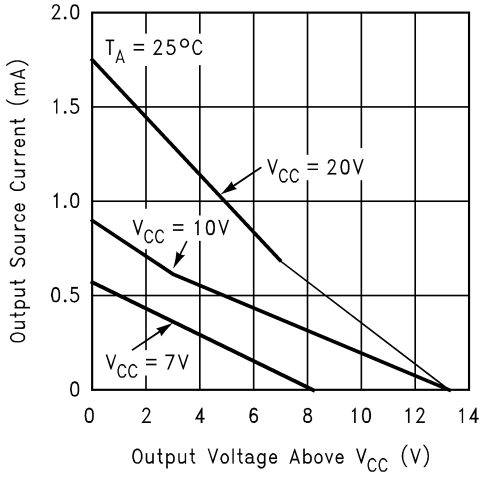


Figure 8. Output Source Current vs Output Voltage

Typical Characteristics (continued)

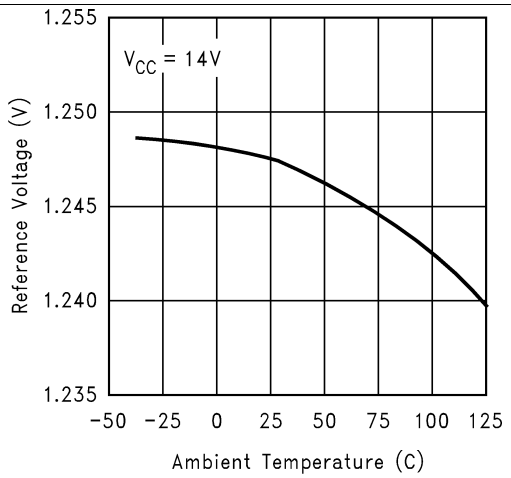


Figure 9. Reference Voltage vs Temperature

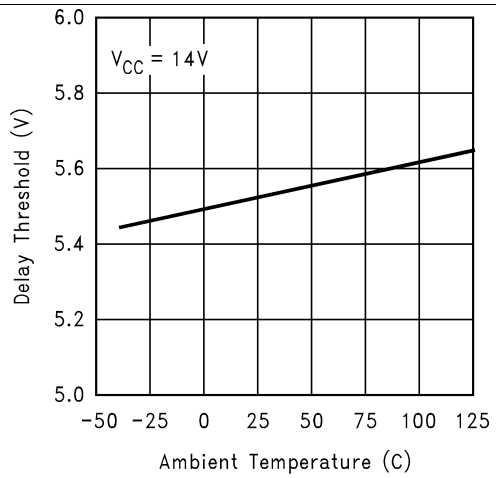


Figure 10. Delay Threshold vs Temperature

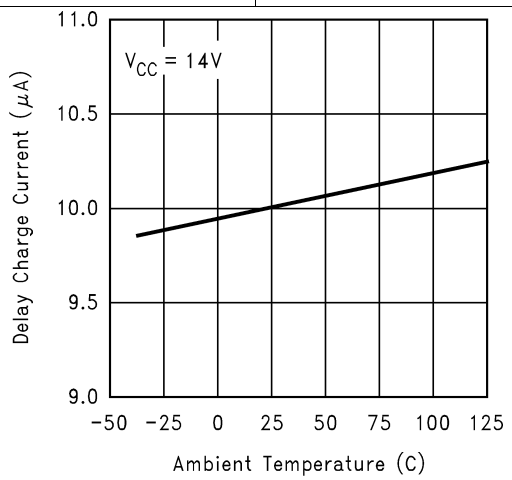


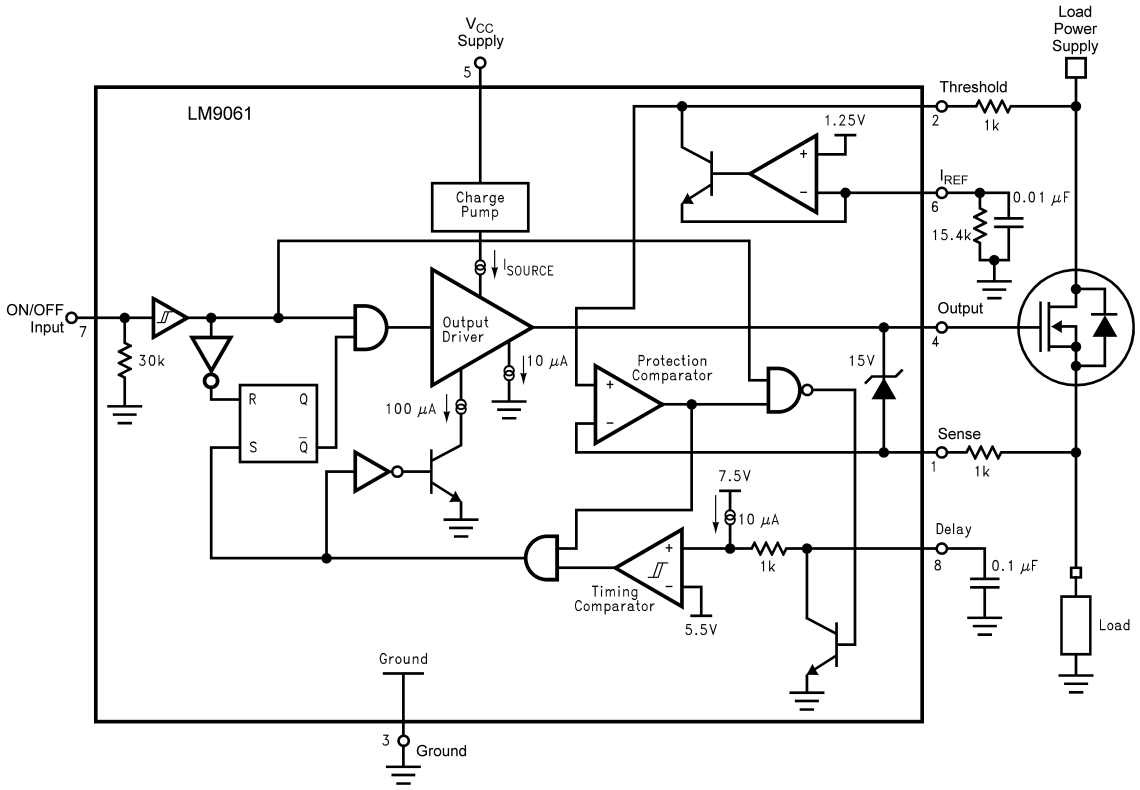
Figure 11. Delay Charge Current vs Temperature

7 Detailed Description

7.1 Overview

The LM9061 is a high-side controller that can protect the load from overcurrent and overvoltage. An internal charge pump circuit generates the gate voltage to drive the high-side MOSFET. The voltage drop, V_{DS}, across the MOSFET is monitored to protect from excessive current. Should the V_{DS} voltage, due to excessive load current, exceed the threshold voltage, the output is latched OFF after a programmable delay time interval.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 MOSFET Gate Drive

The LM9061 contains a charge pump circuit that generates a voltage in excess of the applied supply voltage to provide the gate drive to high-side MOSFET transistors. Any size of N-channel power MOSFET, including multiple parallel connected MOSFETs for very high current applications, can be used to apply power to a ground referenced load circuit in what is referred to as “high-side drive” applications. Figure 12 shows the basic application of the LM9061.

Feature Description (continued)

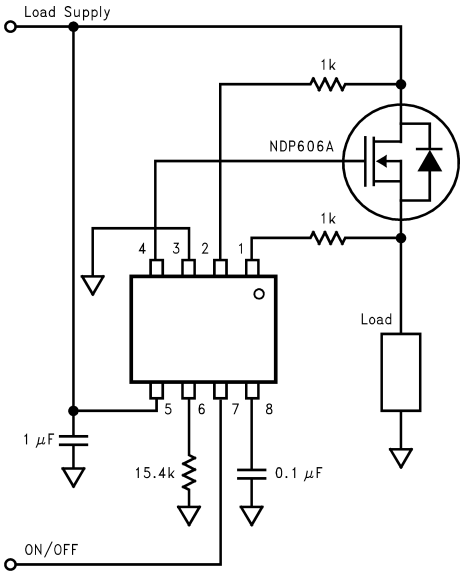


Figure 12. Basic Application Circuit

7.3.2 Basic Operation

When commanded ON by a logic “1” input to pin 7 the gate drive output, pin 4, rises quickly to the V_{CC} supply potential at pin 5. Once the gate voltage exceeds the gate-source threshold voltage of the MOSFET, $V_{GS(ON)}$, (the source is connected to ground through the load) the MOSFET turns ON and connects the supply voltage to the load. With the source at near the supply potential, the charge pump continues to provide a gate voltage greater than the supply to keep the MOSFET turned ON. To protect the gate of the MOSFET, the output voltage of the LM9061 is clamped to limit the maximum V_{GS} to 15 V.

It is important to remember that during the Turn-ON of the MOSFET the output current to the Gate is drawn from the V_{CC} supply pin. The V_{CC} pin should be bypassed with a capacitor with a value of at least 10 times the Gate capacitance, and no less than 0.1 µF. The output current into the Gate will typically be 30 mA with V_{CC} at 14 V and the Gate at 0 V. As the Gate voltage rises to V_{CC}, the output current will decrease. When the Gate voltage reaches V_{CC}, the output current will typically be 1 mA with V_{CC} at 14 V.

A logic “0” on pin 7 turns the MOSFET OFF. When commanded OFF a 110 µA current sink is connected to the output pin. This current discharges the gate capacitances of the MOSFET linearly. When the gate voltage equals the source voltage (which is near the supply voltage) plus the $V_{GS(ON)}$ threshold of the MOSFET, the source voltage starts following the gate voltage and ramps toward ground. Eventually the source voltage equals 0 V and the gate continues to ramp to zero thus turning OFF the power device. This gradual Turn-OFF characteristic, instead of an abrupt removal of the gate drive, can, in some applications, minimize the power dissipation in the MOSFET or reduce the duration of negative transients, as is the case when driving inductive loads. In the event of an overstress condition on the power device, the turn OFF characteristic is even more gradual as the output sinking current is only 10 µA (see *Lossless Overcurrent Protection*).

7.3.3 Turn On and Turn Off Characteristics

The actual rate of change of the voltage applied to the gate of the power device is directly dependent on the input capacitances of the MOSFET used. These times are important to know if the power to the load is to be applied repetitively as is the case with pulse width modulation drive. Of concern are the capacitances from gate to drain, C_{GD}, and from gate to source, C_{GS}. Figure 13 details the turn ON and turn OFF intervals in a typical application. An inductive load is assumed to illustrate the output transient voltage to be expected. At time t1, the ON/OFF input goes high. The output, which drives the gate of the MOSFET, immediately pulls the gate voltage

Feature Description (continued)

towards the V_{CC} supply of the LM9061. The source current from pin 4 is typically 30 mA which quickly charges C_{GD} and C_{GS}. As soon as the gate reaches the $V_{GS(ON)}$ threshold of the MOSFET, the switch turns ON and the source voltage starts rising towards V_{CC}. V_{GS} remains equal to the threshold voltage until the source reaches V_{CC}. While V_{GS} is constant only C_{GD} is charging. When the source voltage reaches V_{CC}, at time t2, the charge pump takes over the drive of the gate to ensure that the MOSFET remains ON.

The charge pump is basically a small internal capacitor that acquires and transfers charge to the output pin. The clock rate is set internally at typically 300 kHz. In effect the charge pump acts as a switched capacitor resistor (approximately 67k) connected to a voltage that is clamped at 13V above the Sense input pin of the LM9061 which is equal to the V_{CC} supply in typical applications. The gate voltage rises above V_{CC} in an exponential fashion with a time constant dependent upon the sum of C_{GD} and C_{GS}. At this time however the load is fully energized. At time t3, the charge pump reaches its maximum potential and the switch remains ON.

At time t4, the ON/OFF input goes low to turn OFF the MOSFET and remove power from the load. At this time the charge pump is disconnected and an internal 110 µA current sink begins to discharge the gate input capacitances to ground. The discharge rate ($\Delta V/\Delta T$) is equal to 110 µA/ (C_{GD} + C_{GS}).

The load is still fully energized until time t5 when the gate voltage has reached a potential of the source voltage (V_{CC}) plus the $V_{GS(ON)}$ threshold voltage of the MOSFET. Between time t5 and t6, the V_{GS} voltage remains constant and the source voltage follows the gate voltage. With the voltage on C_{GD} held constant the discharge rate now becomes 110 µA/C_{GD}.

At time t6 the source voltage reaches 0V. As the gate moves below the $V_{GS(ON)}$ threshold the MOSFET tries to turn OFF. With an inductive load, if the current in the load has not collapsed to zero by time t6, the action of the MOSFET turning OFF will create a negative voltage transient (flyback) across the load. The negative transient will be clamped to $-V_{GS(ON)}$ because the MOSFET must turn itself back ON to continue conducting the load current until the energy in the inductance has been dissipated (at time t7).

7.3.4 Lossless Overcurrent Protection

A unique feature of the LM9061 is the ability to sense excessive power dissipation in the MOSFET and latch it OFF to prevent permanent failure. Instead of sensing the actual current flowing through the MOSFET to the load, which typically requires a small valued power resistor in series with the load, the LM9061 monitors the voltage drop from drain to source, V_{DS}, across the MOSFET. This “lossless” technique allows all of the energy available from the supply to be conducted to the load as required. The only power loss is that of the MOSFET itself and proper selection of a particular power device for an application will minimize this concern. Another benefit of this technique is that all applications use only standard inexpensive ¼W or less resistors.

To use this lossless protection technique requires knowledge of key characteristics of the power MOSFET used. In any application the emphasis for protection can be placed on either the power MOSFET or on the amount of current delivered to the load, with the assumption that the selected MOSFET can safely handle the maximum load current.

Feature Description (continued)

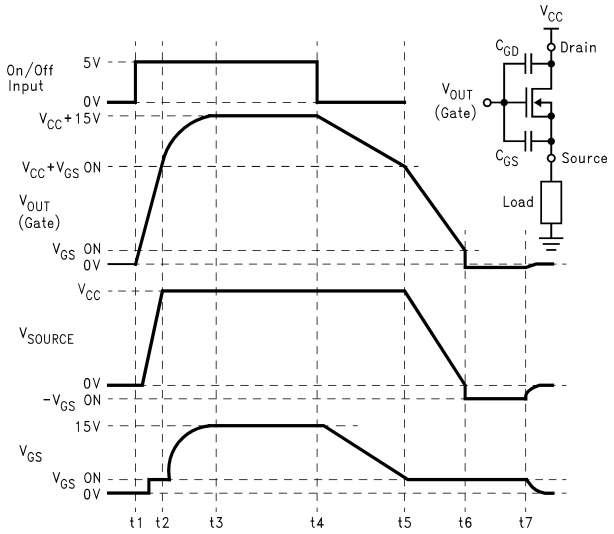


Figure 13. Turn ON and Turn OFF Waveforms

To protect the MOSFET from exceeding its maximum junction temperature rating, the power dissipation must be limited. The maximum power dissipation allowed (derated for temperature) and the maximum drain to source ON resistance, $R_{DS(ON)}$, with both at the maximum operating ambient temperature, needs to be determined. When switched ON the power dissipation in the MOSFET will be:

$$P_{DISS} = \frac{V_{DS}^2}{R_{DS(ON)}} \quad (1)$$

The V_{DS} voltage to limit the maximum power dissipation is therefore:

$$V_{DS\ (MAX)} = \sqrt{P_{D\ (MAX)}} \times R_{DS(ON)\ (MAX)} \quad (2)$$

With this restriction the actual load current and power dissipation obtained will be a direct function of the actual $R_{DS(ON)}$ of the MOSFET at any particular ambient temperature but the junction temperature of the power device will never exceed its rated maximum.

To limit the maximum load current requires an estimate of the minimum $R_{DS(ON)}$ of the MOSFET (the minimum $R_{DS(ON)}$ of discrete MOSFETs is rarely specified) over the required operating temperature range.

The maximum current to the load will be:

$$I_{LOAD\ (MAX)} = \frac{V_{DS}}{R_{DS(ON)\ (MIN)}} \quad (3)$$

The maximum junction temperature of the MOSFET and/or the maximum current to the load can be limited by monitoring and setting a maximum operational value for the drain to source voltage drop, V_{DS}. In addition, in the event that the load is inadvertently shorted to ground, the power device will automatically be turned-OFF.

In all cases, should the MOSFET be switched OFF by the built in protection comparator, the output sink current is switched to only 10 µA to gradually turn OFF the power device.

Figure 14 illustrates how the threshold voltage for the internal protection comparator is established.

Two resistors connect the drain and source of the MOSFET to the LM9061. The Sense input, pin 1, monitors the source voltage while the Threshold input, pin 2, is connected to the drain, which is also connected to the constant load power supply. Both of these inputs are the two inputs to the protection comparator. Should the voltage at the sense input ever drop below the voltage at the threshold input, the protection comparator output goes high and initiates an automatic latch-OFF function to protect the power device. Therefore the switching threshold voltage of the comparator directly controls the maximum V_{DS} allowed across the MOSFET while conducting load current.

Feature Description (continued)

The threshold voltage is set by the voltage drop across resistor $R_{THRESHOLD}$. A reference current is fixed by a resistor to ground at I_{REF}, pin 6. To precisely regulate the reference current over temperature, a stable band gap reference voltage is provided to bias a constant current sink. The reference current is set by:

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \quad (4)$$

The reference current sink output is internally connected to the threshold pin. I_{REF} then flows from the load supply through $R_{THRESHOLD}$. The fixed voltage drop across $R_{THRESHOLD}$ is approximately equal to the maximum value of V_{DS} across the MOSFET before the protection comparator trips.

It is important to note that the programmed reference current serves a multiple purpose as it is used internally for biasing and also has a direct effect on the internal charge pump switching frequency. The design of the LM9061 is optimized for a reference current of approximately 80 µA, set with a 15.4 kΩ ±1% resistor for R_{REF}. To obtain the ensured performance characteristics it is recommended that a 15.4-kΩ resistor be used for R_{REF}.

The protection comparator is configured such that during normal operation, when the output of the comparator is low, the differential input stage of the comparator is switched in a manner that there is virtually no current flowing into the noninverting input of the comparator. Therefore, only I_{REF} flows through resistor $R_{THRESHOLD}$. All of the input bias current, 20 µA maximum, for the comparator input stage (twice the I_{SENSE} specification of 10 µA maximum, defined for equal potentials on each of the comparator inputs) however flows into the inverting input through resistor R_{SENSE}. At the comparator threshold, the current through R_{SENSE} will be no more than the I_{SENSE} specification of 10 µA.

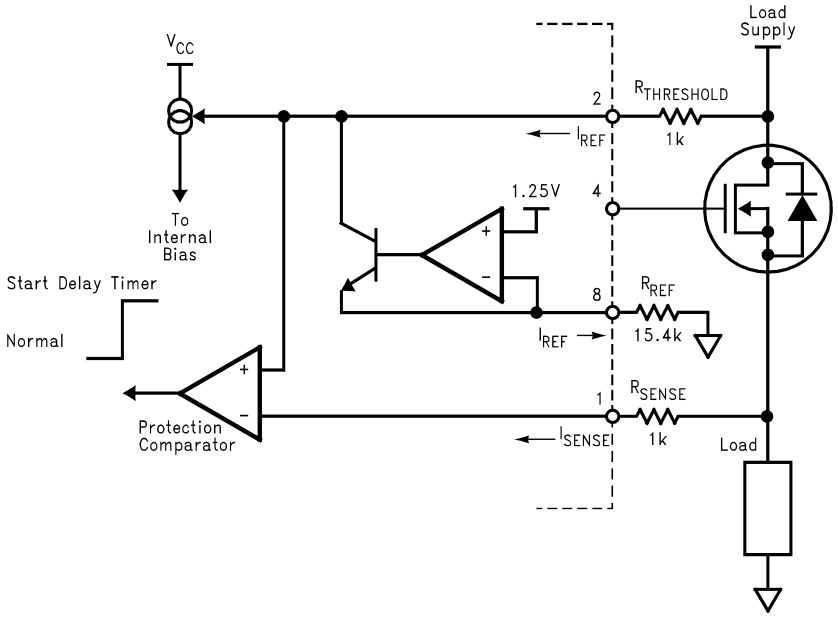


Figure 14. Protection Comparator Biasing

To tailor the $V_{DS\ (MAX)}$ threshold for any particular application, the resistor $R_{THRESHOLD}$ can be selected per the following formula:

$$V_{DS\ (MAX)} = \frac{V_{REF} \times R_{THR}}{R_{REF}} - (I_{SENSE} \times R_{SENSE}) + V_{OS} \quad (5)$$

where

- R_{REF} = 15.4 kΩ.
- I_{SENSE} is the input bias current to the protection comparator.
- R_{SENSE} is the resistor connected to pin 1.
- V_{OS} is the offset voltage of the protection comparator (typically in the range of ±10 mV).

Feature Description (continued)

The resistor R_{SENSE} is optional, but is strongly recommended to provide transient protection for the Sense pin, especially when driving inductive type loads. A minimum value of 1 kΩ will protect the pin from transients ranging from −25V to +60V. This resistor should be equal to, or less than, the resistor used for $R_{THRESHOLD}$. Never set R_{SENSE} to a value larger than $R_{THRESHOLD}$. When the protection comparator output goes high , the total bias current for the input stage transfers from the Sense pin to the Threshold pin, thereby changing the voltages present at the inputs to the comparator. For consistent switching of the comparator right at the desired threshold point, the voltage drop that occurs at the noninverting input (Threshold) should equal, or exceed, the rise in voltage at the inverting input (Sense).

A bypass capacitor across R_{REF} is optional and is used to help keep the reference voltage constant in applications where the V_{CC} supply is subject to high levels of transient noise. This bypass capacitor should be no larger than 0.1 µF, and is not needed for most applications.

7.3.5 Delay Timer

To allow the MOSFET to conduct currents beyond the protection threshold for a brief period of time, a delay timer function is provided. This timer delays the actual latching OFF of the MOSFET for a programmable interval. This feature is important to drive loads which require a surge of current in excess of the normal ON current upon start-up, or at any point in time, such as lamps and motors. Figure 15 details the delay timer circuitry. A capacitor connected from the Delay pin 8, to ground sets the delay time interval. With the MOSFET turned ON and all conditions normal, the output of the protection comparator is low and this keeps the discharge transistor ON. This transistor keeps the delay capacitor discharged. If a surge of load current trips the protection comparator high, the discharge transistor turns OFF and an internal 10-µA current source begins linearly charging the delay capacitor.

If the surge current, with excessive V_{DS} voltage, lasts long enough for the capacitor to charge to the timing comparator threshold of typically 5.5 V, the output of the comparator will go high to set a flip-flop and immediately latch the MOSFET OFF. It will not restart until the ON/OFF Input is toggled low then high.

The delay time interval is set by the selection of C_{DELAY} and can be found from:

$$T_{DELAY} = \frac{(V_{TIMER} \times C_{DELAY})}{I_{DELAY}} \quad (6)$$

where

- Typically, V_{TIMER} = 5.5 V.
- I_{DELAY} = 10 µA.

Charging of the delay capacitor is clamped at approximately 7.5 V which is the internal bias voltage for the 10 µA current source.

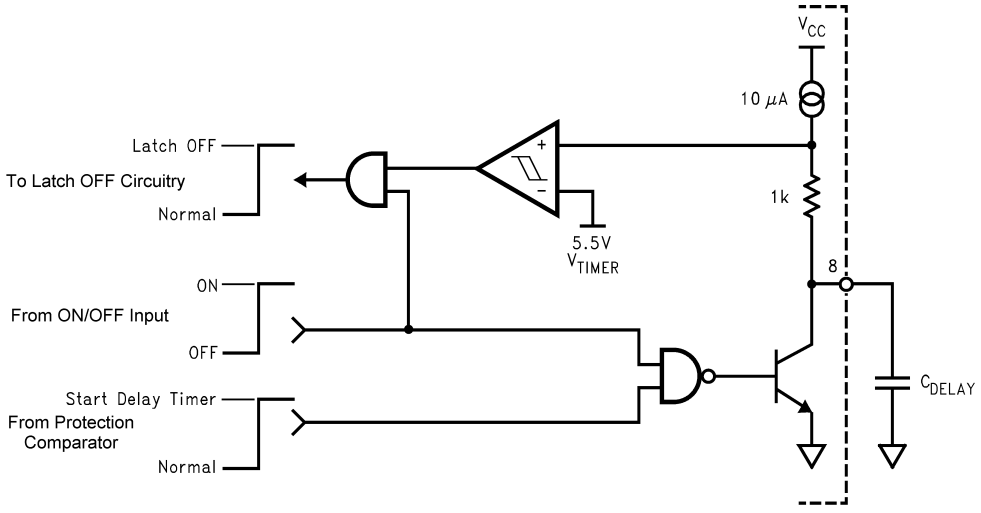


Figure 15. Delay Timer

Feature Description (continued)

7.3.5.1 Minimum Delay Time

A minimum delay time interval is required in all applications due to the nature of the protection circuitry. At the instant the MOSFET is commanded ON, the voltage across the MOSFET, V_{DS}, is equal to the full load supply voltage because the source is held at ground by the load. This condition will immediately trip the protection comparator. Without a minimum delay time set, the timing comparator will trip and force the MOSFET to latch-OFF thereby never allowing the load to be energized.

To prevent this situation a delay capacitor is required at pin 8. The selection of a minimum capacitor value to ensure proper start-up depends primarily on the load characteristics and how much time is required for the MOSFET to raise the load voltage to the point where the Sense input is more positive than the Threshold input ($T_{START-UP}$). Some experimentation is required if a specific minimum delay time characteristic is desired. Therefore:

$$C_{DELAY} = \frac{(I_{DELAY} \times T_{START-UP})}{V_{TIMER}} \quad (7)$$

In the absence of a specific delay time requirement, TI recommends a value for C_{DELAY} of 0.1 µF.

7.3.6 Overvoltage Protection

The LM9061 will remain operational with up to +26 V on V_{CC}. If V_{CC} increases to more than typically +30 V the LM9061 will turn off the MOSFET to protect the load from excessive voltage. When V_{CC} has returned to the normal operating range the device will return to normal operation without requiring toggling the ON/OFF input. This feature will allow MOSFET operation to continue in applications that are subject to periodic voltage transients, such as automotive applications.

For circuits where the load is sensitive to high voltages, the circuit shown in Figure 16 can be used. The addition of a Zener on the Sense input (pin 1) will provide a maximum voltage reference for the Protection Comparator. The Sense resistor is required in this application to limit the Zener current. When the device is ON, and the load supply attempts to rise higher than (V_{ZENER} + $V_{THRESHOLD}$), the Protection comparator will trip, and the Delay Timer will start. If the high supply voltage condition lasts long enough for the Delay Timer to time out, the MOSFET will be latched off. The ON/OFF input must be toggled to restart the MOSFET.

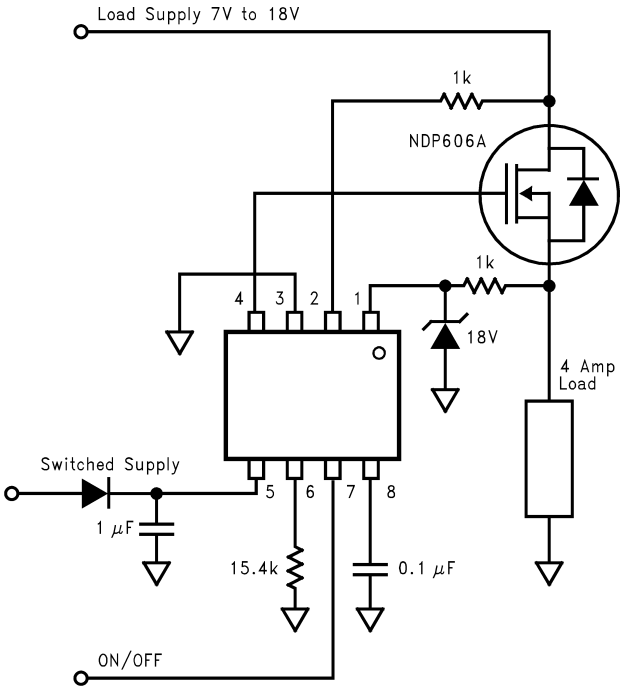


Figure 16. Adding Overvoltage Protection

Feature Description (continued)

7.3.7 Reverse Battery

If the V_{CC} supply should be taken negative with respect to ground, the current from the V_{CC} pin should be limited to 20 mA. The addition of a diode in series with the V_{CC} input is recommended. This diode drop does not subtract significantly from the charge pump gate overdrive output voltage.

7.3.8 Low Battery

An additional feature of the LM9061 is an Undervoltage Shut-OFF function (UVSO). The typical UVSO threshold is 6.2 V, and does not have hysteresis. When V_{CC} is between the ensured minimum operating voltage of 7.0V, and the UVSO threshold, the operation of the MOSFET gate drive, the delay timer, and the protection circuitry is not ensured. Operation in this region should be avoided. When V_{CC} falls below the UVSO threshold the charge pump will be disabled and the gate will be discharged at the Normal-OFF current sink rate, typically 110 µA.

Figure 17 shows the LM9061 used as an electronic circuit breaker. This circuit provides low voltage shutdown, overvoltage latch-OFF, and overcurrent latch-OFF.

The low voltage shutdown uses the 'On' and 'Off' voltage thresholds, and the typical 1.2 V of hysteresis, to disable the LM9061 if V_{CC} falls near, or below, the 7.0 V minimum operating voltage. The low voltage shutdown is accomplished with a voltage divider biased off V_{CC}. The voltage divider is formed by R1 (30 kΩ), R2 (82 kΩ), and the internal pull-down resistor of the ON/OFF pin (30 kΩ typical). In normal operation, V_{CC} will be above the minimum operating voltage of 7.0 V, and the On/Off pin will be biased above the 'Off' threshold of 1.5-V maximum (1.8-V typical). When V_{CC} falls to 7.0V the On/Off pin voltage will fall below the 'Off' threshold voltage and the LM9061 will be turned off.

In the event of a latch-OFF shutdown, the circuit can be reset by shutting the main supply off, then back on. An optional, normally open, switch (Clear) from the ON/OFF pin to ground, will allow a “push button clear” of the circuit after latching OFF.

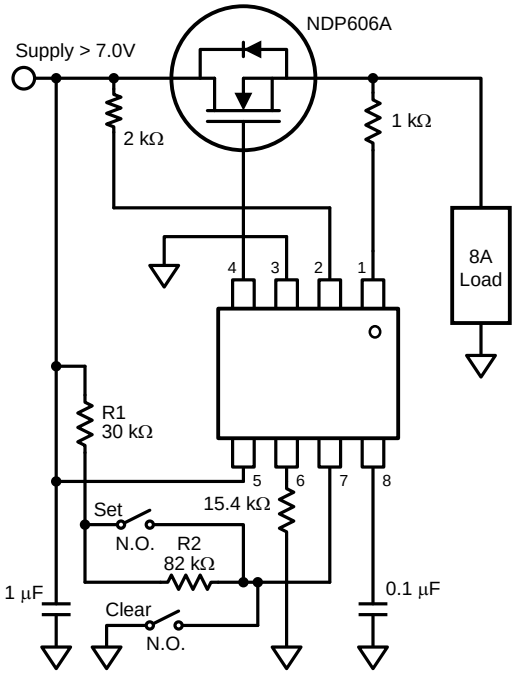


Figure 17. Electronic Circuit Breaker

Feature Description (continued)

This voltage divider arrangement requires a mechanism to raise the ON/OFF pin above the 'On' threshold of 3.5 V minimum (3.1 V typical) when V_{CC} is less than typically 16V. This can be accomplished with a second, normally open, switch from the ON/OFF pin across R2 (Set), so that closing the switch will short R2 and the voltage at the ON/OFF pin will be typically one-half of V_{CC}. When V_{CC} is at the minimum operating voltage of 7.0 V this will bias the ON/OFF pin to about 3.5 V causing the LM9061 to turn on. When V_{CC} is above typically 16.5 V the resistor divider will have the ON/OFF pin biased above 3.5 V and shorting of the resistor R2 will not be needed.

While the scaling of the external resistor values between V_{CC} and the ON/OFF input pin, against the internal 30-kΩ resistor, can be used to increase the startup voltage, it is important that the resistor ratio always has the ON/OFF pin biased below the 'Off' threshold (1.5 V) when V_{CC} falls below the minimum operating voltage of 7.0 V.

The accuracy of this voltage divider arrangement is affected by normal manufacturing variations of the 'On' and 'Off' voltage thresholds and the value of internal resistor at the ON/OFF pin. If any application needs to detect with greater precision when V_{CC} is near to 7.0 V, an external voltage monitor should be used to drive the ON/OFF pin. The external voltage monitor would also eliminate both the need for the switch to short R2 to start the LM9061, as well as R2.

7.3.9 Increasing MOSFET Turnon Time

The ability of the LM9061 to quickly turn on the MOSFET is an important factor in the management of the MOSFET power dissipation. Caution should be exercised when trying to increase the MOSFET turnon time by limiting the Gate drive current. The MOSFET average dissipation, and the LM9061 Delay time, must be recalculated with the extended switching transition time.

Figure 18 shows a method of increasing the MOSFET turnon time, without affecting the turnoff time. In this method the Gate is charged at an exponential rate set by the added external Gate resistor and the MOSFET Gate capacitances.

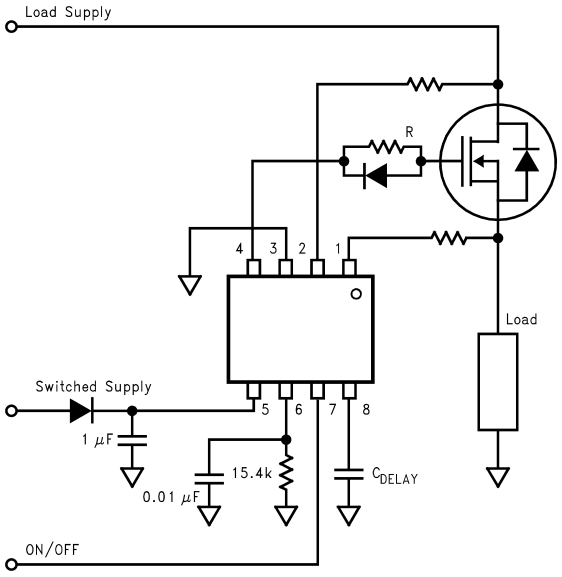


Figure 18. Increasing MOSFET Turnon Time

7.4 Device Functional Modes

7.4.1 Operation With V_{CC} > 30 V

If V_{CC} increases to more than typically 30 V the LM9061 will turn off the MOSFET to protect the load from excessive voltage. When V_{CC} has returned to the normal operating range the device will return to normal operation without requiring toggling the ON/OFF input. This feature will allow MOSFET operation to continue in applications that are subject to periodic voltage transients, such as automotive applications.

7.4.2 Operation With V_{CC} < 6.2 V

When V_{CC} falls below the UVSO threshold of 6.2 V the charge pump will be disabled and the gate will be discharged at the Normal-OFF current sink rate, typically 110 µA.

7.4.3 Operation With ON/OFF Control

In the ON state, the charge pump voltage, which is well above the available V_{CC} supply, is directly applied to the gate of the MOSFET. When commanded OFF a 110 µA current sink discharges the gate capacitances of the MOSFET for a gradual turn-OFF characteristic to minimize the duration of inductive load transient voltages and further protect the power MOSFET.

7.4.4 MOSFET Latch-OFF

In the event of excessive power dissipation in the MOSFET as detected by the LM9061 sense and threshold pins, the MOSFET is latched OFF to prevent permanent failure. It will not restart until the ON/OFF Input is toggled low then high.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM9061 can be configured to drive the gate to any size external high-side power MOSFET, including multiple parallel connected MOSFETs for very high current applications. See *Basic Operation* for details on the gate drive operation and *Turn On and Turn Off Characteristics* for details on the gate drive timing characteristics.

8.2 Typical Application

The LM9061 is an ideal driver for any application that requires multiple parallel MOSFETs to provide the necessary load current. Figure 19 shows a circuit with four parallel NDP706A MOSFETs. This circuit configuration will provide a typical maximum load current of 150 A at 25°C, and a typical maximum load current of 100 A at 125°C.

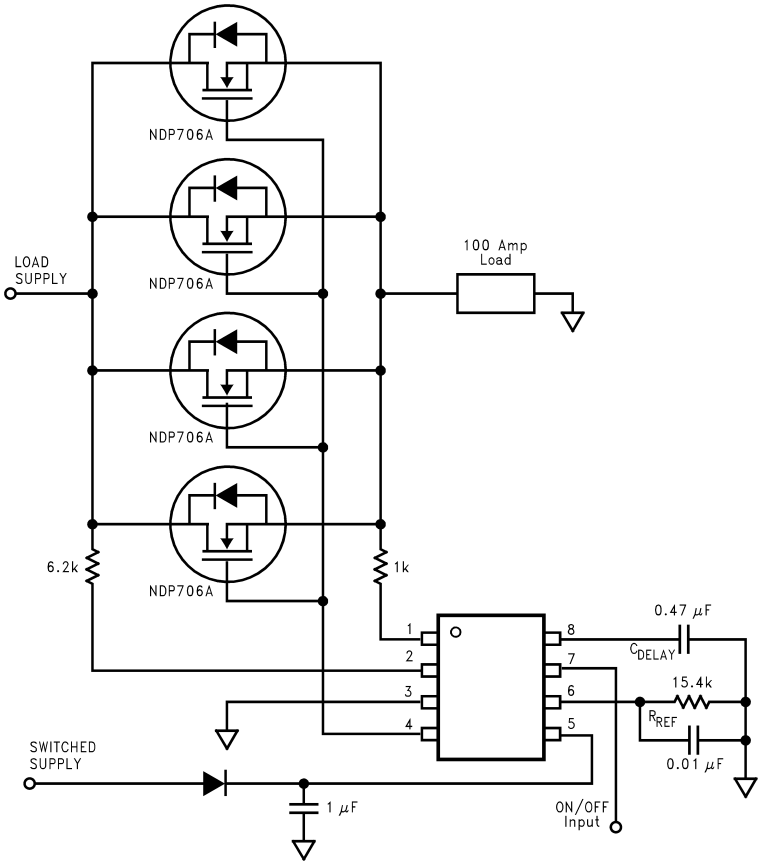


Figure 19. Driving Multiple MOSFETs

Typical Application (continued)

8.2.1 Design Requirements

Only a few “common sense” precautions need to be observed. All MOSFETs in the array must have identical electrical and thermal characteristics. This can be solved by using the same part number from the same manufacturer for all of the MOSFETs in the array. Also, all MOSFETs should have the same style heat sink or, ideally, all mounted on the same heat sink. The electrical connection of the MOSFETs should get special attention. With typical $R_{DS(ON)}$ values in the range of tens of milli-Ohms, a poor electrical connection for one of the MOSFETs can render it useless in the circuit. Also, the MOSFET dissipation during the Normal-OFF discharge of the gate capacitance, 70 µA minimum and 110 µA typical, needs consideration. One particular caution is that, in the event of a fault condition, the Latch-OFF current sink, 10 µA typical, may not be able to discharge the total gate capacitance in a timely manner to prevent damage to the MOSFETs.

8.2.2 Detailed Design Procedure

The NDP706A MOSFET has a typical $R_{DS(ON)}$ of 0.013 Ω with a T_J of 25°C, and 0.020Ω with a T_J of +125°C. An $R_{THRESHOLD}$ value of 6.2 kΩ as shown in Figure 19 will set the V_{DS} threshold voltage to approximately 500 mV. This will provide a typical maximum load current of 150 A at 25°C, and a typical maximum load current of 100 A at 125°C. See *Lossless Overcurrent Protection* for details on calculating $R_{THRESHOLD}$.

The maximum dissipation, per MOSFET, will be nearly 20 W at 25°C, and 12.5 W at 125°C. With up to 20 W being dissipated by each of the four devices, an effective heat sink will be required to keep the T_J as low as possible when operating near the maximum load currents.

8.2.3 Application Curves

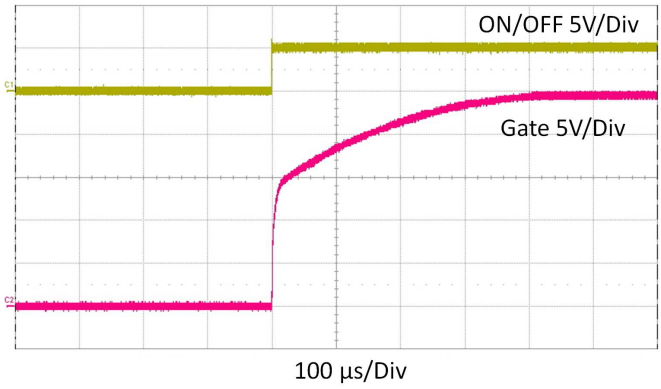


Figure 20. MOSFET Gate During Start-up, Total Gate Capacitance = 11200 pF

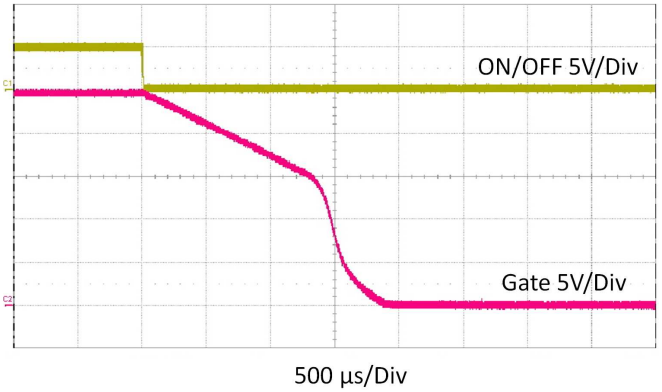


Figure 21. MOSFET Gate During Shut Down, Total Gate Capacitance = 11200 pF

9 Power Supply Recommendations

It is important to remember that during the Turn-ON of the MOSFET the output current to the Gate is drawn from the V_{CC} supply pin. The V_{CC} pin should be bypassed with a capacitor with a value of at least ten times the Gate capacitance, and no less than 0.1 µF. If the V_{CC} supply should be taken negative with respect to ground, for example during a reverse battery condition, the current from the V_{CC} pin should be limited to 20 mA. The addition of a diode in series with the V_{CC} input is recommended. This diode drop does not subtract significantly from the charge pump gate overdrive output voltage.

10 Layout

10.1 Layout Guidelines

1. The bypass capacitor for V_{CC} should be placed as close as possible to the V_{CC} pin.
2. The resistor R_{REF} should be placed as close as possible to the I_{REF} and Ground pins with minimal trace length to keep the I_{REF} current as accurate as possible. The LM9061 is optimized for use with a 15.4 kΩ ±1% resistor for R_{REF}.
3. In applications where the V_{CC} supply is subject to high levels of transient noise, a bypass capacitor across R_{REF} is recommended. This bypass capacitor should be no larger than 0.1 µF and should be placed as close as possible to the I_{REF} pin.
4. The $R_{THRESHOLD}$ and R_{SENSE} resistors should be placed as close as possible to the MOSFET drain and source pins respectively. This will allow accurate monitoring of the V_{DS} voltage across the MOSFET.
5. An array of vias can be placed along the high current path to the output load. These vias can help conduct heat to any inner plane areas or to a bottom-side copper plane.

10.2 Layout Example

Figure 22 and Figure 23 are layout examples for the LM9061/LM9061-Q1. These examples are taken from the LM9061EVM. For information on the operation and schematic of the EVM, see the LM9061EVM User's Guide (SNOU132).

Layout Example (continued)

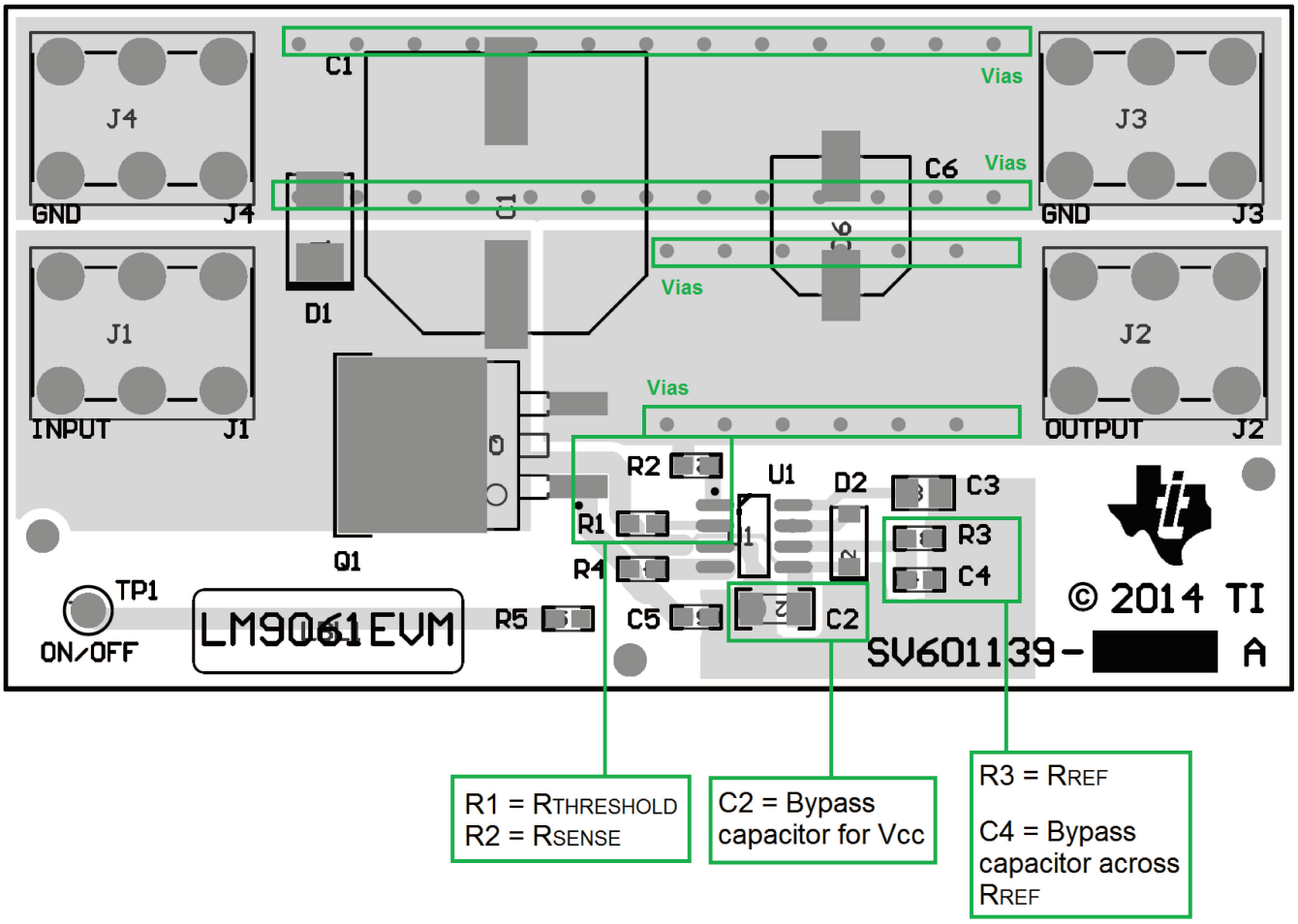


Figure 22. LM9061EVM Layout Example (Top)

Layout Example (continued)

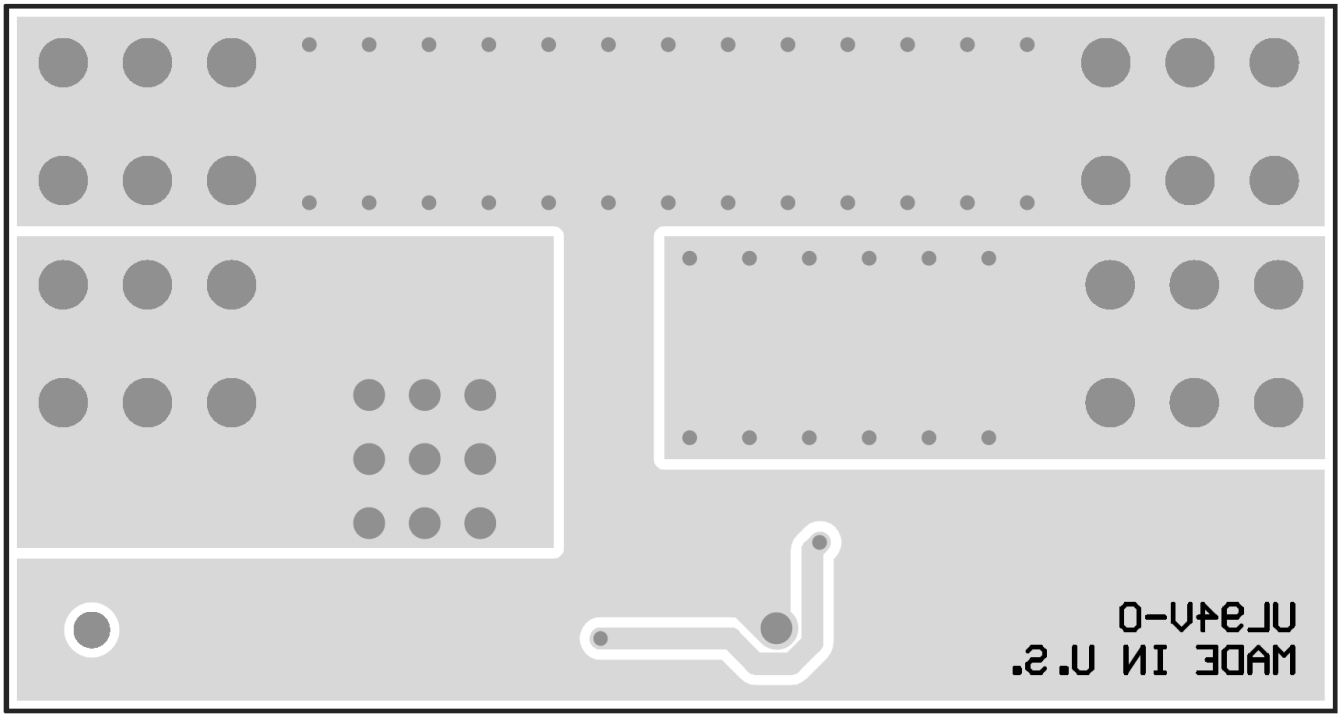


Figure 23. LM9061EVM Layout Example (Bottom)

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM9061	Click here	Click here	Click here	Click here	Click here
LM9061-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9061M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM90 61M	Samples
LM9061MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM90 61M	Samples
LM9061QDQ1	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	9061Q1	
LM9061QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HRS	-40 to 125	9061Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM9061, LM9061-Q1 :

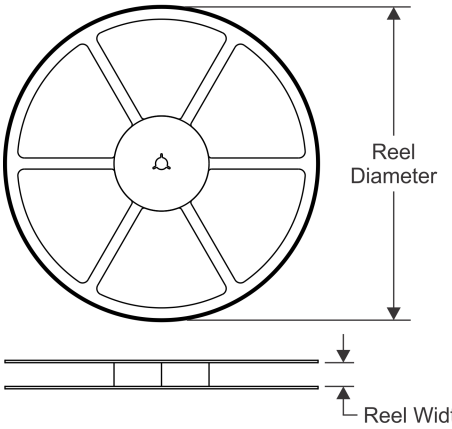
- Catalog: LM9061
- Automotive: LM9061-Q1

NOTE: Qualified Version Definitions:

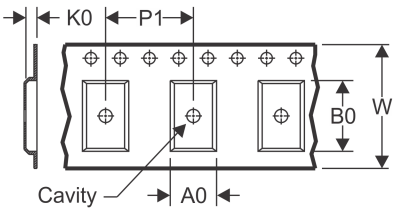
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

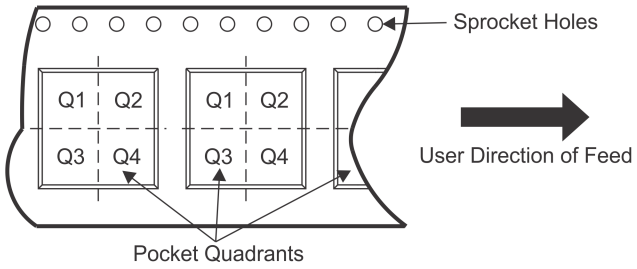


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

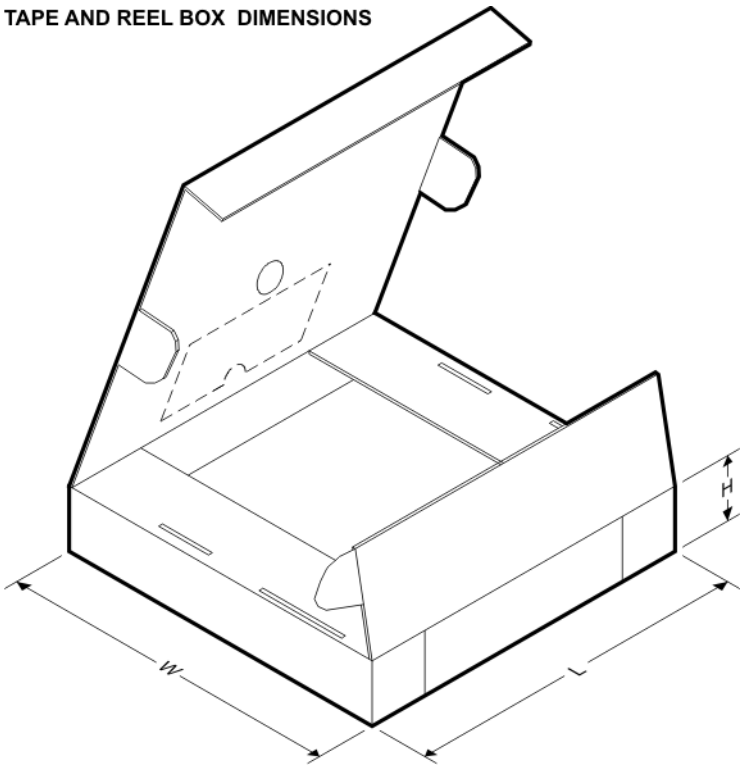
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9061MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9061QDRQ1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

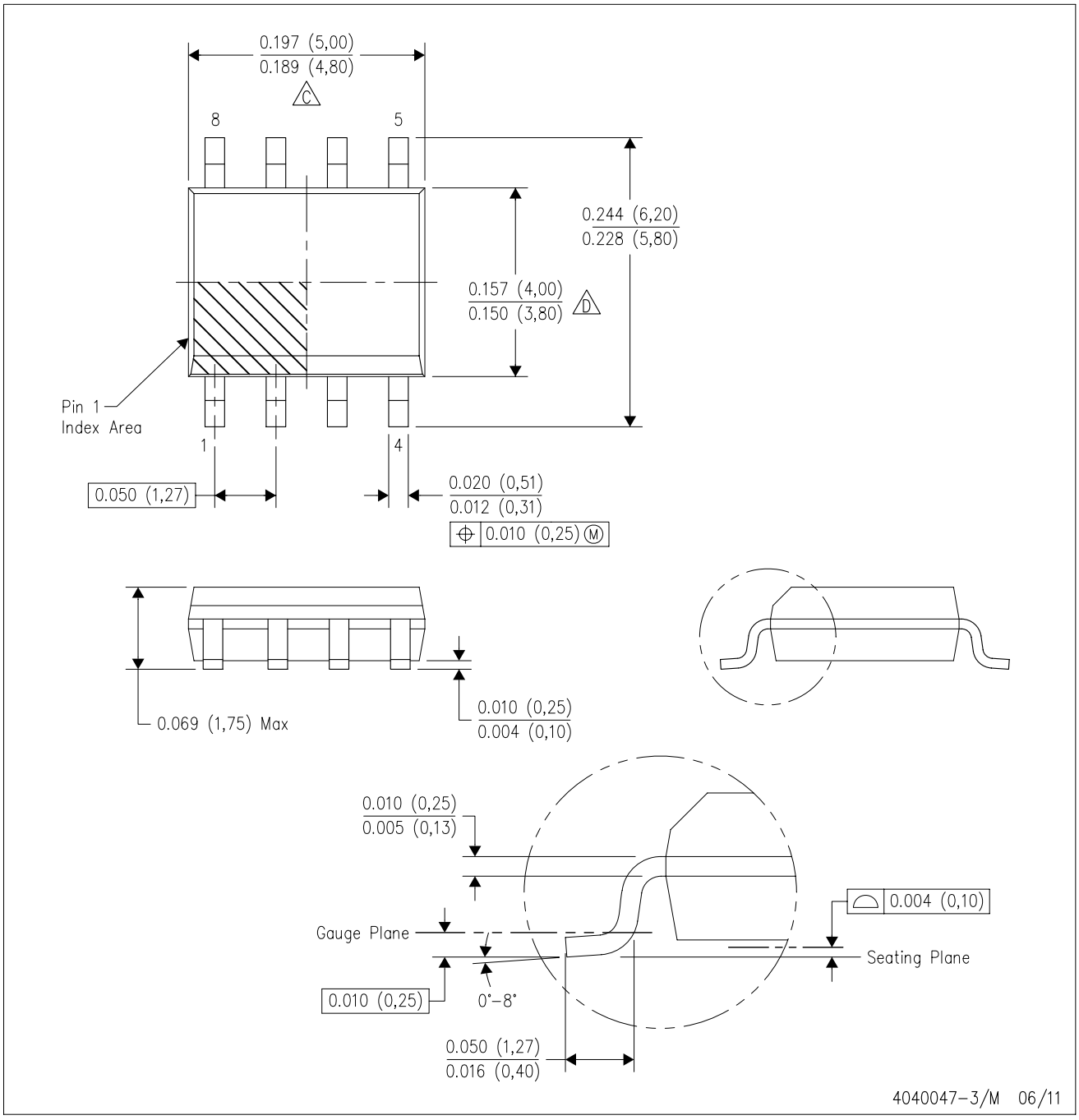
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

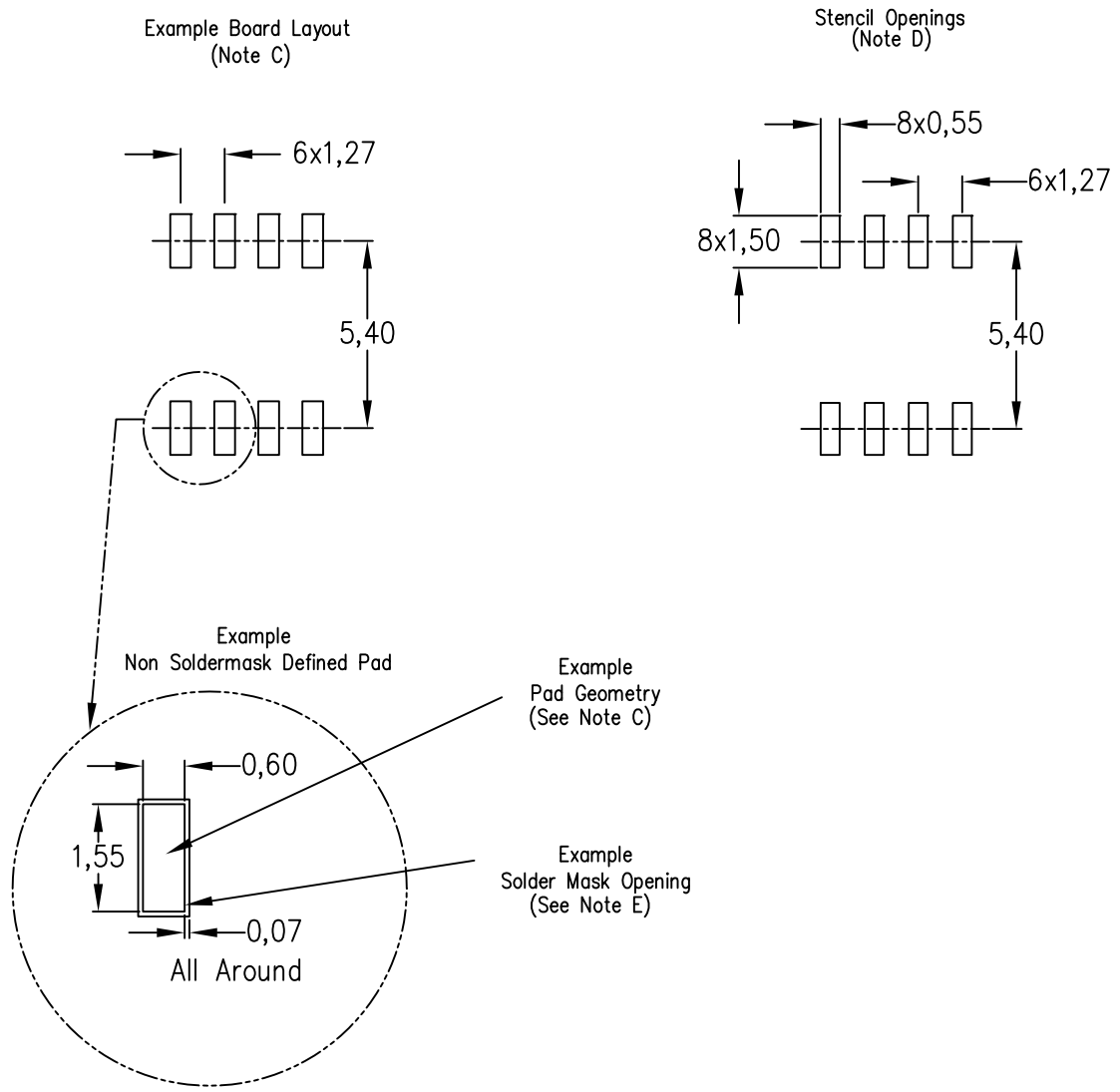
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9061MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9061QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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