

## LM98555 CCD Driver

 Check for Samples: [LM98555](#)

### FEATURES

- All CCD Drivers Integrated into One Package
- High Strength Drivers Designed Specifically for CCD Loads
- Ability to Scale Clock Driver Strength
- Skew Specifications Ensured
- Separate Input and Output Power Supplies
- CMOS Process Technology
- 64-Pin HTSSOP Package with Extended Power Handling Capability

### DESCRIPTION

The LM98555 is a highly integrated driver circuit intended for CCD driving applications. It combines 25 drivers of varying drive strengths into one chip to provide a complete CCD driving solution. Due to this one-chip integration, optimal skew control is achieved for this demanding application.

### KEY SPECIFICATIONS

- Supply Voltage
  - Inputs 3.0 to 5.5V
  - Drivers 4.5 to 5.8V
- Maximum Output Skew Between P1A and P2A Outputs 0.5 ns
- Maximum Power Handling 2.0W

### Functional Description

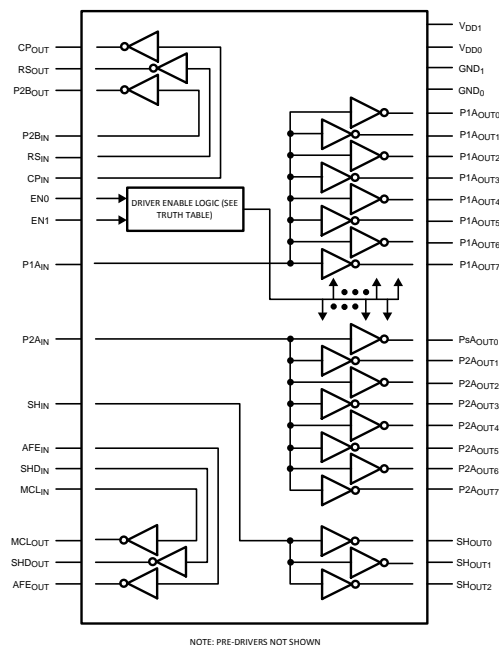


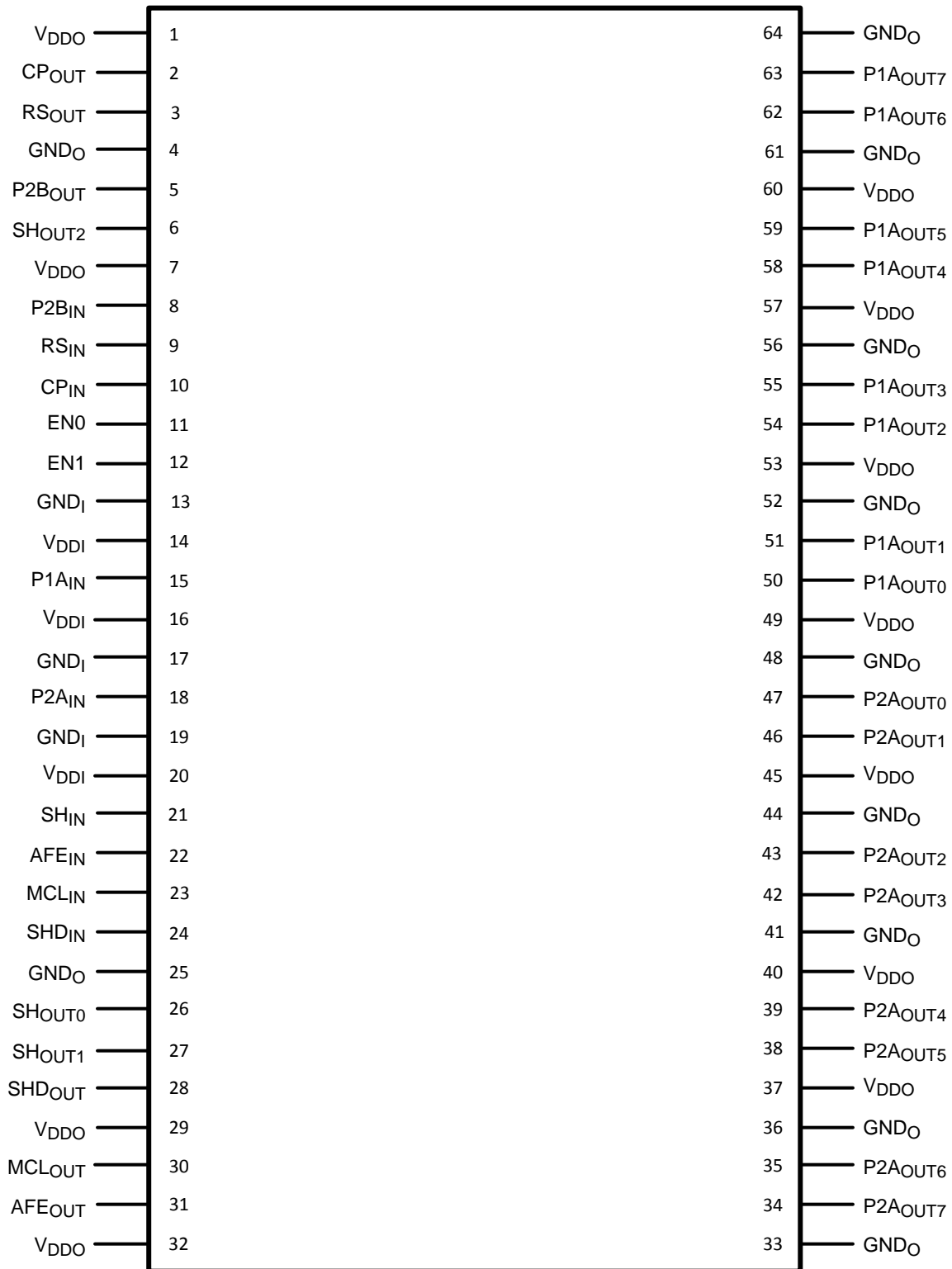
Figure 1. Functional Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**Connection Diagram**



**Figure 2. HTSSOP Package  
See Package Number DCA0064A**

### Pin Descriptions

Pin Name	Pin No.	Type	Description
<b>Driver inputs</b>			
P2B <sub>IN</sub>	8	Input	CMOS logic input for the P2B driver.
RS <sub>IN</sub>	9	Input	CMOS logic input for the RS driver.
CP <sub>IN</sub>	10	Input	CMOS logic input for the CP driver.
P1A <sub>IN</sub>	15	Input	CMOS logic input for the P1A ganged (8) driver set.
P2A <sub>IN</sub>	18	Input	CMOS logic input for the P2A ganged (8) driver set.
SH <sub>IN</sub>	21	Input	CMOS logic input for the SH ganged (3) driver set.
AFE <sub>IN</sub>	22	Input	CMOS logic input for the AFE driver.
MCL <sub>IN</sub>	23	Input	CMOS logic input for the MCL driver.
SHD <sub>IN</sub>	24	Input	CMOS logic input for the SHD driver.
<b>Driver Outputs</b>			
SHD <sub>OUT</sub>	28	Output; Low-Strength	Driver output for the SHD <sub>IN</sub> input signal.
MCL <sub>OUT</sub>	30	Output; Low-Strength	Driver output for the MCL <sub>IN</sub> input signal.
AFE <sub>OUT</sub>	31	Output; Low-Strength	Driver output for the AFE <sub>IN</sub> input signal.
CP <sub>OUT</sub>	2	Output; Low-Strength	Driver output for the CP <sub>IN</sub> input signal. Typically used to drive the Clamp Gate input of the CCD.
RS <sub>OUT</sub>	3	Output; Low-Strength	Driver output for the RS <sub>IN</sub> input signal. Typically used to drive the Reset Gate input of the CCD.
P2B <sub>OUT</sub>	5	Output; Low-Strength	Driver output for the P2B <sub>IN</sub> input signal.
P2A <sub>OUT0</sub>	47	Output; TRI-STATE; High-Strength	Ganged driver outputs for the P2A <sub>IN</sub> input. Typically the user may join together these outputs to drive the $\phi$ 2 clock input of the CCD. Some of these outputs may be disabled using the EN(1:0) inputs - see <a href="#">Application Information</a> .
P2A <sub>OUT1</sub>	46		
P2A <sub>OUT2</sub>	43		
P2A <sub>OUT3</sub>	42		
P2A <sub>OUT4</sub>	39		
P2A <sub>OUT5</sub>	38		
P2A <sub>OUT6</sub>	35		
P2A <sub>OUT7</sub>	34		
P1A <sub>OUT0</sub>	50	Output; TRI-STATE; High-Strength	Ganged driver outputs for the P1A <sub>IN</sub> input. Typically the user may join together these outputs to drive the $\phi$ 1 clock input of the CCD. Some of these outputs may be disabled using the EN(1:0) inputs - see <a href="#">Application Information</a> .
P1A <sub>OUT1</sub>	51		
P1A <sub>OUT2</sub>	54		
P1A <sub>OUT3</sub>	55		
P1A <sub>OUT4</sub>	58		
P1A <sub>OUT5</sub>	59		
P1A <sub>OUT6</sub>	62		
P1A <sub>OUT7</sub>	63		
SH <sub>OUT0</sub>	26	Output; Low-Strength	Ganged driver outputs for the SH <sub>IN</sub> input signal. Typically used to drive the Shift Gate input of the CCD.
SH <sub>OUT1</sub>	27		
SH <sub>OUT2</sub>	6		
<b>Logic Inputs</b>			
EN0	11	Input	Driver enable control. Some of the P1A and P2A drivers can be disabled using these inputs. See <a href="#">Application Information</a> .
EN1	12		
<b>Power &amp; Ground Pins</b>			
V <sub>DDI</sub>	14 16 20	Power	V <sub>DD</sub> for pre-drivers.

**Pin Descriptions (continued)**

Pin Name	Pin No.	Type	Description
V <sub>DDO</sub>	1 7 29 32 37 40 45 49 53 57 60	Power	V <sub>DD</sub> for final-stage driver.
GND <sub>I</sub>	13 17 19	Ground	Ground connection for all circuitry other than the Final-Stage Drivers.
GND <sub>O</sub>	4 25 33 36 41 44 48 52 56 61 64	Ground	Ground connection for the Final-Stage Drivers.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage		-0.5V to 6.2V
Package Power Rating at 25°C <sup>(3)</sup>		2.0 Watts
Voltage on Any Input or Output Pin		-0.5V to $V_{DD}+0.5V$
DC Input Current at Any Pin		25 mA
DC Package Input Current		50 mA
Storage Temperature		-65°C to +150°C
Lead temperature (Soldering, 10 sec.)		300°C
ESD Susceptibility	Human Body Model	2000V
	Machine Model	200V

- (1) Absolute maximum ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Package power rating assumes the exposed thermal pad is soldered to the printed circuit board as recommended, with significant heat spreading provided by vias to internal or bottom heat dissipation planes or pad. If this is not the case, then the package power rating should be reduced. See [THERMAL GUIDELINES](#) in [Application Information](#) for more information.

### Operating Conditions

Supply Voltage	$V_{DDI}$	+3.0V to +5.5V
Supply Voltage	$V_{DDO}$	+4.5V to +5.8V
Supply Sequencing <sup>(1)</sup>		$V_{DDI} < V_{DDO}+0.2V$
Ambient Temperature ( $T_A$ )		0 to 70°C
Operating Frequency		30 MHz
Power Dissipation <sup>(2)</sup>		2.0W

- (1) When powering up and down, transient voltage levels on  $V_{DDI}$  must be lower than ( $V_{DDO} + 0.2V$ )
- (2) This is the power dissipated on-chip due to all currents flowing through the device - both DC and AC. This operating condition will be violated if all driver outputs are fully loaded and operating at the same time at the rated  $F_{MAX}$ . The system design must constrain the chip's operating conditions (loads, power supply, number of parallel drivers enabled, frequency of operation) to make certain that this limit is never exceeded.

### Package Thermal Resistances

Package	$\theta_{J-A}$ <sup>(1)</sup>	$\theta_{J-PAD}$ (Thermal Pad)
64-Lead HTSSOP	36.8°C / W	6.2°C / W

- (1) Package thermal resistance for junction to ambient is based on a 5.5 inch by 3 inch, 4 layer printed circuit board, with thermal vias connecting the heat sinking pad to a full internal ground plane. Tests were done in still air, with a power dissipation of 2.0 W, at an ambient temperature of 22°C.

### DC Electrical Characteristics

The following specifications apply for  $GND = 0V$ ,  $V_{DDI} = 3.3V$ ,  $V_{DDO} = 5.0V$ , unless noted otherwise. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = 25^\circ C$

Parameter		Test Conditions	Min	Typical	Max	Units
$I_I$	Logic 1 Input Current	$V_I = V_{DDI}$	<b>-1</b>	0.004	<b>1</b>	$\mu A$
	Logic 0 Input Current	$V_I = GND_I$	<b>-1</b>	0.006	<b>1</b>	$\mu A$
$V_{IT}$	Input Threshold	$V_{DDI} = 3.3V$	<b>1.41</b>	1.57	<b>1.75</b>	V
	Input Threshold	$V_{DDI} = 5.0V$		2.48		V
	Input Threshold Hysteresis	$V_{DDI} = 3.3V$	<b>-72</b>	11	<b>100</b>	mV
$\Delta V_{IT}$	Input Threshold Variation	Between P1A, P2A inputs	-100		100	mV

## DC Electrical Characteristics (continued)

The following specifications apply for GND = 0V,  $V_{DDI} = 3.3V$ ,  $V_{DDO} = 5.0V$ , unless noted otherwise. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = 25^\circ C$

Parameter		Test Conditions	Min	Typical	Max	Units
R <sub>O</sub>	Output Impedance P1A and P2A Outputs	$I_{LOAD} = 525 \text{ mA}$		6.1	<b>9.9</b>	$\Omega$
		$R_O = (V_{DDO} - V_O)/I_{OH}$ or				
		$R_O = V_O/I_{OL}$				
R <sub>O</sub>	Output Impedance All Other Outputs	$I_{LOAD} = 280 \text{ mA}$		10.2	<b>17.4</b>	$\Omega$
		$R_O = (V_{DDO} - V_O)/I_{OH}$ or				
		$R_O = V_O/I_{OL}$				

## AC Electrical Characteristics

The following specifications apply for GND = 0V,  $V_{DDI} = 3.3V$ ,  $V_{DDO} = 5.0V$ , unless noted otherwise. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = 25^\circ C$

Parameter		Test Conditions	Min	Typical	Max	Units
t <sub>PHL</sub>	Prop Delay: High-to-Low P1A and P2A Outputs	$C_L = 220 \text{ pF}$ , $R_L = 10\Omega^{(1)}$	<b>3.06</b>	4.6	<b>6.55</b>	ns
t <sub>PHL</sub>	Prop Delay: High-to-Low CP, RS, P2B Outputs	$C_L = 82 \text{ pF}$ , $R_L = 10\Omega^{(1)(2)}$		4.1		ns
t <sub>PLH</sub>	Prop Delay: Low-to-High P1A and P2A Outputs	$C_L = 220 \text{ pF}$ , $R_L = 10\Omega^{(3)}$	<b>3.38</b>	4.9	<b>6.68</b>	ns
t <sub>PLH</sub>	Prop Delay: Low-to-High CP, RS, P2B Outputs	$C_L = 82 \text{ pF}$ , $R_L = 10\Omega^{(3)(2)}$		4.2		ns
t <sub>SKEW</sub>	Prop Delay Skew High-to-Low	Between any P1A or P2A Outputs on a Single Unit $C_L = 220 \text{ pF}$ , $R_L = 10\Omega$		109	<b>387</b>	ps
	Prop Delay Skew Low-to-High			157	<b>490</b>	

- (1) Propagation Delay High-to-Low with output low trigger voltage at  $V_{DDO} * 0.75$ .
- (2) Typical values determined from characterization testing only. Not production tested or ensured.
- (3) Propagation Delay Low-to-High with output high trigger voltage at  $V_{DDO} * 0.25$ .

### Test Conditions

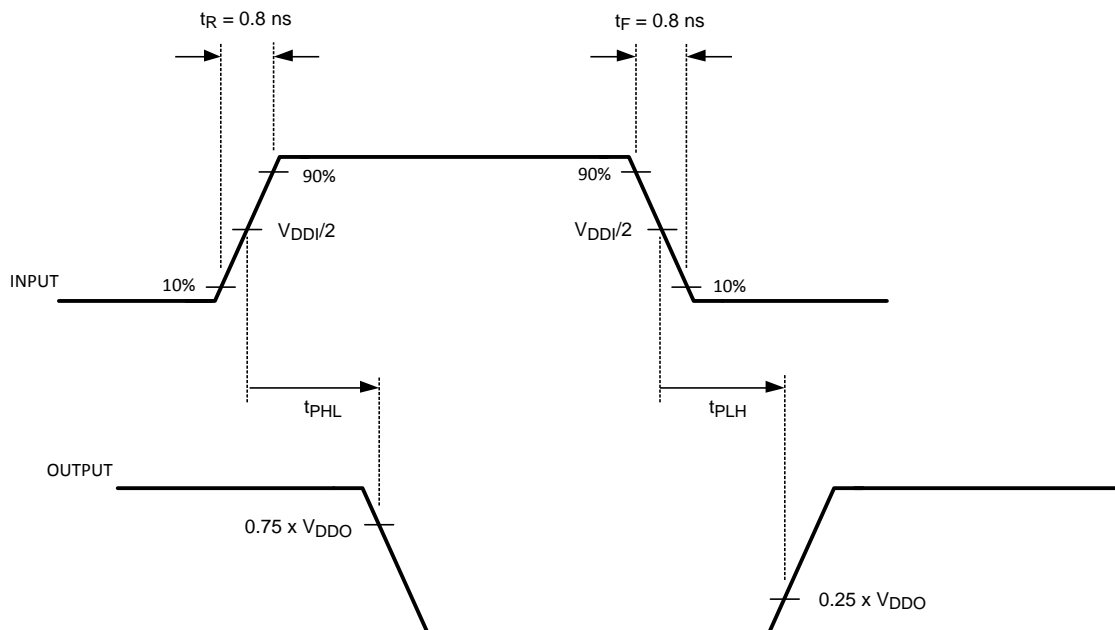


Figure 3. AC Test Conditions

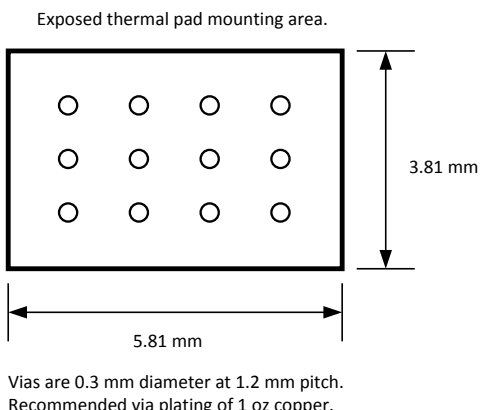
## APPLICATION INFORMATION

The LM98555 is a fully integrated clock driver/buffer for high speed CCD applications. It provides high performance low impedance drivers, with optimized low skew performance of the P1 and P2 outputs. Enable inputs allow use of two, four, six, or all eight P1 and P2 drivers to optimize the amount of drive for the application. The 64 pin thermally enhanced HTSSOP provides excellent power handling through the use of an exposed heat transfer pad on the underside of the package.

### THERMAL GUIDELINES

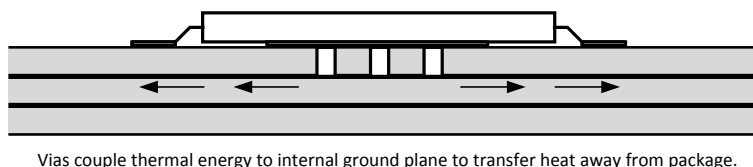
The LM98555's maximum power dissipation limit, shown in [Operating Conditions](#), must be strictly adhered to. The product's multiple high-strength drivers, with their ability to drive a wide-range of loads, make it possible to be within spec on each output and yet violate the aggregate maximum power dissipation limit for the total product. Special caution must be paid to this by limiting the chip's operating conditions (loads, power supply, number of parallel drivers enabled, frequency of operation) to make certain that the maximum power dissipation limit is never exceeded.

Thermal characterization of the device has been done to provide reference points under specific conditions.  $\theta$  junction to ambient was measured using a 5.5 inch by 3 inch, 4 layer PCB. The thermal contact pad on the board was connected using vias to a full ground plane on one of the internal layers. The recommended thermal pad is shown in [Figure 4](#).

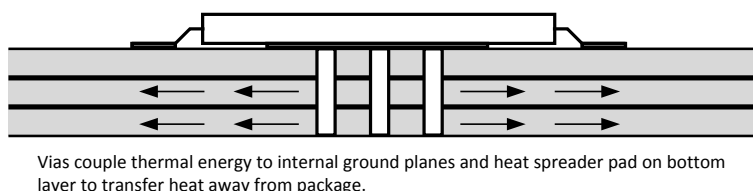


**Figure 4. Exposed Pad Land Pattern**

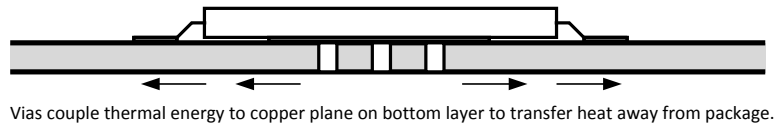
The vias shown provide a path for heat to flow from the pad to a heat sinking or dissipating area of the printed circuit board. The following figures show several typical examples of how this can be done, and illustrate how heat is conducted away from the IC to larger areas where it is dissipated.



**Figure 5. 4 Layer PCB - Example 1**



**Figure 6. 4 Layer PCB - Example 2**



**Figure 7. 2 Layer PCB**

In multi-layer board applications, one or more internal planes are usually dedicated as a ground plane. Connecting the thermal pad to this ground plane with vias will usually provide adequate heat management. In 2 layer boards, it is important to provide a large heat spreading pad on the opposite side of the board. The vias will provide a good thermal connection between the pad under the IC, and the heat spreading pad on the bottom of the board. Thermal modelling can be done using the  $\theta$  junction to pad information provided, to calculate the required area of copper based on the ambient temperature of the system, and the calculated amount of thermal dissipation in the LM98555.

## POWER DISSIPATION

The amount of power dissipated in the device can be determined by considering the following factors:

- Power dissipated delivering energy to the load capacitance
- Power dissipated delivering energy to parasitic capacitance
- Power dissipated due to leakage in the IC

The amount of power dissipated due to leakage is very small in this CMOS device. Most of the power will be due to the load capacitance being switched, with a small additional amount caused by the parasitic capacitance of the output circuitry, output pins, and PCB traces. A typical parasitic capacitance would be on the order of 5 pF. Since the load capacitance will be on the order of 100 pF or more, this usually dominates the power dissipation calculation. The following equation can be used to calculate the power dissipation due to capacitive switching of the loads:

$$P = \text{Sum}[\text{Output Frequency} \times \text{Load Capacitance} \times \text{Output Voltage Squared}] \text{ (summed for all outputs)}$$

## INPUT SIGNALS

Care should be taken to match the trace lengths between timing signals that require low skew. Usually, the P1A and P2A signals will be the most critical. In some applications, the timing of P2B with respect to P1A and P2A can also be important, and that input trace should also be carefully designed.

Trace shape and width should also be carefully controlled. The trace geometry will determine the characteristic impedance of each trace. The impedance should be set to give reasonable immunity to noise coupling into the trace. With a known trace impedance, the signals can be terminated using a series resistor at the source that is equal to the characteristic impedance. This will provide a signal with minimum overshoot and ringing, and will contribute to better performance of the final signal reaching the CCD.

## OUTPUT CONNECTIONS AND LOADING EXAMPLES

The LM98555 can be used with a wide variety of different CCD sensors. The P1Aoutx and P2Aoutx outputs can be selectively enabled to provide 2, 4, 6, or 8 drivers. This allows the available drive strength to be optimized for the sensor and application. Connecting multiple outputs together in parallel as shown in the typical application circuit provides lower drive impedance as needed to suit the load being driven. When driving smaller loads, lower switching noise will be generated if the minimum necessary outputs are enabled and used.

The output signal traces should also be designed for a known impedance. Source terminating resistors should be used in series with each output to provide good matching to the trace characteristic impedance. The resistors should be located as close as possible to each output pin. If multiple outputs will be combined to drive a single load pin, the output signals should be combined after the termination resistors. This will provide the best summing of adjacent outputs. The combined signal should then pass through an EMI type ferrite bead. This component can be selected to change the bandwidth or shape of the clocking signal to achieve the best CCD transfer efficiency.



Several other techniques will also help maintain signal quality, and minimize timing differences between critical signals. Vias should not be used for critical timing signals. These can add impedance discontinuities that will affect the waveform quality. Traces should have gradual bends and avoid sharp changes in direction that can also introduce impedance discontinuities.

### SELECTIVE DRIVER ENABLING

With the Enable pins, the user has the capability to enable only the drivers that are required for the application, thus eliminating unnecessary outputs switching. The following table shows the details.

EN1	EN0	Driver-set State
0	0	P1Aout(1:0) and P2Aout(1:0) are enabled; all others disabled.
0	1	P1Aout(3:0) and P2Aout(3:0) are enabled; all others disabled.
1	0	P1Aout(5:0) and P2Aout(5:0) are enabled; all others disabled.
1	1	All P1Aout and P2Aout drivers are enabled.

Note: The disabled drivers' outputs are in TRI-STATE.

### POWER SUPPLY SEQUENCING

During device power-up and power-down,  $V_{DDI}$  must be maintained less than  $(V_{DDO} + 0.2V)$  to prevent excessive current flow through the internal ESD protection circuitry. Since most applications will involve 3V on  $V_{DDI}$  and 5V on  $V_{DDO}$ , this can be easily met. If this voltage relationship cannot be met, then the DC pin and package limits for input current must be maintained by controlling the source impedance of the  $V_{DDI}$  supply.

### POWER AND GROUND - PLANES VERSUS BUSES

The best performance will be achieved by using planes rather than traces for power and ground. Planes provide lower electrical and thermal impedance. Ground bounce and ringing are reduced, electromagnetic emissions are minimized and the best thermal performance will be realized.

A single common ground plane should be used for all power and signal domains.

Another circuit board layer can be used to provide power to the various circuitry. Different power buses can be provided by isolated planes within this layer of the circuit board.

### EMI MANAGEMENT

Good EMI control will be achieved by addressing the following items:

- Provide proper source termination of output signals
- Limit length of output traces
- Ensure adequate power supply decoupling
- Provide power and ground planes as much as possible
- Provide common ground plane for all signals, especially between LM98555 outputs and load CCD
- Enable and use the minimum number of outputs needed

## REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">9</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM98555CCMH/NOPB	ACTIVE	HTSSOP	DCA	64	28	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-4-260C-72 HR	0 to 70	LM98555 CCMH	<a href="#">Samples</a>
LM98555CCMHX/NOPB	ACTIVE	HTSSOP	DCA	64	1000	Green (RoHS & no Sb/Br)	CU SN   Call TI	Level-4-260C-72 HR	0 to 70	LM98555 CCMH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)