

MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range:** 1.8 V to 3.6 V
- **Ultra-Low Power Consumption**
 - **Active Mode:** 220 μ A at 1 MHz, 2.2 V
 - **Standby Mode:** 0.5 μ A
 - **Off Mode (RAM Retention):** 0.1 μ A
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μ s**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
 - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to $\pm 1\%$**
 - **Internal Very-Low-Power Low-Frequency Oscillator**
 - **32-kHz Crystal ⁽¹⁾**
 - **External Digital Clock Source**
- **16-Bit Timer_A With Two Capture/Compare Registers**
- **10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan**
- **Universal Serial Interface (USI) Supports SPI and I2C**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members:**
 - **2kB + 256B Flash Memory**
 - **128B RAM**
- **Available in 8-Pin Plastic Packages (D)**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extended ($-40^{\circ}\text{C}/125^{\circ}\text{C}$) Temperature Range ⁽²⁾**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Crystal oscillator cannot be operated beyond 105°C

(2) Custom temperature ranges available

DESCRIPTION

The MSP430G2230 is an ultra-low-power microcontroller. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.

The MSP430G2230 is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer and four I/O pins. In addition, the MSP430G2230 has a built-in communication capability using synchronous protocols (SPI or I2C) and a 10-bit A/D converter.

Table 1. Available Options⁽¹⁾

| T _A | PACKAGED DEVICES ⁽²⁾ | | TOPS-SIDE MARKING | VID NUMBER |
|----------------|---------------------------------|---------------------|-------------------|------------------|
| | PLASTIC 8-PIN (D) | | | |
| -40°C to 125°C | MSP430G2230QDREP | Tape and reel, 2500 | G230EP | V62/12620-01XE |
| | MSP430G2230QDEP | Tube, 75 | | V62/12620-01XE-T |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging



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Device Pinout and Functional Block Diagram

See [Application Information](#) for detailed I/O information.

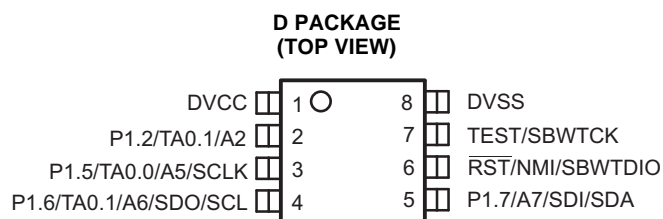


Figure 1. Device Pinout

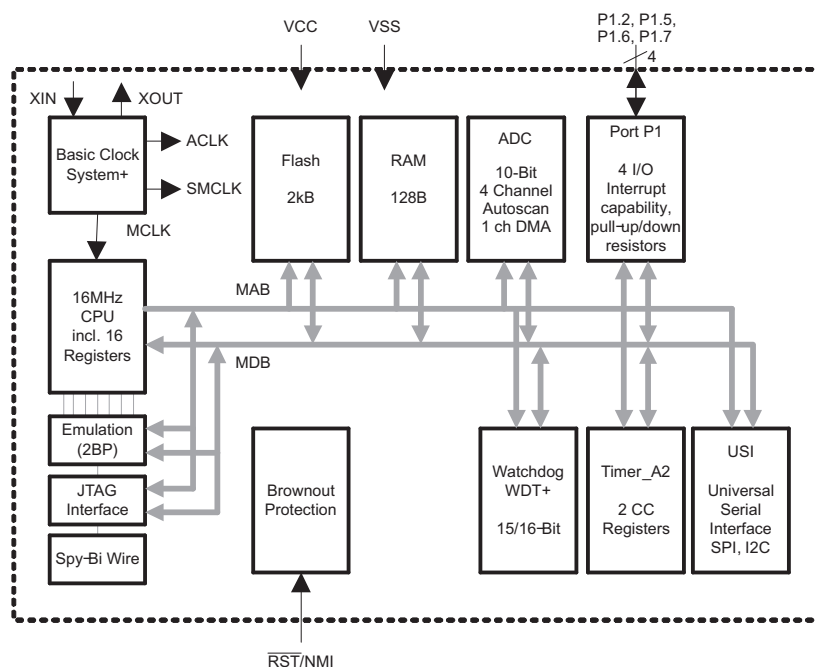


Table 2. Terminal Functions⁽¹⁾

| TERMINAL | | | DESCRIPTION |
|---------------------------------------|----------|-----|---|
| NAME | NO. D | I/O | |
| P1.2/ TA0.1/ A2 | 2 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare Out1 output ADC10 analog input A2 |
| P1.5/ TA0.0/ A5/ SCLK | 3 | I/O | General-purpose digital I/O pin Timer_A, compare Out0 output ADC10 analog input A5 USI: clock input in I2C mode; clock input/output in SPI mode |
| P1.6/ TA0.1/ A6/ SDO/ SCL | 4 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode USI: I2C clock in I2C mode |
| P1.7/ A7/ SDI/ SDA | 5 | I/O | General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode USI: Data input in I2C mode |
| RST/ NMI/ SBWTDIO | 6 | I | Reset input Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| TEST/ SBWTCK | 7 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |
| DVCC | 1 | | Digital supply voltage |
| DVSS | 8 | | Digital ground reference |

(1) The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source (see the *MSP430x2xx Family User's Guide* ([SLAU144](#))).

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 3](#) shows examples of the three types of instruction formats; [Table 4](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 3. Instruction Word Formats

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 ---> R5 |
| Single operands, destination only | CALL R8 | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 4. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|-----------------|------------------|-------------------------------|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11 R10 + 2 → R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active. MCLK is disabled
 - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0x0FFFF to 0x0FFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0x0FFFE) contains 0x0FFFF (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|--|--|------------------|-----------------|
| Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range ⁽¹⁾ | PORIFG RSTIFG WDTIFG KEYV ⁽²⁾ | Reset | 0xFFFE | 31, highest |
| NMI Oscillator fault Flash memory access violation | NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾ | (non)-maskable, (non)-maskable, (non)-maskable | 0xFFFC | 30 |
| | | | 0xFFFA | 29 |
| | | | 0xFFFF8 | 28 |
| Watchdog Timer+ | WDTIFG | maskable | 0xFFFF4 | 26 |
| Timer_A2 | TACCR0 CCIFG ⁽⁴⁾ | maskable | 0xFFFF2 | 25 |
| Timer_A2 | TACCR1 CCIFG, TAIFG ⁽²⁾⁽⁴⁾ | maskable | 0xFFFF0 | 24 |
| | | | 0xFFEE | 23 |
| | | | 0xFFEC | 22 |
| ADC10 (MSP430G2230 Only) | ADC10IFG ⁽⁴⁾ | maskable | 0xFFEA | 21 |
| USI (MSP430G2230 Only) | USIIFG, USISTTIFG ⁽²⁾⁽⁴⁾ | maskable | 0xFFE8 | 20 |
| | | | 0xFFE6 | 19 |
| I/O Port P1(four flags) | P1IFG.2, P1IFG.5, P1IFG.6, and P1IFG.7 ⁽²⁾⁽⁴⁾⁽⁵⁾ | maskable | 0xFFE4 | 18 |
| | | | 0xFFE2 | 17 |
| | | | 0xFFE0 | 16 |
| See ⁽⁶⁾ | | | 0xFFDE to 0xFFC0 | 15 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) All eight interrupt flags P1IFG.0 to P1IFG.7 are implemented while four are connected to pins.

(6) The interrupt vectors at addresses 0xFFDE to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.






| | | |
|---------------|---|---|
| Legend | rw: | Bit can be read and written. |
| | rw-0,1: | Bit can be read and written. It is reset or set by PUC. |
| | rw-(0,1): | Bit can be read and written. It is reset or set by POR. |
| |  | SFR bit is not present in device. |

Table 6. Interrupt Enable Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------------|--------------|--|---|-------------|--------------|
| 00h |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE Oscillator fault interrupt enable. Set to 0.
NMIIE (Non)maskable interrupt enable
ACCVIE Flash access violation interrupt enable




















| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--|---|---|---|
| 01h |  |  |  |  |  |  |  |  |

Table 7. Interrupt Flag Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---------------|---------------|---------------|--------------|---------------|
| 02h |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{\text{RST}}$ /NMI pin in reset mode.
OFIFG Flag set on oscillator fault. The XIN/XOUT pins are not available as device terminals.
PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$ /NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG Set by $\overline{\text{RST}}$ /NMI pin

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--|---|---|---|
| 03h |  |  |  |  |  |  |  |  |

Memory Organization

Table 8. Memory Organization

| | | MSP430G2230 |
|---|------------------------------|---|
| Memory Main: interrupt vector Main: code memory | Size Flash Flash | 2KB Flash 0xFFFF-0xFFC0 0xFFFF-0xF800 |
| Information memory | Size Flash | 256 Byte 0x10FF - 0x1000 |
| RAM | Size | 128 Byte 0x027F - 0x0200 |
| Peripherals | 16-bit 8-bit 8-bit SFR | 0x01FF - 0x0100 0x00FF - 0x0010 0x000F - 0x0000 |

Flash Memory

The flash memory can be programmed by the Spy-Bi-Wire or JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* ([SLAU144](#)).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF (VLOCLK) oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

NOTE

The LFXT1 oscillator is not available. LFXT1Sx bits of the BCSCTL3 register should be configured to use VLOCLK (see the *MSP430x2xx Family User's Guide* ([SLAU144](#))).

Table 9. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

| DCO FREQUENCY | CALIBRATION REGISTER | SIZE | ADDRESS |
|---------------|----------------------|------|---------|
| 1 MHz | CALBC1_1MHZ | byte | 010FFh |
| | CALDCO_1MHZ | byte | 010FEh |
| 8 MHz | CALBC1_8MHZ | byte | 010FDh |
| | CALDCO_8MHZ | byte | 010FCh |
| 12 MHz | CALBC1_12MHZ | byte | 010FBh |
| | CALDCO_12MHZ | byte | 010FAh |
| 16 MHz | CALBC1_16MHZ | byte | 010F9h |
| | CALDCO_16MHZ | byte | 010F8h |

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are four pins of one 8-bit I/O port implemented—port P1:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the four bits of port P1.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 10. Timer_A2 Signal Connections

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|---------------------|------------------------|----------------------|-----------------|----------------------------|----------------------|
| D | | | | | D |
| - | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| - | TACLK | INCLK | | | |
| - | TA0 | CCI0A | CCR0 | TA0 | |
| | ACLK (internal) | CCI0B | | | |
| | V _{SS} | GND | | | |
| | V _{CC} | V _{CC} | | | |
| 2 - P1.2 | TA1 | CCI1A | CCR1 | TA1 | 2 - P1.2 |
| 4 - P1.6 | TA1 | CCI1B | | | 4 - P1.6 |
| | V _{SS} | GND | | | |
| | V _{CC} | V _{CC} | | | |

USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 11. Peripherals With Word Access

| | | | |
|------------------------|---|--|---|
| ADC10 | ADC control 0 ADC10 control 1 ADC memory | ADC10CTL0 ADC10CTL1 ADC10MEM | 01B0h 01B2h 01B4h |
| Timer_A | Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector | TACCR1 TACCR0 TAR TACCTL1 TACCTL0 TACTL TAIV | 0174h 0172h 0170h 0164h 0162h 0160h 012Eh |
| Flash Memory | Flash control 3 Flash control 2 Flash control 1 | FCTL3 FCTL2 FCTL1 | 012Ch 012Ah 0128h |
| Watchdog Timer+ | Watchdog/timer control | WDTCTL | 0120h |

Table 12. Peripherals With Byte Access

| | | | |
|----------------------------|---|--|--|
| ADC10 | Analog Enable | ADC10AE | 04Ah |
| USI | USI control 0 USI control 1 USI clock control USI bit counter USI shift register | USICTL0 USICTL1 USICKCTL USICNT USISR | 078h 079h 07Ah 07Bh 07Ch |
| Basic Clock System+ | Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control | BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL | 053h 058h 057h 056h |
| Port P1 | Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input | P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN | 027h 026h 025h 024h 023h 022h 021h 020h |
| Special Function | SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1 | IFG2 IFG1 IE2 IE1 | 003h 002h 001h 000h |

Absolute Maximum Ratings⁽¹⁾

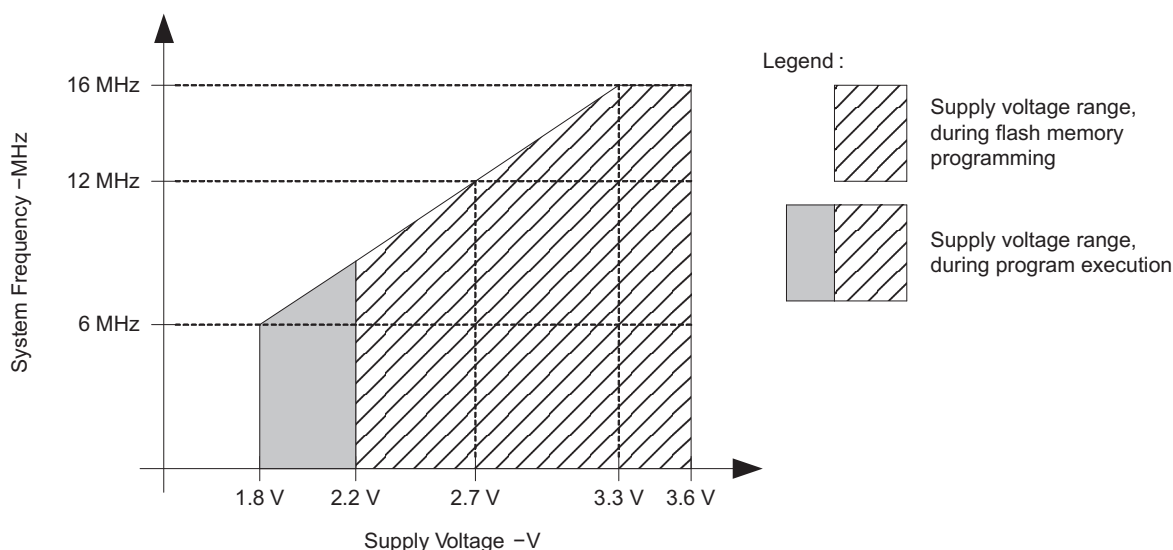
| | | | |
|---|------------------------------------|-----------------------------------|----------------|
| Voltage applied at V _{CC} to V _{SS} | | -0.3 V to 4.1 V | |
| Voltage applied to any pin ⁽²⁾ | | -0.3 V to V _{CC} + 0.3 V | |
| Diode current at any device terminal | | ±2 mA | |
| T _{stg} | Storage temperature ⁽³⁾ | Unprogrammed device | -55°C to 150°C |
| | | Programmed device | -40°C to 150°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

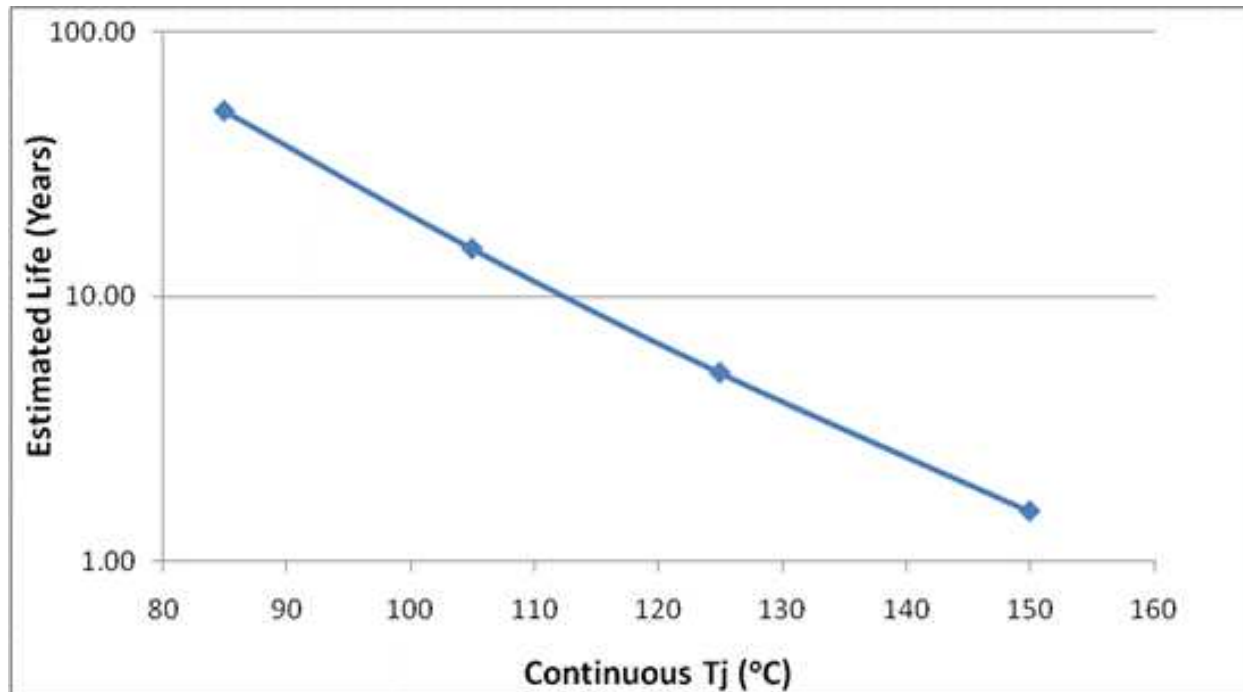
| | | | MIN | NOM | MAX | UNIT |
|---------------------|--|--|-----|-----|-----|------|
| V _{CC} | Supply voltage | During program execution | 1.8 | | 3.6 | V |
| | | During flash program/erase | 2.2 | | 3.6 | |
| V _{SS} | Supply voltage | | | 0 | | V |
| T _A | Operating free-air temperature | | -40 | | 125 | °C |
| f _{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽¹⁾⁽²⁾ | V _{CC} = 1.8 V, Duty cycle = 50% ± 10% | dc | | 6 | MHz |
| | | V _{CC} = 2.7 V, Duty cycle = 50% ± 10% | dc | | 12 | |
| | | V _{CC} ≥ 3.3 V, Duty cycle = 50% ± 10% | dc | | 16 | |

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 3. Safe Operating Area



- See data sheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at 110°C junction temperature (does not include package interconnect life).
- The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 4. Operating Life Derating Chart

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | MSP430G2230 | UNITS |
|-------------------------------|---|-------------|-------|
| | | D | |
| | | 8 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 101.2 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 42.3 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 42.9 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 4.0 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 42.2 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | N/A | |

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|---|-------|----------|-----|-----|-----|---------------|
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$, $f_{ACLK} = 0\text{ Hz}$, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 2.2 V | | 220 | | μA |
| | | | 3 V | | 300 | 390 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

Typical Characteristics – Active Mode Supply Current (Into V_{CC})

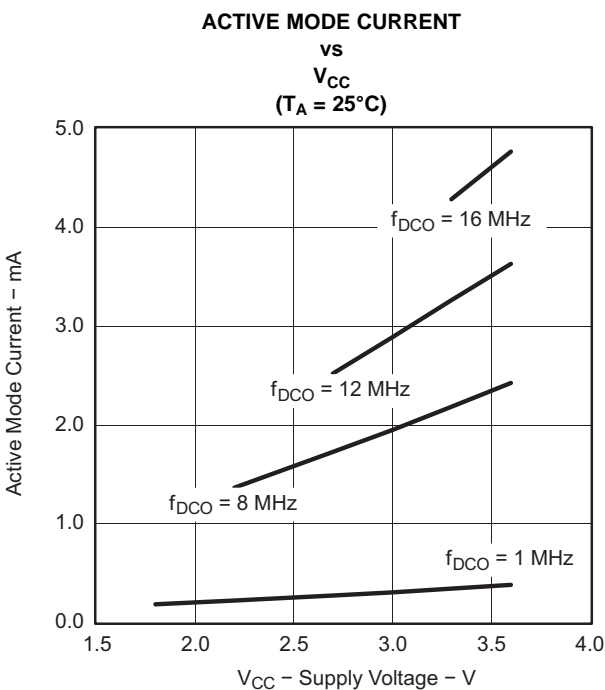


Figure 5.

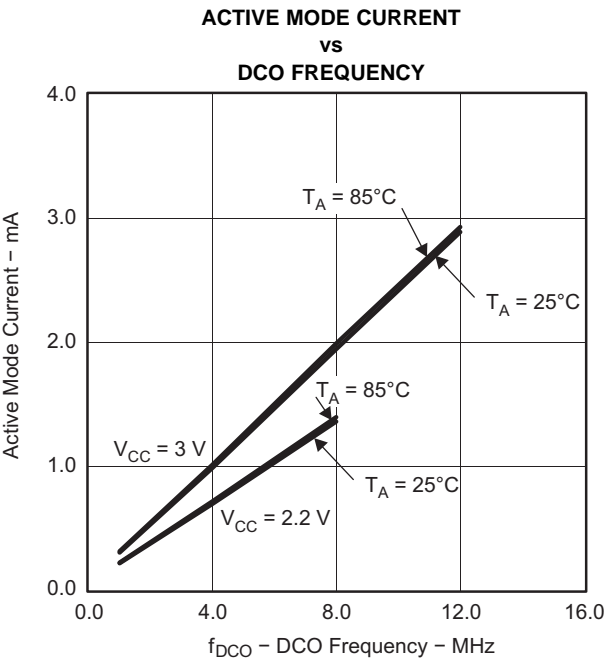


Figure 6.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|--|-------|----------|-----|-----|-----|---------|
| $I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current ⁽²⁾ | $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 25°C | 2.2 V | | 65 | | μA |
| I_{LPM2} Low-power mode 2 (LPM2) current ⁽³⁾ | $f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 22 | 29 | μA |
| | | 125°C | | | | 46 | |
| $I_{LPM3,VLO}$ Low-power mode 3 (LPM3) current ⁽³⁾ | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.5 | 0.7 | μA |
| | | 125°C | | | 2 | 9.3 | |
| I_{LPM4} Low-power mode 4 (LPM4) current ⁽⁴⁾ | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | 25°C | 2.2 V | | 0.1 | 0.5 | μA |
| | | 85°C | | | 0.8 | 1.5 | |
| | | 125°C | | | 2 | 7.1 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Current for brownout and WDT clocked by SMCLK included.

(3) Current for brownout and WDT clocked by ACLK included.

(4) Current for brownout included.

Schmitt-Trigger Inputs (Port P1)

over recommended ranges of supply voltage and up to operating free-air temperature, $T_A = 105^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--|--|----------|---------------|-----|---------------|------------|
| V_{IT+} Positive-going input threshold voltage | | | 0.45 V_{CC} | | 0.75 V_{CC} | V |
| | | 3 V | 1.35 | | 2.25 | |
| V_{IT-} Negative-going input threshold voltage | | | 0.25 V_{CC} | | 0.55 V_{CC} | V |
| | | 3 V | 0.75 | | 1.65 | |
| V_{hys} Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 3 V | 0.3 | | 1.0 | V |
| R_{Pull} Pullup/pulldown resistor | For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | k Ω |
| C_I Input capacitance | $V_{IN} = V_{SS}$ or V_{CC} | | | 5 | | pF |

Leakage Current (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | MAX | UNIT |
|---|-----------------|----------|-----|-----------|------|
| $I_{lkg}(P_{x,y})$ High-impedance leakage current | | 3 V | | ± 120 | nA |

Outputs (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|------------------------------------|-------------------------------------|----------|-----|----------------|-----|------|
| V_{OH} High-level output voltage | $I_{(OHmax)} = -6 \text{ mA}^{(1)}$ | 3 V | | $V_{CC} - 0.3$ | | V |
| V_{OL} Low-level output voltage | $I_{(OLmax)} = 6 \text{ mA}^{(1)}$ | 3 V | | $V_{SS} + 0.3$ | | V |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed $\pm 48 \text{ mA}$ to hold the maximum voltage drop specified.

Output Frequency (Port P1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--|---|----------|-----|-----|-----|------|
| $f_{Px,y}$ Port output frequency (with load) | $C_L = 20 \text{ pF}$, $R_L = 1 \text{ k}\Omega^{(1) (2)}$ | 3 V | | 12 | | MHz |
| f_{Port^*CLK} Clock output frequency | $C_L = 20 \text{ pF}^{(2)}$ | 3 V | | 16 | | MHz |

(1) A resistive divider with two 0.5-k Ω resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

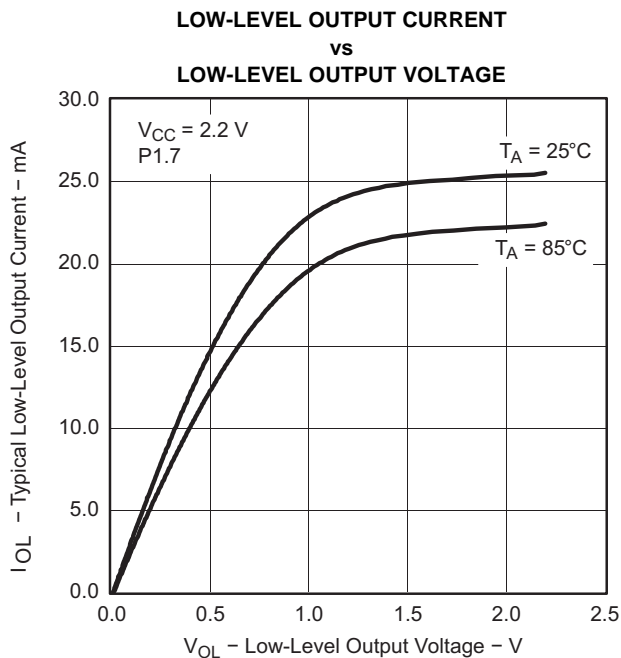


Figure 7.

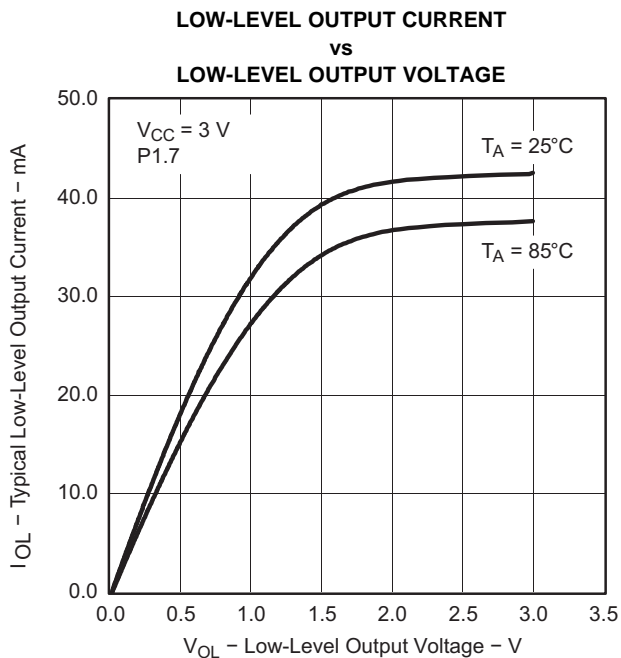


Figure 8.

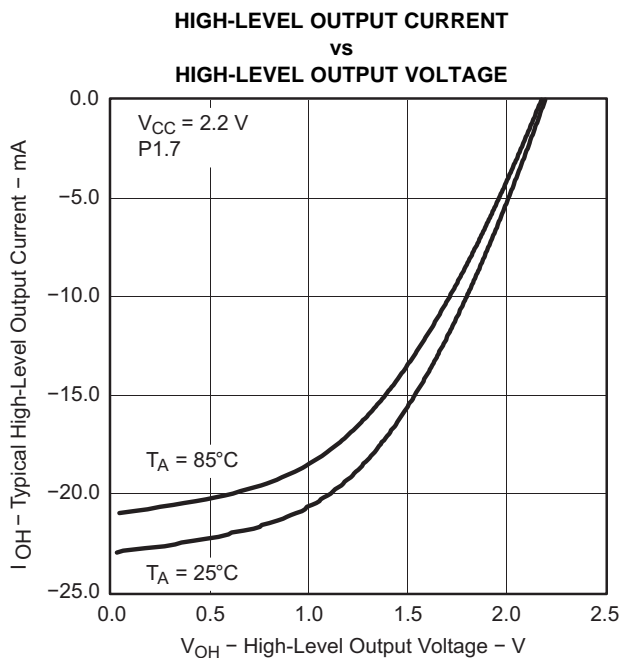


Figure 9.

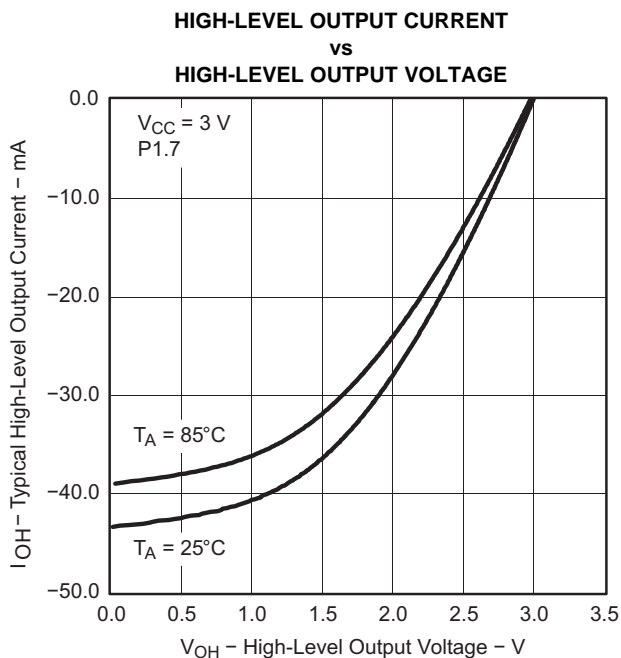


Figure 10.

POR/Brownout Reset (BOR)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|------------------------------|-----|----------------------------|------|------|
| V _{CC(start)} | See Figure 11 | dV _{CC} /dt ≤ 3 V/s | | 0.7 × V _(B_IT-) | | V |
| V _(B_IT-) | See Figure 11 through Figure 13 | dV _{CC} /dt ≤ 3 V/s | | 1.35 | 1 | V |
| V _{hys(B_IT-)} | See Figure 11 | dV _{CC} /dt ≤ 3 V/s | | 140 | | mV |
| t _{d(BOR)} | See Figure 11 | See (2) | | | 2000 | μs |
| t _(reset) | Pulse length needed at $\overline{\text{RST}}$ /NMI pin to accept reset internally | See (2) | 3 V | 2 | | μs |

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.

(2) Minimum and maximum parameters are characterized up to T_A = 105°C unless otherwise noted.

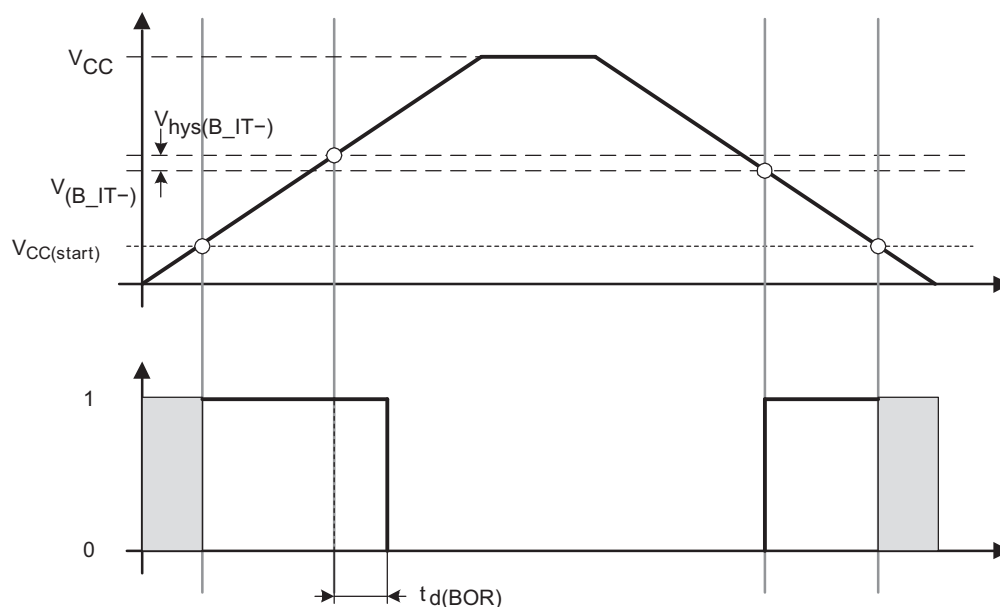


Figure 11. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics – POR/Brownout Reset (BOR)

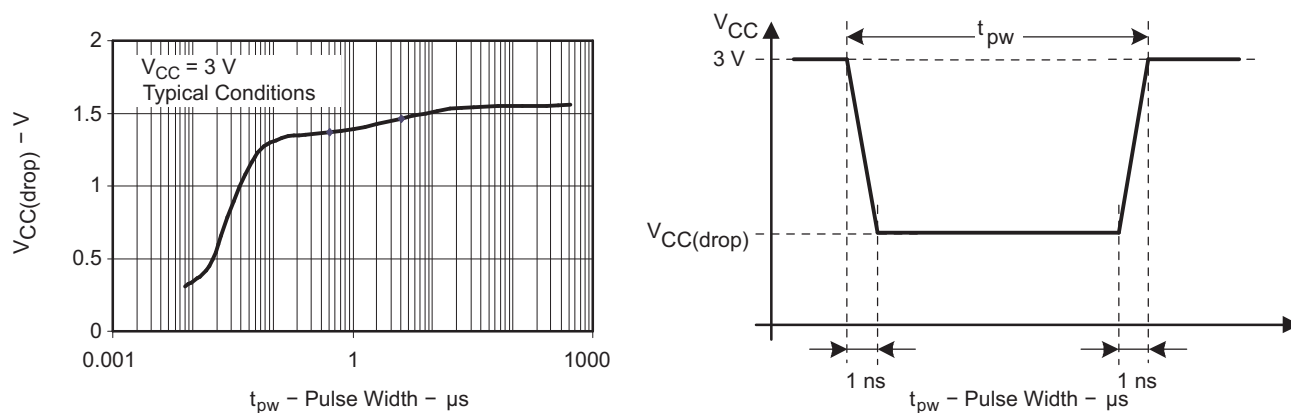


Figure 12. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

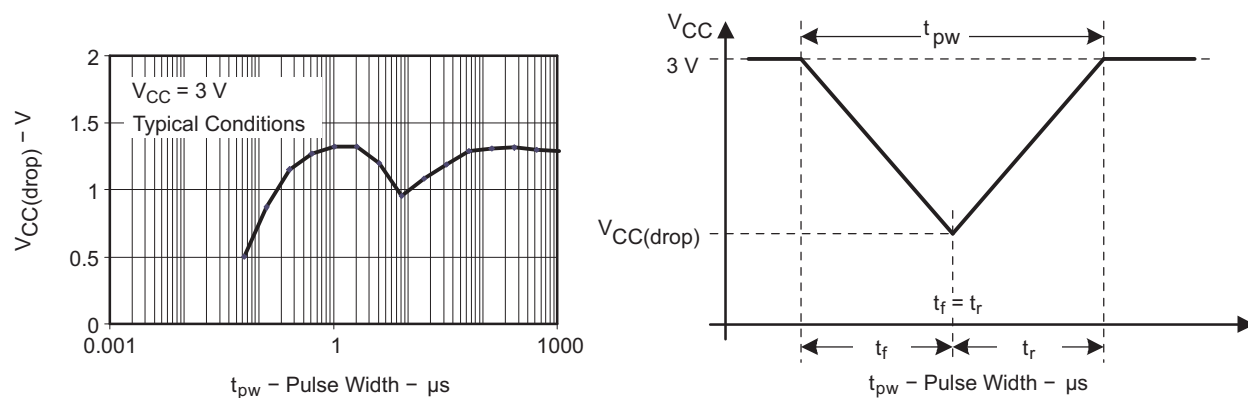


Figure 13. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often f_{DCO(RSEL,DCO+1)} is used within the period of 32 DCOCLK cycles. The frequency f_{DCO(RSEL,DCO)} is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|-------|------|-------|
| V _{CC} | Supply voltage | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | |
| | | RSELx = 15 | | 3.0 | | 3.6 | |
| f _{DCO(0,0)} | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 3 V | | 0.096 | | MHz |
| f _{DCO(0,3)} | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 3 V | | 0.12 | | MHz |
| f _{DCO(1,3)} | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 3 V | | 0.15 | | MHz |
| f _{DCO(2,3)} | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 3 V | | 0.21 | | MHz |
| f _{DCO(3,3)} | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 3 V | | 0.30 | | MHz |
| f _{DCO(4,3)} | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 3 V | | 0.41 | | MHz |
| f _{DCO(5,3)} | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 3 V | | 0.58 | | MHz |
| f _{DCO(6,3)} | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 3 V | | 0.80 | | MHz |
| f _{DCO(7,3)} | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 3 V | 0.80 | | 1.50 | MHz |
| f _{DCO(8,3)} | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 3 V | | 1.6 | | MHz |
| f _{DCO(9,3)} | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 3 V | | 2.3 | | MHz |
| f _{DCO(10,3)} | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 3 V | | 3.4 | | MHz |
| f _{DCO(11,3)} | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 3 V | | 4.25 | | MHz |
| f _{DCO(12,3)} | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 3 V | 4.3 | | 7.30 | MHz |
| f _{DCO(13,3)} | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 3 V | | 7.8 | | MHz |
| f _{DCO(14,3)} | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 3 V | 8.6 | | 13.9 | MHz |
| f _{DCO(15,3)} | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3 V | | 15.25 | | MHz |
| f _{DCO(15,7)} | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3 V | | 21 | | MHz |
| S _{RSEL} | Frequency step between range RSEL and RSEL+1 | S _{RSEL} = f _{DCO(RSEL+1,DCO)} /f _{DCO(RSEL,DCO)} | 3 V | | 1.35 | | ratio |
| S _{DCO} | Frequency step between tap DCO and DCO+1 | S _{DCO} = f _{DCO(RSEL,DCO+1)} /f _{DCO(RSEL,DCO)} | 3 V | | 1.08 | | ratio |
| Duty cycle | | | 3 V | | 50 | | % |

Calibrated DCO Frequencies - Tolerance Over Temperature -40°C to 125°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|----------------|-----------------|-----|------|-----|------|
| 1-MHz tolerance over temperature | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | -40°C to 125°C | 3 V | -3 | ±0.5 | 3 | % |
| 8-MHz tolerance over temperature | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | -40°C to 125°C | 3 V | -3 | ±1.0 | 3 | % |
| 12-MHz tolerance over temperature | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | -40°C to 125°C | 3 V | -3 | ±1.0 | 3 | % |
| 16-MHz tolerance over temperature | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | -40°C to 125°C | 3 V | -3 | ±2.0 | 3 | % |

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|----------------|-----------------|-----|-----|-----|------|
| 1-MHz tolerance over V _{CC} | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 8-MHz tolerance over V _{CC} | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 12-MHz tolerance over V _{CC} | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | 25°C | 2.2 V to 3.6 V | -3 | ±2 | +3 | % |
| 16-MHz tolerance over V _{CC} | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | 25°C | 3 V to 3.6 V | -6 | ±2 | +3 | % |

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|--|----------------|-----------------|-----|-----|-----|------|
| 1-MHz tolerance overall | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 8-MHz tolerance overall | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 12-MHz tolerance overall | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 2.2 V to 3.6 V | -5 | ±2 | +5 | % |
| 16-MHz tolerance overall | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 3 V to 3.6 V | -6 | ±3 | +6 | % |

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|-----|---|-----|---------------|
| $t_{\text{DCO,LPM3/4}}$ DCO clock wake-up time from LPM3/4 ⁽¹⁾ | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ | 2.2 V/3 V | | 2 | | μs |
| | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ | | | 1.5 | | |
| | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ | | | 1 | | |
| | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ | 3 V | | 1 | | |
| $t_{\text{CPU,LPM3/4}}$ CPU wake-up time from LPM3/4 ⁽²⁾ | | | | $1 / f_{\text{MCLK}} + t_{\text{Clock,LPM3/4}}$ | | |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

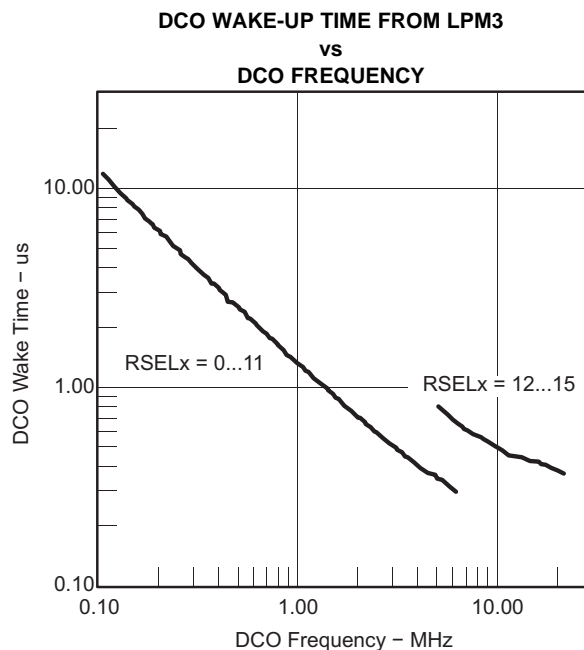


Figure 14.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---|----------------|-----------------|-----|-----|-----|------|
| f _{VLO} VLO frequency | -40°C to 85°C | 3 V | 4 | 12 | 20 | kHz |
| | 125°C | | | | 23 | |
| df _{VLO} /dT VLO frequency temperature drift ⁽¹⁾ | -40°C to 85°C | 3 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} VLO frequency supply voltage drift ⁽²⁾ | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|---------------------|-----|------|
| f _{TA} Timer_A clock frequency | Internal: SMCLK External: TACLK, INCLK Duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz |
| t _{TA,cap} Timer_A capture timing | TAx | 3 V | 20 | | | ns |

USI, Universal Serial Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----------------|---------------------|-----------------------|------|
| f _{USI} USI clock frequency | External: SCLK, Duty cycle = 50% ±10%, SPI slave mode USI module in I ² C mode, I _(OLmax) = 1.5 mA | | | f _{SYSTEM} | | MHz |
| V _{OL,I2C} Low-level output voltage on SDA and SCL | | 3 V | V _{SS} | | V _{SS} + 0.4 | V |

Typical Characteristics, USI Low-Level Output Voltage on SDA and SCL

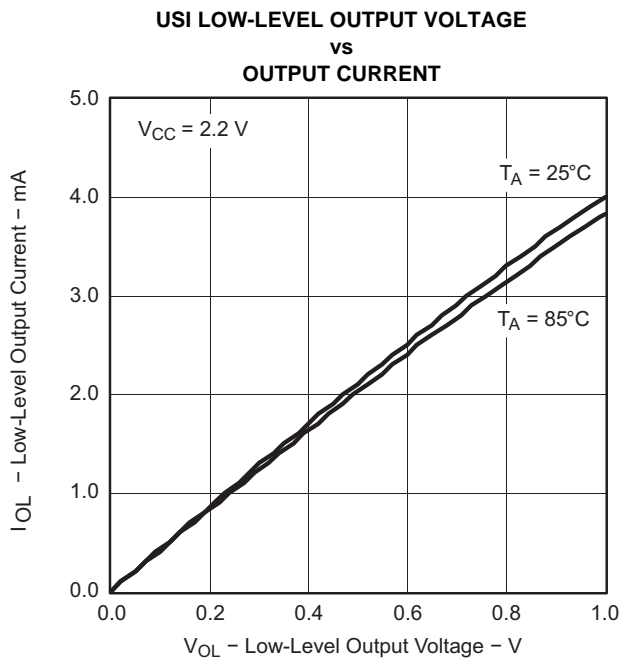


Figure 15.

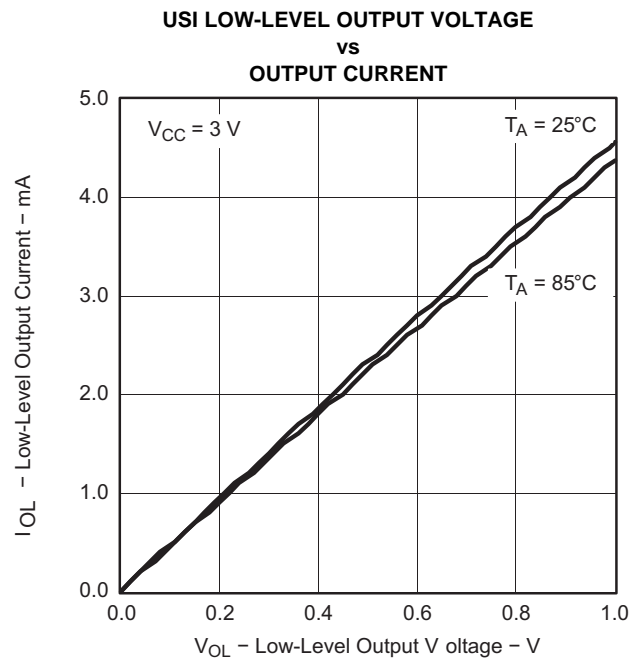


Figure 16.

10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----|------|-----------------|------|
| V _{CC} | Analog supply voltage | V _{SS} = 0 V | 2.2 | | 3.6 | V |
| V _{Ax} | Analog input voltage ⁽²⁾ | All Ax terminals, Analog inputs selected in ADC10AE register | 3 V | 0 | V _{CC} | V |
| I _{ADC10} | ADC10 supply current ⁽³⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0 | 3 V | 0.6 | | mA |
| I _{REF+} | Reference supply current, reference buffer disabled ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0 | 3 V | 0.25 | | mA |
| | | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0 | | 0.25 | | |
| I _{REFB,0} | Reference buffer supply current with ADC10SR = 0 ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0 | 3 V | 1.1 | | mA |
| I _{REFB,1} | Reference buffer supply current with ADC10SR = 1 ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1 | 3 V | 0.5 | | mA |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time | 3 V | | 27 | pF |
| R _I | Input MUX ON resistance | 0 V ≤ V _{Ax} ≤ V _{CC} | 3 V | 1000 | | Ω |

(1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.

(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.

(4) The internal reference current is supplied by terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|-----------------|------|-----|------|--------|
| V _{CC,REF+} | Positive built-in reference analog supply voltage range I _{VREF+} ≤ 1 mA, REF2_5V = 0 | | 2.2 | | | V |
| | I _{VREF+} ≤ 1 mA, REF2_5V = 1 | | 3 | | | |
| V _{REF+} | Positive built-in reference voltage I _{VREF+} ≤ I _{VREF+} max, REF2_5V = 0 | 3 V | 1.4 | 1.5 | 1.59 | V |
| | I _{VREF+} ≤ I _{VREF+} max, REF2_5V = 1 | | 2.34 | 2.5 | 2.65 | |
| I _{LD,VREF+} | Maximum VREF+ load current See ⁽¹⁾ | 3 V | | | ±1 | mA |
| VREF+ load regulation | I _{VREF+} = 500 µA ± 100 µA, Analog input voltage V _{AX} ≠ 0.75 V, REF2_5V = 0 | 3 V | | | ±2 | LSB |
| | I _{VREF+} = 500 µA ± 100 µA, Analog input voltage V _{AX} ≠ 1.25 V, REF2_5V = 1 | | | | ±2 | |
| VREF+ load regulation response time | I _{VREF+} = 100 µA → 900 µA, V _{AX} ≠ 0.5 × VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0 ⁽¹⁾ | 3 V | | | 400 | ns |
| C _{VREF+} | Maximum capacitance at pin VREF+ I _{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1 ⁽¹⁾ | 3 V | | | 100 | pF |
| TC _{REF+} | Temperature coefficient I _{VREF+} = const with 0 mA ≤ I _{VREF+} ≤ 1 mA | 3 V | | | ±190 | ppm/°C |
| t _{REFON} | Settling time of internal reference voltage to 99.9% VREF I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1 ⁽¹⁾ | 3.6 V | | | 30 | µs |
| t _{REFBURST} | Settling time of reference buffer to 99.9% VREF I _{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0 ⁽¹⁾ | 3 V | | | 2 | µs |

(1) Minimum and maximum parameters are characterized up to T_A = 105°C, unless otherwise noted.

10-Bit ADC, External Reference⁽¹⁾

over recommended ranges of supply voltage and up to operating free-air temperature, $T_A = 105^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|----------|-----|-----|----------|------|
| VEREF+ | Positive external reference input voltage range ⁽²⁾ | VEREF+ > VREF–, SREF1 = 1, SREF0 = 0 | | 1.4 | | V_{CC} | V |
| | | VEREF– ≤ VREF+ ≤ $V_{CC} - 0.15\text{ V}$, SREF1 = 1, SREF0 = 1 ⁽³⁾ | | 1.4 | | 3 | |
| VEREF– | Negative external reference input voltage range ⁽⁴⁾ | VEREF+ > VREF– | | 0 | | 1.2 | V |
| ΔVEREF | Differential external reference input voltage range, $\Delta\text{VEREF} = \text{VEREF+} - \text{VEREF-}$ | VEREF+ > VREF– ⁽⁵⁾ | | 1.4 | | V_{CC} | V |
| $I_{\text{VEREF+}}$ | Static input current into VREF+ | $0\text{ V} \leq \text{VEREF+} \leq V_{CC}$, SREF1 = 1, SREF0 = 0 | 3 V | | ±1 | | μA |
| | | $0\text{ V} \leq \text{VEREF+} \leq V_{CC} - 0.15\text{ V} \leq 3\text{ V}$, SREF1 = 1, SREF0 = 1 ⁽³⁾ | 3 V | | 0 | | |
| $I_{\text{VEREF-}}$ | Static input current into VREF– | $0\text{ V} \leq \text{VEREF-} \leq V_{CC}$ | 3 V | | ±1 | | μA |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB} . The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and up to operating free-air temperature, $T_A = 105^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|-------------------------------------|--|-------------|-----------------|---|-----|------|------|
| f _{ADC10CLK} | ADC10 input clock frequency | For specified performance of ADC10 linearity parameters | ADC10SR = 0 | 3 V | 0.45 | | 6.3 | MHz |
| | | | ADC10SR = 1 | | 0.45 | | 1.5 | |
| f _{ADC10OSC} | ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | | 3 V | 3.7 | | 6.3 | MHz |
| t _{CONVERT} | Conversion time | ADC10 built-in oscillator, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | | 3 V | 2.06 | | 3.51 | μs |
| | | f _{ADC10CLK} from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0 | | | 13 × ADC10DIV × 1/f _{ADC10CLK} | | | |
| t _{ADC10ON} | Turn-on settling time of the ADC | (1) | | | | | 100 | ns |

- (1) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and up to operating free-air temperature, $T_A = 105^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------|--------------------------------------|----------|-----|------|-----|------|
| E_I | Integral linearity error | | 3 V | | | ±1 | LSB |
| E_D | Differential linearity error | | 3 V | | | ±1 | LSB |
| E_O | Offset error | Source impedance $R_S < 100\ \Omega$ | 3 V | | | ±1 | LSB |
| E_G | Gain error | | 3 V | | ±1.1 | ±2 | LSB |
| E_T | Total unadjusted error | | 3 V | | ±2 | ±5 | LSB |

10-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|---|--|-----|------|-----|-------|
| I _{SENSOR} | Temperature sensor supply current ⁽¹⁾ | REFON = 0, INCHx = 0Ah, T _A = 25°C | 3 V | 60 | | μA |
| TC _{SENSOR} | | ADC10ON = 1, INCHx = 0Ah ⁽²⁾ | 3 V | 3.55 | | mV/°C |
| t _{Sensor(sample)} | Sample time required if channel 10 is selected ⁽³⁾ | ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB | 3 V | 30 | | μs |
| I _{VMID} | Current into divider at channel 11 | ADC10ON = 1, INCHx = 0Bh | 3 V | | (4) | μA |
| V _{MID} | V _{CC} divider at channel 11 | ADC10ON = 1, INCHx = 0Bh, V _{MID} ≠ 0.5 × V _{CC} | 3 V | 1.5 | | V |
| t _{VMID(sample)} | Sample time required if channel 11 is selected ⁽⁵⁾ | ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB | 3 V | 1220 | | ns |

- (1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
- (2) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}]$$

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$$
- (3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (4) No additional current is needed. The V_{MID} is used during sampling.
- (5) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.

Flash Memory⁽¹⁾

over recommended ranges of supply voltage and up to operating free-air temperature, T_A = 105°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|--------------------------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | 2.2 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from V _{CC} during program | 3 V | | 1 | 5 | mA |
| I _{ERASE} | Supply current from V _{CC} during erase | 3 V | | 1 | 7 | mA |
| t _{CPT} | Cumulative program time ⁽²⁾ | 2.2 V/3.6 V | | | 10 | ms |
| t _{CMErase} | Cumulative mass erase time | 2.2 V/3.6 V | 20 | | | ms |
| | Program/erase endurance | -40°C ≤ T _J ≤ 105°C | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 15 | | | years |
| t _{Word} | Word or byte program time | See ⁽³⁾ | | 30 | | t _{FTG} |
| t _{Block, 0} | Block program time for first byte or word | See ⁽³⁾ | | 25 | | t _{FTG} |
| t _{Block, 1-63} | Block program time for each additional byte or word | See ⁽³⁾ | | 18 | | t _{FTG} |
| t _{Block, End} | Block program end-sequence wait time | See ⁽³⁾ | | 6 | | t _{FTG} |
| t _{Mass Erase} | Mass erase time | See ⁽³⁾ | | 10593 | | t _{FTG} |
| t _{Seg Erase} | Segment erase time | See ⁽³⁾ | | 4819 | | t _{FTG} |

- (1) Additional flash retention documentation located in application report [SLAA392](#).
- (2) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- (3) These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----|-----|------|
| V _(RAMh) | RAM retention supply voltage ⁽¹⁾ CPU halted | 1.6 | | V |

- (1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---------------------------------|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | | 2.2 V/3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse length | | 2.2 V/3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge ⁽¹⁾) | T _A = -40°C to 105°C | 2.2 V/3 V | | | 1 | μs |
| t _{SBW,Ret} | Spy-Bi-Wire return to normal operation time | | 2.2 V/3 V | 15 | | 100 | μs |
| R _{Internal} | Internal pulldown resistance on TEST | T _A = -40°C to 105°C | 2.2 V/3 V | 25 | 60 | 90 | kΩ |

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t_{SBW,En} time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.

JTAG Fuse⁽¹⁾

T_A = 25°C, over recommended ranges of supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | | 2.5 | | V |
| V _{FB} | Voltage level on TEST for fuse blow | | 6 | 7 | V |
| I _{FB} | Supply current into TEST during fuse blow | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | 1 | ms |

- (1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 (P1.2) Pin Schematics

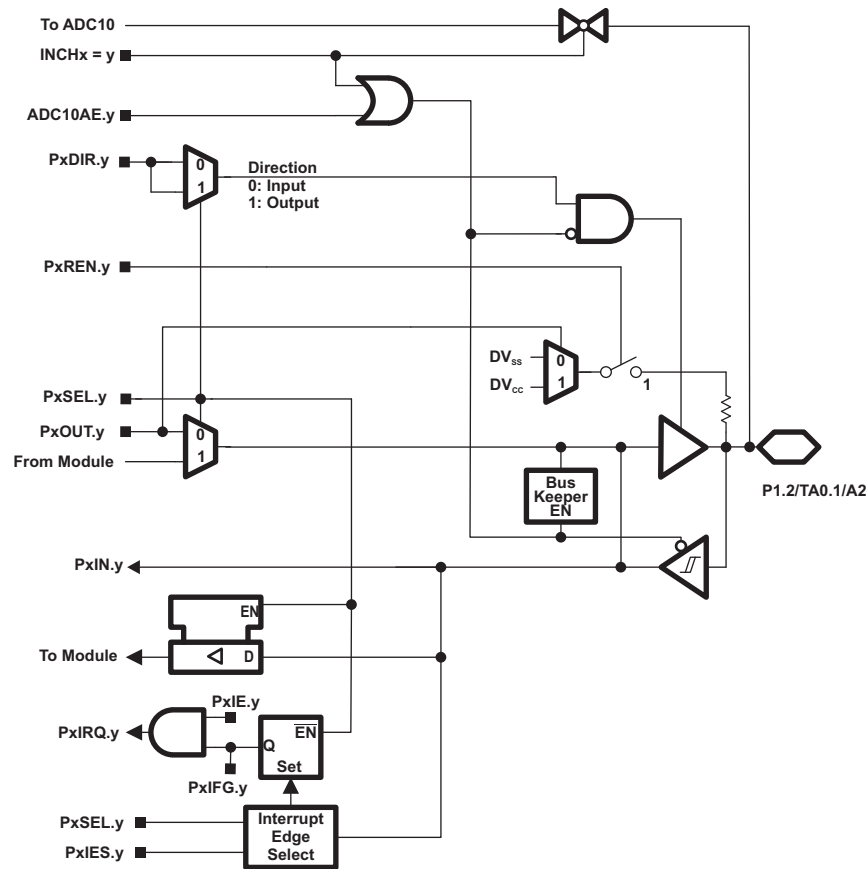


Figure 17.

Table 13. Port P1 (P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|---------------------------------------|---------|---------------------------|
| | | | P1DIR.x | P1SEL.x | ADC10AE.x (INCH.y = 1) |
| P1.2/ TA0.1/ | 2 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.1 | 1 | 1 | 0 |
| | | TA0.CCI1A | 0 | 1 | 0 |
| A2 | | A2 | X | X | 1 (y = 2) |

(1) $X = \text{don't care}$

Port P1 (P1.5) Pin Schematics

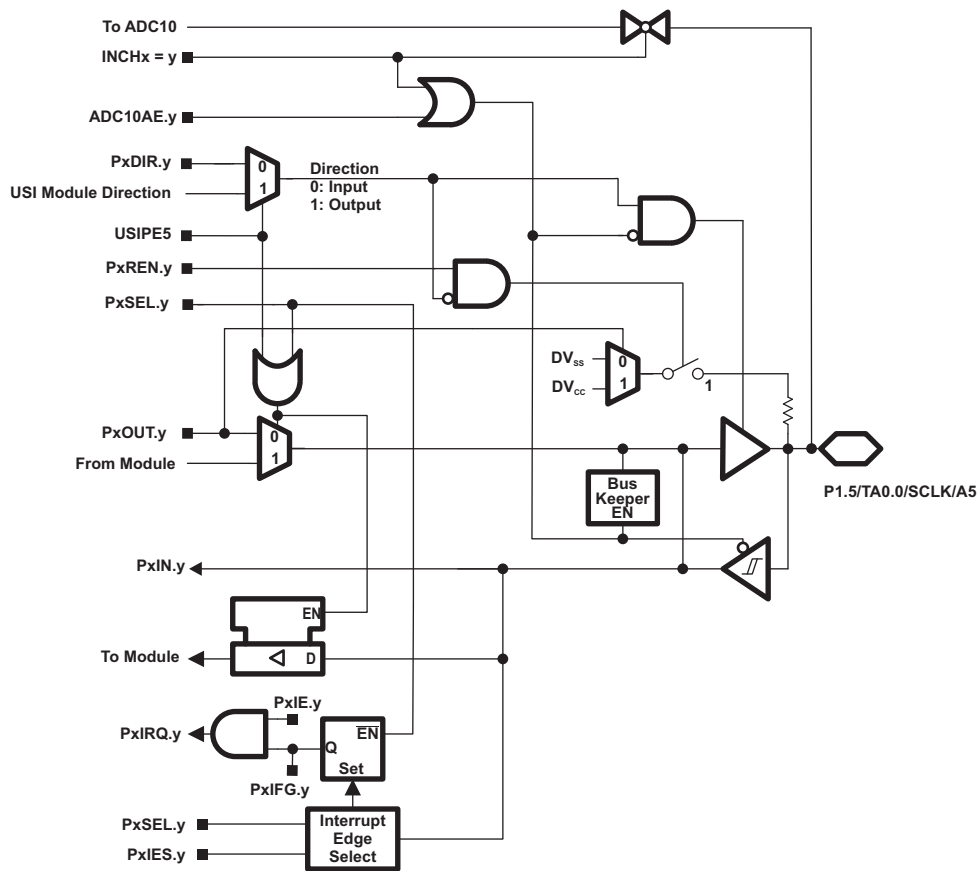


Figure 18.

Table 14. Port P1 (P1.5) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | | |
|--------------------------------|---|------------|---------------------------------------|---------|---------------------------|-------|
| | | | P1DIR.x | P1SEL.x | ADC10AE.x (INCH.y = 1) | INCHx |
| P1.5/ TA0.0/ SCLK/ A5 | 5 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.0 | 1 | 1 | 0 | X |
| | | SCLK | X | X | X | X |
| | | A5 | X | X | 1 (y = 5) | 5 |

(1) X = don't care

Port P1 (P1.6 and 1.7) Pin Schematic

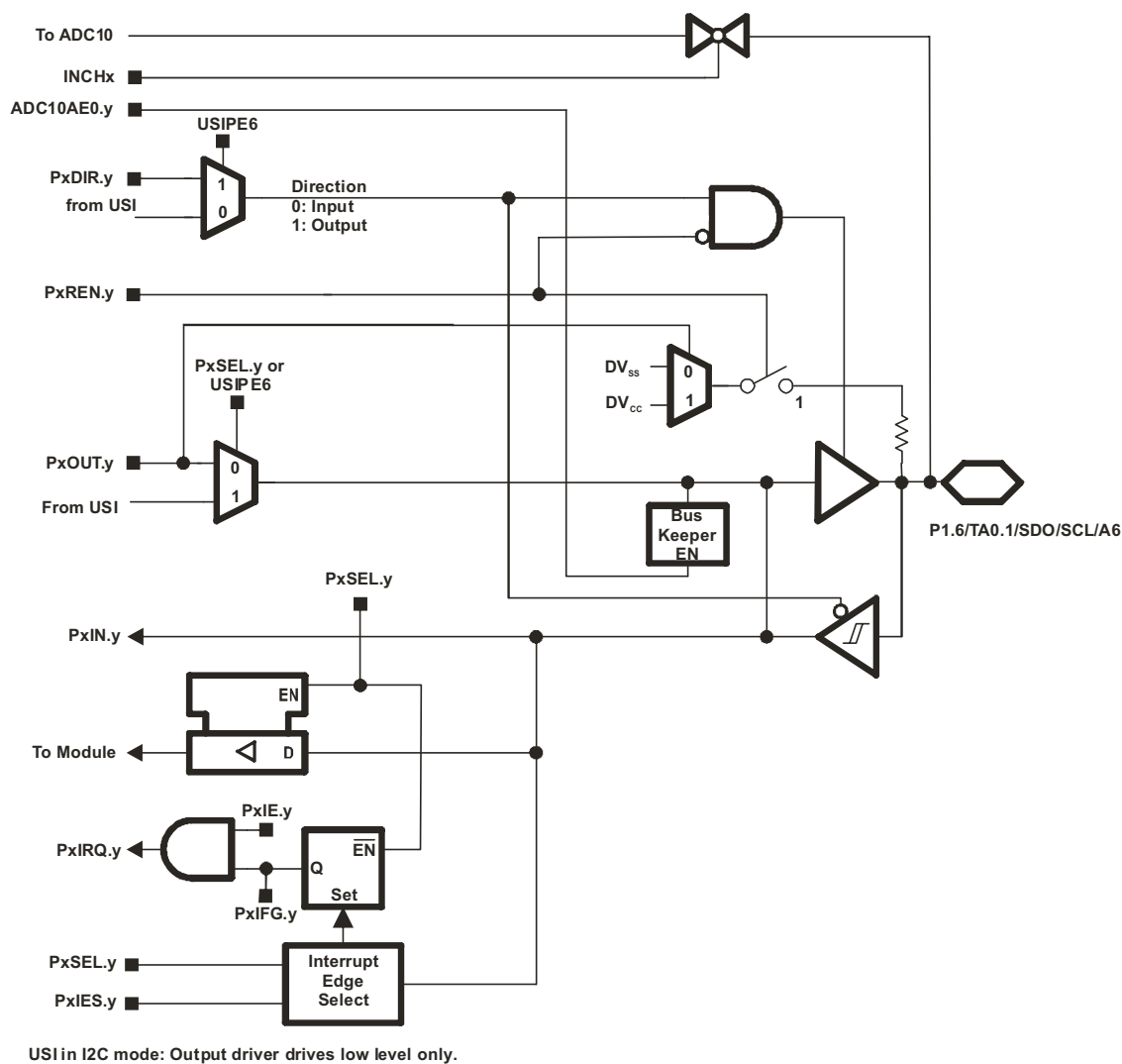


Figure 19.

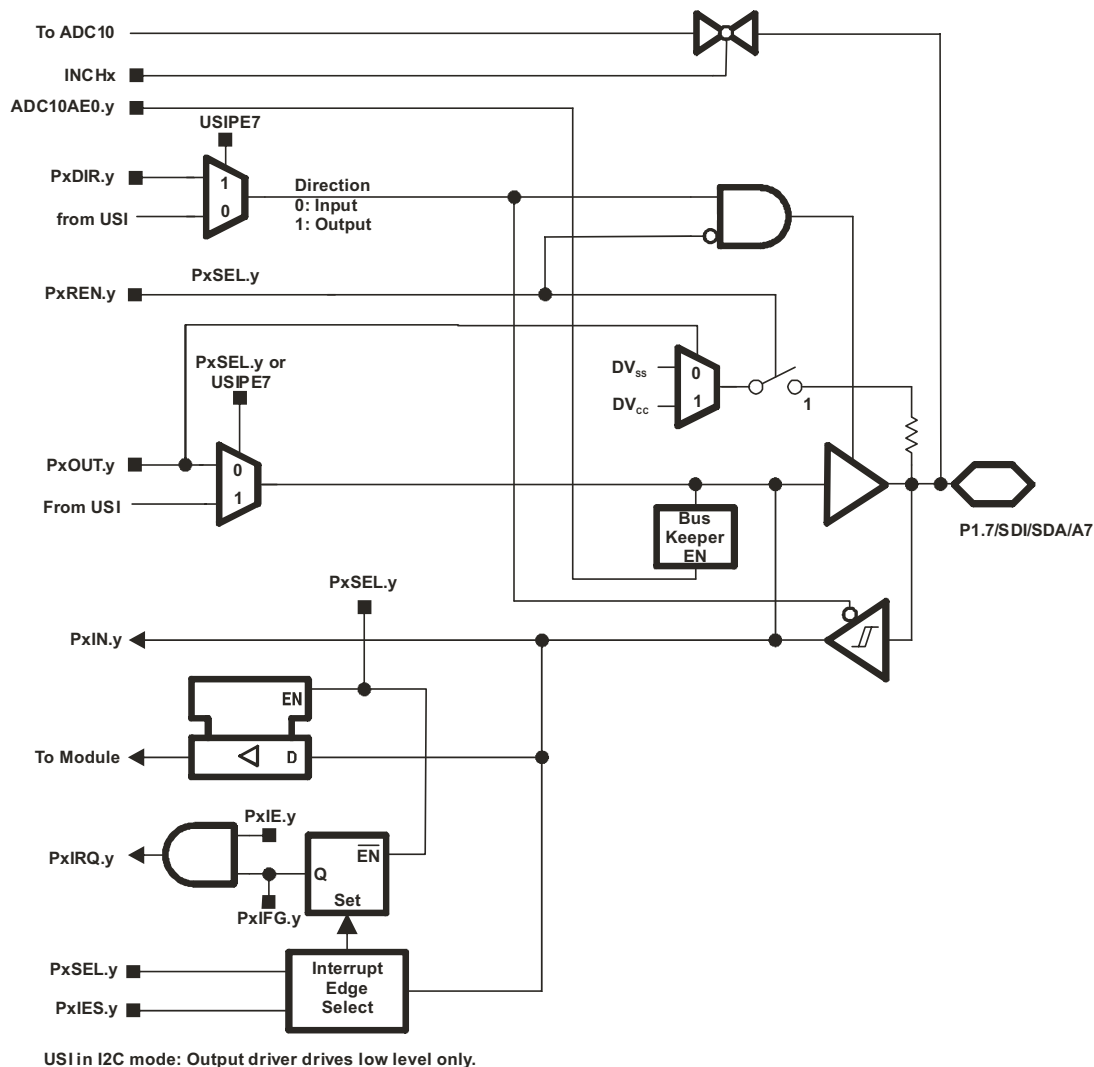


Figure 20.

Table 15. Port P1 (P1.6 and P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS | | | |
|---|---|------------|------------------------|---------|--------|-----------|
| | | | P1DIR.x | P1SEL.x | USIP.x | ADC10AE.x |
| P1.6/ TA0.1/ SDO/ SCL/ A6 | 6 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0.CC1A | 0 | 1 | 0 | 0 |
| | | TA0.1 | 1 | 1 | 0 | 0 |
| | | SPI Mode | from USI | 1 | 1 | 0 |
| | | I2C Mode | from USI | 1 | 1 | 0 |
| | | A6 | X | X | 0 | 1 (y = 6) |
| P1.7/ SDI/ SDA/ A7 | 7 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | SDI | X | 1 | 1 | 0 |
| | | SDA | X | 1 | 1 | 0 |
| | | A7 | X | X | 0 | 1 (y = 7) |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430G2230QDEP | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | G230EP | Samples |
| MSP430G2230QDREP | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | G230EP | Samples |
| V62/12620-01XE | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | G230EP | Samples |
| V62/12620-01XE-T | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | G230EP | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MSP430G2230-EP :

- Catalog: [MSP430G2230](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430G2230QDREP | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430G2230QDREP | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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