5-V TTL-to-Differential PECL Translator

Check for Samples: SN65ELT20

FEATURES

- **1.25-ns Maximum Propagation Delay**
- **Operating Range: V_{CC} = 4.2 V to 5.7 V With GND = 0 V**
- **Flow-Through Pinout Enables Easy Layout**
- **Built-In Temperature Compensation**
- **Drop-In Compatible With MC10ELT20, MC100ELT20**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65ELT20 is a TTL-to-differential PECL translator. It operates on a 5-V supply and ground only. The output is undetermined when the inputs are left floating. The low output skew makes the device an ideal solution for clock or data signal translation.

The SN65ELT20 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 package.

PINOUT ASSIGNMENT

D-8, DGK-8 Package
(Top View)

P0065-04
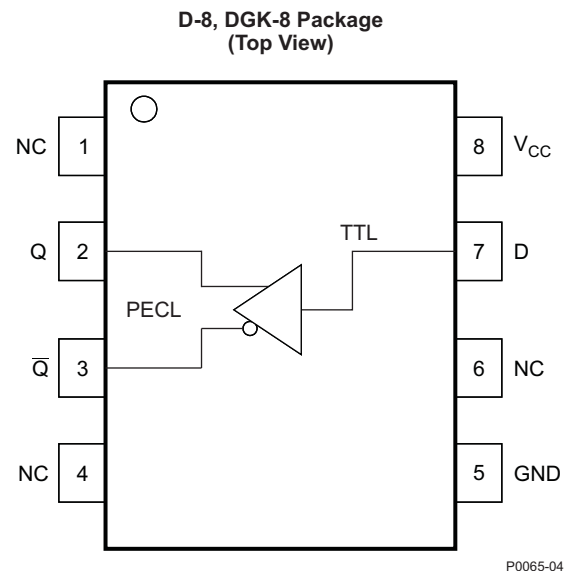
Table 1. Pin Description

PIN	FUNCTION
D	TTL input
Q,$\overline{Q}$	PECL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION[1]

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT20D	SN65ELT20	SOIC	NiPdAu
SN65ELT20DGK	SN65ELT20	SOIC-TSSOP	NiPdAu

(1)   Leaded device options not initially available; contact a sales representative for further details.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[(1)]

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL-mode supply voltage	V_{CC} (GND = 0 V)	6	V
V_{IN} input voltage	GND = 0 V; $V_I \leq V_{CC}$	6	V
Output current	Continuous	50	mA
	Surge	100	mA
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT-BOARD MODEL	POWER RATING $T_A < 25°C$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW	DERATING FACTOR $T_A > 25°C$ (mW/°C)	POWER RATING $T_A = 85°C$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to-case thermal resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTIC	VALUE
Moisture sensitivity level	SO-8: Level 1
	TSSOP-8: Level 3
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD—human body model	>4 kV
ESD—machine model	200 V
ESD—charged-device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

PECL DC CHARACTERISTICS[1] (V_{CC} = 5 V; GND = 0 V)[2]

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power-supply current		9.6	16		10.1	16		10.7	16	mA
V_{OH}	Output HIGH voltage[3]	3915	3958	4120	3915	3963	4120	3915	3967	4120	mV
V_{OL}	Output LOW voltage [3]	3170	3247	3380	3170	3244	3380	3170	3244	3380	mV

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.
(2) Output parameters vary 1:1 with Vcc.
(3) Outputs are terminated through a 50-Ω resistor to V_{CC} – 2 V.

TTL INPUT DC CHARACTERISTICS[1] (V_{CC} = 4.2 V to 5.7 V; T_A = –40°C to 85°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input HIGH current	V_{IN} = 2.7 V			20	μA
I_{IH}		V_{IN} = V_{CC}			20	
I_{IL}	Input LOW current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input clamp diode voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	Input HIGH voltage		2			V
V_{IL}	Input LOW voltage				0.8	V

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.

AC CHARACTERISTICS[1] (V_{CC} = 4.2 V to 5.7 V; GND = 0 V)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency[2] (See Figure 4.)		400			430			430		MHz
t_{PLH}	Propagation delay, 1.5 V to 50% (see Figure 2)	0.9		1.25	0.9		1.25	0.9		1.25	ns
t_{PHL}	Propagation delay, 1.5 V to 50% (see Figure 2)	0.7		1.2	0.7		1.2	0.7		1.2	ns
t_{JITTER}	Random clock jitter (RMS)		0.5			0.5			0.5		ps
t_r/t_f	Q-output rise/fall times (20%–80%) (see Figure 3)	1		1.5	1		1.5	1		1.5	ns

(1) The device meets these specifications after thermal equilibrium has been established when mounted in a test socket or printed-circuit board with maintained transverse airflow greater than 500 lfpm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and are not valid simultaneously.
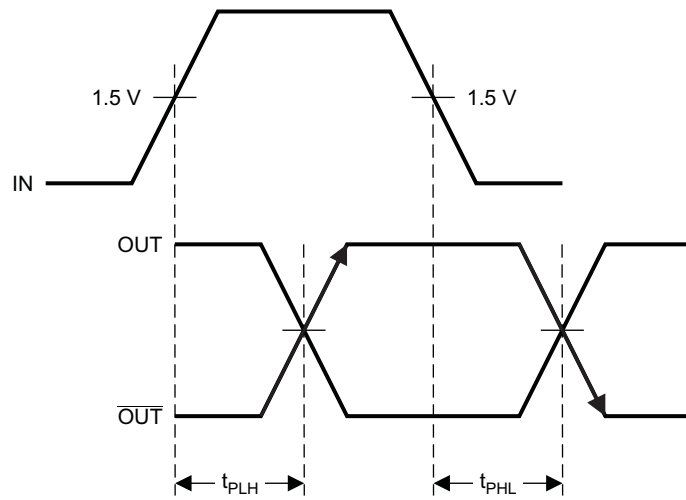(2) Maximum switching frequency is measured at an output amplitude of 300 mV_{PP}.
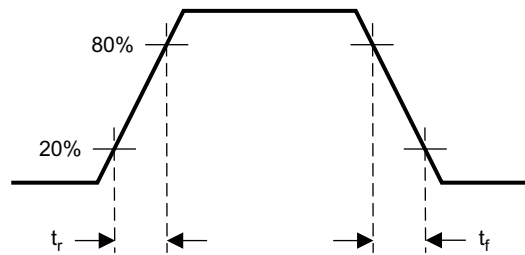
Typical Termination for Output Driver
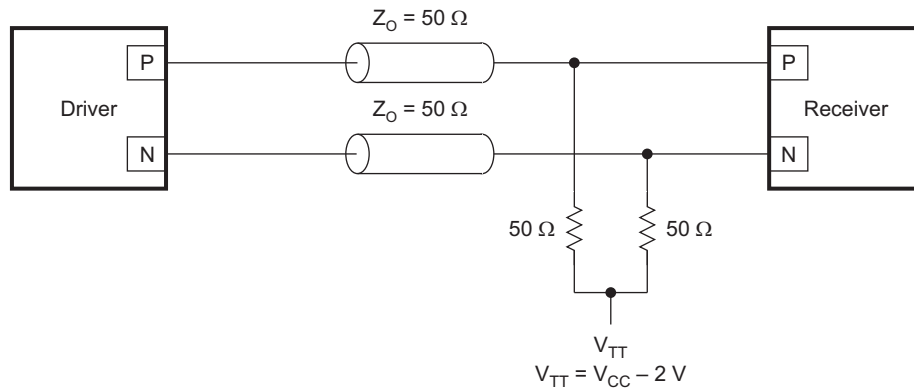
Figure 1. Typical Termination for Output Driver

Figure 2. Output Propagation Delay

Figure 3. Output Rise and Fall Times

OUTPUT AMPLITUDE
vs
FREQUENCY

Figure 4.

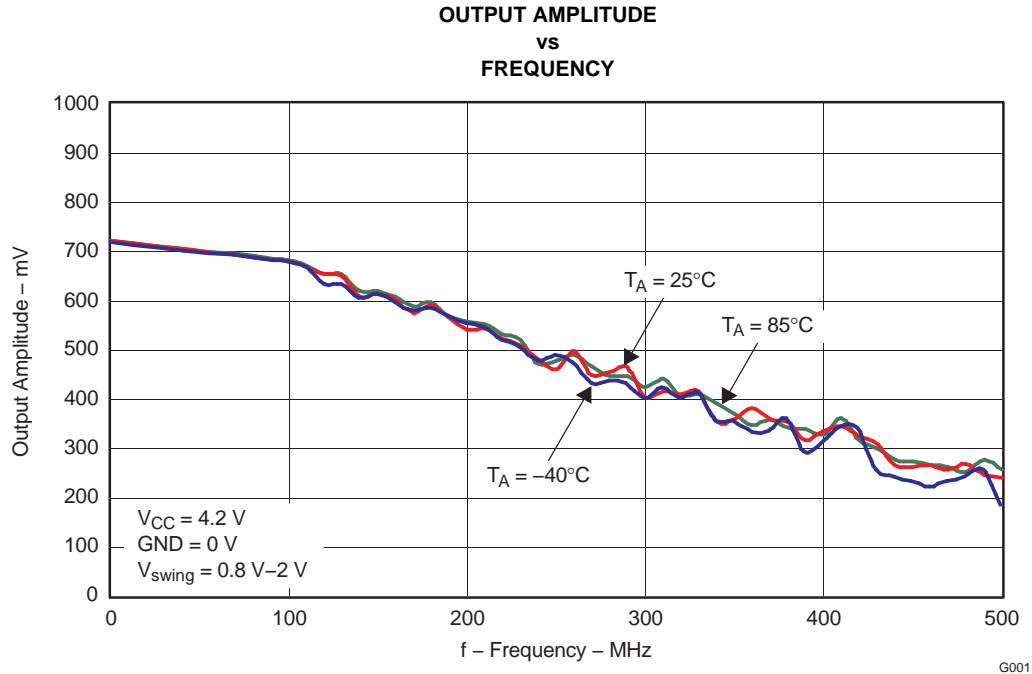## REVISION HISTORY

Changes from Original (December 2008) to Revision A   **Page**

• Changed the ORDERING INFORMATION Table Part Number From: SN65ELT206D To: SN65ELT20D 1

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24-Sep-2015

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ELT20D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20	Samples
SN65ELT20DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SISI	Samples
SN65ELT20DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT20	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT20DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT20DR	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S−PDSO−G8)　　　　　　PLASTIC SMALL−OUTLINE PACKAGE
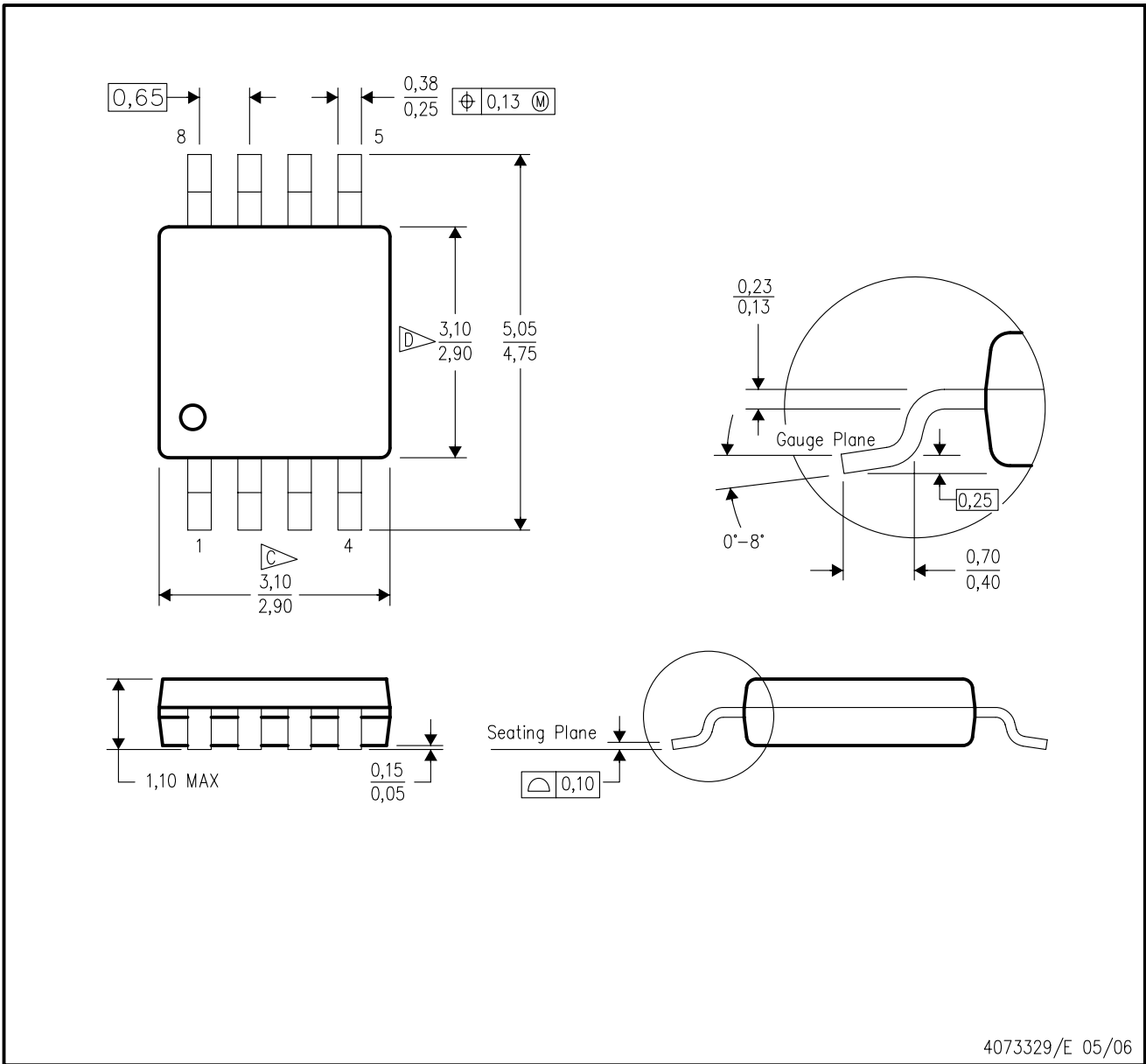
0,65

0,38
0,25
⊕ |0,13 Ⓜ|

8

5

◁D| 3,10
2,90

5,05
4,75

1

4

◁C|
3,10
2,90

0,23
0,13

Gauge Plane

0,25

0°−8°

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

|⌒|0,10|

1,10 MAX

4073329/E 05/06

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　◁C│　Body length does not include mold flash, protrusions, or gate burrs.　Mold flash, protrusions, or gate burrs shall
　　　　　not exceed 0.15 per end.
　　◁D│　Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
　　　　　E.　Falls within JEDEC MO−187 variation AA, except interlead flash.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
⟨C⟩

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

Pin 1
Index Area

1   4

0.050 (1,27)   0.020 (0,51)
                                0.012 (0,31)

⊕ | 0.010 (0,25) ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
           not exceed 0.006 (0,15) each side.
      ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AA.

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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50

6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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