- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**

- **State-of-the-Art _EPIC_-II_B_™ BiCMOS Design Significantly Reduces Power Dissipation**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**

- **Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT2827 . . . JT PACKAGE
SN74ABT2827 . . . DW OR NT PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	24	V_{CC}
A1	2	23	Y1
A2	3	22	Y2
A3	4	21	Y3
A4	5	20	Y4
A5	6	19	Y5
A6	7	18	Y6
A7	8	17	Y7
A8	9	16	Y8
A9	10	15	Y9
A10	11	14	Y10
GND	12	13	$\overline{OE2}$

SN54ABT2827 . . . FK PACKAGE
(TOP VIEW)

Pins (top, left to right): A2, A1, $\overline{OE1}$, NC, V_{CC}, Y1, Y2 (4, 3, 2, 1, 28, 27, 26)

Left side: A3 (5), A4 (6), A5 (7), NC (8), A6 (9), A7 (10), A8 (11)

Right side: Y3 (25), Y4 (24), Y5 (23), NC (22), Y6 (21), Y7 (20), Y8 (19)

Bottom (12, 13, 14, 15, 16, 17, 18): A9, A10, GND, NC, $\overline{OE2}$, Y10, Y9

NC – No internal connection

description

These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.
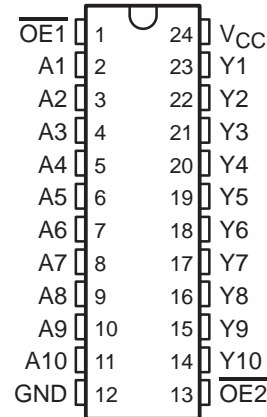
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The 'ABT2827 provide true data at their outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
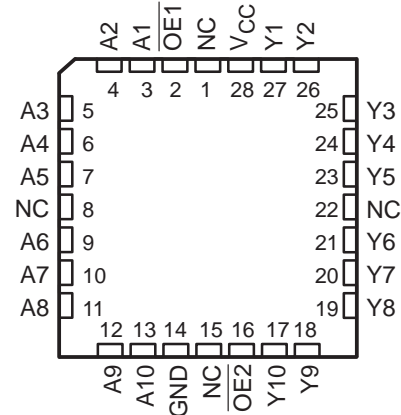
The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

The SN54ABT2827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2827 is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†
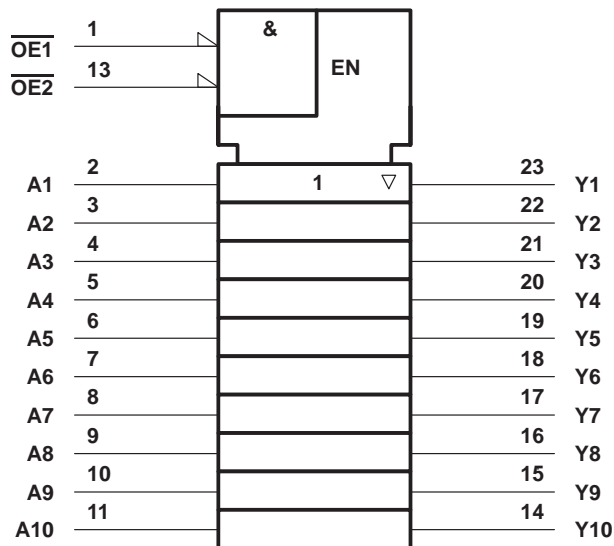
logic diagram (positive logic)

To Nine Other Channels
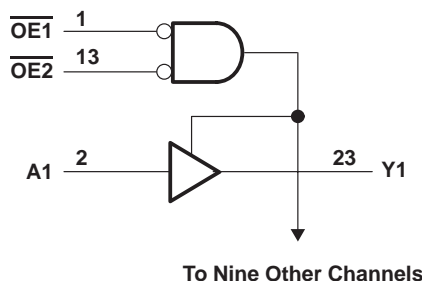
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
 IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2827 . . . . 96 mA
                                             SN74ABT2827 . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . 81°C/W
                                                    NT package . . . . 67°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
 functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
 implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
           2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages,
              which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT2827 MIN	SN54ABT2827 MAX	SN74ABT2827 MIN	SN74ABT2827 MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−12		−12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP†	$T_A = 25°C$ MAX	SN54ABT2827 MIN	SN54ABT2827 MAX	SN74ABT2827 MIN	SN74ABT2827 MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = −18$ mA			−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = −1$ mA	2.5			2.5		2.5		V
	$V_{CC} = 5$ V,	$I_{OH} = −1$ mA	3			3		3		
	$V_{CC} = 4.5$ V	$I_{OH} = −3$ mA	2.4			2.4		2.4		
		$I_{OH} = −12$ mA	2			2		2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA			0.8		0.8		0.8	V
V_{hys}				100						mV
I_I	$V_{CC} = 0$ to 5.5 V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			10‡		10		10‡	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−10‡		−10		−10‡	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O§	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−140	−225‡	−50	−225‡	−50	−225‡	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		80	250		250		250	µA
		Outputs low		35	40‡		40‡		40‡	mA
		Outputs disabled		80	250		250		250	µA
ΔI_{CC}¶	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5		1.5	mA
		Outputs disabled			50		50		50	µA
		Control inputs			1.5		1.5		1.5	mA
C_i	$V_I = 2.5$ V or 0.5 V			4						pF
C_O	$V_O = 2.5$ V or 0.5 V			8.5						pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ This data sheet limit may vary among suppliers.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

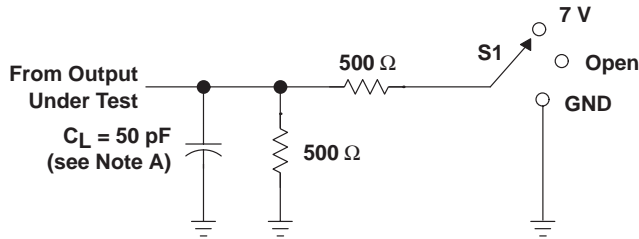| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2827		SN74ABT2827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3.3	5.1	1.1	5.6	1.1	5.5	ns
t_{PHL}			1.1	2.7	4.5	1.1	5.2	1.1	5.1	
t_{PZH}	$\overline{OE}$	Y	1	4	5.9	1	6.8	1	6.7	ns
t_{PZL}			1	4.2	6.8	1	8	1	7.8	
t_{PHZ}	$\overline{OE}$	Y	2	5.3	6.7	2	7.4	2	7.2	ns
t_{PLZ}			1.3	4.8	7.2	1.3	8.5	1.3	7.5	

![Texas Instruments logo]
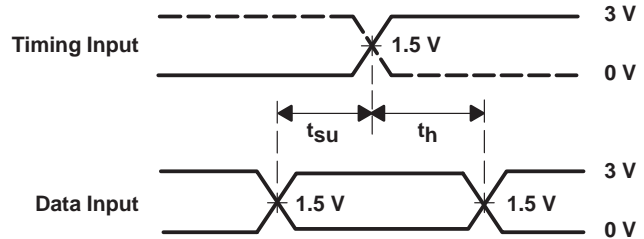
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

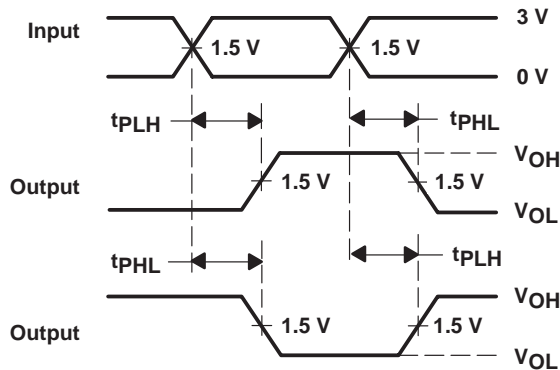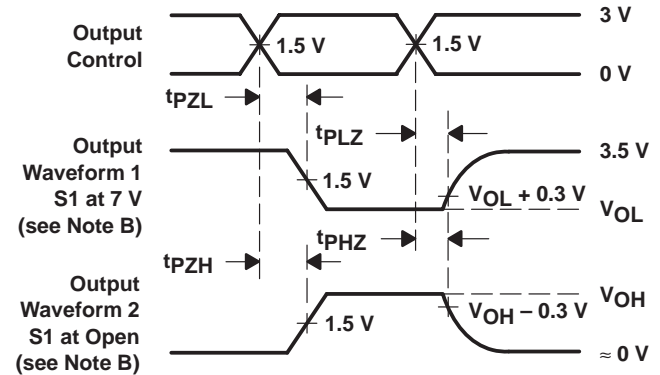| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
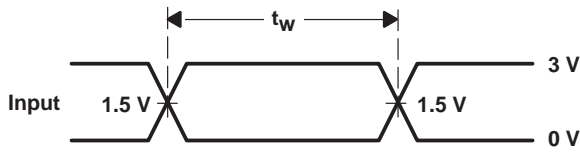
**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 n
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT2827DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2827	Samples
SN74ABT2827DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2827	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2827DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2827DWR	SOIC	DW	24	2000	367.0	367.0	45.0

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11
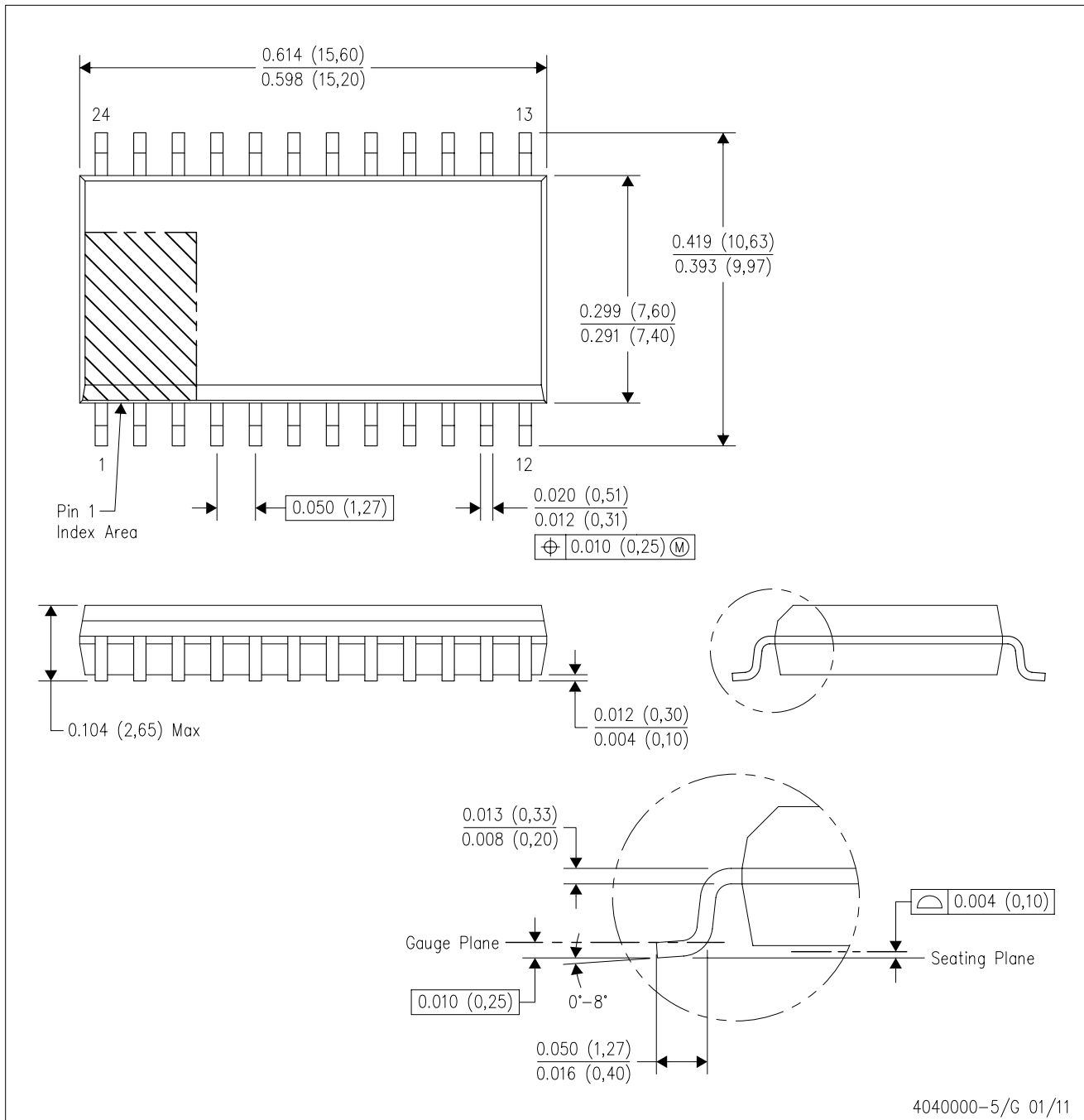
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−013 variation AD.

DW (R—PDSO—G24)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

22x1,27

24x0,55   22x1,27

24x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around
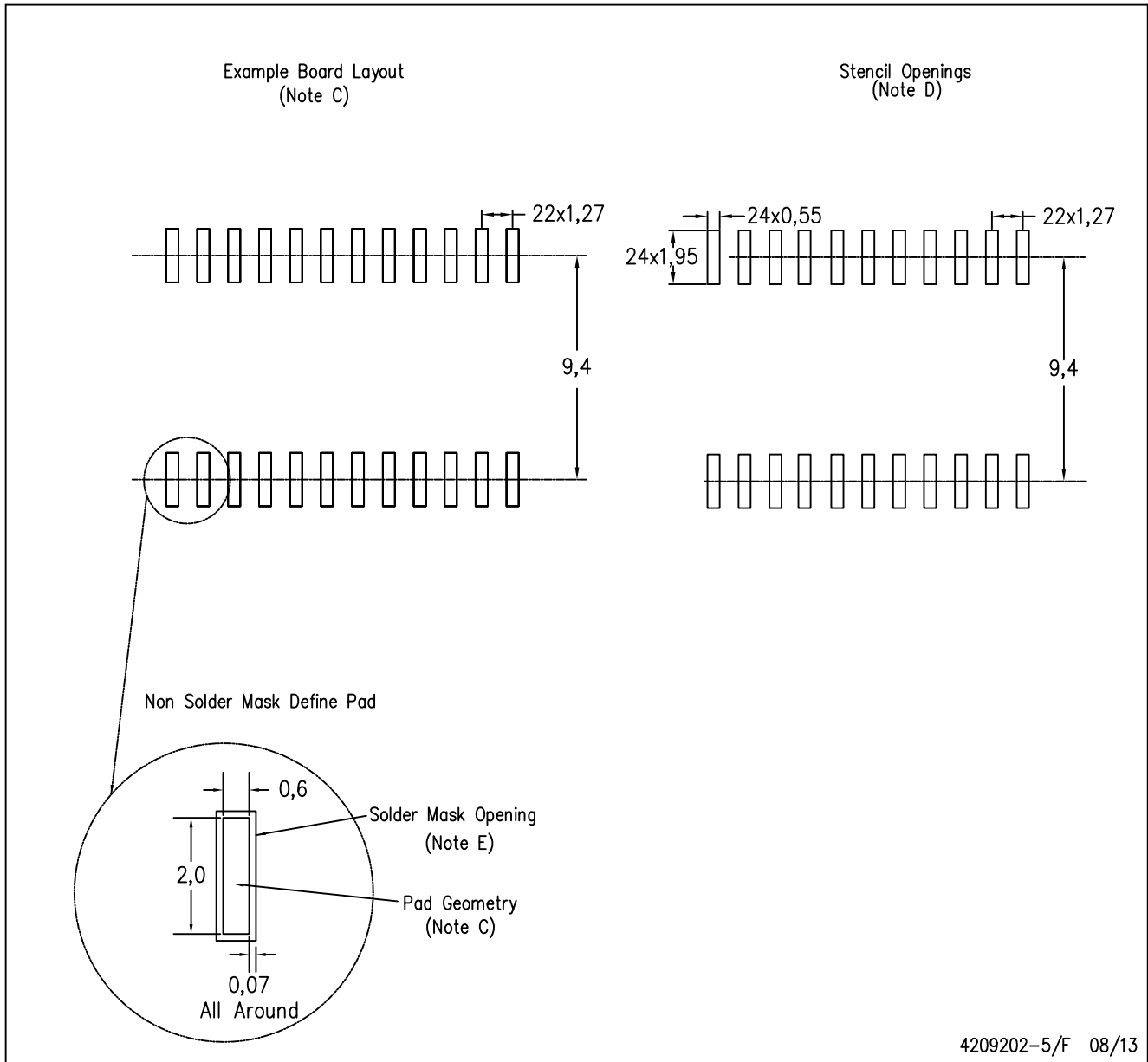
4209202—5/F   08/13

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Refer to IPC7351 for alternate board design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC—7525
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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