- Members of the Texas Instruments *Widebus*™ Family

- State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation

- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C

- High-Impedance State During Power Up and Power Down

- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise

- Flow-Through Architecture Optimizes PCB Layout

- High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})

- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors

- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABTH16823 . . . WD PACKAGE
SN74ABTH16823 . . . DGG OR DL PACKAGE
(TOP VIEW)

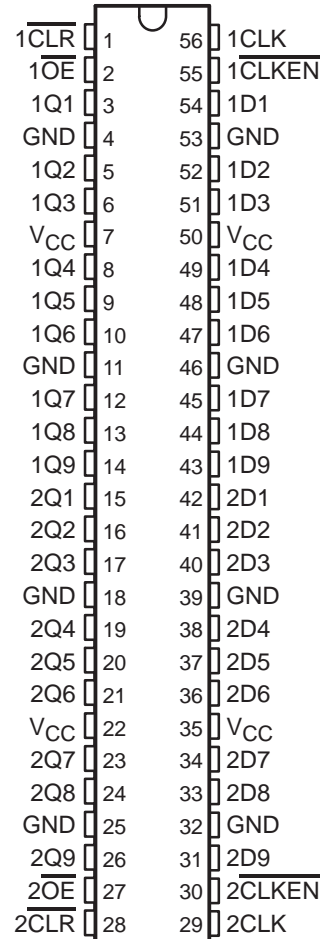|				
1$\overline{\text{CLR}}$	1		56	1CLK
1$\overline{\text{OE}}$	2		55	1$\overline{\text{CLKEN}}$
1Q1	3		54	1D1
GND	4		53	GND
1Q2	5		52	1D2
1Q3	6		51	1D3
V_{CC}	7		50	V_{CC}
1Q4	8		49	1D4
1Q5	9		48	1D5
1Q6	10		47	1D6
GND	11		46	GND
1Q7	12		45	1D7
1Q8	13		44	1D8
1Q9	14		43	1D9
2Q1	15		42	2D1
2Q2	16		41	2D2
2Q3	17		40	2D3
GND	18		39	GND
2Q4	19		38	2D4
2Q5	20		37	2D5
2Q6	21		36	2D6
V_{CC}	22		35	V_{CC}
2Q7	23		34	2D7
2Q8	24		33	2D8
GND	25		32	GND
2Q9	26		31	2D9
2$\overline{\text{OE}}$	27		30	2$\overline{\text{CLKEN}}$
2$\overline{\text{CLR}}$	28		29	2CLK

description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABTH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH16823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH16823 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

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logic symbol†

Input	Pin	Label		Label	Pin	Output
1OE	2	EN1				
1CLR	1	R2				
1CLKEN	55	G3				
1CLK	56	3C4				
2OE	27	EN5				
2CLR	28	R6				
2CLKEN	30	G7				
2CLK	29	7C8				
1D1	54	4D	1, 2 ▽	3	1Q1	
1D2	52			5	1Q2	
1D3	51			6	1Q3	
1D4	49			8	1Q4	
1D5	48			9	1Q5	
1D6	47			10	1Q6	
1D7	45			12	1Q7	
1D8	44			13	1Q8	
1D9	43			14	1Q9	
2D1	42	8D	5, 6 ▽	15	2Q1	
2D2	41			16	2Q2	
2D3	40			17	2Q3	
2D4	38			19	2Q4	
2D5	37			20	2Q5	
2D6	36			21	2Q6	
2D7	34			23	2Q7	
2D8	33			24	2Q8	
2D9	31			26	2Q9	
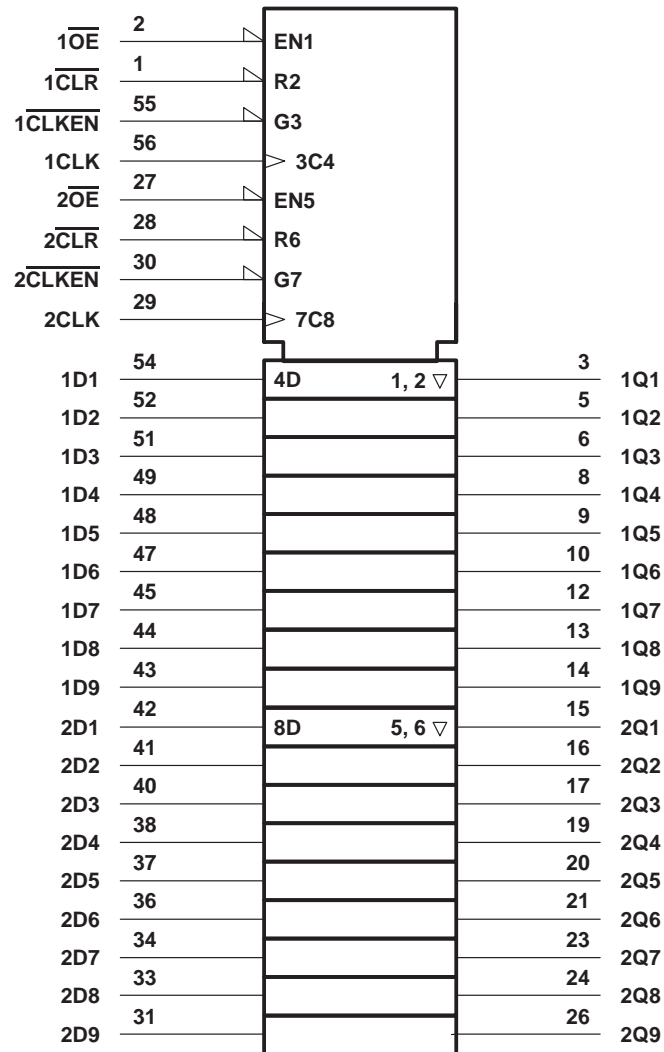
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

```
1OE̅     2 ─────────────────────────────▷○────┐
1CLR̅    1 ──────▷○──┐                          │
                    │                          │
1CLKEN̅  55 ─────▷○──┼──●──────────┤CE          │
                    │             │            │
                    │        ┌──●─┤R           │
1CLK    56 ─────▷───┼──●─────┤  ┌─│>C1    ┌────┼──● 3  1Q1
1D1     54 ─────────┼──┼─────┤  └─┤1D     │▷───┘
                    │  │     └────────┘    │
                    ▽  ▽  ▽               ▽
                    └──────────┬──────────┘
                  To Eight Other Channels
```

```
2OE̅     27 ────────────────────────────▷○────┐
2CLR̅    28 ──────▷○──┐                         │
                     │                         │
2CLKEN̅  30 ─────▷○──┼──●──────────┤CE          │
                     │            │            │
                     │       ┌──●─┤R           │
2CLK    29 ─────▷───┼──●─────┤  ┌─│>C1    ┌───┼──● 15  2Q1
2D1     42 ─────────┼──┼─────┤  └─┤1D     │▷──┘
                     │  │    └────────┘    │
                     ▽  ▽  ▽              ▽
                     └──────────┬─────────┘
                  To Eight Other Channels
```
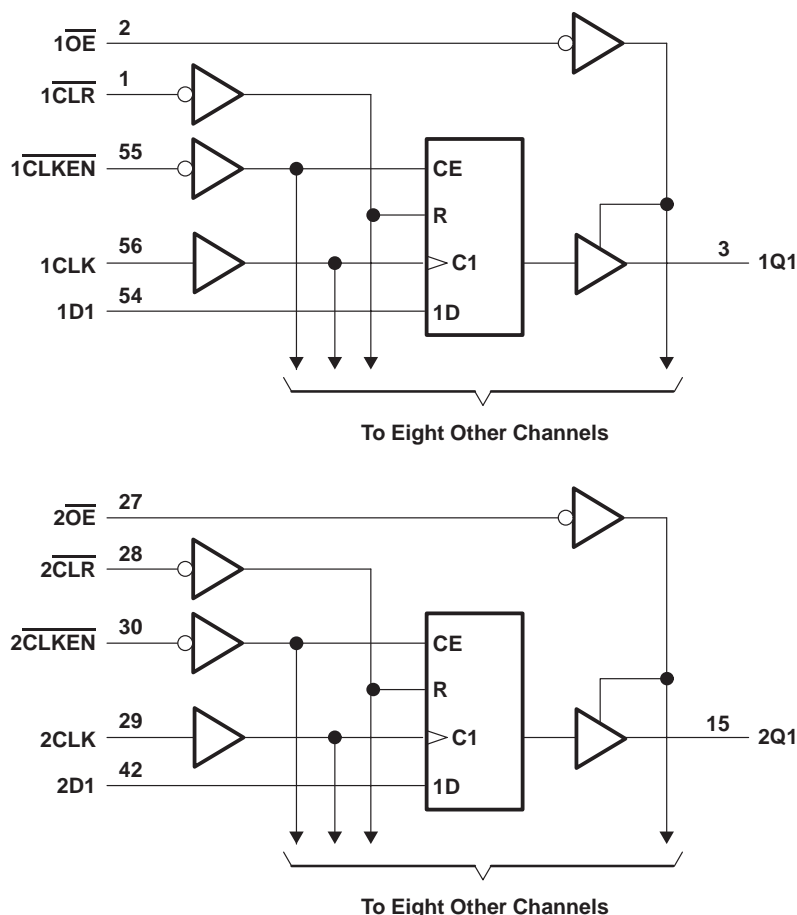
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V

Voltage range applied to any output in the high or power-off state, V_O . . . . −0.5 V to 5.5 V

Current into any output in the low state, I_O: SN54ABTH16823 . . . . 96 mA

SN74ABTH16823 . . . . 128 mA

Input clamp current, I_{IK} ($V_I < 0$) . . . . −18 mA

Output clamp current, I_{OK} ($V_O < 0$) . . . . −50 mA

Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 81°C/W

DL package . . . . 74°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH16823		SN74ABTH16823		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABTH16823		SN74ABTH16823		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2		-1.2		-1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I		$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
$I_{I(hold)}$		$V_{CC} = -4.5$ V	$V_I = 0.8$ V	100			100		100		µA
			$V_I = 2$ V	-100			-100		-100		
I_{OZPU}‡		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZPD}‡		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZH}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10**		50		10	µA
I_{OZL}		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				-10**		-50		-10	µA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}	Outputs high	$V_{CC} = 5.5$ V, $V_O = 5.5$ V				50		50		50	µA
I_O§		$V_{CC} = 5.5$ V, $V_O = 2.5$ V		-50	-100	-200	-50	-200	-50	-200	mA
I_{CC}	Outputs high	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND				0.5		0.5		0.5	mA
	Outputs low					80		80		80	
	Outputs disabled					0.5		0.5		0.5	
ΔI_{CC}¶		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i		$V_I = 2.5$ V or 0.5 V			4						pF
C_o		$V_O = 2.5$ V or 0.5 V			8.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** These limits apply only to the SN74ABTH16823.
† All typical values are at $V_{CC} = 5$ V.
‡ This parameter is characterized, but not production tested.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABTH16823		SN74ABTH16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	1.6		2		1.6		ns
		Data	1.7		1.7		1.7		
		$\overline{CLKEN}$ low	2.8		2.8		2.8		
t_h	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		$\overline{CLKEN}$ low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH16823					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	1.6	3.9	5.5	1.6	7.7	ns
t_{PHL}			2.1	3.9	5.4	2.1	6.4	
t_{PHL}	$\overline{CLR}$	Q	1.9	4.1	6	1.9	6.9	ns
t_{PZH}	$\overline{OE}$	Q	1	3.1	4.2	1	5.1	ns
t_{PZL}			1.5	3.5	4.6	1.5	5.7	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.3	6	2.2	6.8	ns
t_{PLZ}			1.6	4.3	6.4	1.6	9.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABTH16823					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	1.6	3.9	5.5	1.6	6.8	ns
t_{PHL}			2.1	3.9	5.4	2.1	6	
t_{PHL}	$\overline{CLR}$	Q	1.9	4.1	6	1.9	6.7	ns
t_{PZH}	$\overline{OE}$	Q	1	3.1	4.2	1	4.9	ns
t_{PZL}			1.5	3.5	4.6	1.5	5.5	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.3	5.6	2.2	6.1	ns
t_{PLZ}			1.6	4.3	6.4	1.6	8.7	

PARAMETER MEASUREMENT INFORMATION
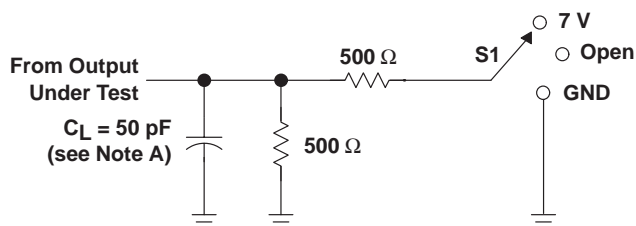
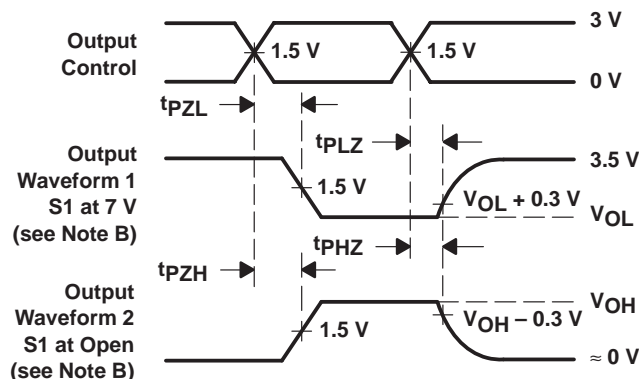| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
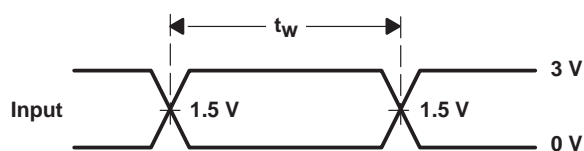
**VOLTAGE WAVEFORMS
PULSE DURATION**
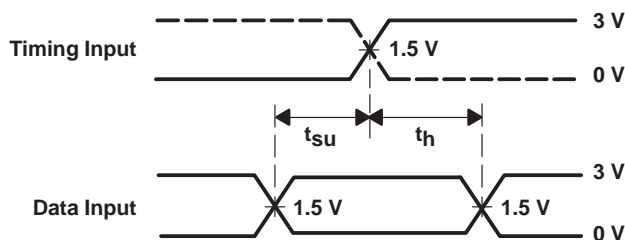
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
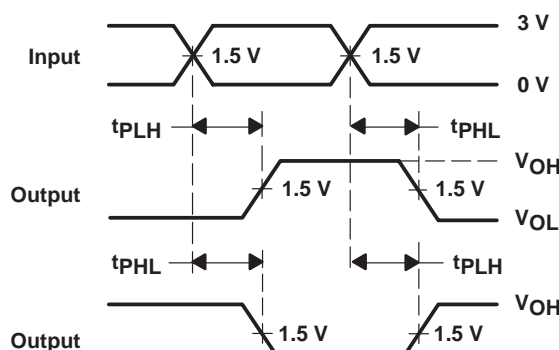
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTH16823DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16823	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS
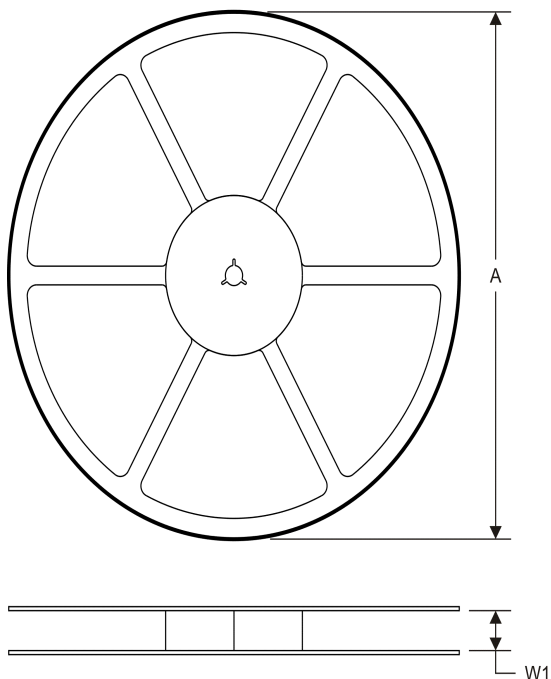
TAPE DIMENSIONS
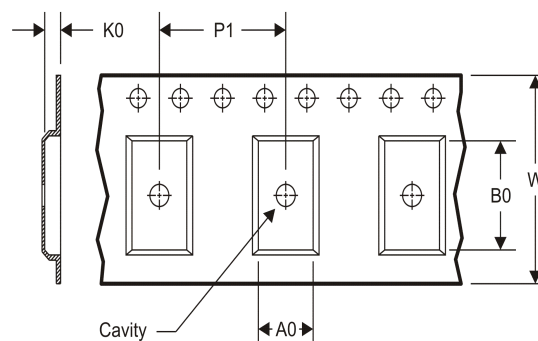
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16823DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16823DLR	SSOP	DL	56	1000	367.0	367.0	55.0

DL (R−PDSO−G56) PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343) / 0.008 (0,203)   ⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67) / 0.395 (10,03)

0.299 (7,59) / 0.291 (7,39)

1   28

0.730 (18,54) / 0.720 (18,29)

0.010 (0,25) / 0.005 (0,13)

Gage Plane

0°−8°

0.010 (0,25)

0.040 (1,02) / 0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane   ⬜ 0.004 (0,10)

4040048−4/F 05/13
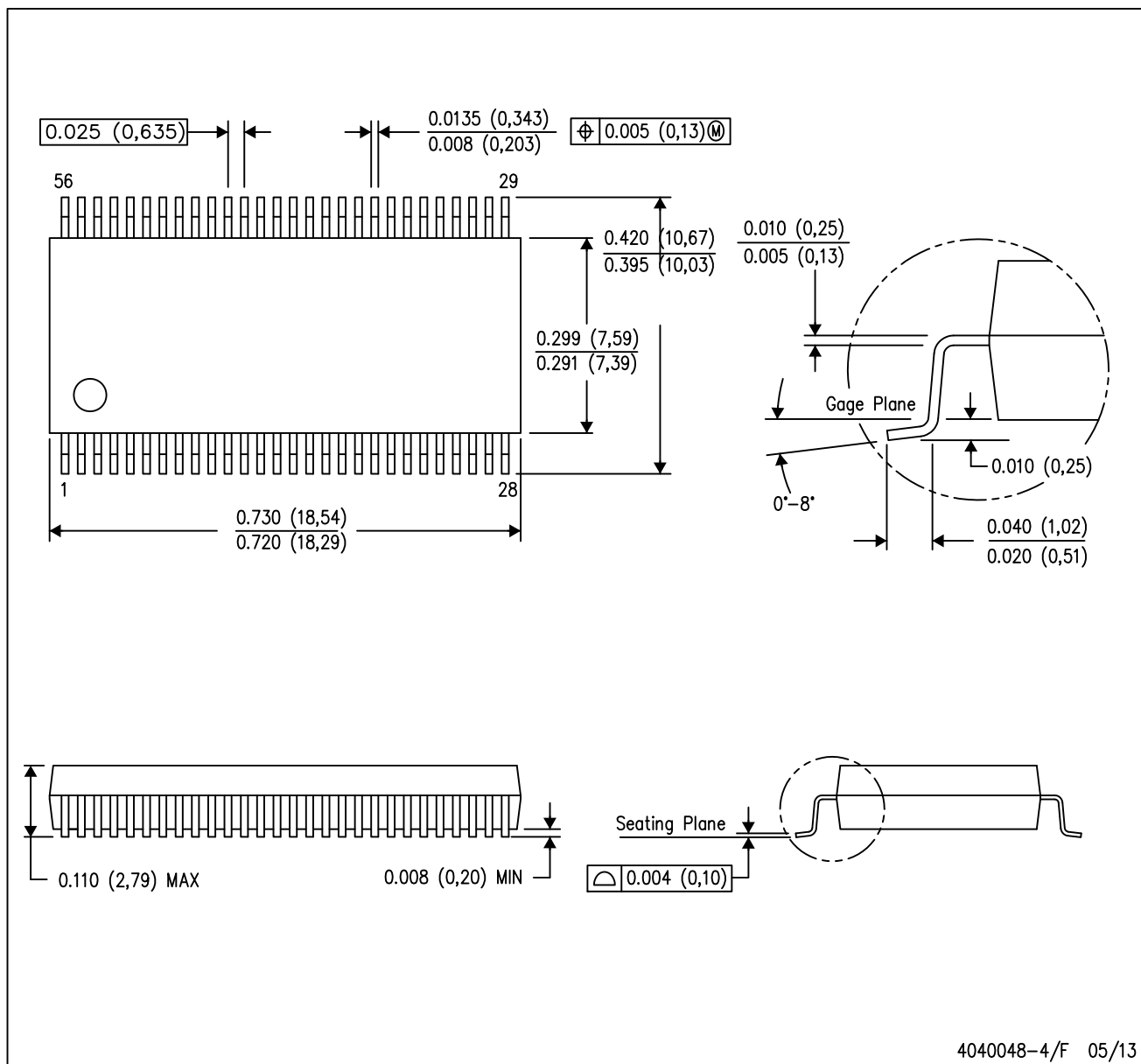
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−118

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