

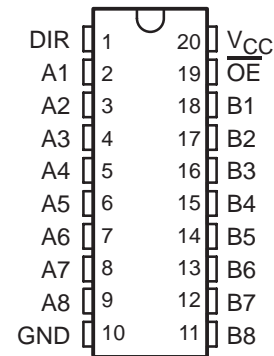
# SN74AC245-EP OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS780 – OCTOBER 2004

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 6-V  $V_{CC}$  Operation**
- **Inputs Accept Voltages to 6 V**
- **Max  $t_{pd}$  of 7 ns at 5 V**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DW PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74AC245 octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

When the output-enable ( $\overline{OE}$ ) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction control (DIR) input. A high on  $\overline{OE}$  disables the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$         | PACKAGE‡  |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-----------|---------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tape and reel | SN74AC245IDWREP       | SAC245IEP        |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

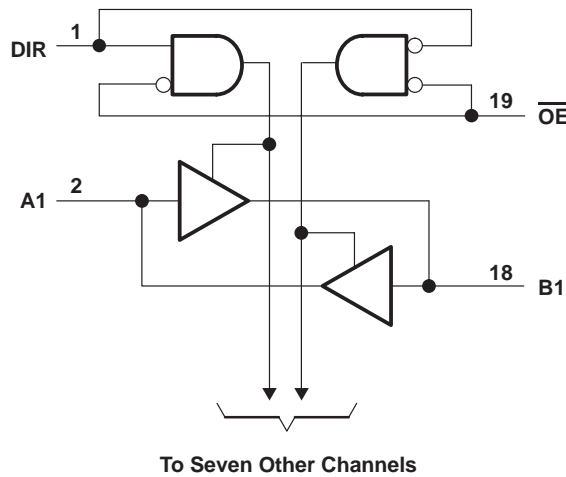
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**SN74AC245-EP**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS780 – OCTOBER 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$ .....                                 | -0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1) .....                        | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1) .....                       | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....  | $\pm 20$ mA                |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) ..... | $\pm 20$ mA                |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....     | $\pm 50$ mA                |
| Continuous current through $V_{CC}$ or GND .....                     | $\pm 200$ mA               |
| Package thermal impedance, $\theta_{JA}$ (see Note 2) .....          | 58°C/W                     |
| Storage temperature range, $T_{stg}$ .....                           | -65°C to 150°C             |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

|                     |                                    | MIN                     | MAX      | UNIT |
|---------------------|------------------------------------|-------------------------|----------|------|
| $V_{CC}$            | Supply voltage                     | 2                       | 6        | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 3\text{ V}$   | 2.1      | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | 3.15     |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | 3.85     |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 3\text{ V}$   | 0.9      | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | 1.35     |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | 1.65     |      |
| $V_I$               | Input voltage                      | 0                       | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                       | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 3\text{ V}$   | -12      | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | -24      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | -24      |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 3\text{ V}$   | 12       | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | 24       |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | 24       |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                         | 8        | ns/V |
| $T_A$               | Operating free-air temperature     | -40                     | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74AC245-EP**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                 | TEST CONDITIONS   | V <sub>CC</sub>                         | T <sub>A</sub> = 25°C |      |      | MIN  | MAX | UNIT |
|---------------------------|---|---|-----------------------|------|------|------|-----|------|
|                           |   |   | MIN                   | TYP  | MAX  |      |     |      |
| V <sub>OH</sub>           | I <sub>OH</sub> = -50 μA  | 3 V                                     | 2.9                   |      |      | 2.9  |     | V    |
|                           |   | 4.5 V                                   | 4.4                   |      |      | 4.4  |     |      |
|                           |   | 5.5 V                                   | 5.4                   |      |      | 5.4  |     |      |
|                           | I <sub>OH</sub> = -12 mA  | 3 V                                     | 2.56                  |      |      | 2.46 |     |      |
|                           |   | 4.5 V                                   | 3.86                  |      |      | 3.76 |     |      |
|                           |   | 5.5 V                                   | 4.86                  |      |      | 4.76 |     |      |
| I <sub>OH</sub> = -75 mA† | 5.5 V   |   |                       |      | 3.85 |      |     |      |
| V <sub>OL</sub>           | I <sub>OL</sub> = 50 μA   | 3 V                                     | 0.002                 |      | 0.1  |      | V   |      |
|                           |   | 4.5 V                                   | 0.001                 |      | 0.1  |      |     |      |
|                           |   | 5.5 V                                   | 0.001                 |      | 0.1  |      |     |      |
|                           | I <sub>OL</sub> = 12 mA   | 3 V                                     |                       |      | 0.36 |      |     |      |
|                           |   | 4.5 V                                   |                       |      | 0.36 |      |     |      |
|                           | I <sub>OL</sub> = 24 mA   | 5.5 V                                   |                       |      | 0.36 |      |     |      |
| I <sub>OL</sub> = 75 mA†  | 5.5 V   |   |                       | 1.65 |      |      |     |      |
| I <sub>I</sub>            | A or B ports‡   | V <sub>I</sub> = V <sub>CC</sub> or GND | 5.5 V                 | ±0.1 |      | ±1   |     | μA   |
|                           | $\overline{\text{OE}}$ or DIR   |   |                       | ±0.1 |      | ±1   |     |      |
| I <sub>OZ</sub>           | V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub> |   | 5.5 V                 | ±0.5 |      | ±5   |     | μA   |
| I <sub>CC</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                                       |   | 5.5 V                 | 4    |      | 40   |     | μA   |
| C <sub>i</sub>            | V <sub>I</sub> = V <sub>CC</sub> or GND   |   | 5 V                   | 4.5  |      |      |     | pF   |
| C <sub>io</sub>           | V <sub>O</sub> = V <sub>CC</sub> or GND   |   | 5 V                   | 15   |      |      |     | pF   |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | T <sub>A</sub> = 25°C |     |      | MIN | MAX  | UNIT |
|------------------|------------------------|-------------|-----------------------|-----|------|-----|------|------|
|                  |                        |             | MIN                   | TYP | MAX  |     |      |      |
| t <sub>PLH</sub> | A or B                 | B or A      | 1.5                   | 5   | 8.5  | 1   | 9    | ns   |
| t <sub>PHL</sub> |                        |             | 1.5                   | 5   | 8.5  | 1   | 9    |      |
| t <sub>PZH</sub> | $\overline{\text{OE}}$ | A or B      | 2.5                   | 7   | 11.5 | 2   | 12.5 | ns   |
| t <sub>PZL</sub> |                        |             | 2.5                   | 7.5 | 12   | 2   | 13.5 |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$ | A or B      | 2                     | 6.5 | 12   | 1   | 12.5 | ns   |
| t <sub>PLZ</sub> |                        |             | 2                     | 7   | 11.5 | 1.5 | 13   |      |



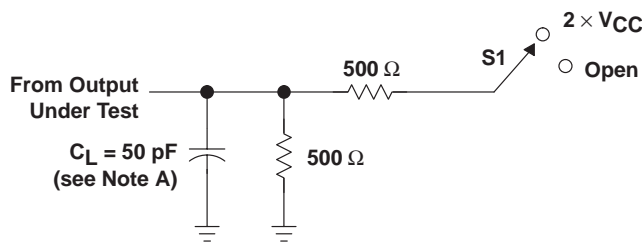
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)           | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|-----------|------------------------|-------------|--------------------------|-----|-----|-----|-----|------|
|           |                        |             | MIN                      | TYP | MAX |     |     |      |
| $t_{PLH}$ | A or B                 | B or A      | 1.5                      | 3.5 | 6.5 | 1   | 7   | ns   |
| $t_{PHL}$ |                        |             | 1.5                      | 3.5 | 6   | 1   | 7   |      |
| $t_{PZH}$ | $\overline{\text{OE}}$ | A or B      | 1.5                      | 5   | 8.5 | 1   | 9   | ns   |
| $t_{PZL}$ |                        |             | 1.5                      | 5.5 | 9   | 1   | 9.5 |      |
| $t_{PHZ}$ | $\overline{\text{OE}}$ | A or B      | 1.5                      | 5.5 | 9   | 1   | 10  | ns   |
| $t_{PLZ}$ |                        |             | 1.5                      | 5.5 | 9   | 1   | 10  |      |

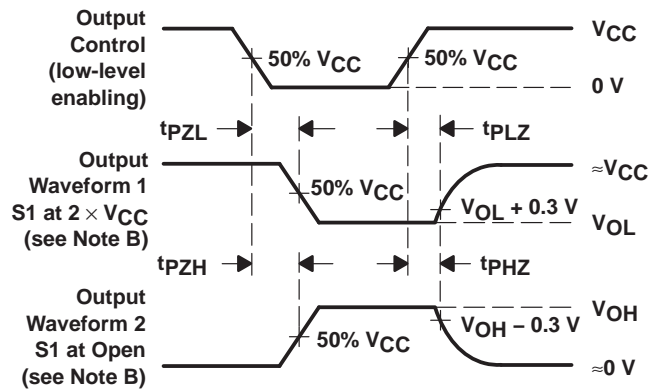
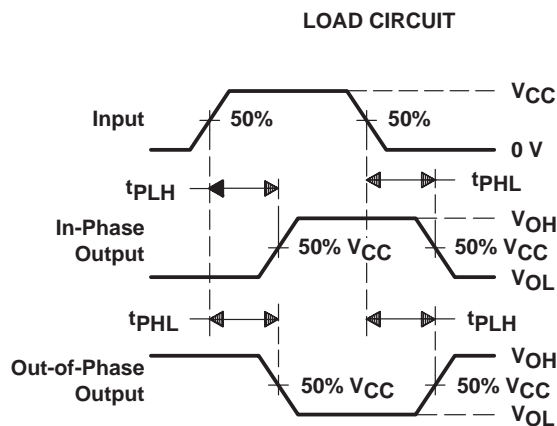
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER  | TEST CONDITIONS                           | TYP | UNIT |
|--|---|-----|------|
| $C_{pd}$ Power dissipation capacitance per transceiver | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 45  | pF   |

### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open              |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AC245IDWREP  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| V62/04760-01XE   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74AC245](#)
- Military: [SN54AC245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AC245IDWREP  | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | SAC245IEP               | <a href="#">Samples</a> |
| V62/04760-01XE   | ACTIVE        | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | SAC245IEP               | <a href="#">Samples</a> |

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**OBSOLETE:** TI has discontinued the production of the device.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Catalog: [SN74AC245](#)
- Military: [SN54AC245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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|                              |  |
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| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
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| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

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