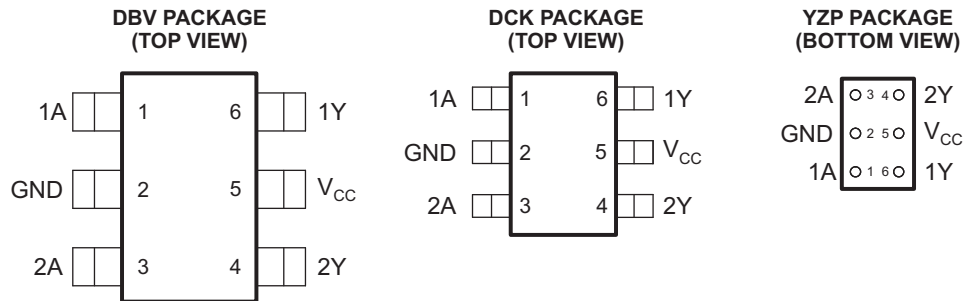


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.5 ns at 1.8 V
- Low Power Consumption, 10 μ A at 1.8 V
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual inverter buffer/driver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The output of the SN74AUC2G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G06YZPR	___UT_
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUC2G06DBVR	U06_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUC2G06DCKR	UT_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUC2G06

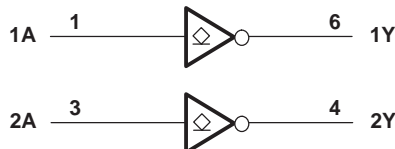
DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES442C–MAY 2003–REVISED JANUARY 2007

**FUNCTION TABLE
(EACH INVERTER)**

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	3.6	V
V_I	Input voltage range ⁽²⁾	-0.5	3.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	3.6	V
V_O	Output voltage range ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current			± 20 mA
	Continuous current through V_{CC} or GND			± 100 mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package		165
		DCK package		259
		YZP package		123
T_{stg}	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.7	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	3.6	V
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7	mA
		V _{CC} = 1.1 V	3	
		V _{CC} = 1.4 V	5	
		V _{CC} = 1.65 V	8	
		V _{CC} = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OL}	I _{OL} = 100 μA	0.8 V to 2.7 V			0.2	V
	I _{OL} = 0.7 mA	0.8 V		0.25		
	I _{OL} = 3 mA	1.1 V			0.3	
	I _{OL} = 5 mA	1.4 V			0.4	
	I _{OL} = 8 mA	1.65 V			0.45	
	I _{OL} = 9 mA	2.3 V			0.6	
I _I	A inputs	V _I = V _{CC} or GND	0 to 2.7 V		±5	μA
I _{off}		V _I or V _O = 2.7 V	0		±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V		10	μA
C _i		V _I = V _{CC} or GND	2.5 V	2.5		pF

(1) All typical values are at T_A = 25°C.

SN74AUC2G06

DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES442C–MAY 2003–REVISED JANUARY 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V ± 0.1 V		$V_{CC} = 1.5$ V ± 0.1 V		$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	4.1	1.8	3.3	1.4	2.8	1.6	2.4	3	1.5	2.3	ns
t_{PHL}			4.2	0.8	2.7	0.6	2	0.6	1	1.7	0.6	1.1	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 1](#))

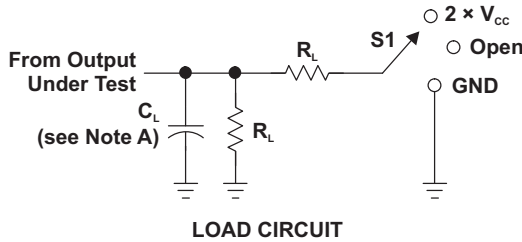
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.6	2	2.5	0.7	1.2	ns
t_{PHL}			0.7	1.5	2.3	0.7	1.8	

Operating Characteristics

$T_A = 25^\circ\text{C}$

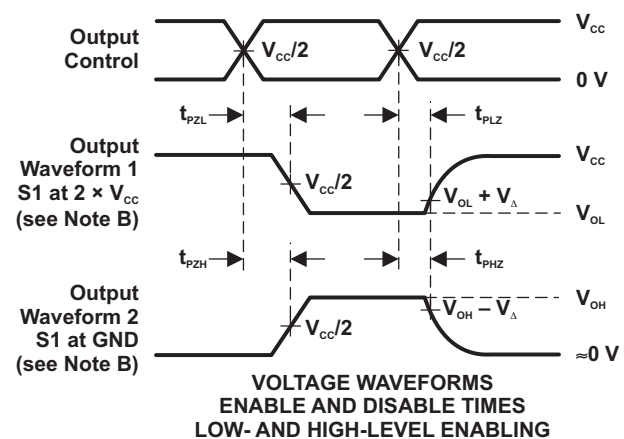
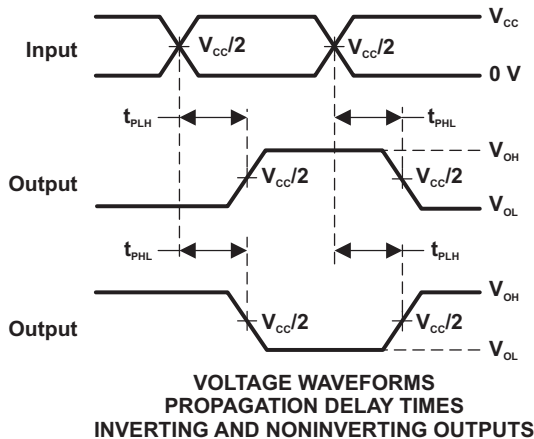
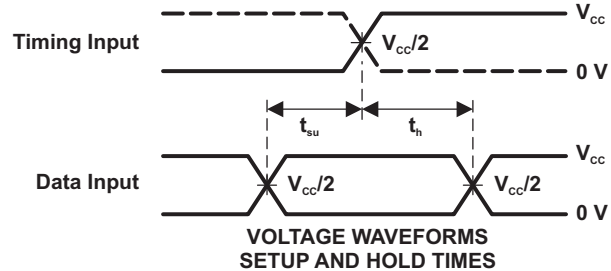
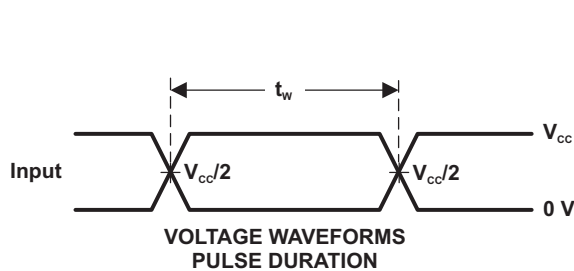
PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V	$V_{CC} = 1.5$ V	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	f = 10 MHz	2	2	2	2	3	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PZL}/t_{PZH}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_A
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \geq 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PZL} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC2G06DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U06R	Samples
SN74AUC2G06DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UTR	Samples
SN74AUC2G06YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(UT7 ~ UTN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G06DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC2G06DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUC2G06YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

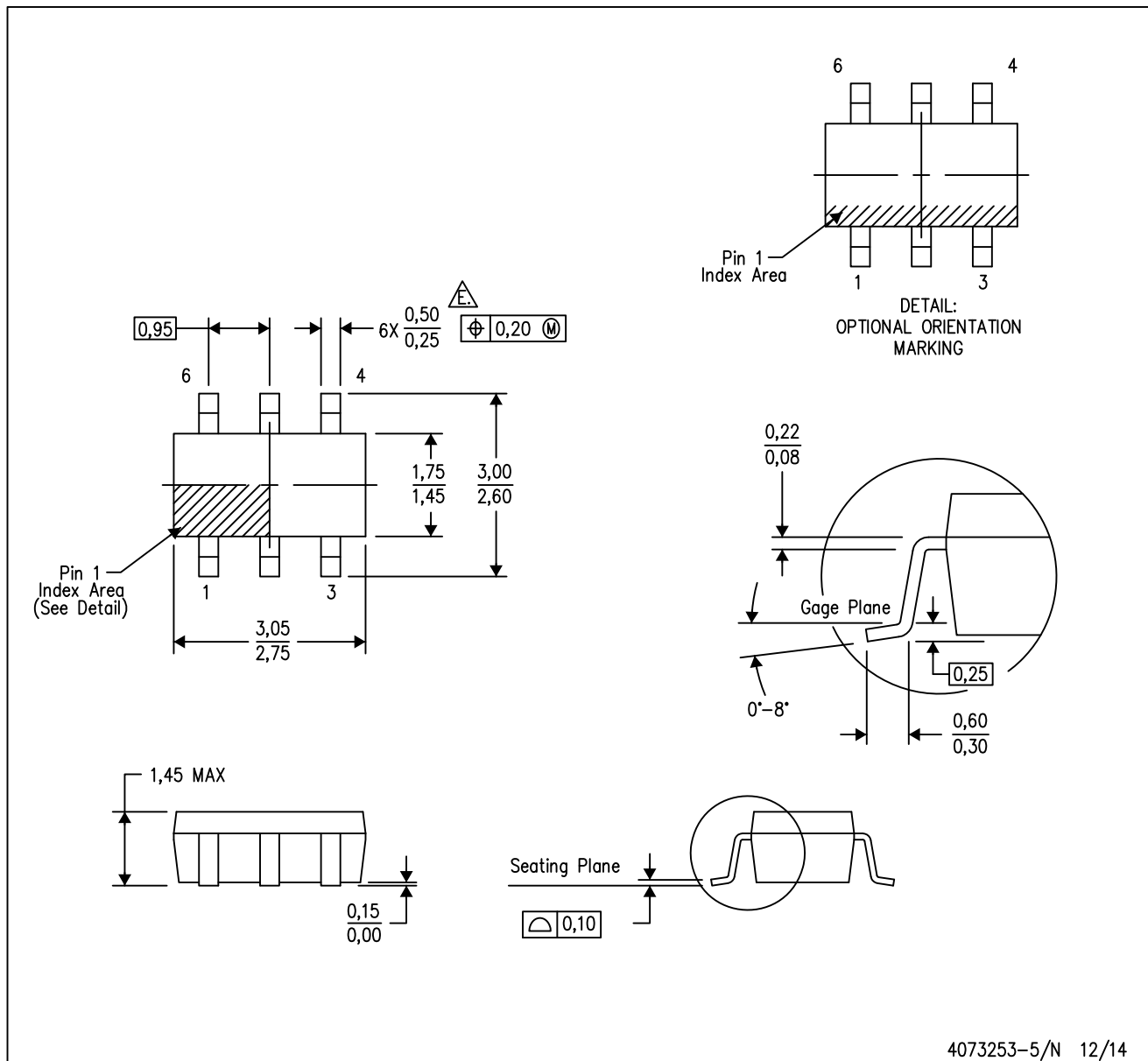

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G06DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUC2G06DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUC2G06YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.

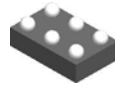
DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

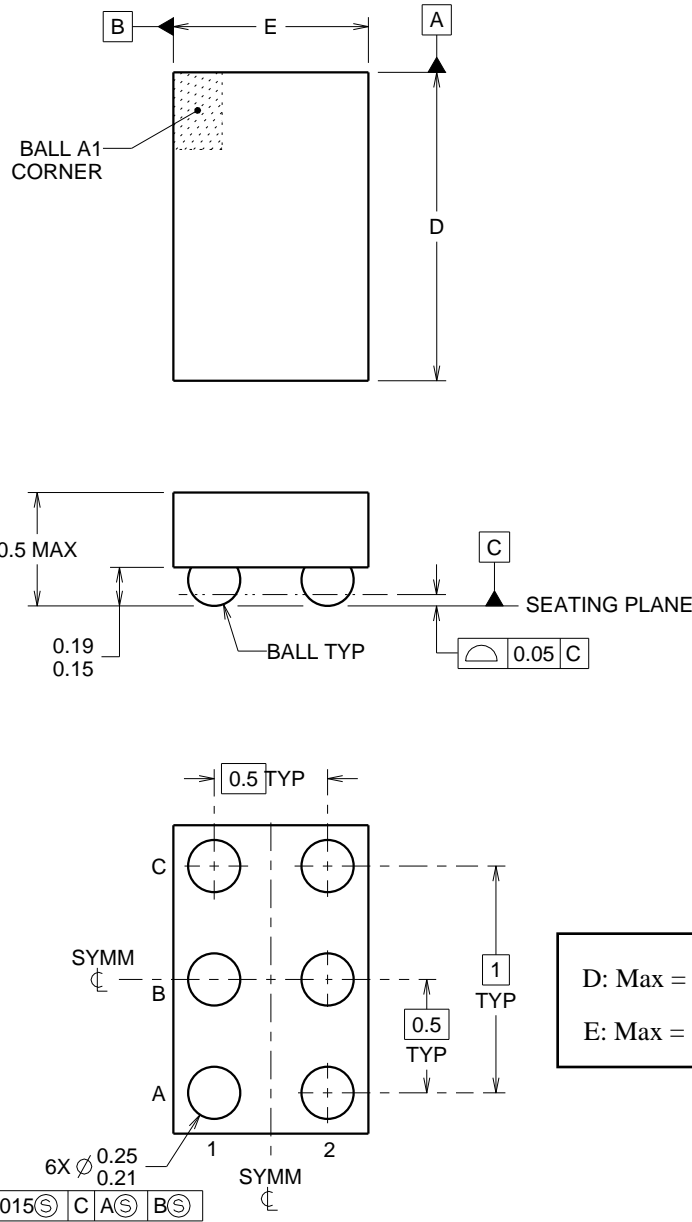
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

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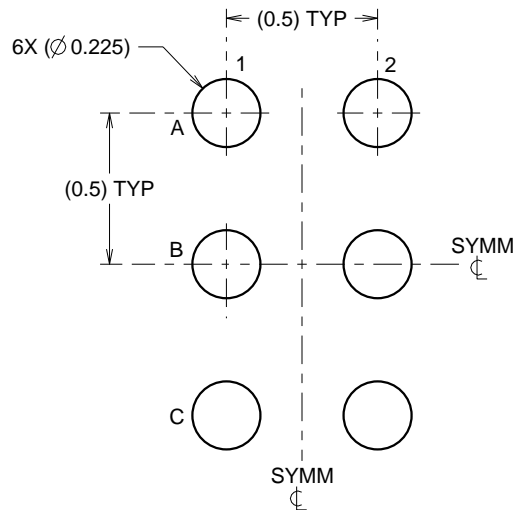
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

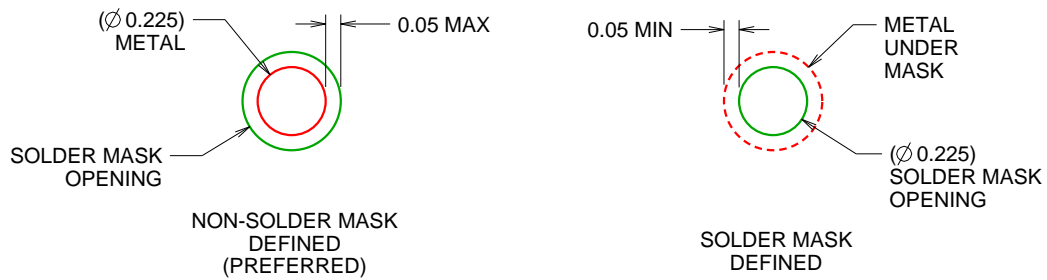
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

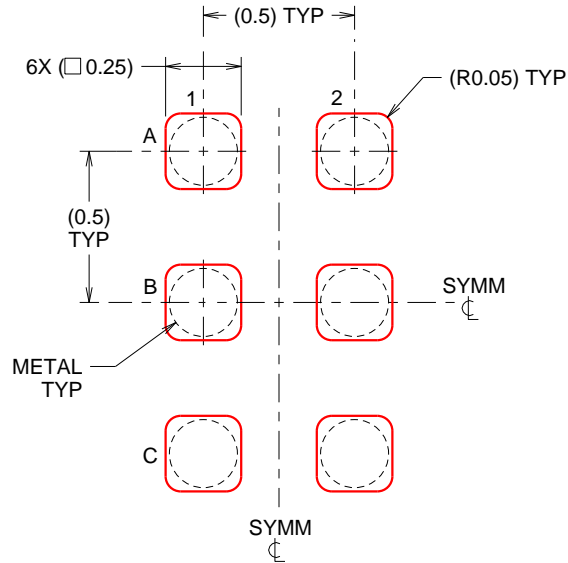
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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