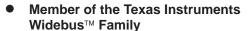
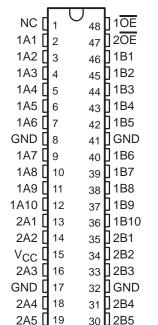
DGG, DGV, OR DL PACKAGE

(TOP VIEW)

SCDS166 - MAY 2004



- High-Bandwidth Data Path (Up To 500 MHz<sup>†</sup>)
- 5-V Tolerant I/Os with Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r<sub>on</sub>)
   Characteristics Over Operating Range (r<sub>on</sub> = 5 Ω Typical)
- Rail-to-Rail Switching on Data I/O Ports
   0-V to 5-V Switching With 3.3-V V<sub>CC</sub>
   0-V to 3.3-V Switching With 2.5-V V<sub>CC</sub>
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C<sub>io(OFF)</sub> = 4 pF Typical)
- Fast Switching Frequency (f<sub>OE</sub> = 20 MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I<sub>CC</sub> = 1 mA Typical)
- V<sub>CC</sub> Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0 V to 5 V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating
  - † For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, CBT-C, CB3T, and CB3Q Signal-Switch Families, literature number SCDA008.



NC - No internal connection

29 **∏** 2B6

28 2B7

27 2B8

26 D2B9

25 D2B10

2A6  $\Pi$  20

2A9 **∏** 23

2A10 24

2A7 21

2A8 🛮 22



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Widebus is a trademark of Texas Instruments.



#### SCDS166 - MAY 2004

### description/ordering information

The SN74CB3Q16210 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r<sub>on</sub>). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16210 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16210 is organized as two 10-bit bus switches with separate output-enable  $(1\overline{OE}, 2\overline{OE})$  inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0000 0	Tube	SN74CB3Q16210DL	000040040
4000 / 0500	SSOP – DL	Tape and reel	SN74CB3Q16210DLR	CB3Q16210
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74CB3Q16210DGGR	CB3Q16210
	TVSOP - DGV	Tape and reel	SN74CB3Q16210DGVR	BW210

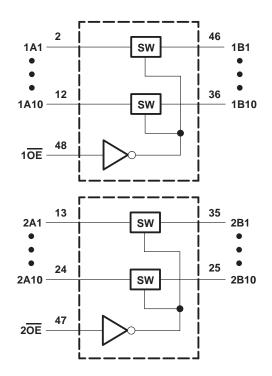
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each 10-bit bus switch)

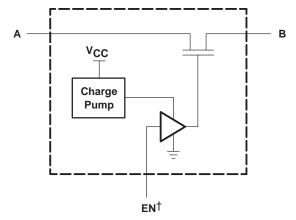
INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect



## logic diagram (positive logic)



## simplified schematic, each FET switch (SW)



<sup>†</sup>EN is the internal enable signal applied to the switch.



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 4.6 V
Control input voltage range, V <sub>IN</sub> (see Notes 1 and 2)	$\dots$ -0.5 V to 7 V
Switch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	$\dots$ -0.5 V to 7 V
Control input clamp current, I <sub>IK</sub> (V <sub>IN</sub> < 0)	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O}$ < 0)	–50 mA
ON-state switch current, I <sub>I/O</sub> (see Note 4)	±64 mA
Continuous current through V <sub>CC</sub> or GND terminals	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 5): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T <sub>sto</sub>	. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
  - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 3. V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
  - 4. II and IO are used to denote specific conditions for II/O.
  - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
.,		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	.,
VIH	High-level control input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			V
.,	Low-level control input voltage $ \frac{V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}}{V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}} $		0	0.7	.,
$V_{IL}$			0	8.0	V
V <sub>I/O</sub>	Data input/output voltage		0	5.5	V
TA	Operating free-air temperature		-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		MIN	TYP <sup>†</sup>	MAX	UNIT		
VIK		V <sub>CC</sub> = 3.6 V,	$I_{I} = -18 \text{ mA}$				-1.8	V
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 3.6 V,	$V_{IN} = 0 \text{ to } 5.5 \text{ V}$				±1	μΑ
loz‡		V <sub>CC</sub> = 3.6 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μΑ
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_0 = 0 \text{ to } 5.5 \text{ V},$	V <sub>I</sub> = 0			1	μΑ
lcc		V <sub>CC</sub> = 3.6 V,	I <sub>I/O</sub> = 0, Switch ON or OFF,	$V_{IN} = V_{CC}$ or GND		1	3	mA
∆l <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V,	Other inputs at V <sub>CC</sub> or GND			30	μΑ
<sup>I</sup> CCD <sup>¶</sup>	Per control input	V <sub>CC</sub> = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle			0.15	0.25	mA/ MHz
C <sub>in</sub>	Control inputs	V <sub>CC</sub> = 3.3 V,	V <sub>IN</sub> = 5.5 V, 3.3 V, or	0		3.5	5	pF
C <sub>io(OFF</sub>	=)	V <sub>CC</sub> = 3.3 V,	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND,	V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		4	5	pF
C <sub>io(ON)</sub>	$C_{io(ON)}$ $V_{CC} = 3.3 \text{ V},$ Switch ON, $V_{IN} = V_{CC}$		Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND,	V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0		10	12.5	pF
		$V_{CC} = 2.3 \text{ V},$	$V_{I} = 0,$	$I_O = 30 \text{ mA}$		5	8	
#		TYP at $V_{CC} = 2.5 \text{ V}$	V <sub>I</sub> = 1.7 V,	$I_{O} = -15 \text{ mA}$		5	9	Ω
r <sub>on</sub> #		Vac - 2 V	V <sub>I</sub> = 0,	I <sub>O</sub> = 30 mA		5	7	22
		VCC = 3 V	$V_{I} = 2.4 \text{ V},$ $I_{O} = -15 \text{ mA}$			5	9	

NOTE 7: V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO	V <sub>CC</sub> =	2.5 V 2 V	V <sub>CC</sub> =	3.3 V 3 V	UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
fOE	ŌĒ	A or B		10		20	MHz
t <sub>pd</sub> ☆	A or B	B or A		0.15		0.25	ns
t <sub>en</sub>	ŌE	A or B	1.5	9	1.5	8	ns
<sup>t</sup> dis	ŌĒ	A or B	1	8	1	7	ns

Il Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5$  V,  $R_L \ge 1$  M $\Omega$ ,  $C_L = 0$ )



 $<sup>^{\</sup>dagger}$  All typical values are at VCC = 3.3 V (unless otherwise noted), TA = 25  $^{\circ}$  C.

<sup>&</sup>lt;sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

<sup>¶</sup> This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

<sup>#</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

<sup>\*</sup>The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

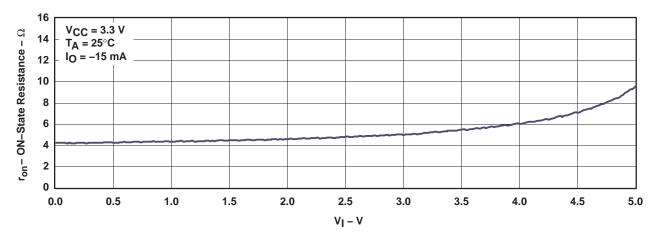


Figure 1. Typical  $r_{on}$  vs  $V_{I}$ 

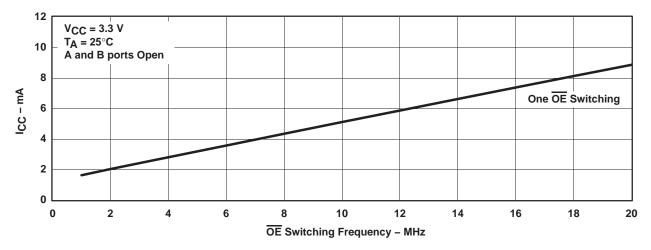
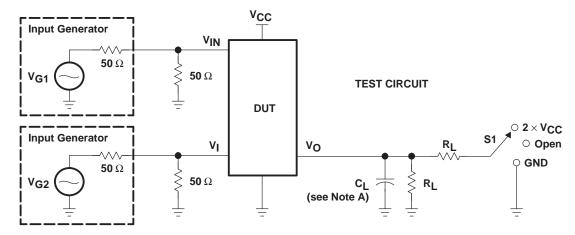


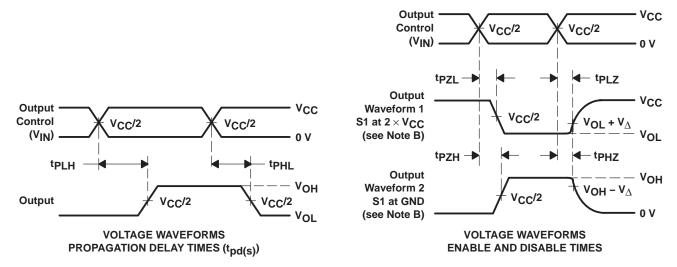
Figure 2. Typical I<sub>CC</sub> vs  $\overline{\text{OE}}$  Switching Frequency



#### PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	$v_{\!\scriptscriptstyle\Delta}$
tpd(s)	2.5 V $\pm$ 0.2 V	Open	500 Ω	V <sub>CC</sub> or GND	30 pF	
-pu(s)	3.3 V $\pm$ 0.3 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
tplz/tpzl	2.5 V $\pm$ 0.2 V	2×V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
'PLZ''PZL	3.3 V $\pm$ 0.3 V	2×V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
4/4	2.5 V ± 0.2 V	GND	500 Ω	VCC	30 pF	0.15 V
tPHZ/tPZH	3.3 V $\pm$ 0.3 V	GND	500 Ω	VCC	50 pF	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms









#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CB3Q16210DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16210DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16210DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16210DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16210DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16210DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16210DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16210DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16210DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16210DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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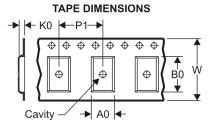
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PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





1	40	Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
ŀ	⟨0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
T	P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q16210DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74CB3Q16210DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CB3Q16210DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q16210DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74CB3Q16210DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0
SN74CB3Q16210DLR	SSOP	DL	48	1000	346.0	346.0	49.0

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

## DL (R-PDSO-G\*\*)

### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

## DGV (R-PDSO-G\*\*)

### **24 PINS SHOWN**

### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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