- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 1000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Operating Voltage Range of 4.5 V to 5.5 V**
- **High-Current Outputs Drive Up To 15 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 13 ns**
- **$\pm$6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

PW PACKAGE
(TOP VIEW)

1$\overline{\text{OE}}$	1	20	V_{CC}
1A1	2	19	2$\overline{\text{OE}}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
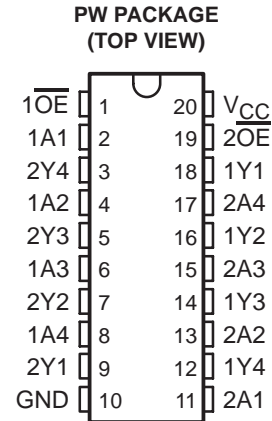
description/ordering information

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT244 device is organized as two 4-bit buffers/drivers with separate output-enable ($\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{\text{OE}}$ is high, the outputs are in the high-impedance state.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	TSSOP – PW	Tape and reel	SN74HCT244QPWRQ1	HT244Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTION TABLE
(each buffer/driver)

| INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
L	H	H
L	L	L
H	X	Z

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TEXAS INSTRUMENTS

logic diagram (positive logic)
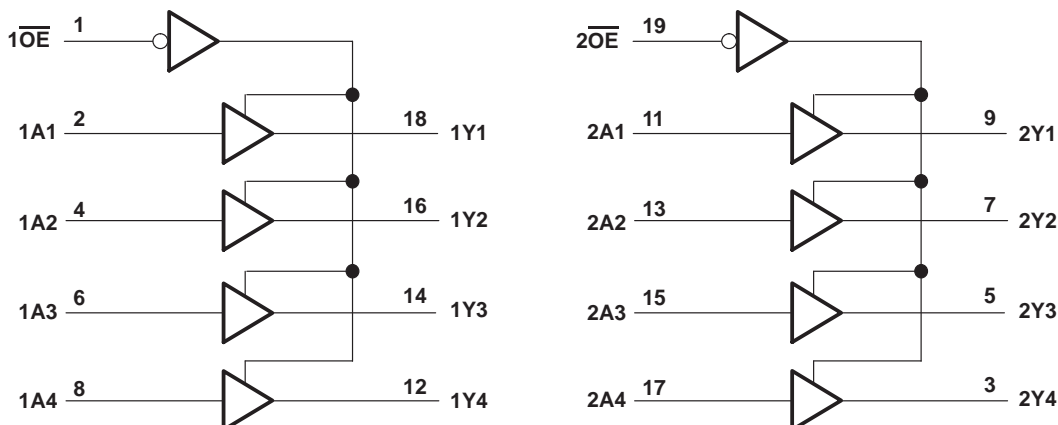
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND .... ±70 mA
Package thermal impedance, θ_{JA} (see Note 2) .... 83°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500	ns
T_A	Operating free-air temperature		–40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	4.5 V	4.4	4.499		4.4		V
		$I_{OH} = -6\ mA$		3.98	4.3		3.7		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	4.5 V		0.001	0.1		0.1	V
		$I_{OL} = 6\ mA$			0.17	0.26		0.4	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0,	$V_I = V_{IH}$ or V_{IL}	5.5 V		±0.01	±0.5		±10	μA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	5.5 V			8		160	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3	mA
C_i			4.5 V to 5.5 V		3	10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	4.5 V		15	28		42	ns
			5.5 V		13	25		38	
t_{en}	$\overline{OE}$	Y	4.5 V		21	35		53	ns
			5.5 V		19	32		48	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	35		53	ns
			5.5 V		18	32		48	
t_t		Y	4.5 V		8	12		18	ns
			5.5 V		7	11		16	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	4.5 V		21	45		68	ns
			5.5 V		18	40		61	
t_{en}	$\overline{OE}$	Y	4.5 V		25	52		79	ns
			5.5 V		22	47		71	
t_t		Y	4.5 V		17	42		63	ns
			5.5 V		14	38		57	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT
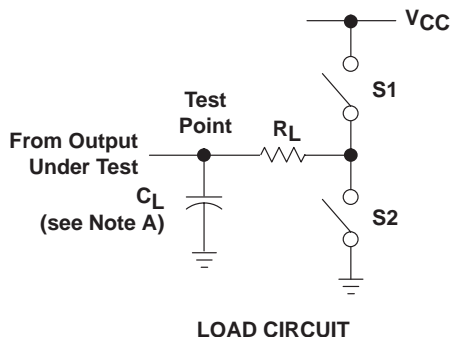
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS
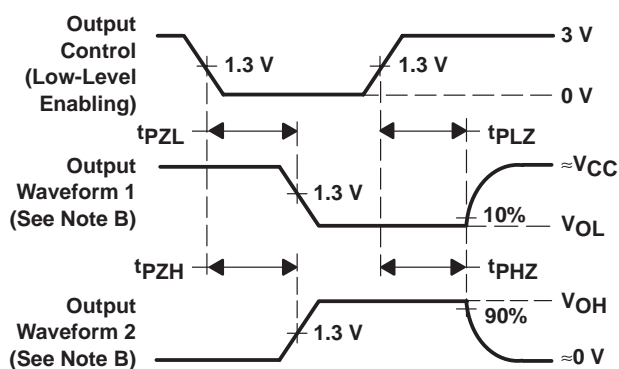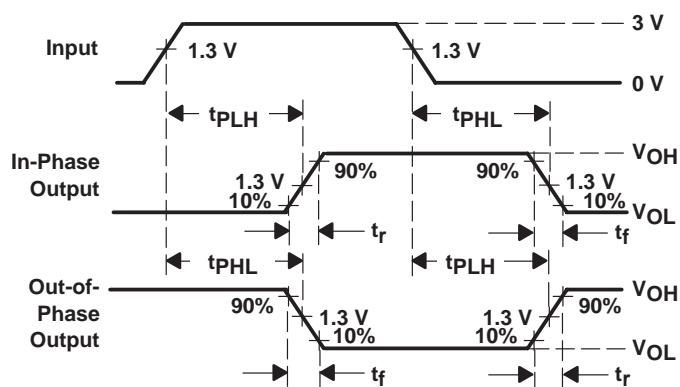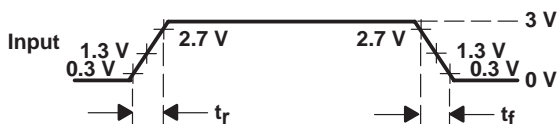
NOTES: A. C_L includes probe and test-fixture capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following
    characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74HCT244QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT244Q	Samples
SN74HCT244QPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	HT244Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74HCT244-Q1 :

- Catalog: SN74HCT244

- Enhanced Product: SN74HCT244-EP

- Military: SN54HCT244

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT244QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT244QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT244QPWRG4Q1	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HCT244QPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ 0,10 Ⓜ

20   11

4,50 / 4,30   6,60 / 6,20

1   10

6,60 / 6,40

△C

0,15 NOM

Gage Plane

0°−8°   0,25

0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane   ◁ 0,10

4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
        △C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
        △D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

PW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

5,6

1,55

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284-5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
           contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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