- **Member of the Texas Instruments** Widebus™ Family
- 5- $\Omega$  Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- **I**off Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

#### description/ordering information

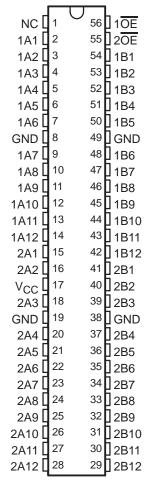
The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable  $(\overline{OE})$ inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is on, and port A is connected to port B. When OE is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

#### ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
			SN74CBTLV16211DL	ODTI \
-40°C to 85°C	SSOP – DL	Tape and reel	SN74CBTLV16211DLR	CBTLV16211
-40 C to 65 C	TSSOP – DGG	Tape and reel	SN74CBTLV16211GR	CBTLV16211
	TVSOP – DGV Tape and reel		SN74CBTLV16211VR	CN211

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

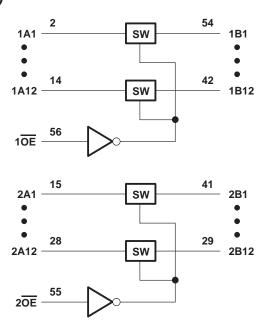
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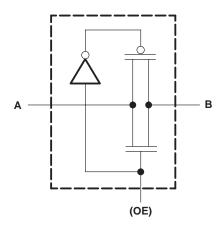
## FUNCTION TABLE (each 12-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect

## logic diagram (positive logic)



## simplified schematic, each FET switch



## SN74CBTLV16211 LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS043I - DECEMBER 1997 - REVISED OCTOBER 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	): DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T <sub>stg</sub>		. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
.,	$V_{CC} = 2.3 \text{ V to}$	2.7 V	1.7		.,
VIH	High-level control input voltage $V_{CC} = 2.7 \text{ V to}$	3.6 V	2		V
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	$V_{CC} = 2.3 \text{ V to}$	2.7 V		0.7	
V <sub>IL</sub>	Low-level control input voltage  VCC = 2.7 V to	3.6 V		0.8	V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITIO	DNS	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK		V <sub>CC</sub> = 3 V,	I <sub>I</sub> = -18 mA				-1.2	V
II		V <sub>CC</sub> = 3.6 V,	$V_I = V_{CC}$ or GND				±1	μΑ
l <sub>off</sub>		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 3.6 $V$				10	μΑ
Icc		$V_{CC} = 3.6 \text{ V},$	I <sub>O</sub> = 0,	$V_I = V_{CC}$ or GND			10	μΑ
Δl <sub>CC</sub> ‡	Control inputs	$V_{CC} = 3.6 \text{ V},$	One input at 3 V,	Other inputs at V <sub>CC</sub> or GND			300	μΑ
Ci	Control inputs	V <sub>I</sub> = 3.3 V or 0				4.5		pF
C <sub>io(OFF</sub>	=)	$V_O = 3.3 \text{ V or } 0,$	OE = V <sub>CC</sub>			6.5		pF
		.,		I <sub>I</sub> = 64 mA		5	8	
		$V_{CC} = 2.3 \text{ V},$ TYP at $V_{CC} = 2.5 \text{ V}$	V <sub>I</sub> = 0	I <sub>I</sub> = 24 mA		5	8	
8		1111 di VCC = 2.5 V	V <sub>I</sub> = 1.7 V,	I <sub>I</sub> = 15 mA		27	40	0
r <sub>on</sub> §				I <sub>I</sub> = 64 mA		5	7	Ω
		VCC = 3 V	V <sub>I</sub> = 0	I <sub>I</sub> = 24 mA		5	7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		10	15	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V (unless otherwise noted),  $T_A$  = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

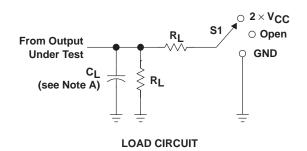
PARAMETER	FROM (INPUT)	TO	V <sub>CC</sub> = ± 0.2		V <sub>CC</sub> =		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A		0.15		0.25	ns
t <sub>en</sub>	ŌĒ	A or B	1	7	1	6.2	ns
<sup>t</sup> dis	ŌĒ	A or B	1	7.2	1	7.7	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

<sup>‡</sup> This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

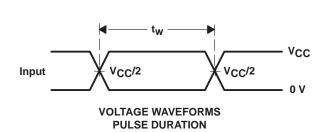
<sup>§</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

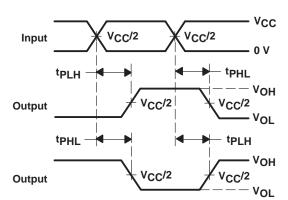
#### PARAMETER MEASUREMENT INFORMATION



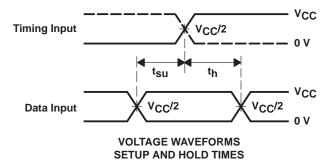
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

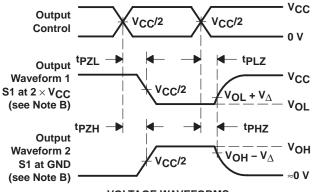
VCC	CL	RL	$v_{\scriptscriptstyle\Delta}$
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS





VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  2 ns,  $t_f \leq$  2 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F. tpZL and tpZH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







com 27-Sep-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
74CBTLV16211DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV16211DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV16211GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV16211GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV16211VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTLV16211VRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV16211DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV16211DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV16211GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTLV16211VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

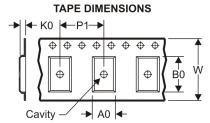
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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74CBTLV16211GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBTLV16211VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1





\*All dimensions are nominal

7 III GITTIOTIOTOTIC GITC TIGITIITIGI							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV16211DLR	SSOP	DL	56	1000	346.0	346.0	49.0
SN74CBTLV16211GR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBTLV16211VR	TVSOP	DGV	56	2000	346.0	346.0	41.0

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

### DL (R-PDSO-G\*\*)

#### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

## DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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