

## LOW NOISE, VERY LOW DRIFT, PRECISION VOLTAGE REFERENCE

Check for Samples: [REF5025-HT](#)

### FEATURES

- Low Temperature Drift: 40 ppm/°C
- Low Noise: 3  $\mu\text{V}_{\text{PP}}/\text{V}$
- High Output Current:  $\pm 7$  mA

### APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

### SUPPORTS EXTREME TEMPERATURE APPLICATIONS

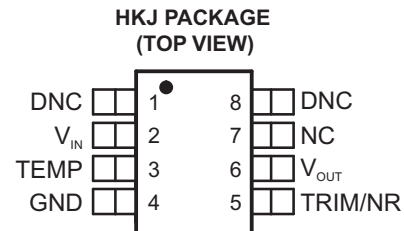
- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme ( $-55^{\circ}\text{C}/210^{\circ}\text{C}$ ) Temperature Range <sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

(1) Custom temperature ranges available

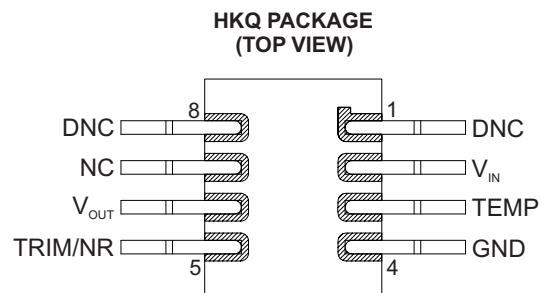
### DESCRIPTION

The REF5025 is a low-noise, low-drift, very high precision voltage reference. This reference is capable of both sinking and sourcing, and is very robust with regard to line and load changes.

Temperature drift (40 ppm/°C) from  $-55^{\circ}\text{C}$  to  $210^{\circ}\text{C}$  is achieved using proprietary design techniques. These features combined with very low noise make the REF5025 ideal for use in down-hole drilling applications.



DNC = Do not connect  
NC = No internal connection



HKQ as formed or HKJ mounted dead bug



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	GND	Al-Cu (0.5%)	598 nm

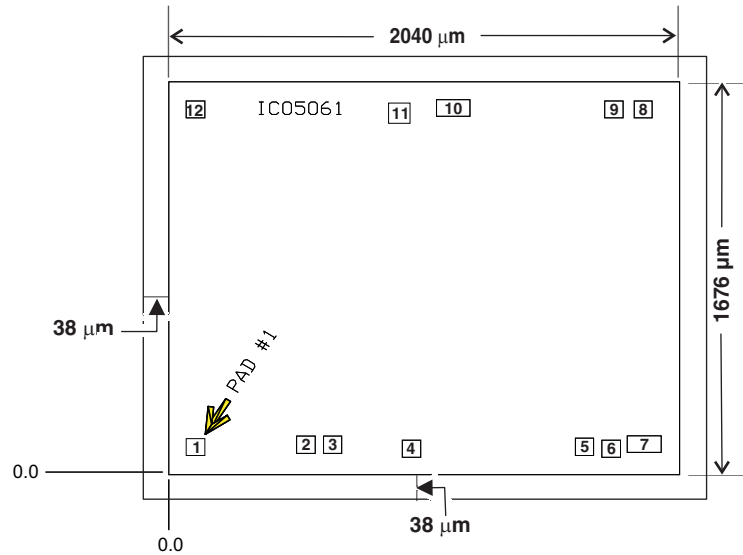


Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X min	Y min	X max	Y max
NC	1	35.45	46.55	111.45	122.55
NC	2	496.75	56.55	572.75	132.55
VIN	3	607.45	56.55	683.45	132.55
NC	4	937.9	39.4	1013.9	115.4
TEMP	5	1660.1	47.2	1736.1	123.2
GND	6	1770.9	38.85	1847.05	115
GND	7	1877.1	59.6	2016.8	135.6
TRIM/NR	8	1904.65	1553.4	1980.65	1629.4
NC	9	1782.15	1553.4	1858.15	1629.4
VOUT	10	1080.2	1559.85	1219.9	1636
VOUT	11	880.25	1543.55	956.25	1619.55
NC	12	35.45	1553.45	111.45	1629.45

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD (bare die)	REF5025SKGD1	NA
		REF5025SKGD2	
	HKJ	REF5025SHKJ	REF5025SHKJ
	HKQ	REF5025SHKQ	REF5025SHKQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

			UNIT
Input Voltage		18	V
Output Short-Circuit		30	mA
Operating Temperature Range		–55 to 210	°C
Storage Temperature Range		–65 to 210	°C
Junction Temperature (T <sub>J</sub> max)		210	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

**THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE**

over operating free-air temperature range (unless otherwise noted)

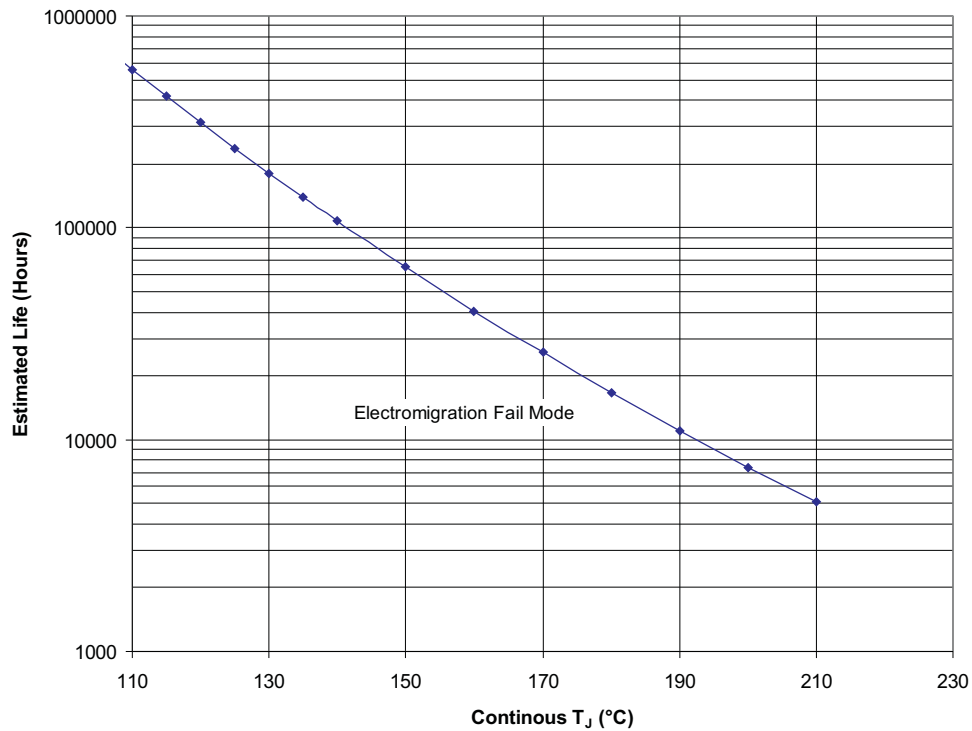
PARAMETER		MIN	TYP	MAX	UNIT
θ <sub>JC</sub>	Junction-to-case thermal resistance	to ceramic side of case		5.7	°C/W
		to top of case lid (metal side of case)		13.7	

**ELECTRICAL CHARACTERISTICS**

T<sub>A</sub> = 25°C, I<sub>LOAD</sub> = 0, C<sub>L</sub> = 1 μF, V<sub>IN</sub> = 3.25 V to 18 V (unless otherwise noted).

PARAMETER	CONDITIONS	T <sub>A</sub> = –55 to 125°C			T <sub>A</sub> = 210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT VOLTAGE (2.5 V)</b>								
Output voltage V <sub>OUT</sub>			2.5			2.5		V
Initial accuracy <sup>(1)</sup>	V <sub>IN</sub> = 3.25 V	0		0.9		0.14		%
<b>NOISE</b>								
Output voltage noise	f = 0.1 Hz to 10 Hz		7.5					μV <sub>PP</sub>
<b>OUTPUT VOLTAGE TEMPERATURE DRIFT</b>								
Output voltage temperature drift <sup>(2)</sup> dV <sub>OUT</sub> /dT	Calculated from –55°C to 210°C						40	ppm/°C
<b>LINE REGULATION</b>								
Line regulation dV <sub>OUT</sub> /dV <sub>IN</sub>	From V <sub>IN</sub> = 3.25 V to V <sub>IN</sub> = 18 V		1	2.2		63	215	ppm/V
<b>LOAD REGULATION</b>								
Load regulation dV <sub>OUT</sub> /dI <sub>LOAD</sub>	–7 mA < I <sub>LOAD</sub> < 10 mA, V <sub>IN</sub> = 3.25 V		20	50		20	75	ppm/mA
<b>SHORT-CIRCUIT CURRENT</b>								
Short-circuit current I <sub>SC</sub>	V <sub>OUT</sub> = 0 V		25			11		mA
<b>TEMP PIN</b>								
Voltage output	At T <sub>A</sub> = 25°C		575					mV
Temperature sensitivity <sup>(3)</sup>			2.64					mV/°C
<b>TURN-ON SETTLING TIME</b>								
Turn-on settling time	To 0.1% with C <sub>L</sub> = 1 μF		200					μs
<b>POWER SUPPLY</b>								
Supply voltage V <sub>S</sub>		3.25		18	3.25		18	V
Quiescent current			0.8	1.2			1.5	mA
<b>TEMPERATURE RANGE</b>								
Specified range	–55°C to 210°C							
Operating range	–55°C to 210°C							

- (1) Refer to [Figure 5](#) of the TYPICAL CHARACTERISTICS.  
 (2) Refer to [Figure 4](#) of the TYPICAL CHARACTERISTICS.  
 (3) Refer to [Figure 10](#) of the TYPICAL CHARACTERISTICS.



**Figure 1. REF5025SKGD1 / REF5025SKGD2 Operating Life Derating Chart**

Notes:

1. See datasheet for Absolute Maximum and minimum Recommended Operating Conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature ( does not include package interconnect life).

**TYPICAL CHARACTERISTICS**

$T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $V_S = 3.25\text{ V}$  (unless otherwise noted).

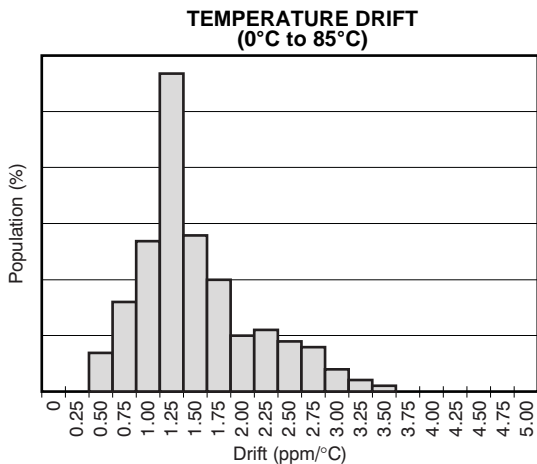


Figure 2.

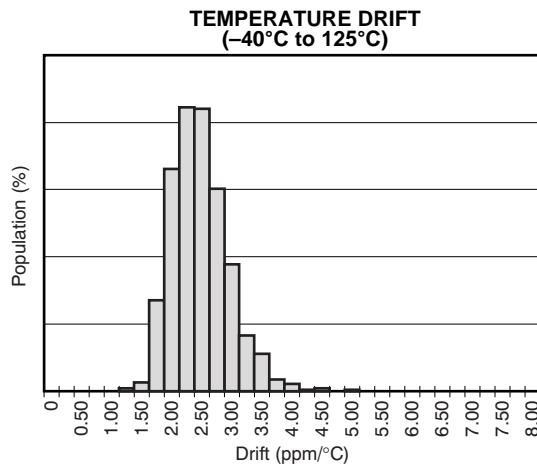


Figure 3.

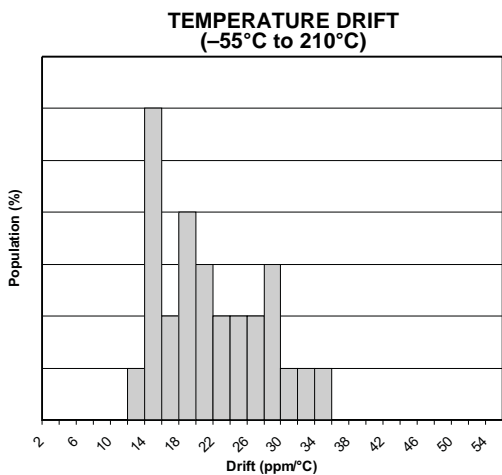


Figure 4.

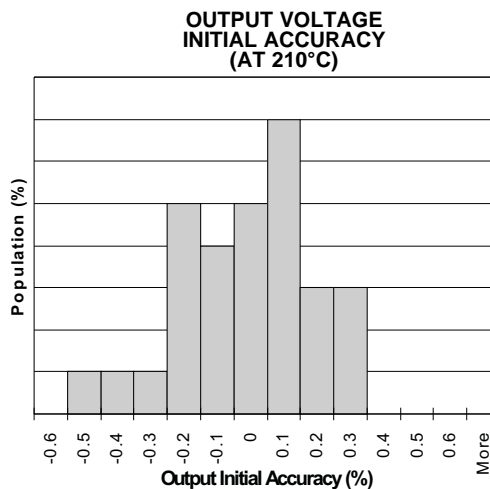


Figure 5.

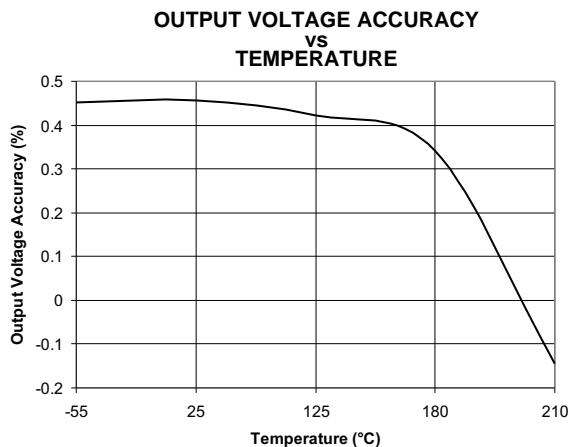


Figure 6.

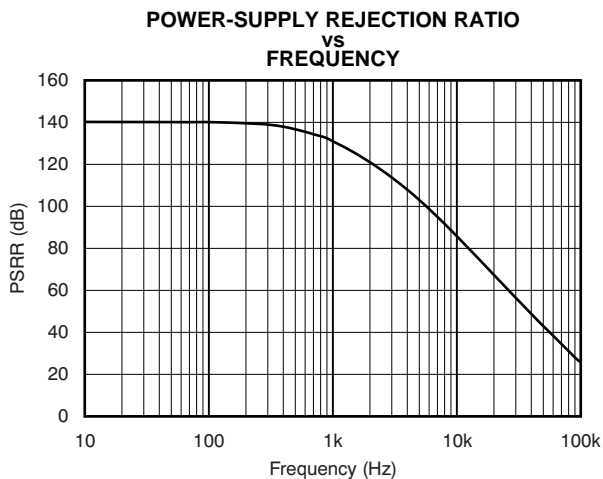


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**

$T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $V_S = 3.25\text{ V}$  (unless otherwise noted).

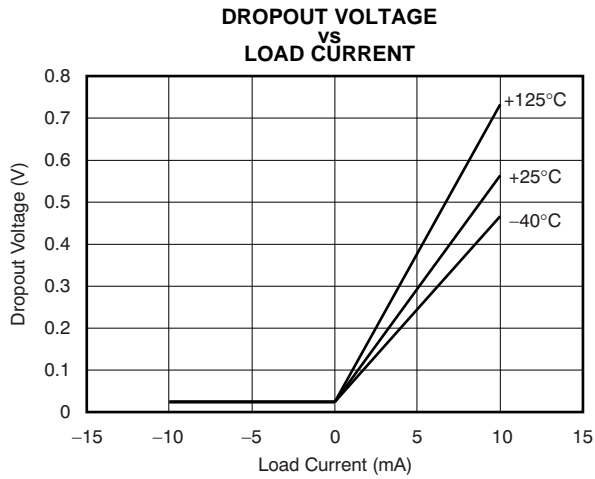


Figure 8.

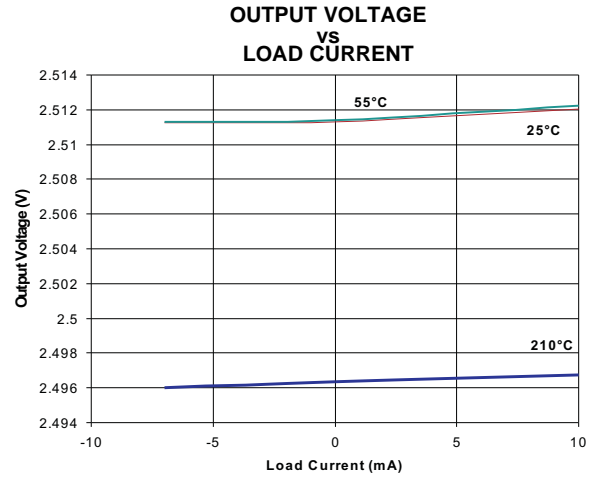


Figure 9.

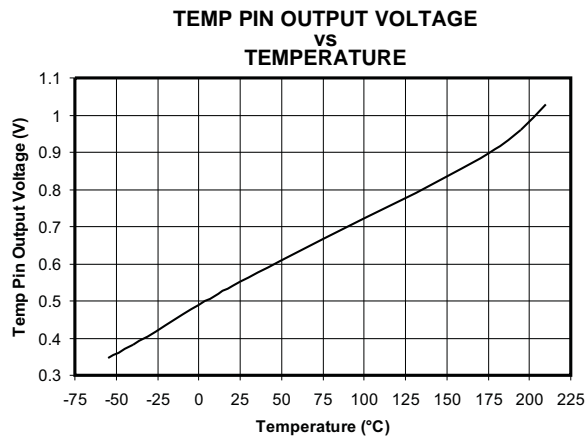


Figure 10.

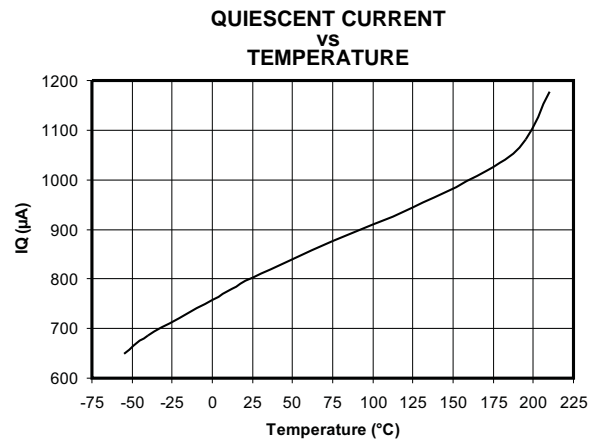


Figure 11.

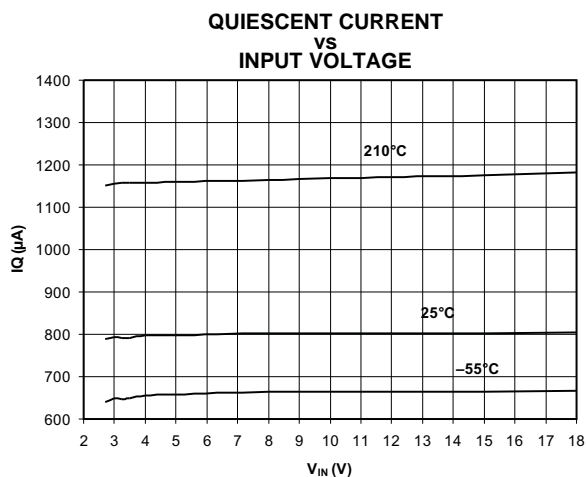


Figure 12.

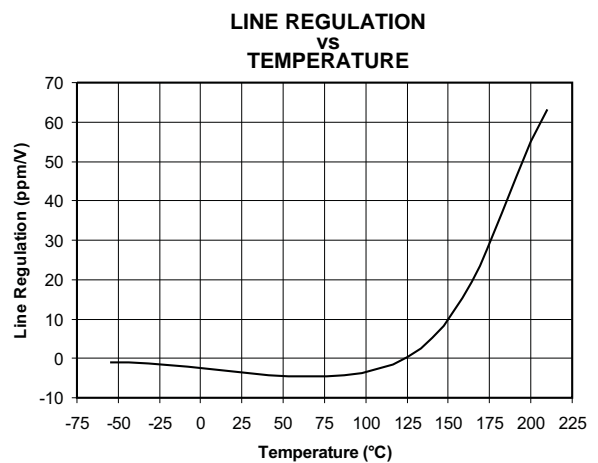


Figure 13.

**TYPICAL CHARACTERISTICS (continued)**

$T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $V_S = 3.25\text{ V}$  (unless otherwise noted).

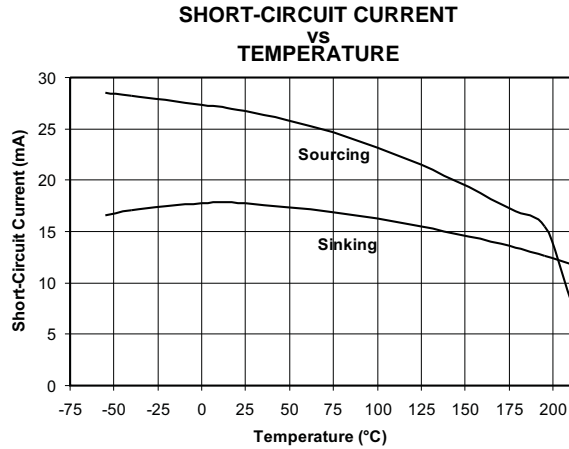


Figure 14.

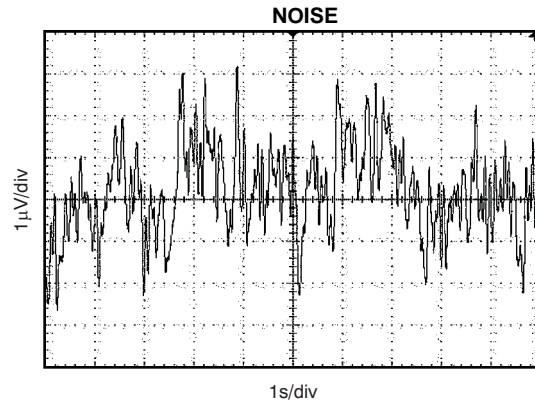


Figure 15.

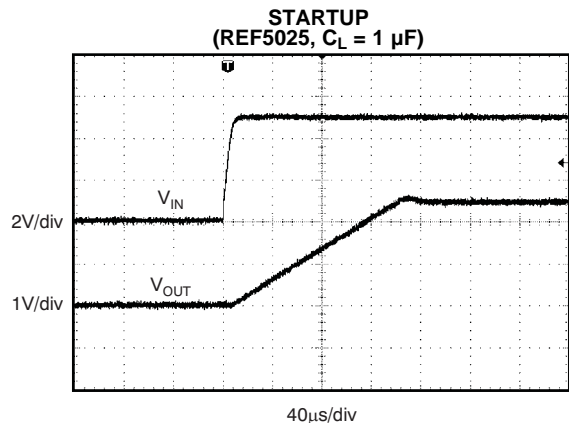


Figure 16.

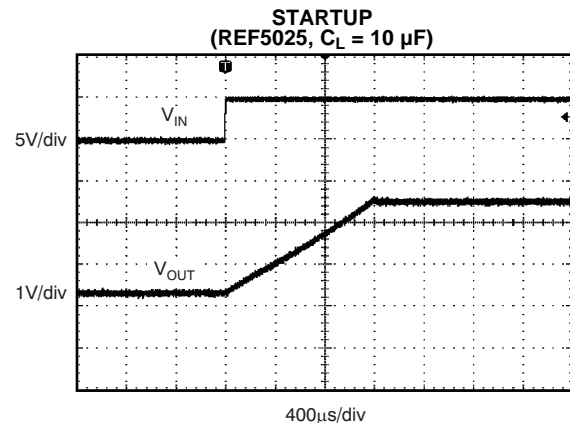


Figure 17.

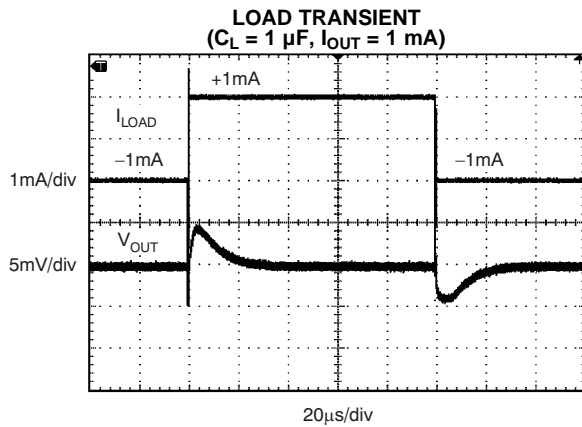


Figure 18.

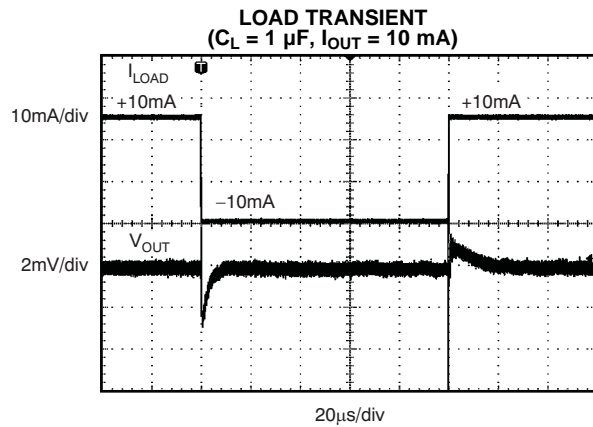


Figure 19.

### TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $V_S = 3.25\text{ V}$  (unless otherwise noted).

**LOAD TRANSIENT**  
( $C_L = 10\ \mu\text{F}$ ,  $I_{\text{OUT}} = 1\ \text{mA}$ )

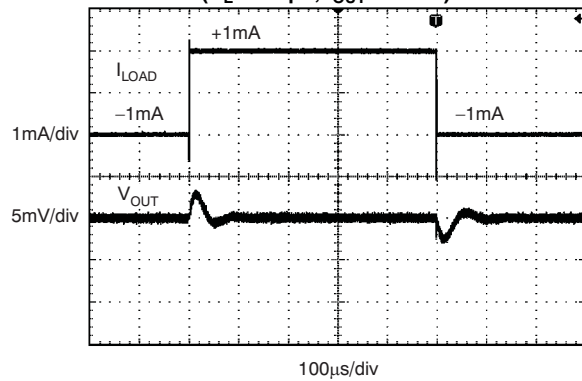


Figure 20.

**LOAD TRANSIENT**  
( $C_L = 10\ \mu\text{F}$ ,  $I_{\text{OUT}} = 10\ \text{mA}$ )

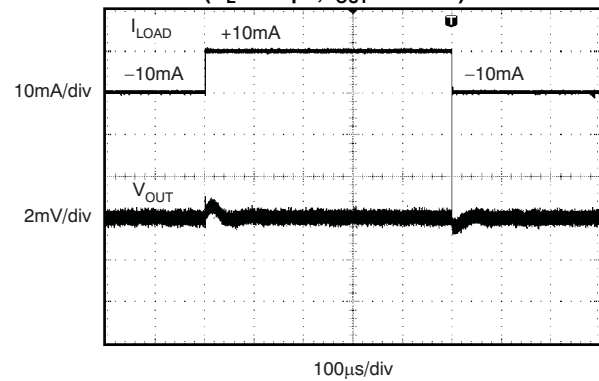


Figure 21.

**LINE TRANSIENT**  
( $C_L = 1\ \mu\text{F}$ )

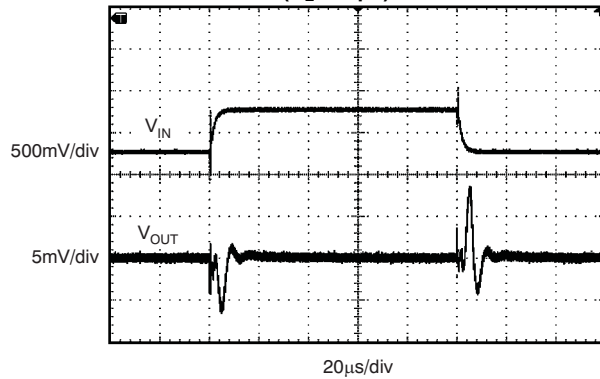


Figure 22.

**LINE TRANSIENT**  
( $C_L = 10\ \mu\text{F}$ )

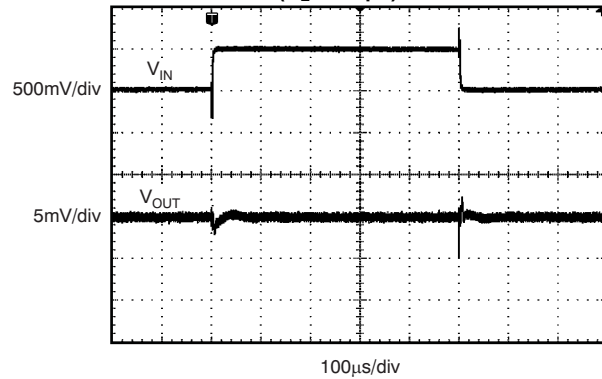


Figure 23.



## APPLICATION INFORMATION

The REF5025 is a low-noise, precision bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. Figure 24 shows a simplified block diagram of the REF5025.

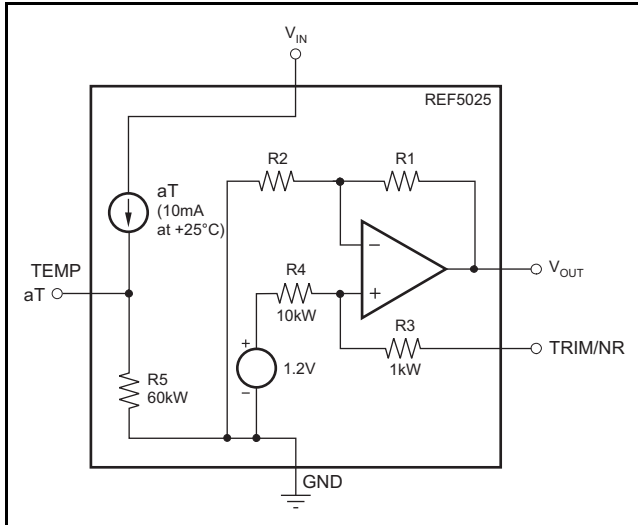


Figure 24. REF5025 Simplified Block Diagram

## BASIC CONNECTIONS

Figure 25 shows the typical connections for the REF5025. A supply bypass capacitor ranging between 1  $\mu\text{F}$  to 10  $\mu\text{F}$  is recommended. A 1- $\mu\text{F}$  to 50- $\mu\text{F}$ , low-ESR output capacitor ( $C_L$ ) must be connected from  $V_{OUT}$  to GND. The ESR value should be less than or equal to 1.5  $\Omega$ . The ESR minimizes gain peaking of the internal 1.2-V reference and thus reduces noise at the  $V_{OUT}$  pin.

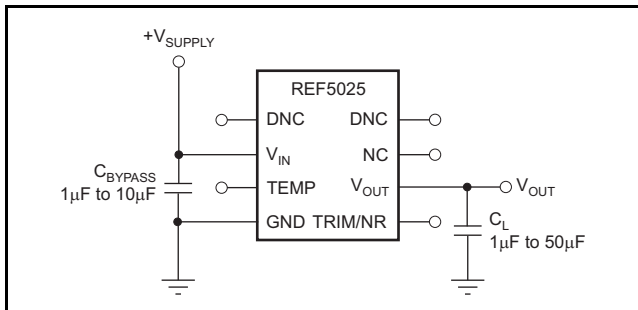


Figure 25. Basic Connections

## SUPPLY VOLTAGE

The REF5025 features extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 8 of *Typical Characteristics*.

## USING THE TRIM/NR PIN

The REF5025 provides a very accurate voltage output. However,  $V_{OUT}$  can be adjusted to reduce noise and shift the output voltage from the nominal value by configuring the trim and noise reduction pin (TRIM/NR, pin 5). The TRIM/NR pin provides a  $\pm 15\text{-mV}$  adjustment of the device bandgap, which produces a  $\pm 15\text{-mV}$  change on the  $V_{OUT}$  pin. Figure 26 shows a typical circuit using the TRIM/NR pin to adjust  $V_{OUT}$ . When using this technique, the temperature coefficients of the resistors can degrade the temperature drift at the output.

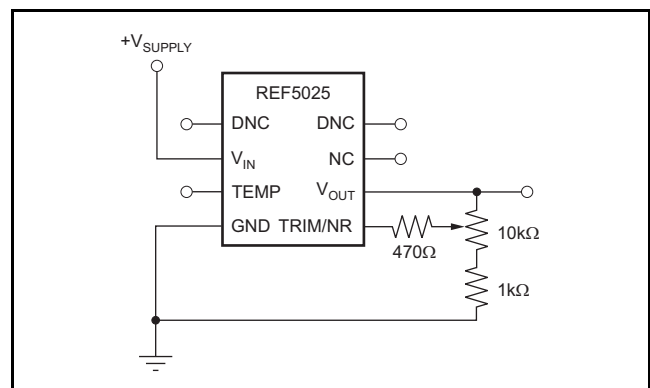


Figure 26.  $V_{OUT}$  Adjustment Using TRIM/NR Pin

The REF5025 allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (as Figure 27 illustrates) in combination with the internal 1-k $\Omega$  resistor creates a low-pass filter that lowers the overall noise measured on the  $V_{OUT}$  pin. A capacitance of 1  $\mu\text{F}$  is suggested for a low-pass filter with a corner frequency of 14.5 Hz. Higher capacitance results in a lower cutoff frequency.

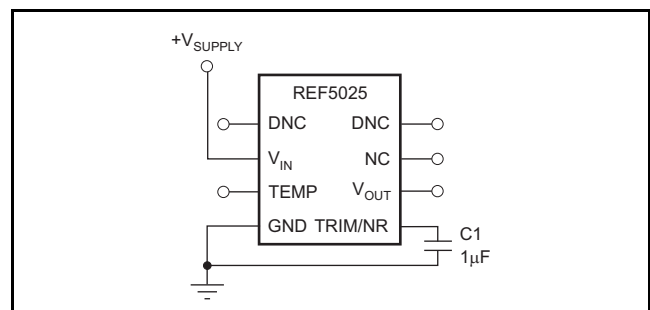


Figure 27. Noise Reduction Using TRIM/NR Pin

## TEMPERATURE DRIFT

The REF5025 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left( \frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

## TEMPERATURE MONITORING

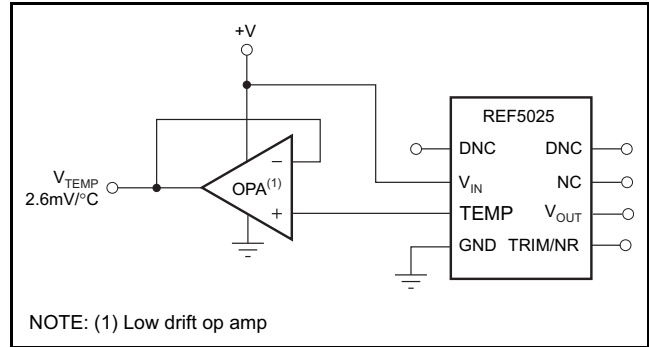
The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-k $\Omega$  source impedance. As seen in [Figure 10](#), the output voltage follows the nominal relationship:

$$V_{\text{TEMP PIN}} = 509 \text{ mV} + 2.64 \times T(^{\circ}\text{C}) \quad (2) \quad (2)$$

(For  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  only. Refer to [Figure 10](#) of the TYPICAL CHARACTERISTICS for  $125^{\circ}\text{C}$  to  $210^{\circ}\text{C}$ .)

This pin indicates general chip temperature, accurate to approximately  $\pm 15^{\circ}\text{C}$ . Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of  $30^{\circ}\text{C}$  corresponds to an approximate 79-mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see [Figure 24](#)). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on  $V_{\text{OUT}}$  accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp as shown in [Figure 28](#).



**Figure 28. Buffering the TEMP Pin Output**

## POWER DISSIPATION

The REF5025 is specified to deliver current loads of  $\pm 10$  mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3) \quad (3)$$

Where:

$T_J$  = Junction temperature ( $^{\circ}\text{C}$ )

$T_A$  = Ambient temperature ( $^{\circ}\text{C}$ )

$P_D$  = Power dissipated (W)

$\theta_{JA}$  = Junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

The REF5025 junction temperature must not exceed the absolute maximum rating of  $210^{\circ}\text{C}$ .

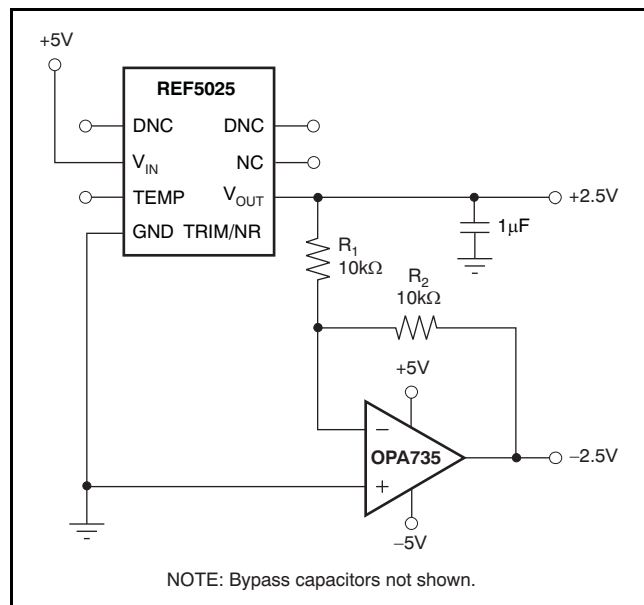
## NOISE PERFORMANCE

Typical 0.1-Hz to 10-Hz voltage noise for each member of the REF5025 is specified in the Electrical Characteristics table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

## APPLICATION CIRCUITS

### NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF5025 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 29 shows the REF5025 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF5025 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of  $R_1$  and  $R_2$ .

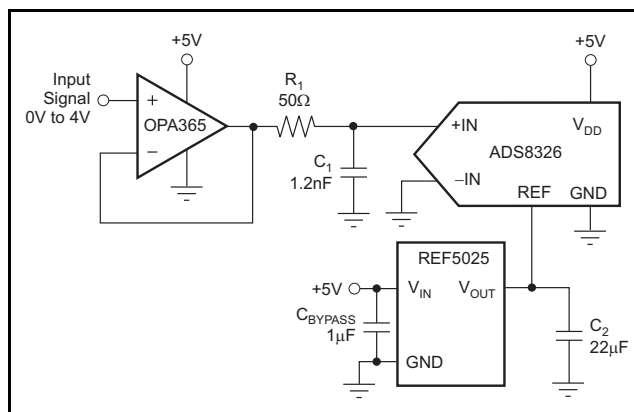


A. OPA735 has not been characterized or tested at 210°C.

**Figure 29. The REF5025 and OPA735 Create Positive and Negative Reference Voltages**

### DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF5025 features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 30 shows the REF5025 in a basic data acquisition system.



A. OPA365 and ADS8326 have not been characterized or tested at 210°C.

**Figure 30. Basic Data Acquisition System**

## REVISION HISTORY

Changes from Revision D (April 2012) to Revision E	Page
• Added KGD2 package option .....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5025SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	REF5025S HKJ	<a href="#">Samples</a>
REF5025SHKQ	ACTIVE	CFP	HKQ	8	25	TBD	AU	N / A for Pkg Type	-55 to 210	REF5025S HKQ	<a href="#">Samples</a>
REF5025SKGD1	ACTIVE	XCEPT	KGD	0	195	TBD	Call TI	N / A for Pkg Type	-55 to 210		<a href="#">Samples</a>
REF5025SKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	N / A for Pkg Type	-55 to 210		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF REF5025-HT :**

- Catalog: [REF5025](#)
- Enhanced Product: [REF5025-EP](#)

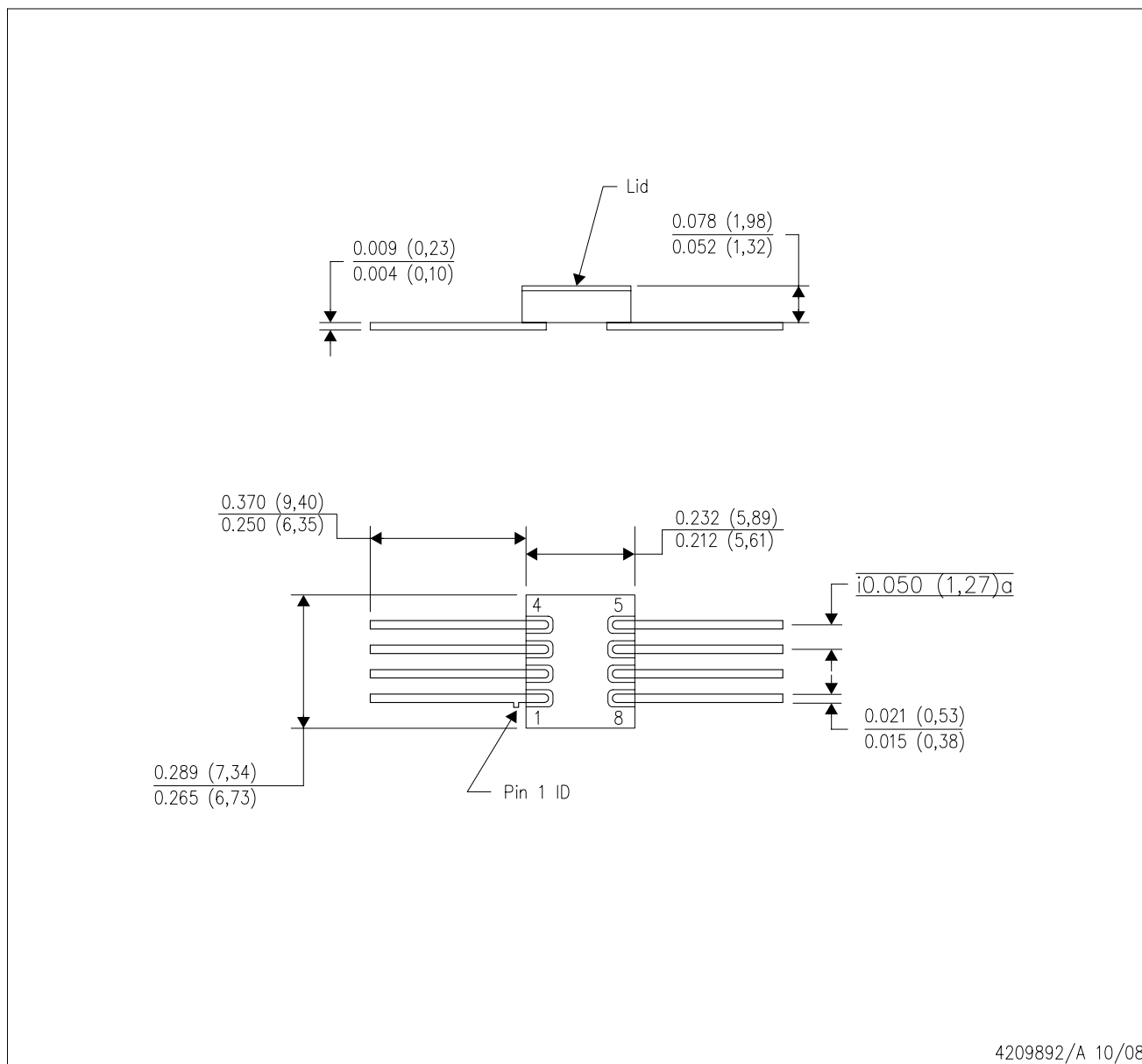
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

# MECHANICAL DATA

HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK

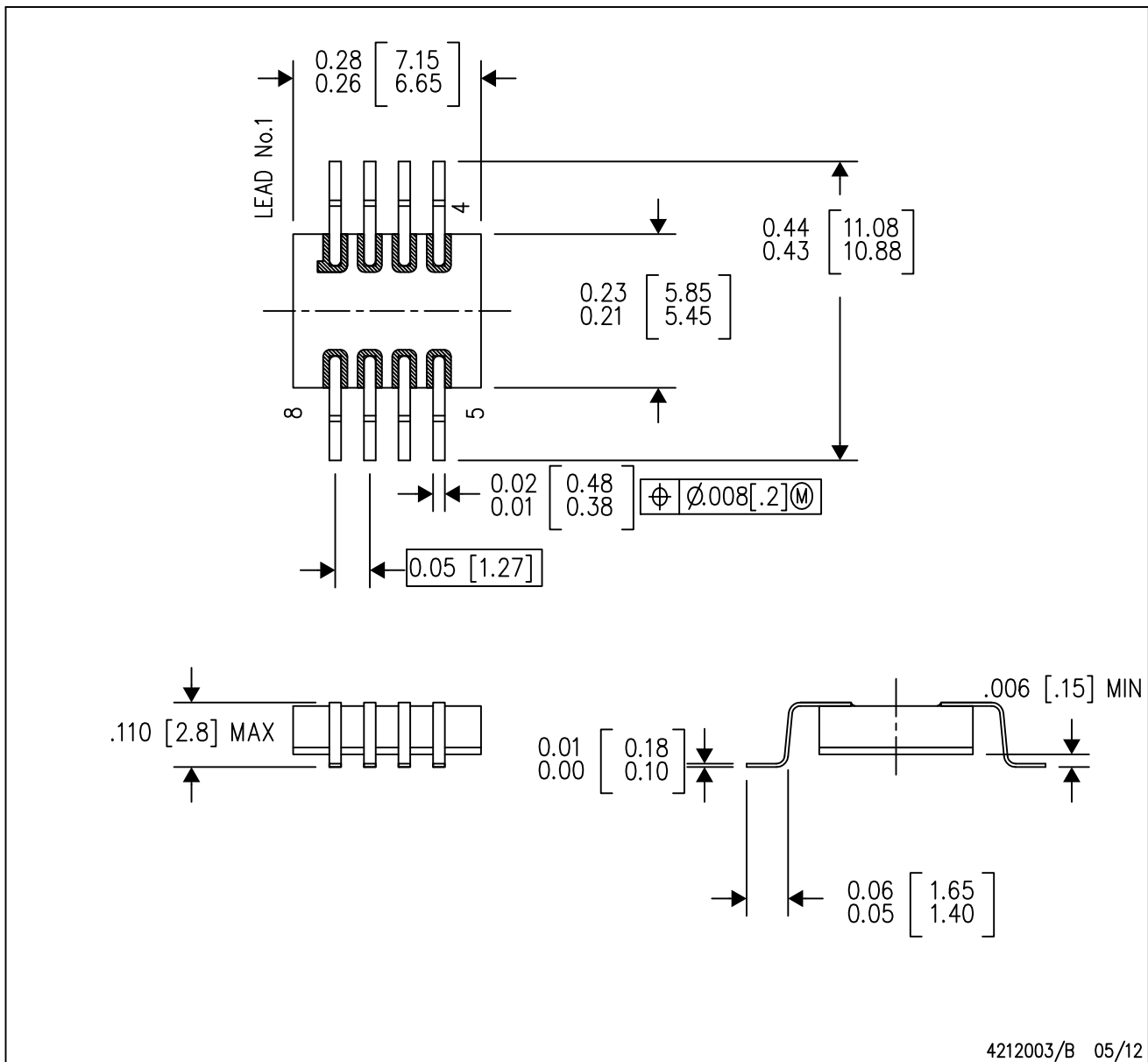


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals will be gold plated.

# MECHANICAL DATA

HKQ (R-CDFP-G8)

CERAMIC GULL WING



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals will be gold plated.
  - Lid is not connected to any lead.



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