TLV34xx Low-Voltage Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown

1 Features

- 1.8-V and 5-V Performance
- Low Offset (A Grade)
  - 1.25 mV Maximum (25°C)
  - 1.7 mV Maximum (–40°C to 125°C)
- Rail-to-Rail Output Swing
- Wide Common-Mode Input Voltage Range: –0.2 V to (V_+ – 0.5 V)
- Input Bias Current: 1 pA (Typical)
- Input Offset Voltage: 0.3 mV (Typical)
- Low Supply Current: 70 μA/Channel
- Low Shutdown Current: 10 pA (Typical) Per Channel
- Gain Bandwidth: 2.3 MHz (Typical)
- Slew Rate: 0.9 V/μs (Typical)
- Turnon Time From Shutdown: 5 μs (Typical)
- Input Referred Voltage Noise (at 10 kHz): 20 nV/$\sqrt{Hz}$
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (HBM)
  - 750-V Charged-device model (CDM)

2 Applications

- Cellular Phones
- Consumer Electronics (Laptops)
- Audio Preamplifier for Voice
- Portable and Battery-Powered Electronic Equipment
- Supply Current Monitoring
- Battery Monitoring
- Buffers
- Filters

3 Description

The TLV34xx devices are single and dual CMOS operational amplifiers, respectively, with low-voltage, low-power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typical) and an offset voltage of 0.3 mV (typical). For applications requiring excellent dc precision, the A grade (TLV34xA) has a low offset voltage of 1.25 mV (maximum) at 25°C.

These single-supply amplifiers are designed specifically for ultra-low-voltage (1.5 V to 5 V) operation, with a common-mode input voltage range that typically extends from –0.2 V to 0.5 V from the positive supply rail.

The TLV341 (single) and TLV342 (dual) in the RUG package also offer a shutdown (SHDN) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 45 pA (typical). Offered in both the SOT-23 and smaller SC70 packages, the TLV341 is suitable for the most space-constrained applications. The dual TLV342 is offered in the standard SOIC, VSSOP, and X2QFN packages.

An extended industrial temperature range from –40°C to 125°C makes the TLV34xx suitable in a wide variety of commercial and industrial applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV341	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm
	SOT (6)	1.60 mm × 1.20 mm
TLV342	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	X2QFN (10)	1.50 mm × 2.00 mm
TLV342S	X2QFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Sample and Hold Circuit Using Two TLV341

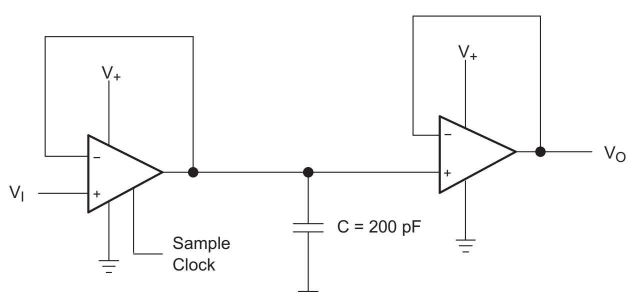

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Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2007) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed DPK package and TLV344 part from the *Pin Configuration and Functions* table 3

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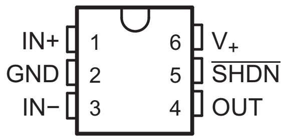
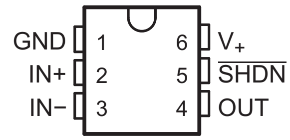
5 Pin Configuration and Functions

TLV341 DBV or DCK Package
6-Pin SOT-23 or SC70
Top View



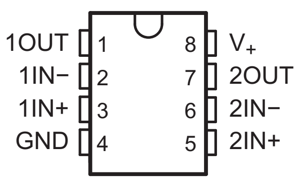
TLV341 DRL Package
6-Pin SOT
Top View



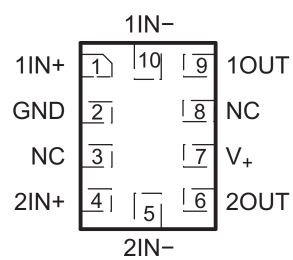
Pin Functions: TLV341

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70	SOT		
1IN+	1	2	I	Noninverting input on channel 1
1IN–	3	3	I	Inverting input on channel 1
1OUT	4	4	O	Output on channel 1
GND	2	1	—	Ground
$\overline{\text{SHDN}}$	5	5	I	Shutdown active low
V_+	6	6	—	Positive power supply

TLV342 D or DGK Package
10-Pin SOIC or VSSOP
Top View



TLV342 RUG Package
10-Pin X2QFN
Top View



Pin Functions: TLV342

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	X2QFN		
1IN+	3	1	I	Noninverting input on channel 1
1IN–	2	10	I	Inverting input on channel 1
1OUT	1	9	O	Output on channel 1
2IN+	5	4	I	Noninverting input on channel 2
2IN–	6	5	I	Inverting input on channel 2
2OUT	7	6	O	Output on channel 2
GND	4	2	—	Ground
NC[1]	—	3, 8	—	Not connected
V_+	8	7	—	Positive power supply

(1) NC – No internal connection

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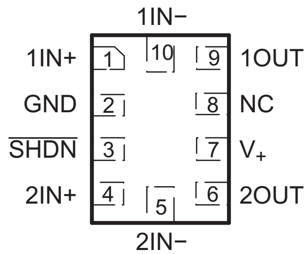
TLV342S RUG Package
10-Pin X2QFN
Top View



Pin Functions: TLV342S

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	1	I	Noninverting input on channel 1
1IN–	10	I	Inverting input on channel 1
1OUT	9	O	Output on channel 1
2IN+	4	I	Noninverting input on channel 2
2IN–	5	I	Inverting input on channel 2
2OUT	6	O	Output on channel 2
GND	2	—	Ground
NC[1]	8	—	Not connected
$\overline{\text{SHDN}}$	3	I	Shutdown active low
V_+	7	—	Positive power supply

(1) NC – No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_+	Supply voltage[2]	–0.3	5.5	V
V_{ID}	Differential input voltage[3]		±5.5	V
V_I	Input voltage (either input or $\overline{\text{shutdown}}$)	–0.3	5.5	V
V_O	Output voltage	–0.3	V_{CC} + 0.3	V
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_+	Supply voltage (single-supply operation)	1.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information: TLV341

THERMAL METRIC(1)		TLV341 DBV (SOT-23)	TLV341 DCK (SC70)	TLV341 DRL (SOT)	UNIT
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	196.8	221.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	145.6	82.4	109.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.1	95.2	111.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.1	1.8	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.4	93.2	109.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: TLV342

THERMAL METRIC(1)		TLV342 D (SOIC)	TLV342 DGK (MSOP)	TLV342 RUG (X2QFN)	UNIT
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.6	192.3	167	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	78.2	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.9	112.6	94.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.4	15.2	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.4	111.2	94	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: TLV342S

THERMAL METRIC(1)		TLV342S RUG (X2QFN)	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.7 Electrical Characteristics: V_+ = 1.8 V

V_+ = 1.8 V, GND = 0 V, $V_{IC} = V_O = V_+/2$, R_L > 1 MΩ (unless otherwise noted). See *Shutdown Characteristics: V_+ = 1.8 V*.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
V_{IO}	Input offset voltage	Standard grade		25°C		0.3	4	mV
				Full range			4.5	
		A grade		25°C		0.3	1.25	
				0°C to 125°C		0.3	1.5	
				–40°C to 125°C		0.3	1.7	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		μV/°C
I_{IB}	Input bias current			25°C		1	100	pA
				–40°C to 85°C			375	
				–40°C to 125°C			3000	
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	$0 \le V_{ICR} \le 1.2$ V		25°C	60	85		dB
				Full range	50			
k_{SVR}	Supply-voltage rejection ratio	1.8 V ≤ V_+ ≤ 5 V		25°C	75	95		dB
				Full range	65			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 60 dB		25°C	0		1.2	V
A_V	Large-signal voltage gain(2)	R_L = 10 kΩ to 1.35 V		25°C	70	110		dB
				Full range	60			
		R_L = 2 kΩ to 1.35 V		25°C	65	100		
				Full range	55			
V_O	Output swing (delta from supply rails)	R_L = 2 kΩ to 1.35 V	Low level	25°C		22	50	mV
				Full range			75	
			High level	25°C		25	50	
				Full range			75	
		R_L = 10 kΩ to 1.35 V	Low level	25°C		14	20	
				Full range			25	
			High level	25°C		7	20	
				Full range			25	
I_{CC}	Supply current (per channel)			25°C		70	150	μA
				Full range			200	
I_{OS}	Output short-circuit current	Sourcing		25°C	6	12		mA
		Sinking			10	20		
SR	Slew rate	R_L = 10 kΩ(3)		25°C		0.9		V/μs
GBW	Unity-gain bandwidth	R_L = 10 kΩ, C_L = 200 pF		25°C		2.2		MHz
φ_m	Phase margin	R_L = 100 kΩ, C_L = 200 pF		25°C		55		°
G_m	Gain margin	R_L = 100 kΩ, C_L = 200 pF		25°C		15		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		33		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_I = 1 V_{PP}		25°C		0.015%		

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ V_O ≤ V_+ – 0.2 V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

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6.8 Electrical Characteristics: $V_+ = 5$ V

$V_+ = 5$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted). See *Shutdown Characteristics: $V_+ = 5$ V*.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP (1)	MAX	UNIT
V_{IO}	Input offset voltage	Standard grade		25°C		0.3	4	mV
				Full range			4.5	
		A grade		25°C		0.3	1.25	
				0°C to 125°C		0.3	1.5	
				–40°C to 125°C		0.3	1.7	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		μV/°C
I_{IB}	Input bias current			25°C		1	200	pA
				–40°C to 85°C			375	
				–40°C to 125°C			3000	
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	$0 \le V_{ICR} \le 4.4$ V		25°C	75	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio	$1.8\text{ V} \le V_+ \le 5$ V		25°C	75	95		dB
				Full range	65			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 70 dB		25°C	0		4.4	V
A_V	Large-signal voltage gain (2)	$R_L = 10$ kΩ to 2.5 V		25°C	80	110		dB
				Full range	70			
		$R_L = 2$ kΩ to 2.5 V		25°C	75	105		
				Full range	60			
V_O	Output swing (delta from supply rails)	$R_L = 2$ kΩ to 2.5 V	Low level	25°C		40	60	mV
				Full range			85	
			High level	25°C		25	60	
				Full range			85	
		$R_L = 10$ kΩ to 2.5 V	Low level	25°C		18	30	
				Full range			40	
			High level	25°C		7	15	
				Full range			20	
I_{CC}	Supply current (per channel)			25°C		75	150	μA
				Full range			200	
I_{OS}	Output short-circuit current	Sourcing		25°C	60	113		mA
		Sinking			80	115		
SR	Slew rate	$R_L = 10$ kΩ (3)		25°C		1		V/μs
GBW	Unity-gain bandwidth	$R_L = 10$ kΩ, $C_L = 200$ pF		25°C		2.3		MHz
φ_m	Phase margin	$R_L = 100$ kΩ, $C_L = 200$ pF		25°C		55		°
G_m	Gain margin	$R_L = 100$ kΩ, $C_L = 200$ pF		25°C		15		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		33		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, $A_V = 1$, $R_L = 600$ Ω, $V_I = 1\ V_{PP}$		25°C		0.012%		

(1) Typical values represent the most likely parametric norm.
(2) $GND + 0.2\text{ V} \le V_O \le V_+ - 0.2$ V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

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6.9 Shutdown Characteristics: V_+ = 1.8 V

V_+ = 1.8 V, GND = 0 V, V_{IC} = V_O = V_+/2, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	V_{SD} = 0 V	25°C		0.01	1	µA
			Full range			1.5	
$t_{(on)}$	Amplifier turnon time		25°C		5		µs
V_{SD}	Recommended shutdown pin voltage range	On mode	25°C	1.5		1.8	V
		Shutdown mode		0		0.5	

6.10 Shutdown Characteristics: V_+ = 5 V

V_+ = 5 V, GND = 0 V, V_{IC} = V_O = V_+/2, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	V_{SD} = 0 V	25°C		0.01	1	µA
			Full range			1.5	
$t_{(on)}$	Amplifier turnon time		25°C		5		µs
V_{SD}	Recommended shutdown pin voltage range	On mode	25°C	4.5		5	V
		Shutdown mode		0		0.8	

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6.11 Typical Characteristics

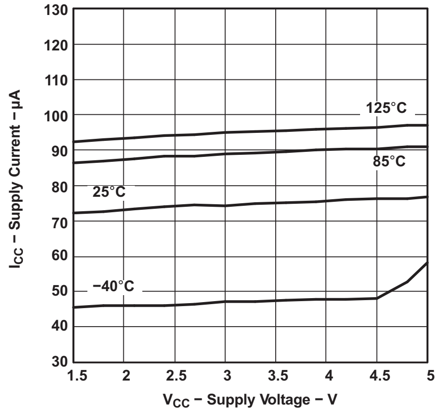

Figure 1. Supply Current vs Supply Voltage

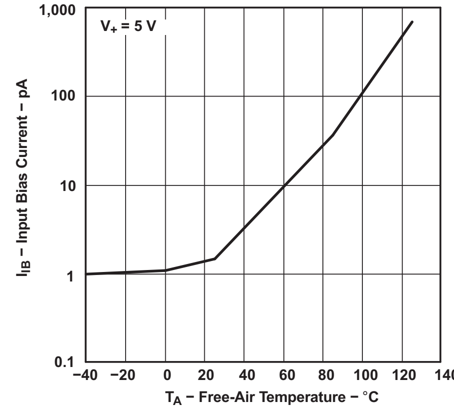

Figure 2. Input Bias Current vs Temperature

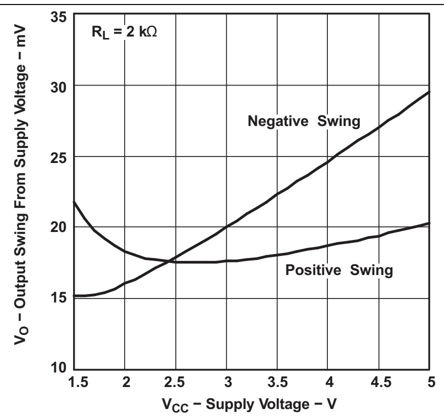

Figure 3. Output Voltage Swing vs Supply Voltage

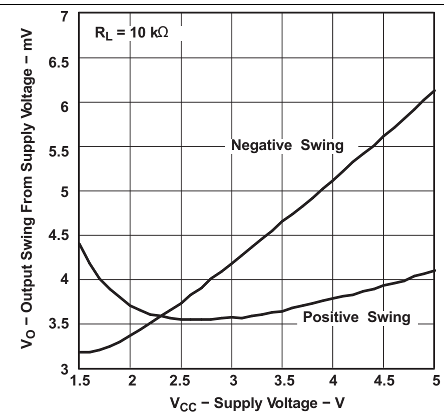

Figure 4. Output Voltage Swing vs Supply Voltage

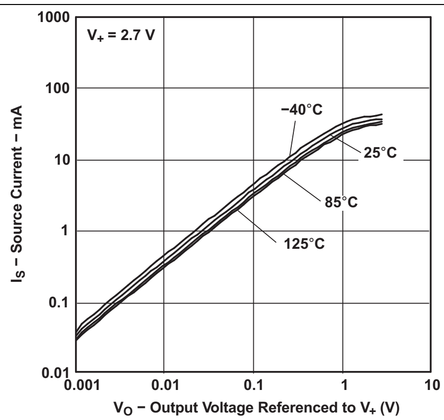

Figure 5. Source Current vs Output Voltage

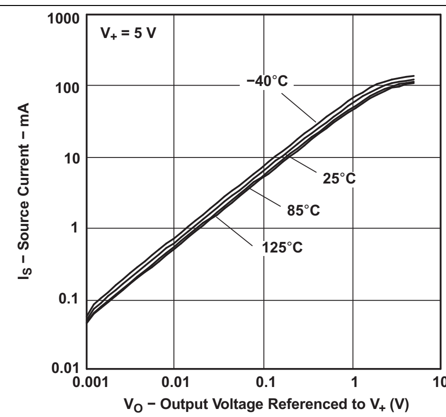

Figure 6. Source Current vs Output Voltage

Typical Characteristics (continued)

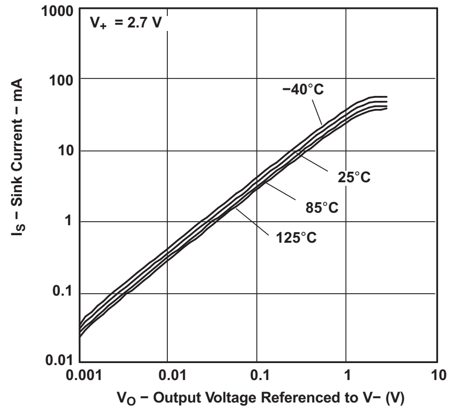

Figure 7. Sink Current vs Output Voltage

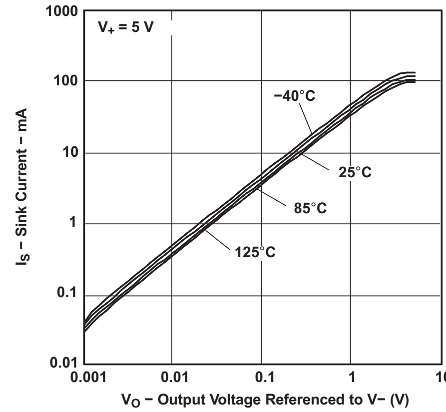

Figure 8. Sink Current vs Output Voltage

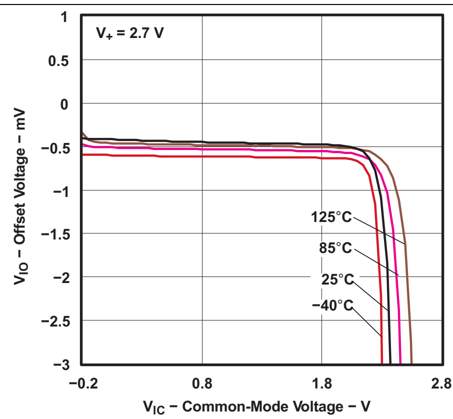

Figure 9. Offset Voltage vs Common-Mode Voltage

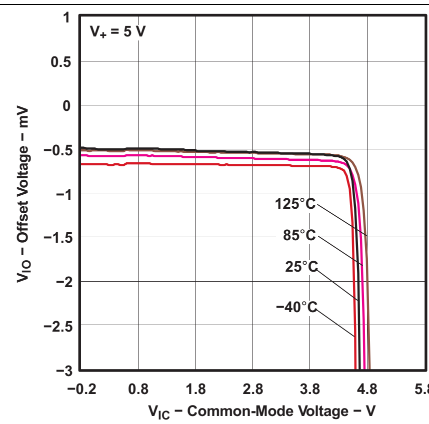

Figure 10. Offset Voltage vs Common-Mode Voltage

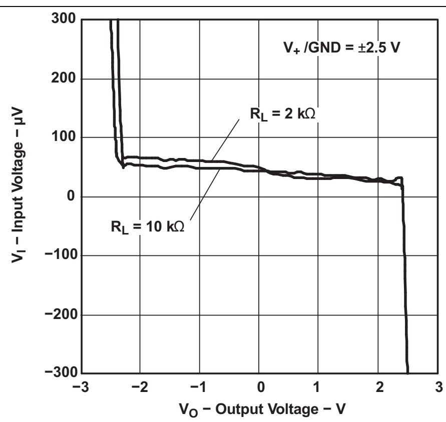

Figure 11. Input Voltage vs Output Voltage

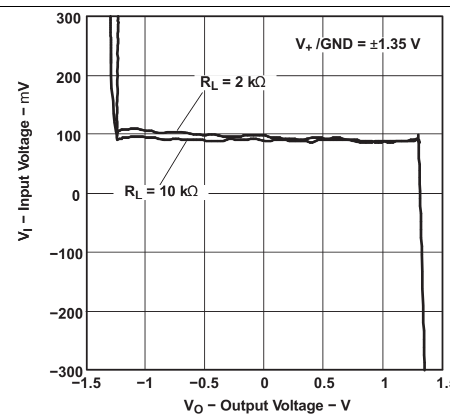

Figure 12. Input Voltage vs Output Voltage

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Typical Characteristics (continued)

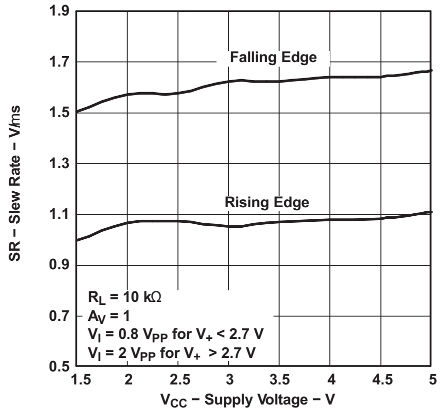

Figure 13. Slew Rate vs Supply Voltage

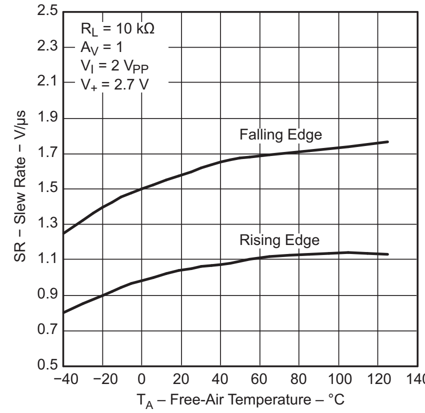

Figure 14. Slew Rate vs Temperature

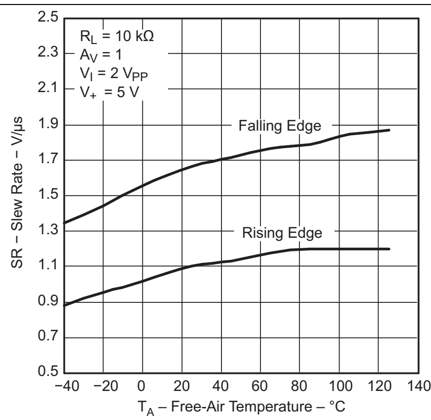

Figure 15. Slew Rate vs Temperature

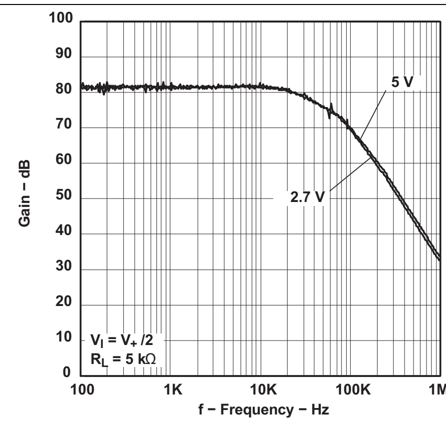

Figure 16. CMRR vs Frequency

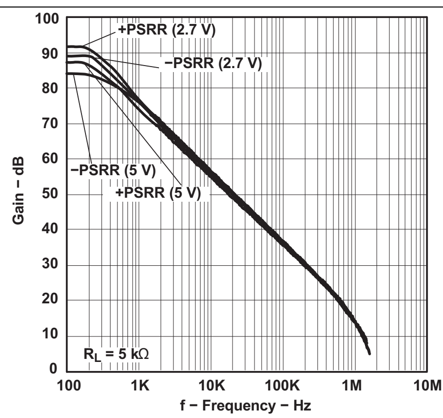

Figure 17. PSRR vs Frequency

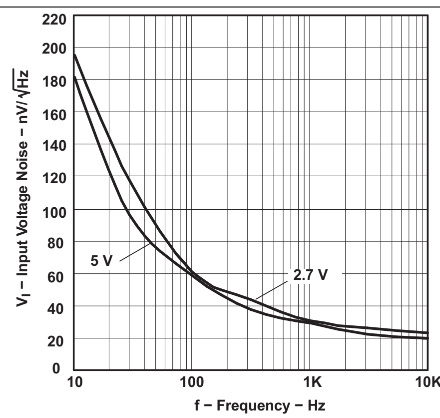

Figure 18. Input Voltage Noise vs Frequency

Typical Characteristics (continued)

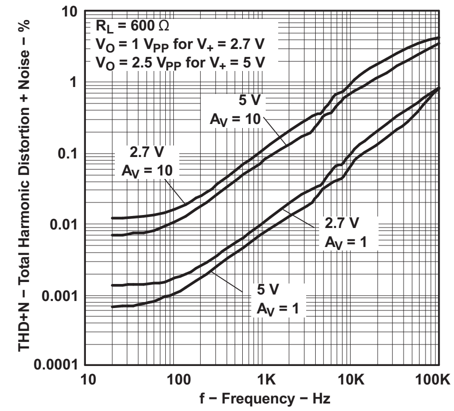

Figure 19. Total Harmonic Distortion +Noise vs Frequency

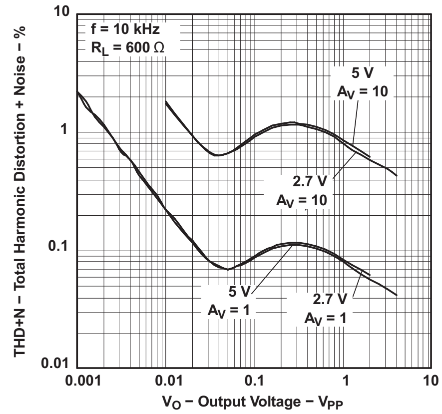

Figure 20. Total Harmonic Distortion +Noise vs Output Voltage

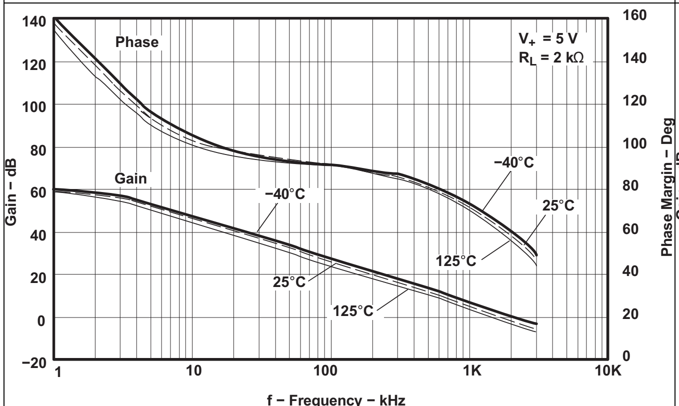

Figure 21. Frequency Response vs Temperature

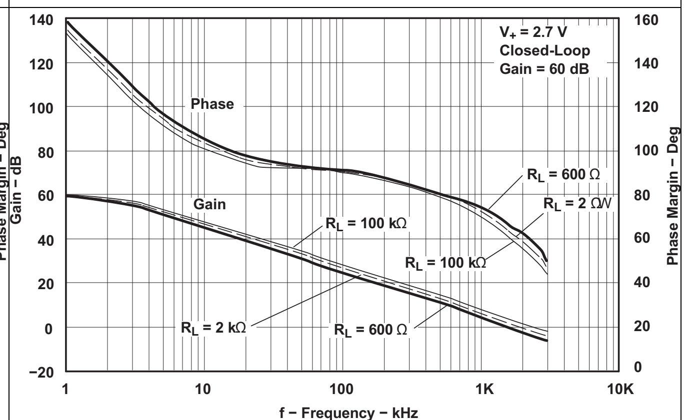

Figure 22. Frequency Response vs R_L

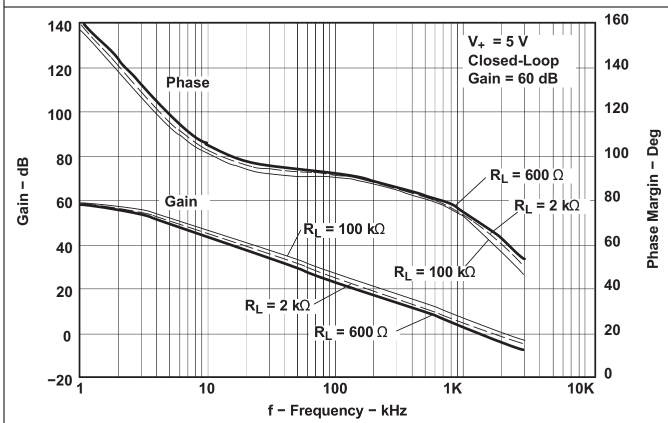

Figure 23. Frequency Response vs R_L

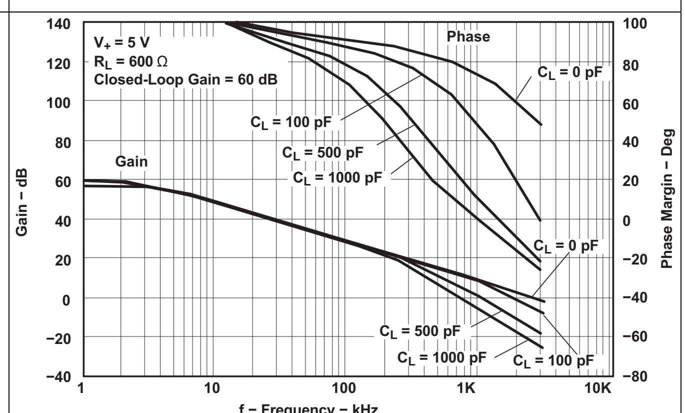

Figure 24. Frequency Response vs C_L

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Typical Characteristics (continued)

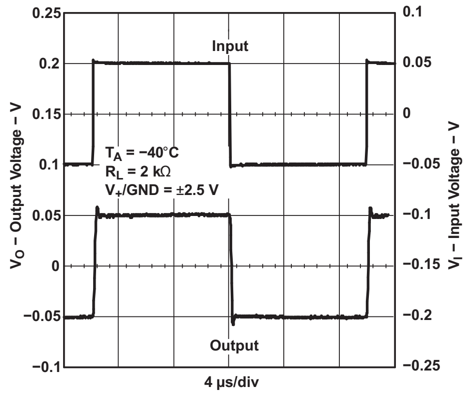

Figure 25. Small-Signal Noninverting Response

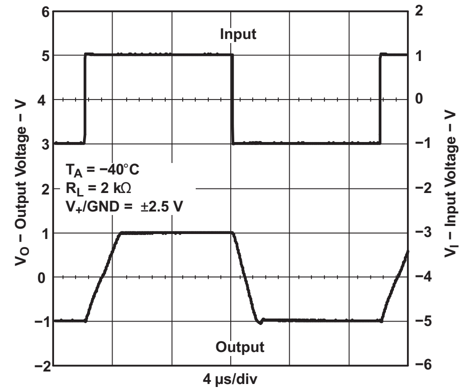

Figure 26. Large-Signal Noninverting Response

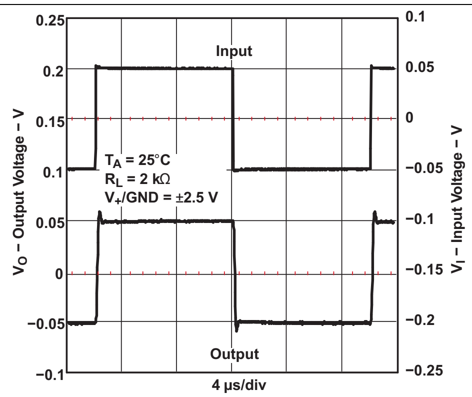

Figure 27. Small-Signal Noninverting Response

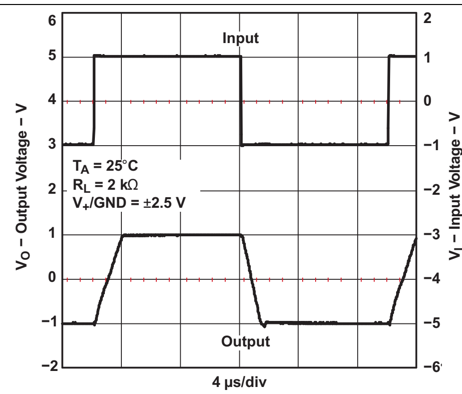

Figure 28. Large-Signal Noninverting Response

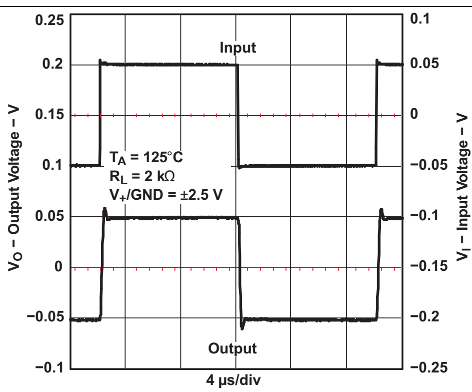

Figure 29. Small-Signal Noninverting Response

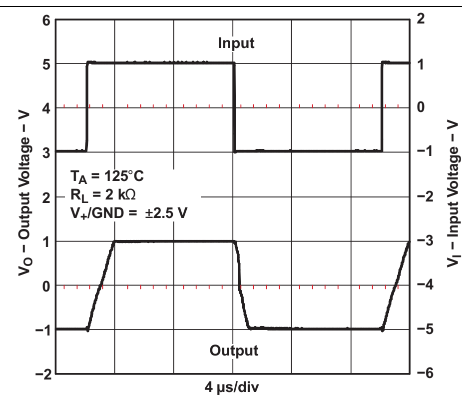

Figure 30. Large-Signal Noninverting Response

Typical Characteristics (continued)

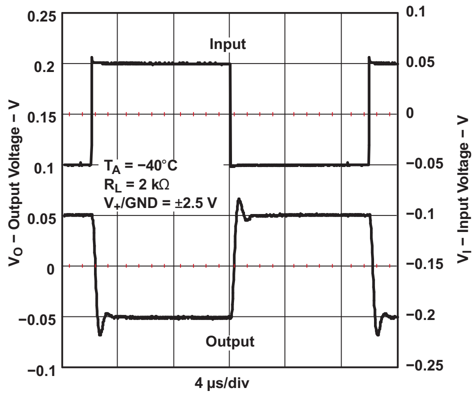

Figure 31. Small-Signal Noninverting Response

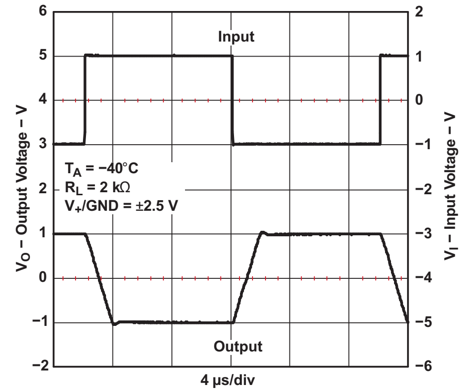

Figure 32. Large-Signal Inverting Response

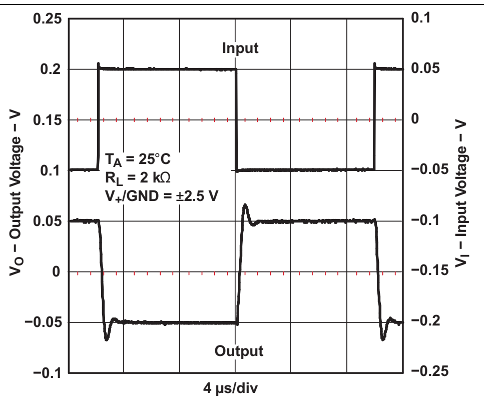

Figure 33. Small-Signal Inverting Response

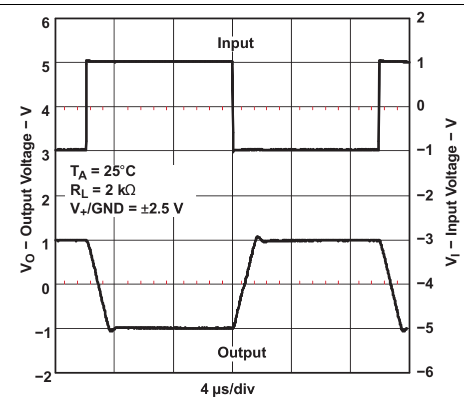

Figure 34. Large-Signal Inverting Response

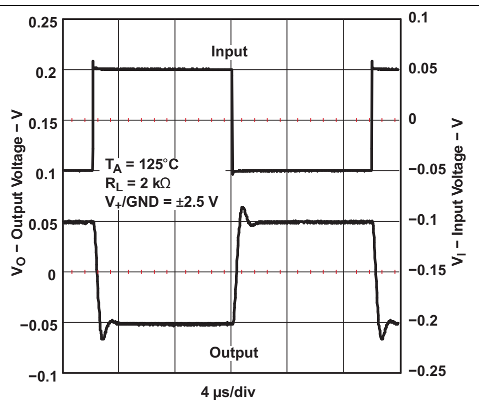

Figure 35. Small-Signal Inverting Response

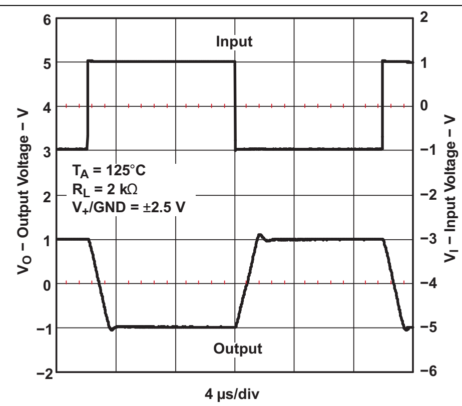

Figure 36. Large-Signal Inverting Response

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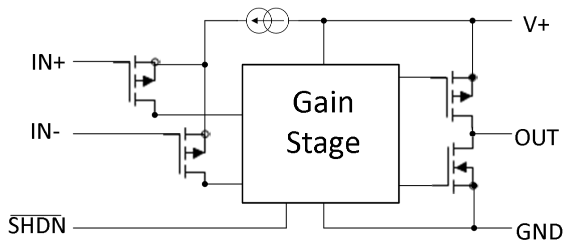
7 Detailed Description

7.1 Overview

The TLV34xx devices are precision operational amplifiers with CMOS inputs for very low input bias current. Grade A devices offer lower V_{IO} for high accuracy in direct-coupled applications. Output is rail to rail and input common mode includes ground. TLV341 and TLV342S have shutdown mode for very low supply current.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PMOS Input Stage

PMOS Input Stage supports a lower input range that includes ground. Upper range limit is VCC – 0.6 V.

7.3.2 CMOS Output Stage

The CMOS drain output topology allows rail-to-rail output swing.

7.3.3 Shutdown

TLV341 and TLV342S include a shutdown pin. During shutdown, I_{CC} is nearly zero and the output becomes high impedance. The typical turnon time coming out of shutdown is 5 µs.

7.4 Device Functional Modes

The TLV34xx devices have two operation modes:

- Normal operation when $\overline{\text{SHDN}}$ pin is at V_+ level or the $\overline{\text{SHDN}}$ pin is not present
- Shutdown mode when $\overline{\text{SHDN}}$ is at GND level; I_{CC} is very low and output is high impedance.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV34xx devices have rail-to-rail output and input range from ground to VCC – 0.6 V. CMOS inputs provide very low input current. Shutdown capability is an option in dual amplifier version. Operation from 1.5 V to 5.5 V is possible.

8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

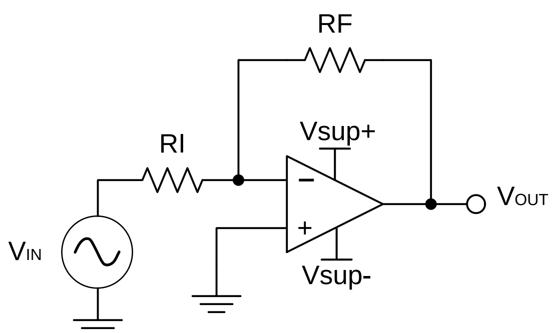

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Figure 37. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output voltage range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ± 2 V is sufficient to accommodate this application. The supplies can power up in any order; however, neither supply can be of opposite polarity relative to ground at any time; otherwise, a large current can flow though the input ESD diodes. TI highliy recommends adding a series resistor to the grounded input to limit current in such an occurrence. Vsup+ must be more positive than Vsup– at all times; otherwise, a large reverse supply current may flow.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the mA range. This ensures the part does not draw too much current. For this example, choose 10 kΩ for RI, which means 36 kΩ is used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

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Typical Application (continued)

8.2.3 Application Curve

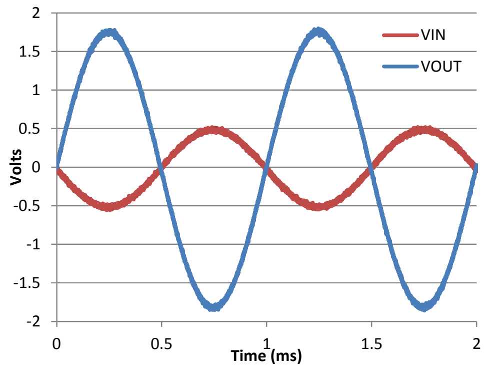

Figure 38. Input and Output Voltages of the Inverting Amplifier

9 Power Supply Recommendations

CAUTION

Supply voltages larger than 5.5 V for a single supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds while paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Guidelines*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

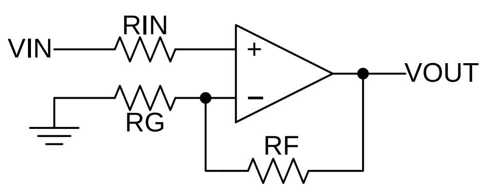

Figure 39. Layout Schematic

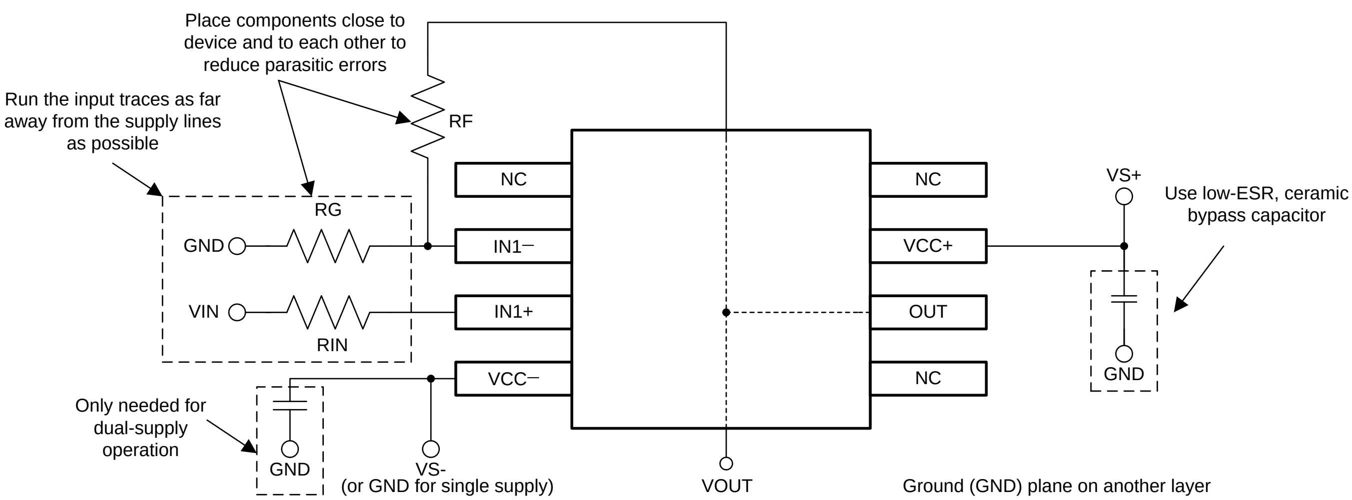

Figure 40. Operational Amplifier Schematic for Noninverting Configuration

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV341	Click here	Click here	Click here	Click here	Click here
TLV341A	Click here	Click here	Click here	Click here	Click here
TLV342	Click here	Click here	Click here	Click here	Click here
TLV342S	Click here	Click here	Click here	Click here	Click here

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV341AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YCGE	Samples
TLV341AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YCGE	Samples
TLV341AIDBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YCGE	Samples
TLV341AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5E	Samples
TLV341AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5E	Samples
TLV341AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5E	Samples
TLV341IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YC9E	Samples
TLV341IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YC9E	Samples
TLV341IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y4E	Samples
TLV341IDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y4E	Samples
TLV341IDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y4E	Samples
TLV341IDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(Y4A ~ Y4W)	Samples
TLV342AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A	Samples
TLV342AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A	Samples
TLV342AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A	Samples
TLV342AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A	Samples
TLV342ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV342IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y6A	Samples
TLV342IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342	Samples
TLV342IRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y6E	Samples
TLV342SIRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2YE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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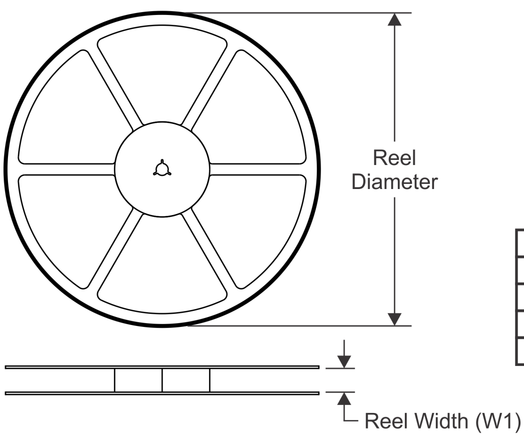
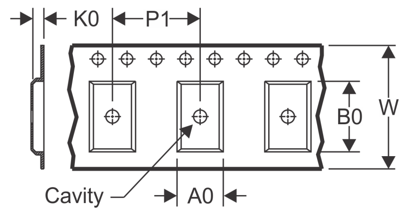
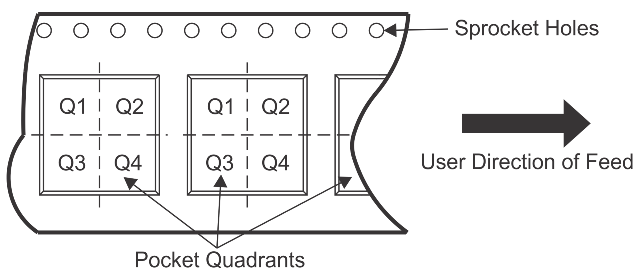
TAPE AND REEL INFORMATION





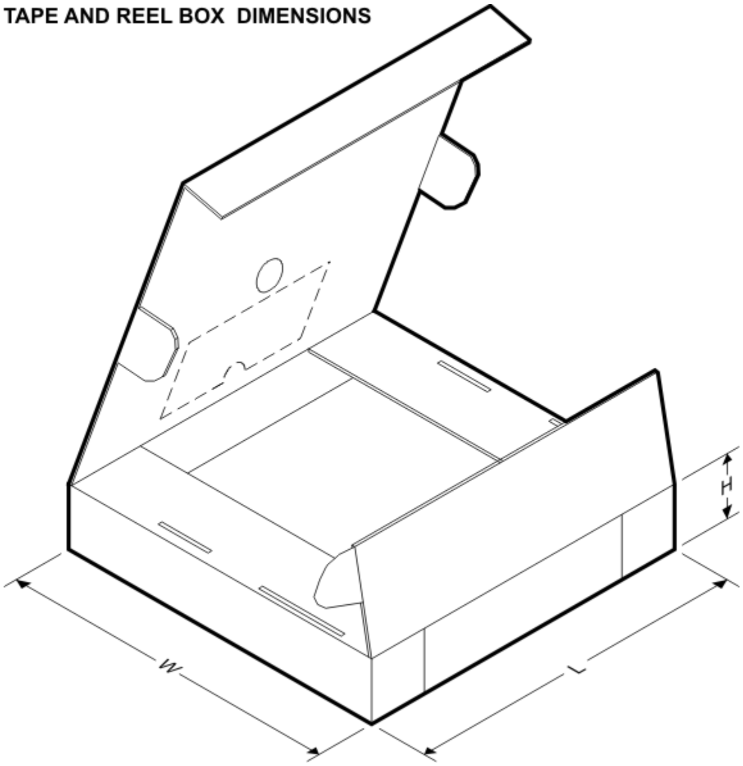
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV341AIDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV341AIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV341AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV341AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV341IDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV341IDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV341IDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV341IDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TLV341IDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV342AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV342IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV342IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV342IRUGR	X2QFN	RUG	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1
TLV342SIRUGR	X2QFN	RUG	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

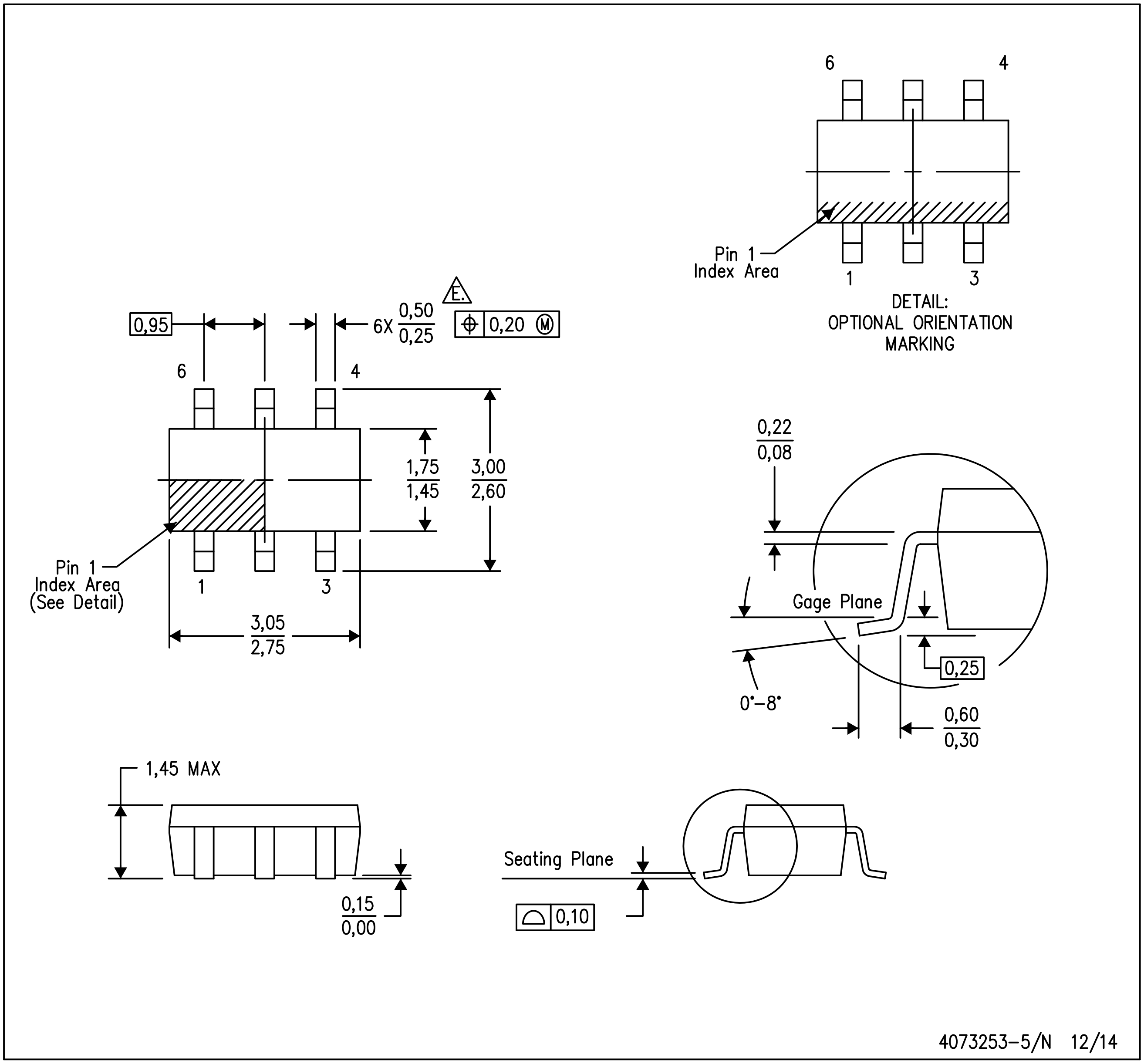
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

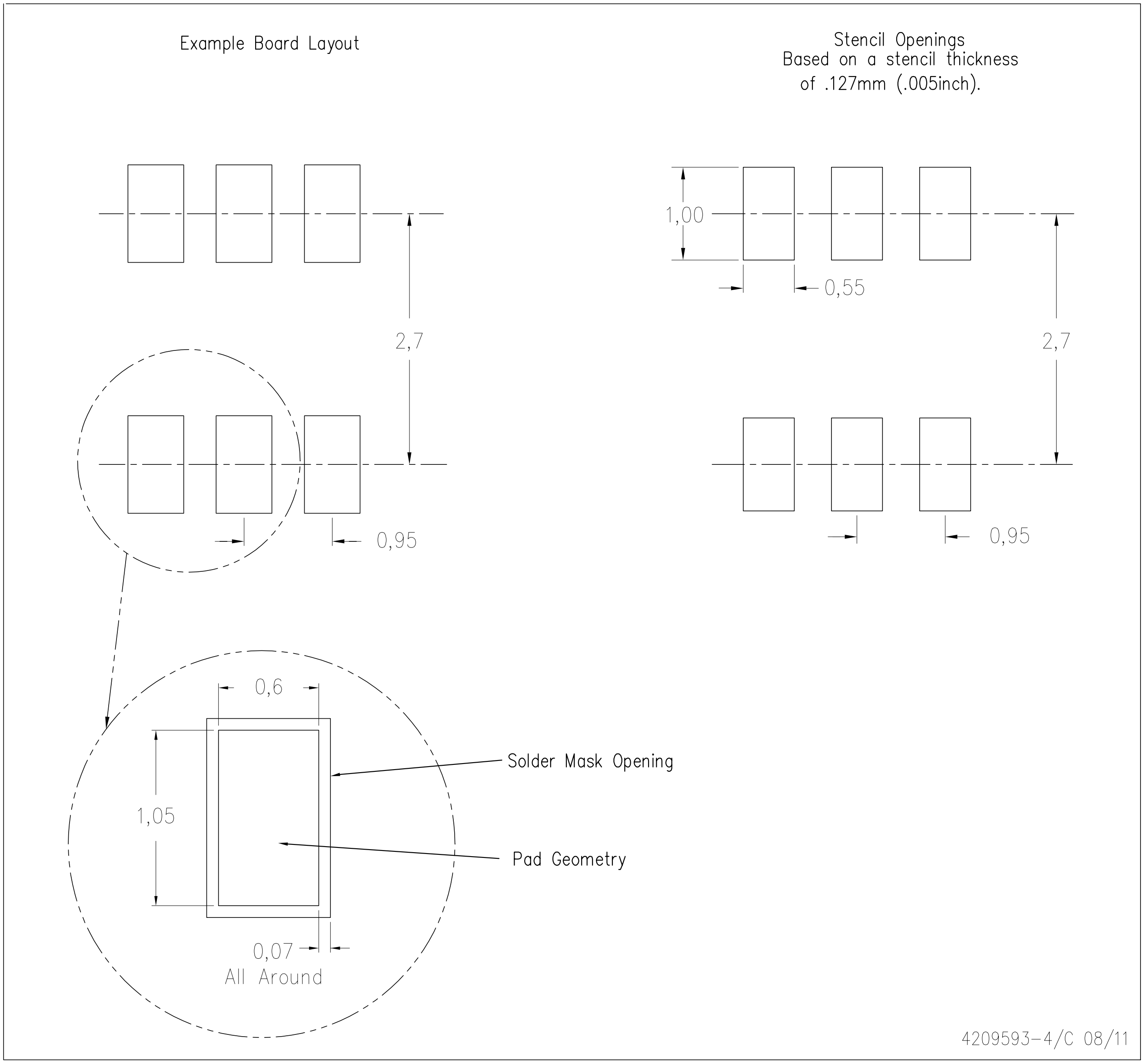
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV341AIDBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TLV341AIDBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
TLV341AIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV341AIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV341IDBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TLV341IDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV341IDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV341IDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TLV341IDRLR	SOT	DRL	6	4000	184.0	184.0	19.0
TLV342AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV342IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV342IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV342IRUGR	X2QFN	RUG	10	3000	203.0	203.0	35.0
TLV342SIRUGR	X2QFN	RUG	10	3000	203.0	203.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



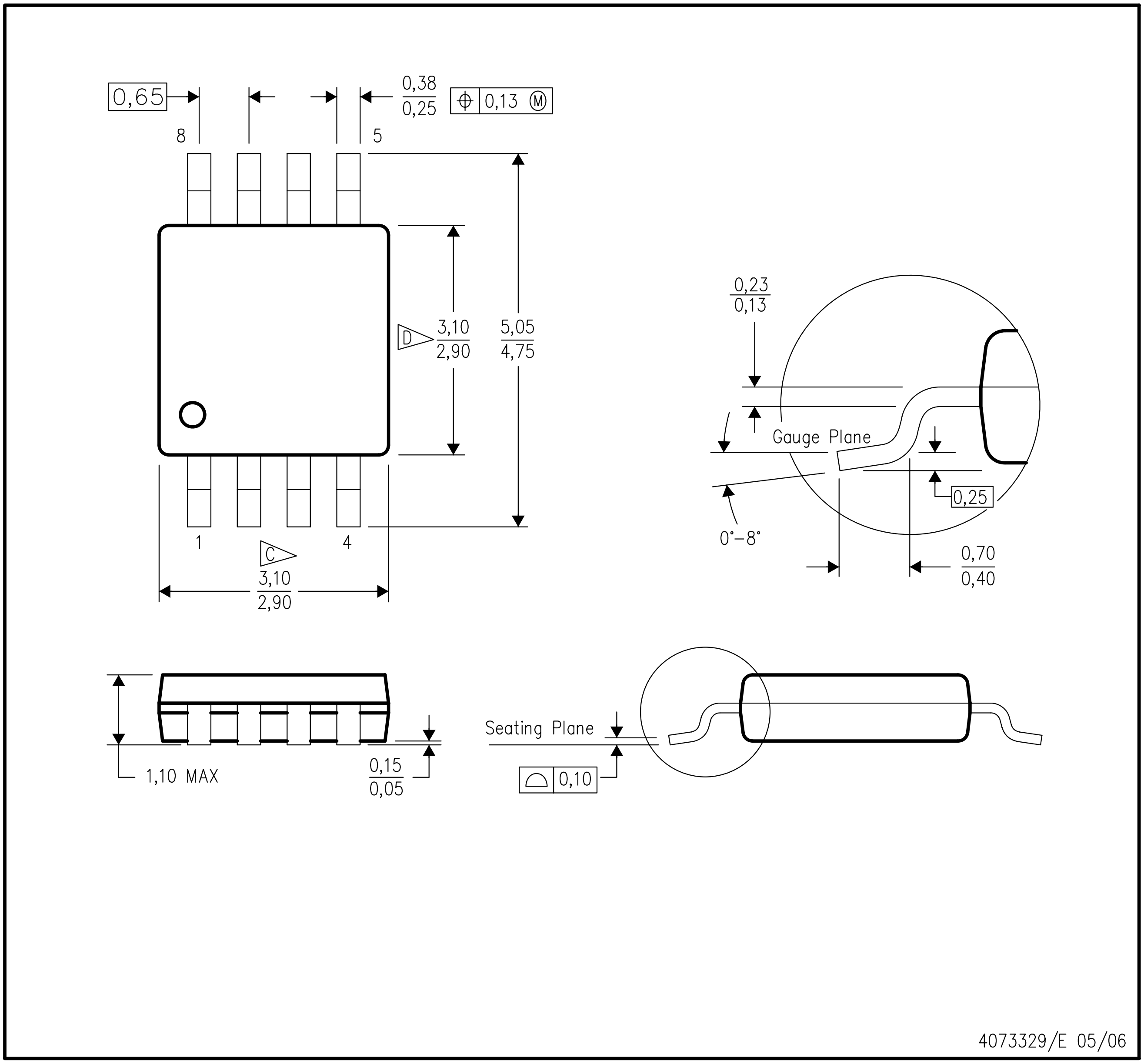
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



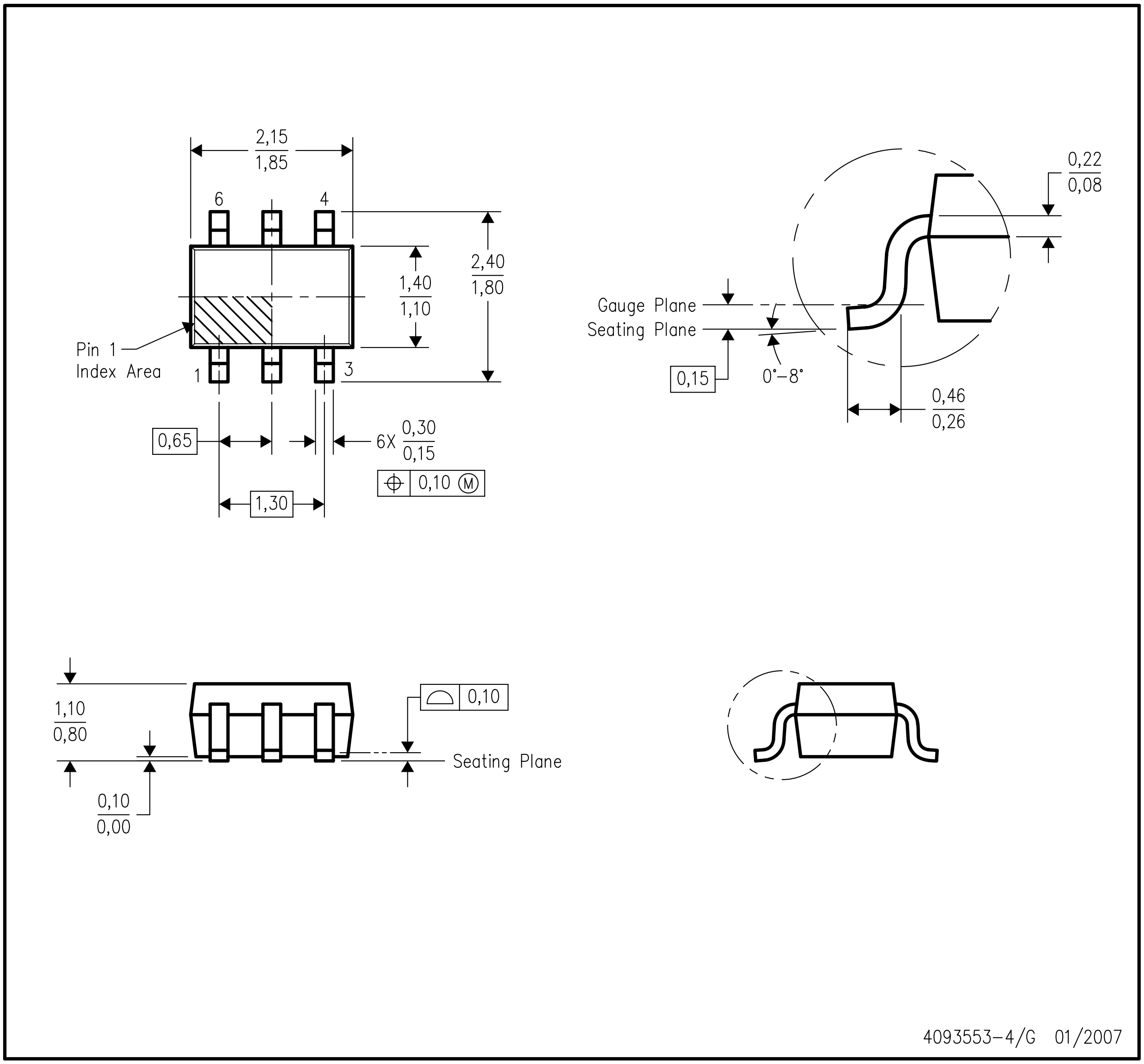
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



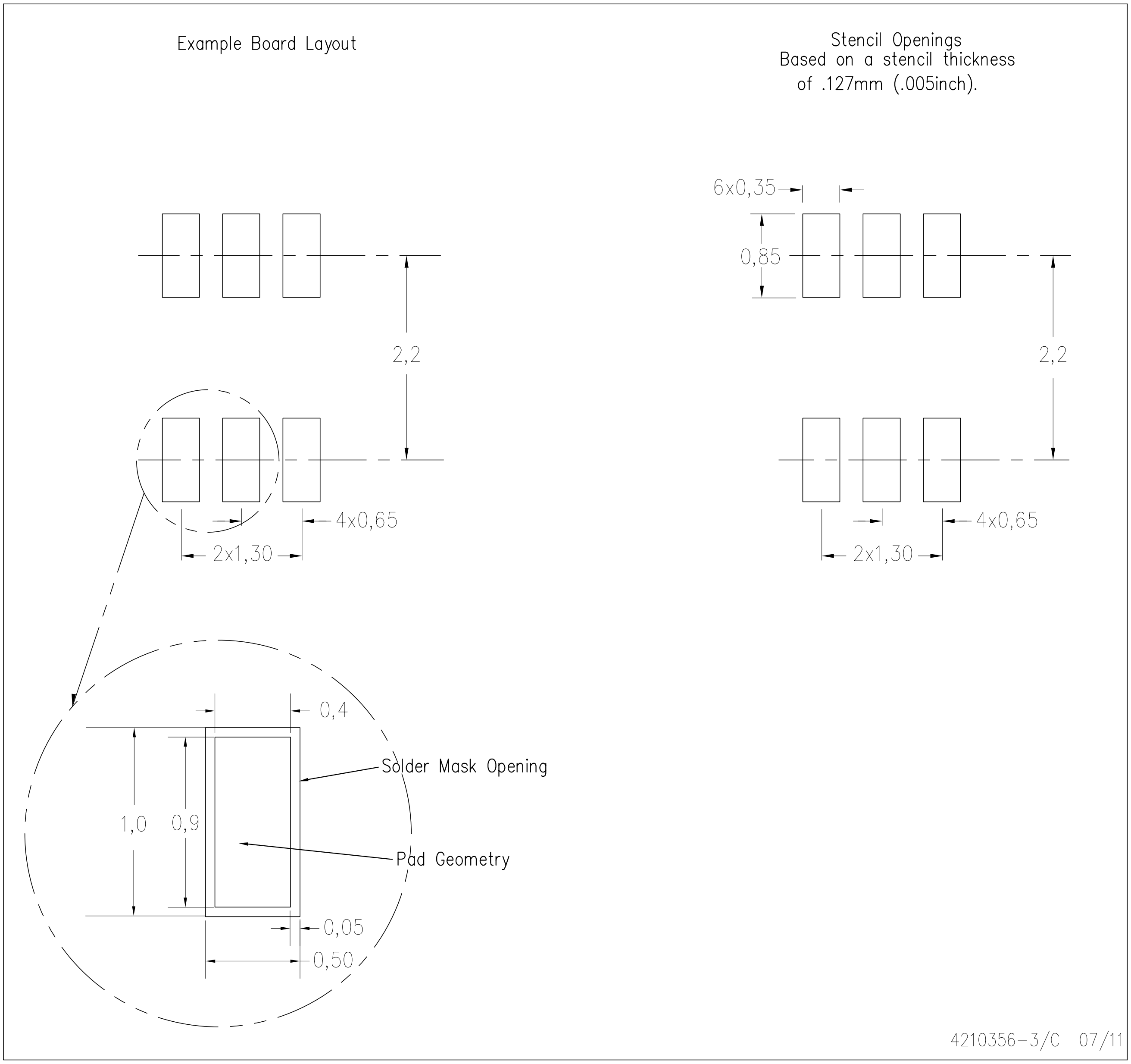
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE

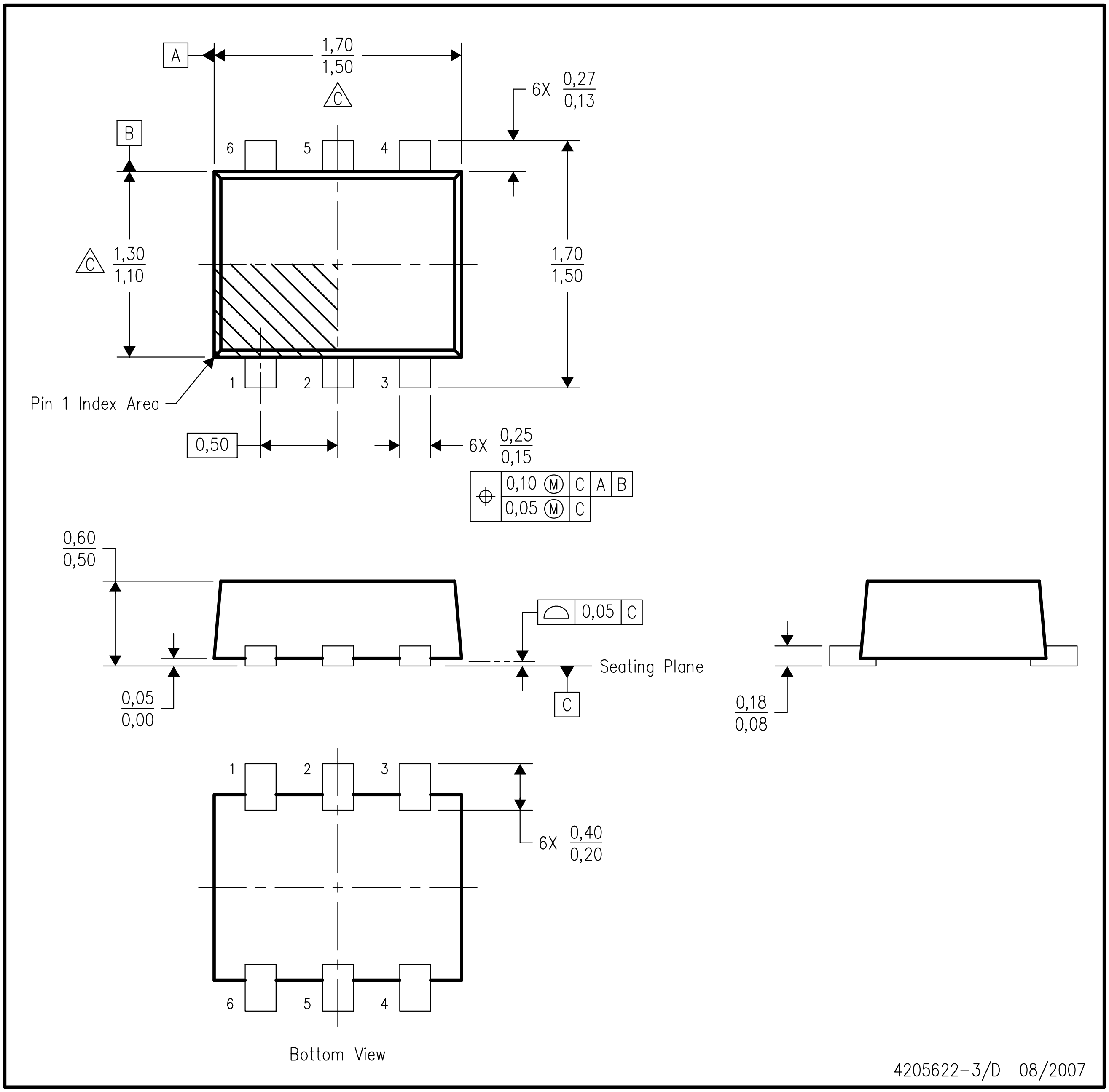


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE

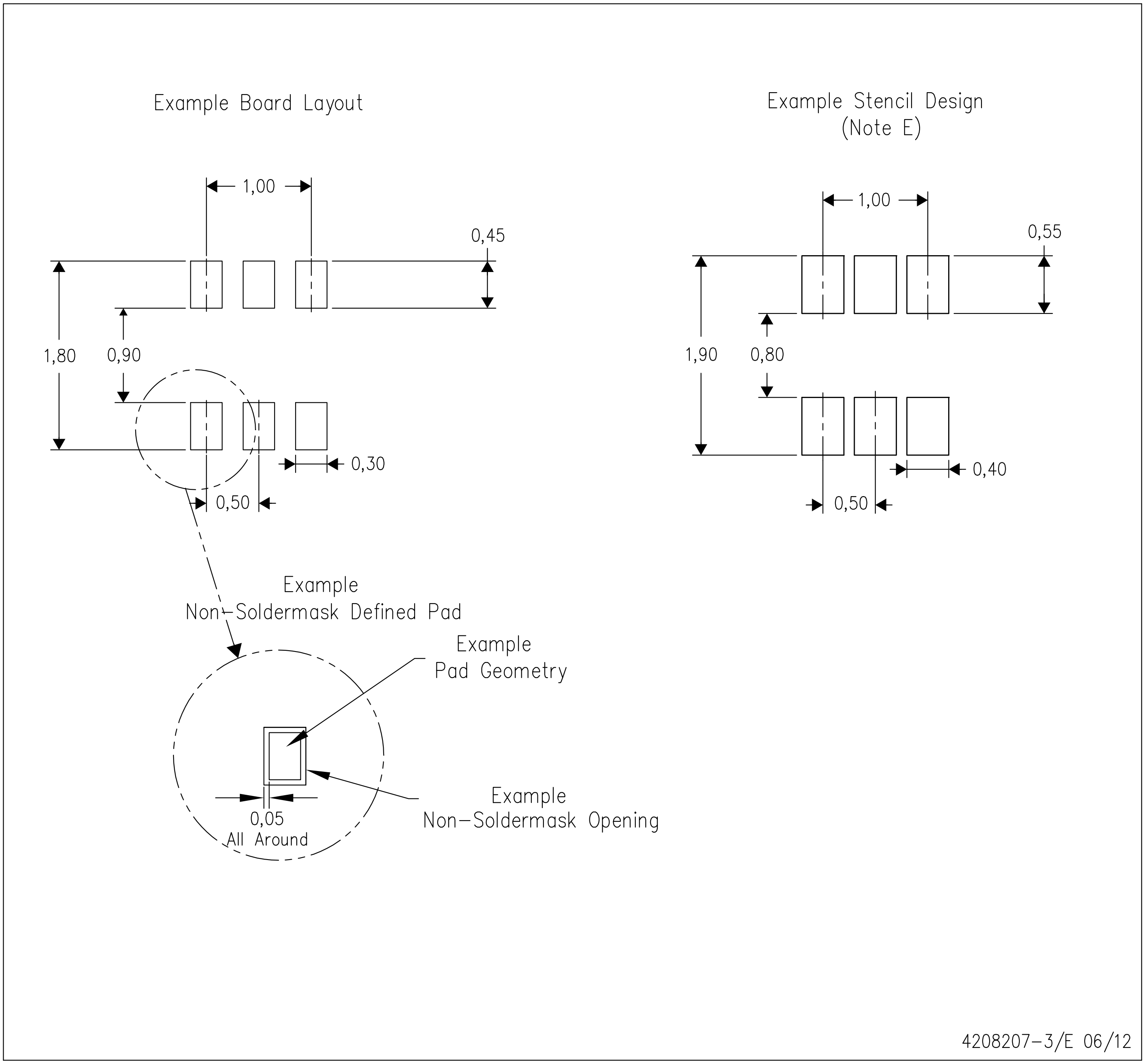


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



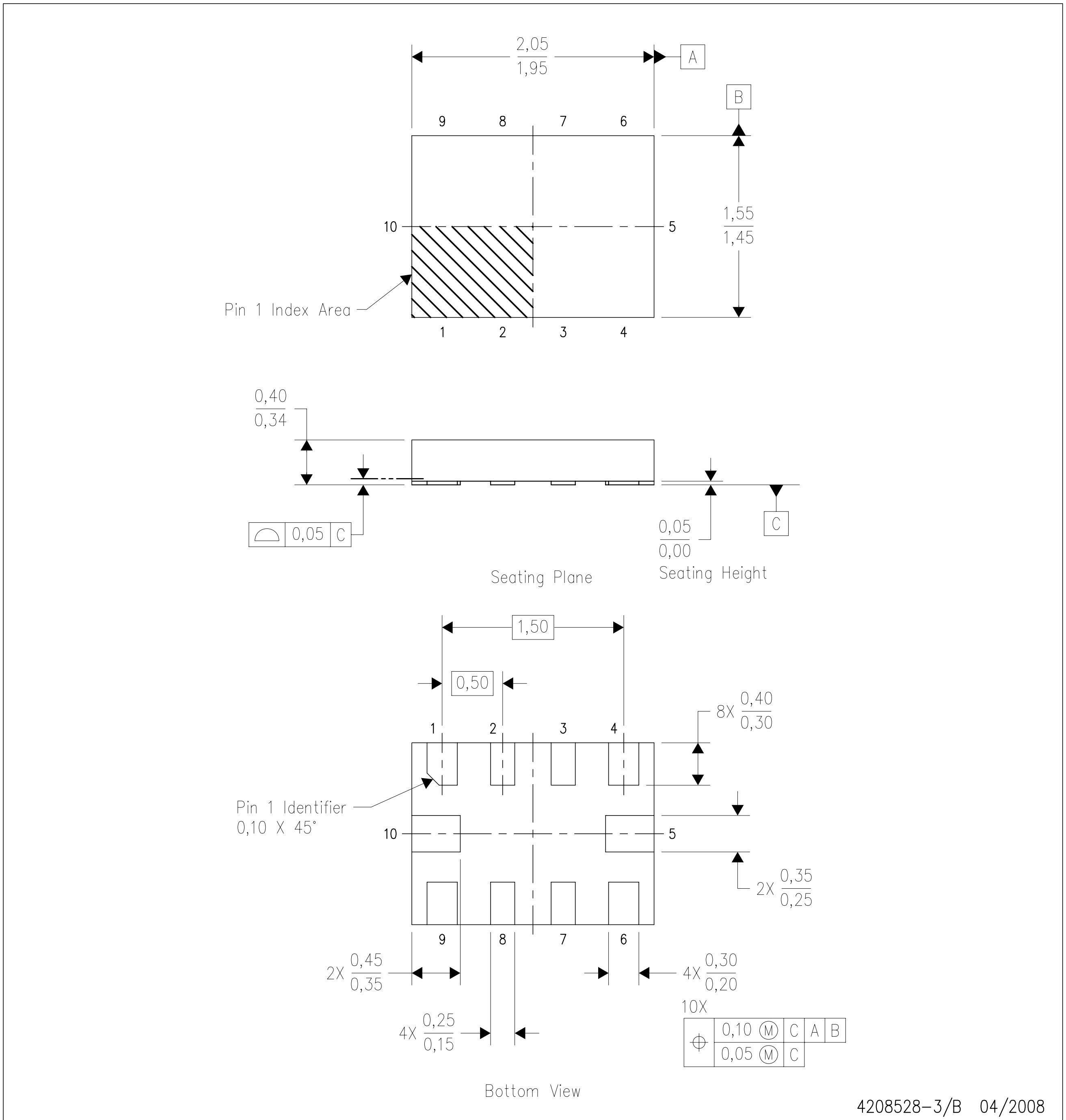
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R-PDSO-N6) PLASTIC SMALL OUTLINE



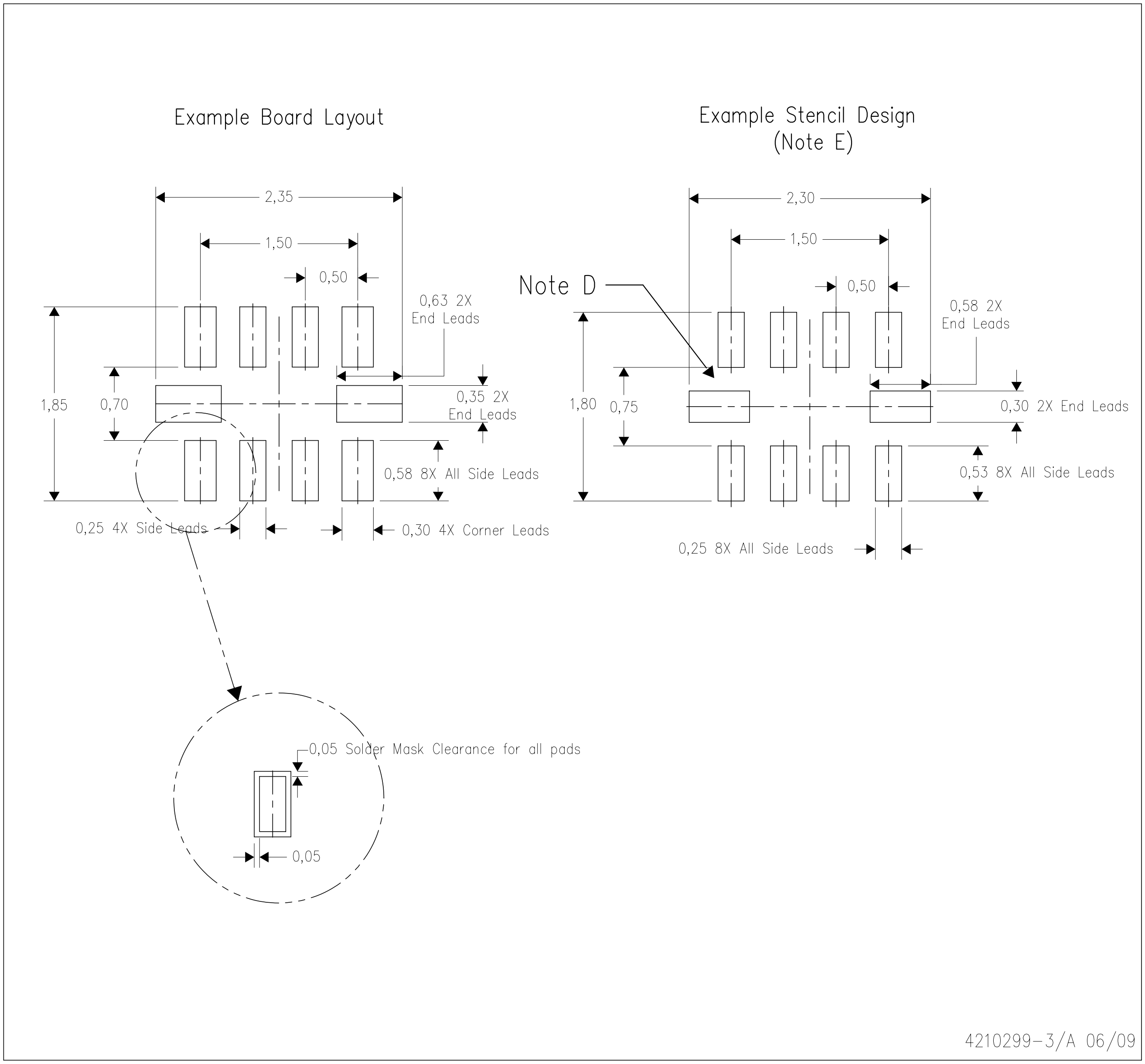
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

RUG (R-PQFP-N10) PLASTIC QUAD FLATPACK



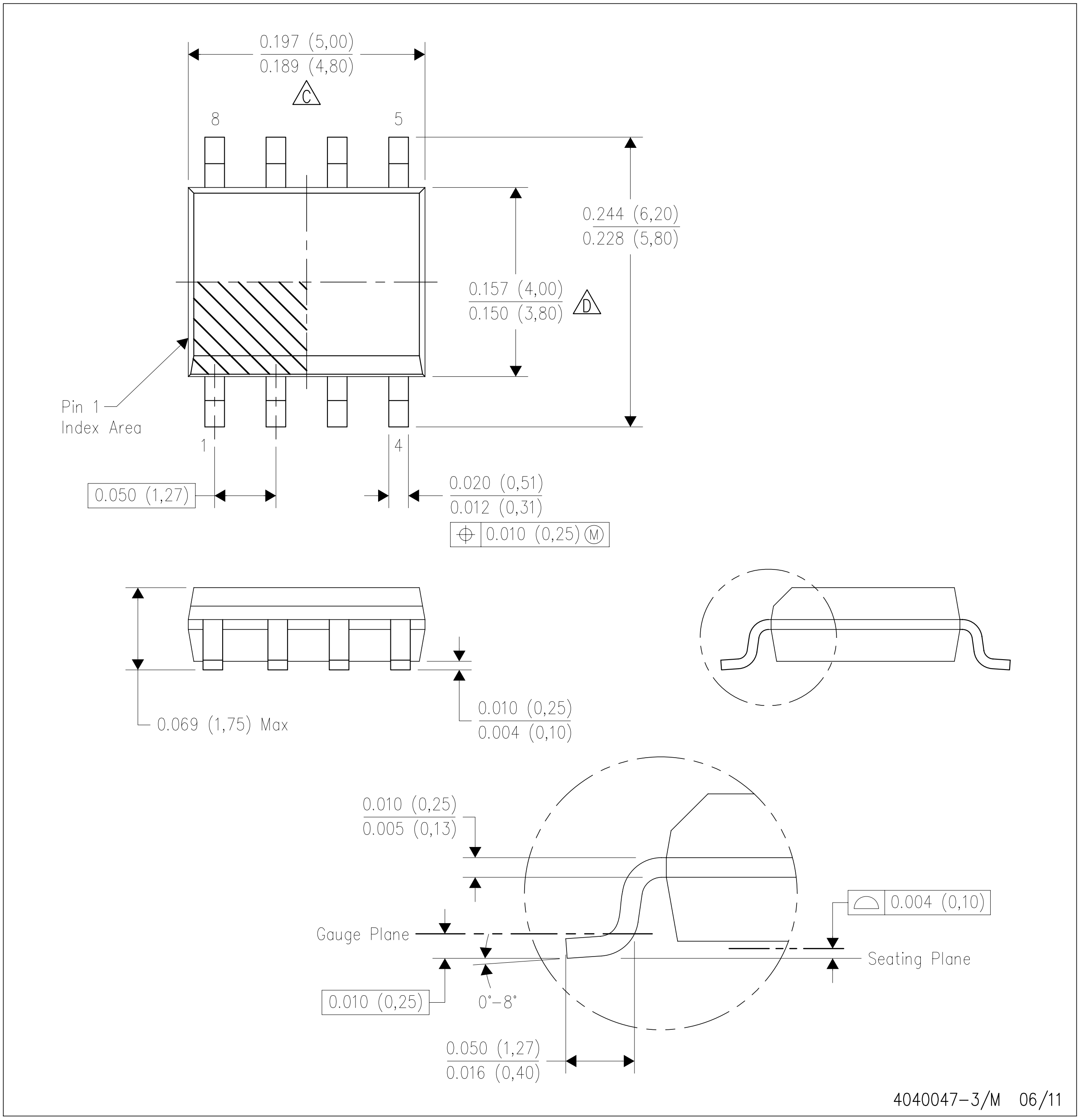
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R–PQFP–N10)



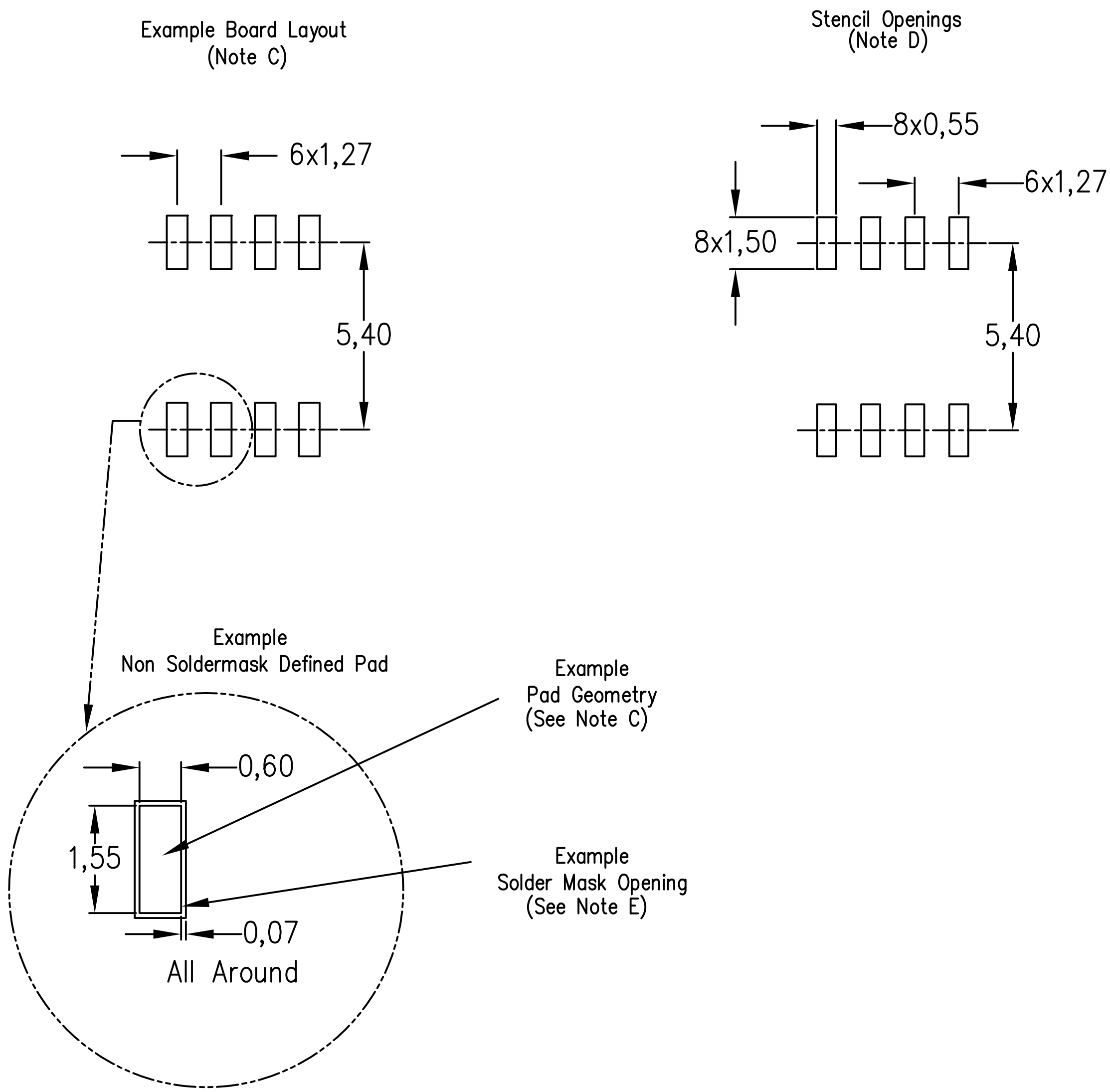
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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