8-Channel Gigabit Signal Conditioning Buffer

Check for Samples: SN65LVCP418

FEATURES

- **8 Input and 8 Output Signal Conditioning Buffer**
- **Up to 4.25 Gbps Operation**
- **30 ps of Deterministic Jitter**
- **Selectable Transmit Pre-Emphasis Per Lane**
- **Selectable Receive Equalization**
- **Available Packaging 64 Pin QFP**
- **Propagation Delay Times: 400 ps Typical**
- **Inputs Electrically Compatible With CML Signal Levels**
- **Operates From a Single 3.3-V Supply**
- **Ability to 3-State Outputs**
- **Integrated Termination Resistors**
- **I^2C™ Control Interface**

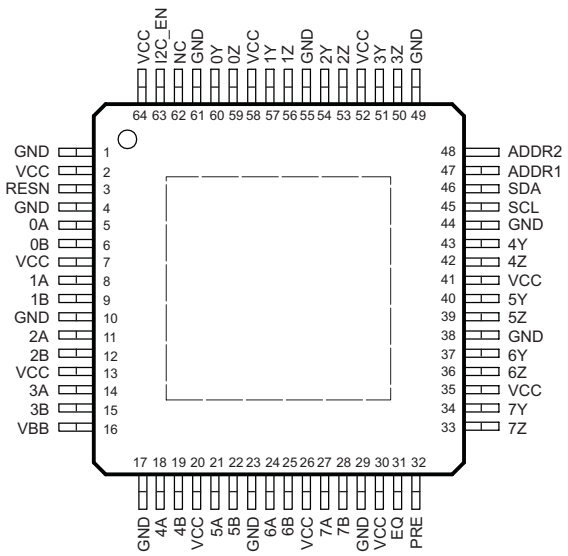
APPLICATIONS

- **Clock Buffering/Clock MUXing**
- **Wireless Base Stations**
- **High-Speed Network Routing**
- **Telecom/Datacom**
- **XAUI 802.3ae Protocol Backplane Repeaters**

DESCRIPTION

The SN65LVCP418 is an 8 Channel signal conditioning buffer in a flow-through pin-out allowing for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVCP418 incorporates 100-Ω termination resistors for those applications where board space is a premium. Built-in transmit pre-emphasis and receive equalization for superior signal integrity performance.

The SN65LVCP418 is characterized for operation from –40°C to 85°C.



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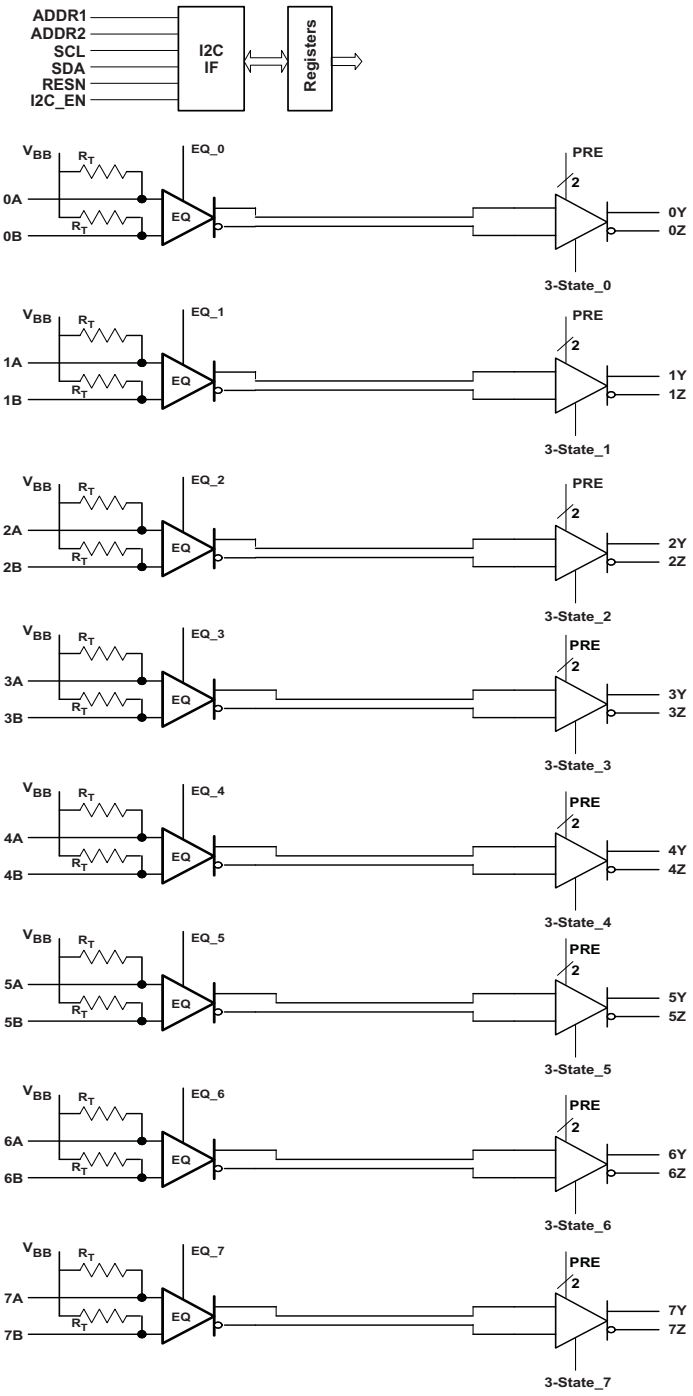
PowerPAD is a trademark of Texas Instruments.
I^2C is a trademark of Philips Electronics.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM



A. V_{BB}: Receiver input internal biasing voltage (allows ac coupling)

B. R_T: Internal 50-Ω receiver termination (100-Ω differential)

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
HIGH SPEED I/O			
xA	5, 8, 11, 14, 18, 21, 24 ,27	Differential Inputs (with 50-Ω termination to Vbb) xA=P; xB=N	Line Side Differential Inputs CML compatible
xB	6, 9, 12, 15, 19, 22, 25, 28		
xY	34, 37, 40 43, 51, 54, 57, 60	Differential Output xY=P; xZ=N	Switch Side Differential Outputs. VML
xZ	33, 36, 39, 42, 50, 53, 56, 59		
CONTROL SIGNALS			
SCL	45	Inputs	I^2C Control Interface (SCL: Clock, SDA: Data, ADDR: Address)
SDA	46		
ADDR1	47		
ADDR2	48		
EQ	31	Input	Equalization setting when I^2C is not enabled. EQ=0 13dB and EQ=1 for 9dB
PRE	32	Input	Pre-Emphasis setting when I^2C is not enabled. PRE=0 for 0 dB and PRE=1 for 6 dB
I2C_EN	63	Input	Enables I^2C control interface I^2C_EN=1 for enable; When EN=0 then the PRE and EQ pins are used to set the Pre-Emphasis and Equalization settings rather than the I^2C register map.
NC	62	Input	No Connect
RESN	3	Input (Active Low)	Configuration Reset. Resets I^2C register space; Note upon device startup the RESN pin must be driven low to reset the device registers.
POWER SUPPLY			
VCC	2, 7, 13, 20, 26, 30, 35, 41, 52, 58, 64	Power	Power Supply 3.3v±5%
GND	1,4, 10, 17, 23, 29 , 38, 44, 49, 55, 61	Ground	
PowerPAD™		Ground	The ground center pad of the package must be connected to GND plane.
V_{BB}	16	Input	Receiver input biasing voltage

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

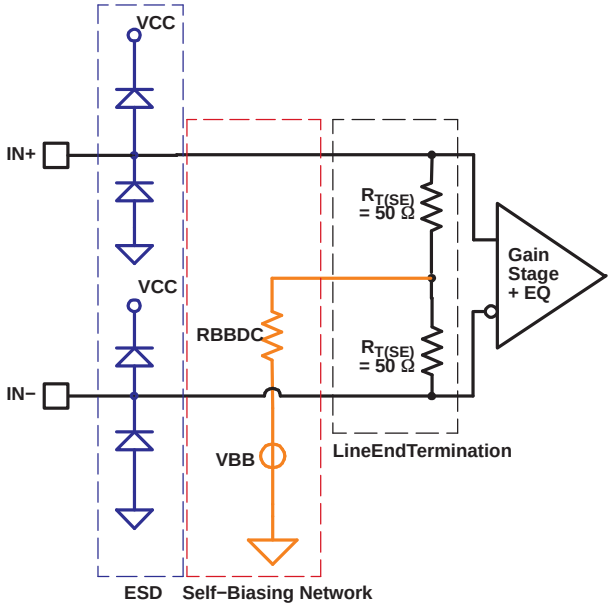


Figure 1. Equivalent Input Circuit Design

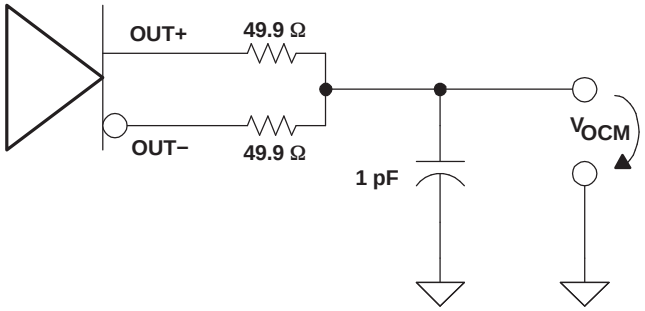


Figure 2. Common-Mode Output Voltage Test Circuit

AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGED DEVICE(1) (2)
		PAP (64 pin)
–40°C to 85°C	Multi Channel Gigabit Signal Conditioner	SN65LVCP418

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP418PAP). Temperature range assumes 1 m/s airflow.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE THERMAL CHARACTERISTICS

PACKAGE THERMAL CHARACTERISTICS(1)		NOM	UNIT
θ_{JA} (junction-to-ambient)	100LFM airflow is required otherwise a 4x4 thermal via array must be implemented with 6 layer or greater PCB	21.2	°C/W

(1) See application note SPRA953 for a detailed explaniation of thermal parameters.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.5 V to 6 V
	Voltage range	Control inputs, all outputs	–0.5 V to (V_{CC} + 0.5 V)
		Receiver inputs	–0.5 V to 4 V
ESD	Human Body Model(3)	All pins	6 kV
	Charged-Device Model(4)	All pins	500 V
T_J	Maximum junction temperature		See Package Thermal Characteristics Table
	Moisture sensitivity level		2

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				4.25	Gbps
V_{CC}	Supply voltage		3.135	3.3	3.465	V
$V_{CC(N)}$	Supply voltage noise amplitude	10 Hz to 2.125 GHz			20	mV
T_J	Junction temperature				125	°C
T_A	Operating free-air temperature(1)	Assumes 4×4 thermal via array is implemented with 6 layer or greater PCB otherwise 100LFM airflow is required.	–40		85	°C
DIFFERENTIALINPUTS						
V_{ID}	Receiver peak-to-peak differential input voltage(2)	$dR_{(in)}$ ≤ 4.25 Gbps	100		1750	mV_{PP}
		1.25 Gbps < $dR_{(in)}$ ≤ 4.25 Gbps	100		1560	mV_{PP}
		$dR_{(in)}$ > 4.25 Gbps	100		1000	mV_{PP}
V_{ICM}	Receiver common-mode input voltage	Note: for best jitter performance ac coupling is recommended.	1.5	1.6	$V_{CC} - \frac{\lvert V_{ID} \rvert}{2}$	V
CONTROL INPUTS						
V_{IH}	High-level input voltage		2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
DIFFERENTIAL OUTPUTS						
R_L	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
(2) Differential input voltage V_{ID} is defined as | IN+ – IN– |.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DIFFERENTIAL INPUTS							
V_{IT+}	Positive going differential input high threshold					50	mV
V_{IT-}	Negative going differential input low threshold			–50			mV
$A_{(EQ)}$	Equalizer gain	at 1.875 GHz (EQ=1)			9		dB
$R_{T(D)}$	Termination resistance, differential			80	100	120	Ω
V_{BB}	Open-circuit Input voltage (input self-bias voltage)	AC-coupled inputs			1.6		V
$R_{(BBDC)}$	Biasing network dc impedance				30		kΩ
$R_{(BBAC)}$	Biasing network ac impedance	375 MHz			42		Ω
		2.125 GHz			8.4		
DIFFERENTIAL OUTPUTS							
V_{ODH}	High-level output voltage	R_L = 100 Ω ±1%, Figure 3			650		mV_{PP}
V_{ODL}	Low-level output voltage				–650		mV_{PP}
V_{ODB}	Output differential voltage without pre-emphasis(2)			1000	1300	1500	mV_{PP}
V_{OCM}	Output common mode voltage	See Figure 2			1.8		V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				1		mV
$V_{(PE)}$	Output preemphasis voltage ratio, $\frac{V_{ODB(PP)}}{V_{ODPE(PP)}}$	R_L = 100 Ω ±1%; x = L or S; See Figure 3			0		dB
					3		
					6		
					10		
$t_{(PRE)}$	Preemphasis duration measurement	Output preemphasis is set to 10 dB during test Measured with a 100-MHz clock signal; R_L = 100 Ω ±1%, See Figure 4			175		ps
r_o	Output resistance	Differential on-chip termination between OUT+ and OUT–			100		Ω
CONTROL INPUTS							
I_{IH}	High-level Input current	VIN = VCC				5	µA
I_{IL}	Low-level Input current	VIN = GND		–125	–90		µA
$R_{(PU)}$	Pullup resistance				35		kΩ
POWER CONSUMPTION							
P_D	Device power dissipation	All outputs terminated 100 Ω				1.32	W
P_Z	Device power dissipation in 3-State	All outputs in 3-state				684	mW
I_{CC}	Device current consumption	All outputs terminated 100 Ω	PRBS 2^{7-1} pattern at 4.25 Gbps			380	mA

(1) All typical values are at T_A = 25°C and V_{CC} = 3.3 V supply unless otherwise noted. They are for reference purposes and are not production tested.

(2) Differential output voltage $V_{(ODB)}$ is defined as | OUT+ – OUT– |.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
DIFFERENTIAL OUTPUTS								
t_{PLH}	Low-to-high propagation delay	Propagation delay input to output, See Figure 6				0.4	0.8	ns
t_{PHL}	High-to-low propagation delay					0.4	0.8	ns
t_r	Rise time	20% to 80% of $V_{O(DB)}$; Test Pattern: 100-MHz clock signal; See Figure 5 and Figure 8				90		ps
t_f	Fall time					90		ps
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$ (2)						11	ps
$t_{sk(o)}$	Output skew (3)	All outputs terminated with 100 Ω				25	75	ps
$t_{sk(pp)}$	Part-to-part skew (4)						150	ps
t_{zd}	3-State switch time to Disable	Assumes 50 Ω to Vcm and 150 pF load on each output					30	ns
t_{ze}	3-State switch time to Enable	Assumes 50 Ω to Vcm and 150 pF load on each output					20	ns
RJ	Device random jitter, rms	See Figure 8 for test circuit. BERT setting 10^{-15} Alternating 10-pattern.				0.8	2	ps-rms
DJ	Intrinsic deterministic device jitter (5), peak-to-peak	0 dB preemphasis See Figure 8 for the test circuit.	PRBS 2^{7-1} pattern	4.25 Gbps			30	ps
DJ	Absolute deterministic output jitter (6), peak-to-peak	0 dB preemphasis See Figure 8 for the test circuit.	PRBS 2^{7-1} pattern	1.25Gbps; EQ=13 Over 25-inch FR4 trace		12		ps
				4.25 Gbps; EQ=0 Over FR4 trace 2-inch to 43 inches long		20		

(1) All typical values are at 25°C and with 3.3 V supply unless otherwise noted.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(5) The SN65LVCP418 built-in passive input equalizer compensates for ISI. For a 25-inch FR4 transmission line with 8-mil trace width, the LVCP418 typically reduces jitter by 33 ps from the device input to the device output.
(6) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP418 output. The value is a real measured value with a Bit error tester as described in Figure 8. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP418))}$.

PARAMETER MEASUREMENT INFORMATION

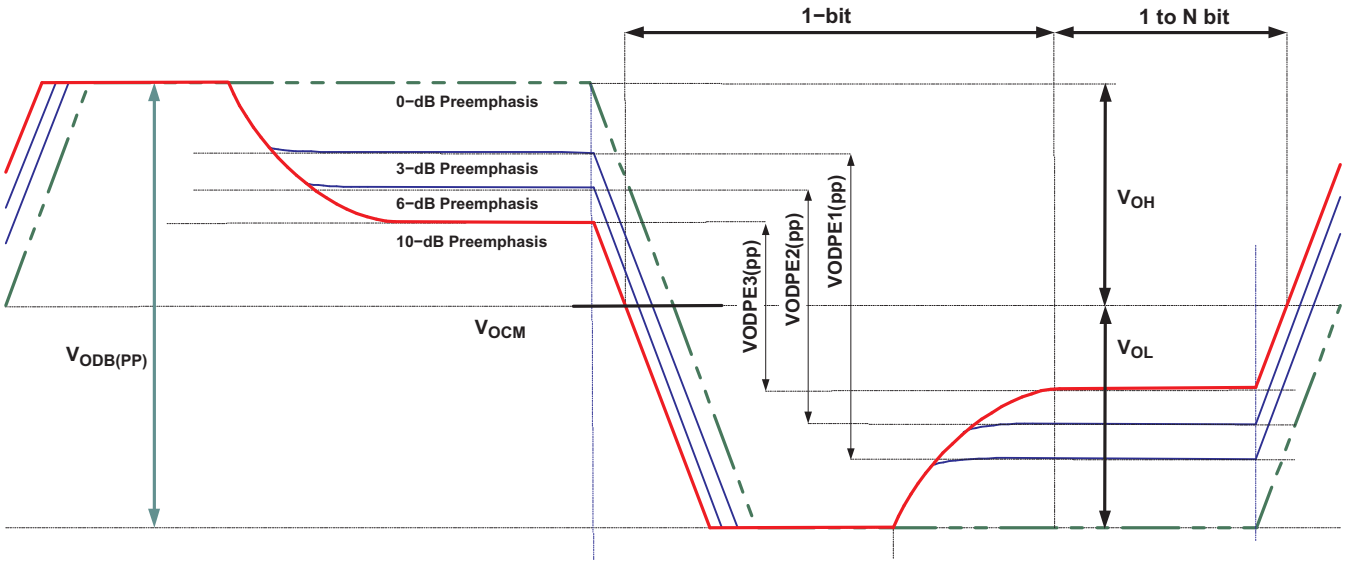


Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

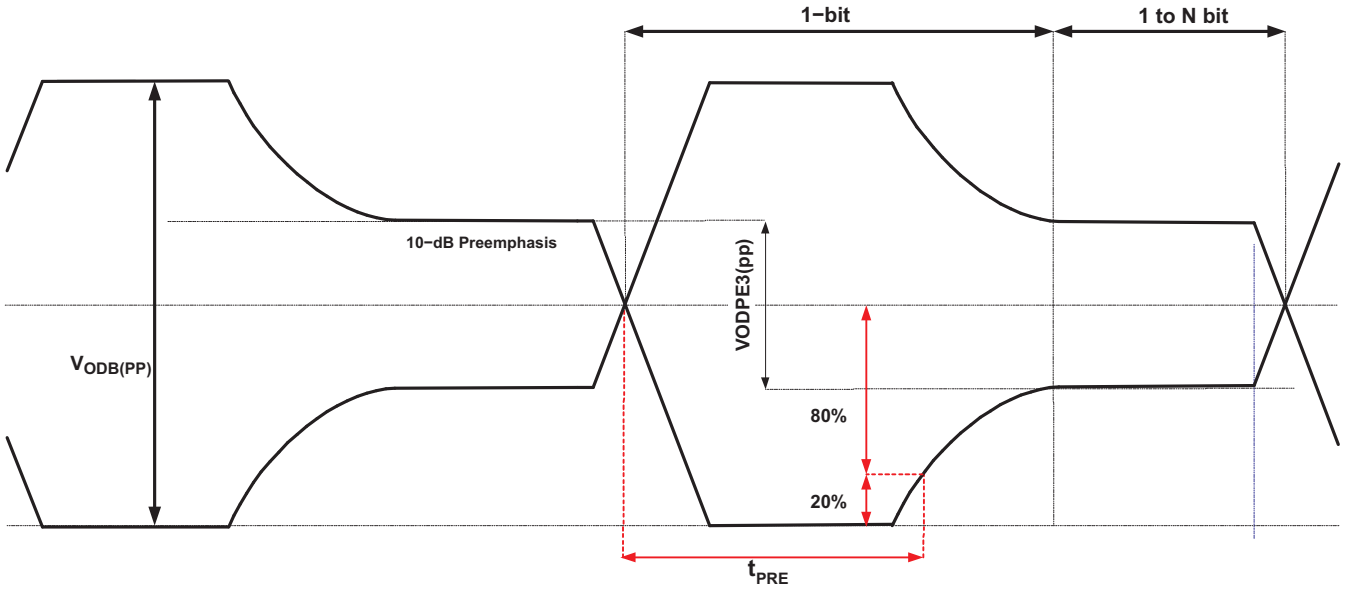


Figure 4. $t_{(PRE)}$ Preemphasis Duration Measurement

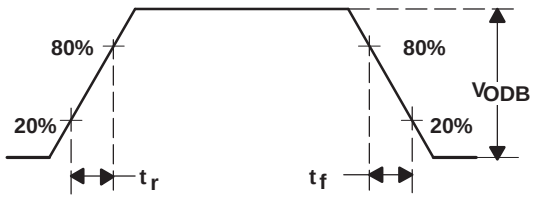


Figure 5. Driver Output Transition Time

PARAMETER MEASUREMENT INFORMATION (continued)

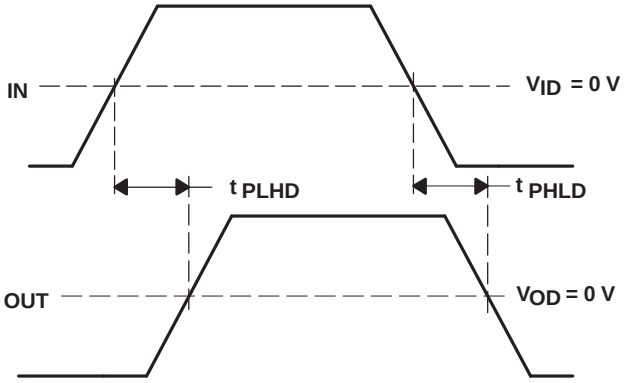
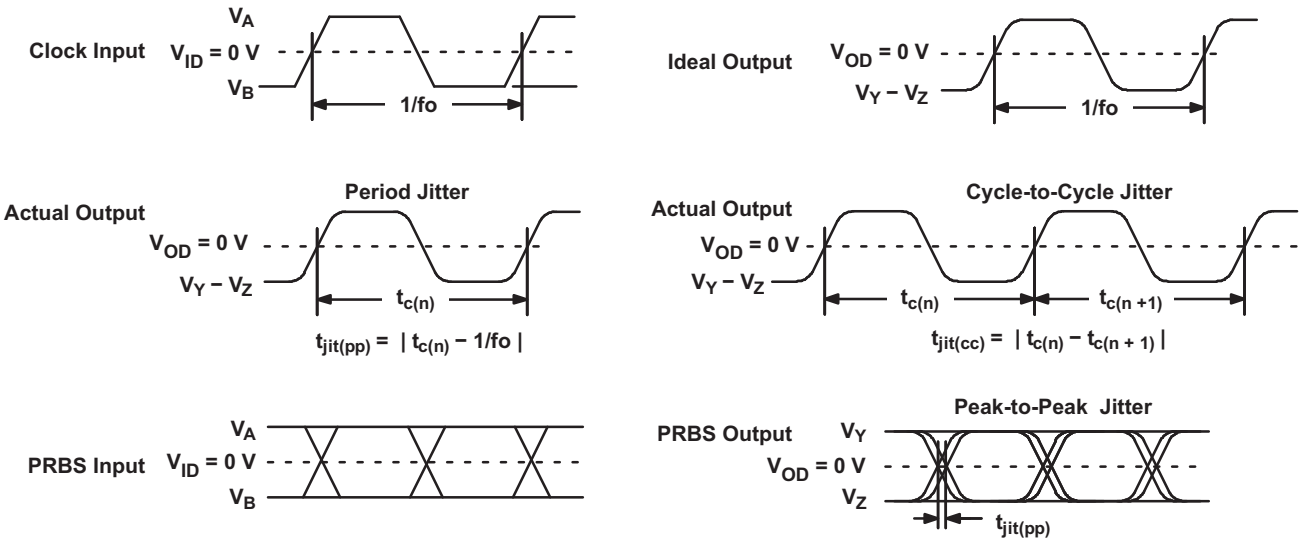


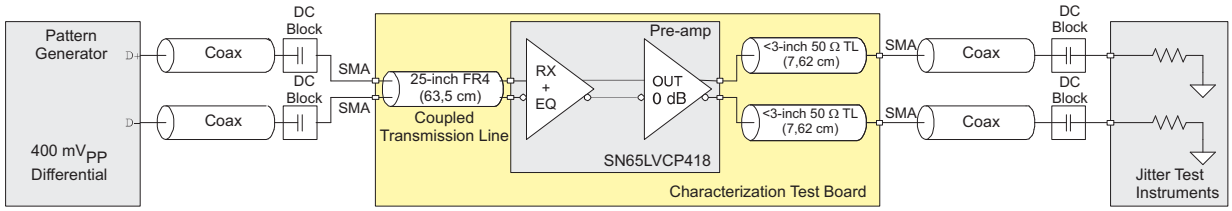
Figure 6. Propagation Delay Input to Output



A. All input pulses are supplied by an Agilent 81250 Stimulus System.

B. The measurement is made with the AgilentParBert measurement software.

Figure 7. Driver Jitter Measurement Waveforms



For the rise/fall time measurements, the 25-inch FR4 transmission line is removed.

Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

The SN65LVCP418 input equalizer provides frequency gain to compensate for frequency loss of a shorter backplane transmission line. For characterization purposes, a 25-inch (63,5 cm) FR-4 coupled transmission line is used in place of the backplane trace. The 25-inch trace provides roughly 5 dB of attenuation between 375 MHz and 2.125 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective ε(r) of 4.1.

TYPICAL DEVICE BEHAVIOR

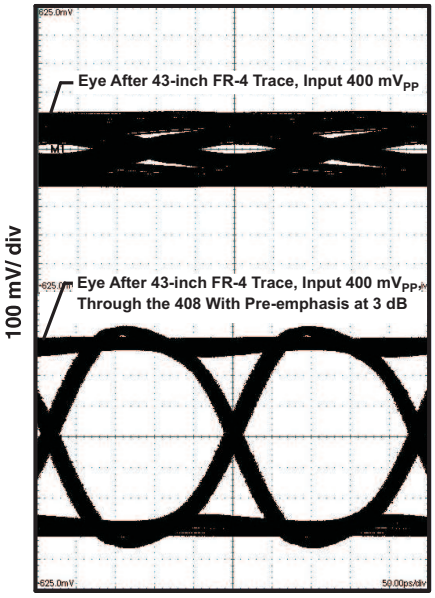


Figure 9. Data Input and Output Pattern

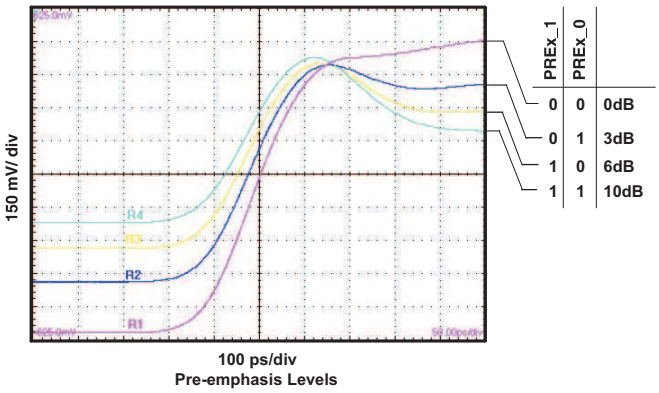


Figure 10. Preemphasis Signal Shape

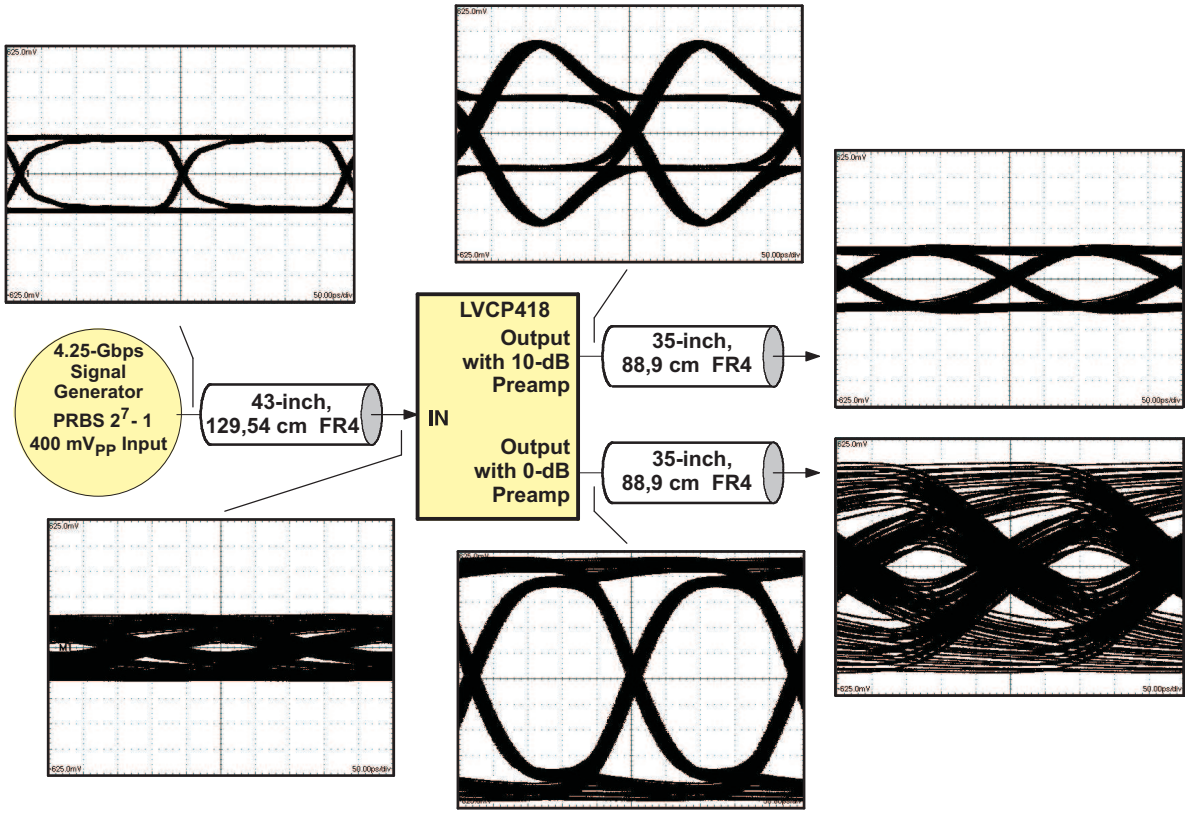


Figure 11. Data Output Pattern

TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs DATA RATE

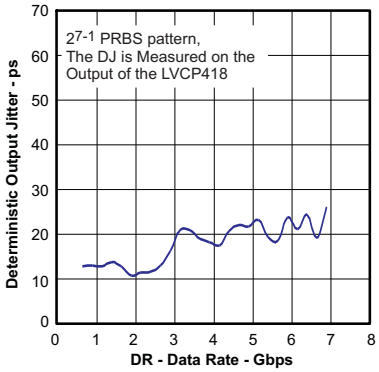


Figure 12.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

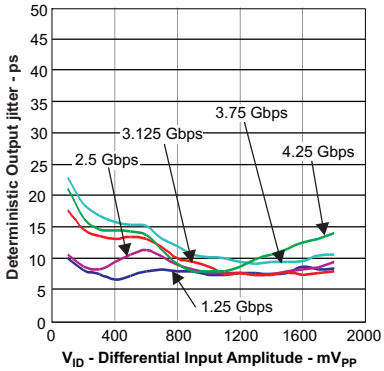


Figure 13.

DIFFERENTIAL OUTPUT VOLTAGE vs DATA RATE

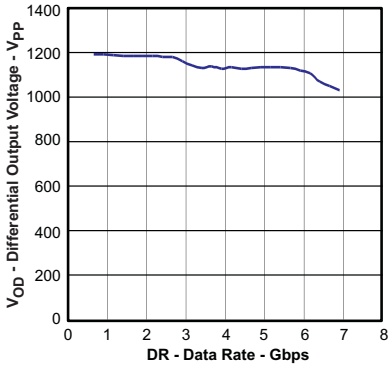


Figure 14.

SUPPLY NOISE vs DETERMINISTIC JITTER vs DATA RATE

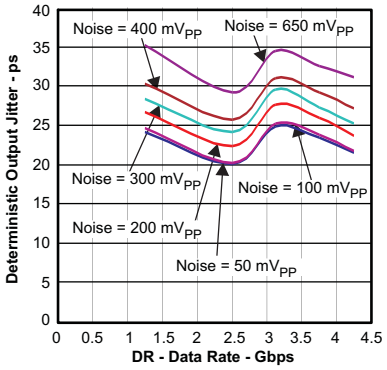


Figure 15.

DETERMINISTIC OUTPUT JITTER vs COMMON-MODE INPUT VOLTAGE

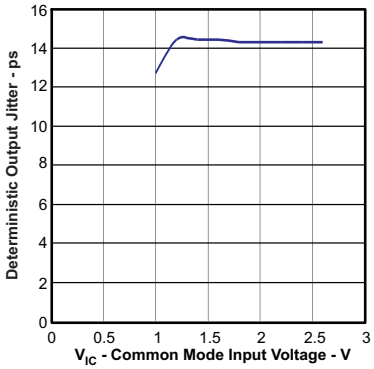


Figure 16.

I²C CONTROL INTERFACE

I²C Interface Notes

The I²C interface is used to access the internal registers of the SN65LVCP418. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The SN65LVCP418 works as a slave and supports the standard mode transfer (100 kbps) .

The basic I²C start and stop access cycles are shown in Figure 17. The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

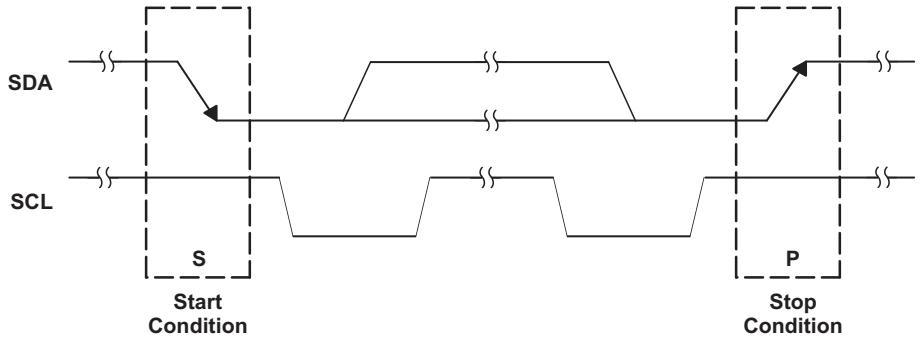


Figure 17. I²C Start and Stop Conditions

General I²C Protocol

- The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 17. All I²C-compatible devices should recognize a start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 18). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 19) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/$\overline{W}$ bit 0) or receive data from the slave (R/$\overline{W}$ bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 20).
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 17). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.
- All bytes are transmitted most significant bit first.

Table 1. I²C Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency for internal register	Local I²C			100	kHz
$t_{W(L)}$	Clock LOW period for I²C register	Local I²C	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Local I²C	4			µs
t_{SU1}	Internal register setup time, SDA to SCL	Local I²C	250			µs
$t_{h(1)}$	Internal register hold time, SCL to SDA	Local I²C	0			µs
$t_{(buf)}$	Internal register bus free time between STOP and START	Local I²C	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Local I²C	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Local I²C	4			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Local I²C	4			µs

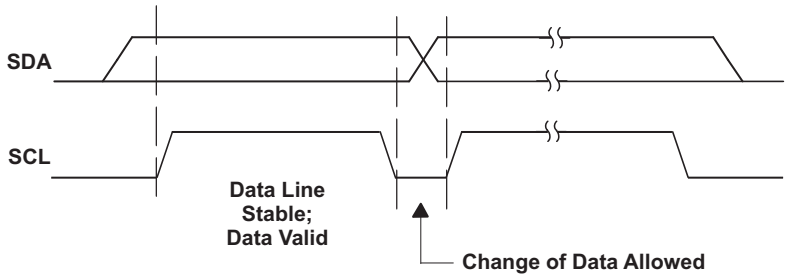


Figure 18. I²C Bit Transfer

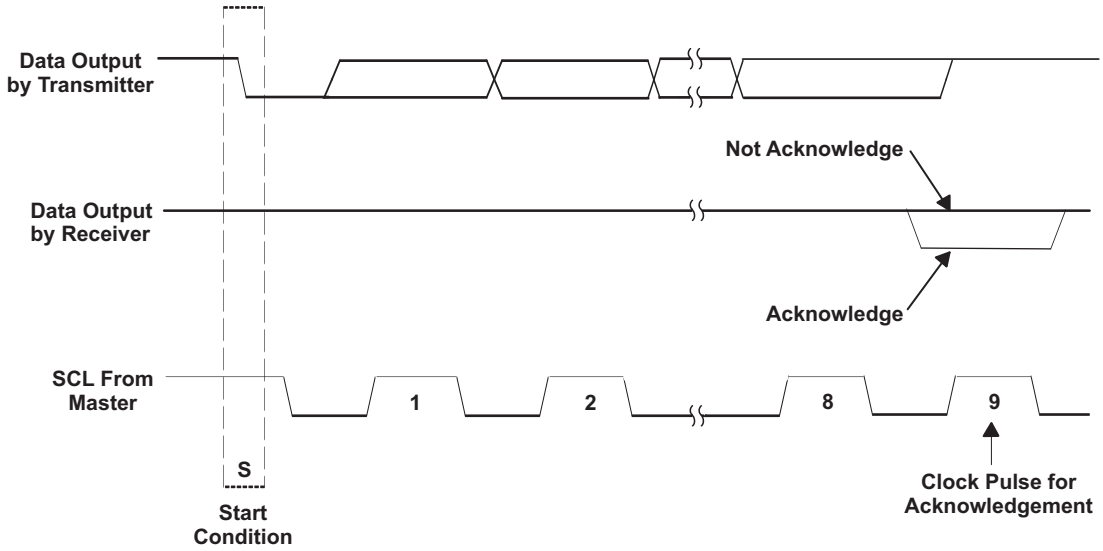


Figure 19. I²C Acknowledge

Note: Following power up, this device must be reset.

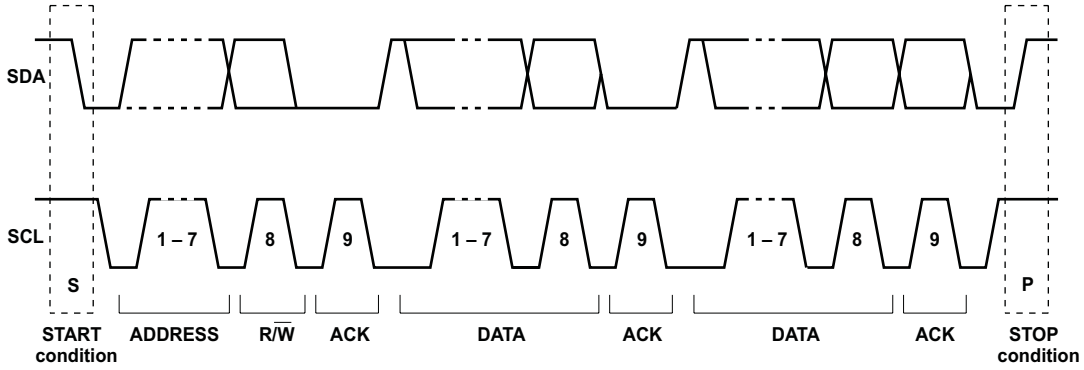


Figure 20. I²C Address and Data Cycles

During a write cycle, the slave sends an acknowledge (A) after every byte that follows the device address. The first byte following the device address is the register address, which maps to the register addresses specific to the device. The second byte following the device address is the data byte to be written at the register address (see Figure 21). If only the register address is to be written for a subsequent read sequence, the data byte is omitted and the sequence ends with a Stop (see Figure 22) or a repeated Start after the register address byte (see Figure 24). If multiple data bytes are to be written at subsequent register addresses, the master may continue to send data bytes after each slave acknowledge, and the slave device automatically increments the register address. Note that the master must not drive the SDA signal line during the slave acknowledge since the slave is in control of the SDA bus and may be holding it low.

During a read cycle, the slave acknowledges the initial address byte if it decodes the device address as its own device address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. The first byte received by the master is the data stored at the register address, while subsequent bytes are data stored at incrementing register addresses. When the master has received all of the requested data bytes from the slave, the not acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the Stop (P) condition. This sequence terminates a read cycle as shown in Figure 23. A combined format is when the read cycle is preceded by a write cycle for setting the register address, and is shown in Figure 24.

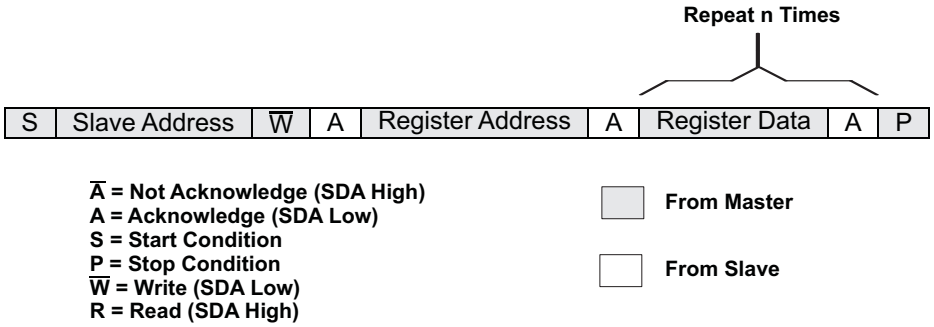


Figure 21. I²C Write Cycle with Register Address and Data

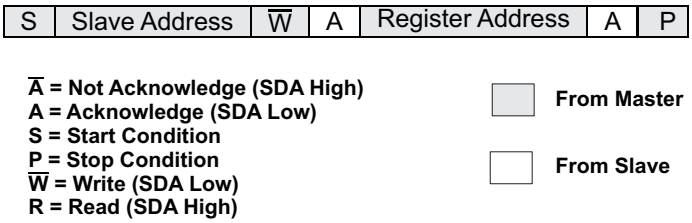


Figure 22. I²C Write Cycle with Register Address Only

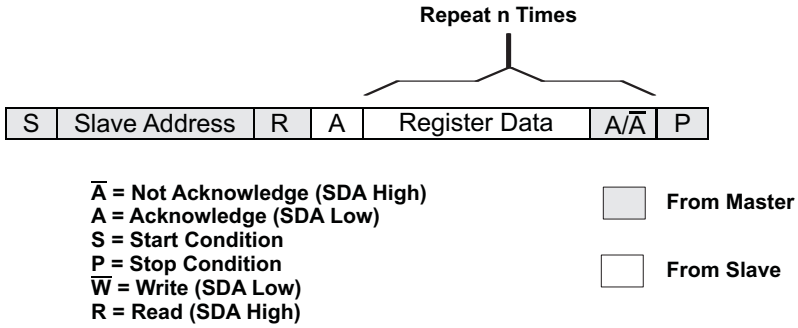


Figure 23. I²C Read Cycle

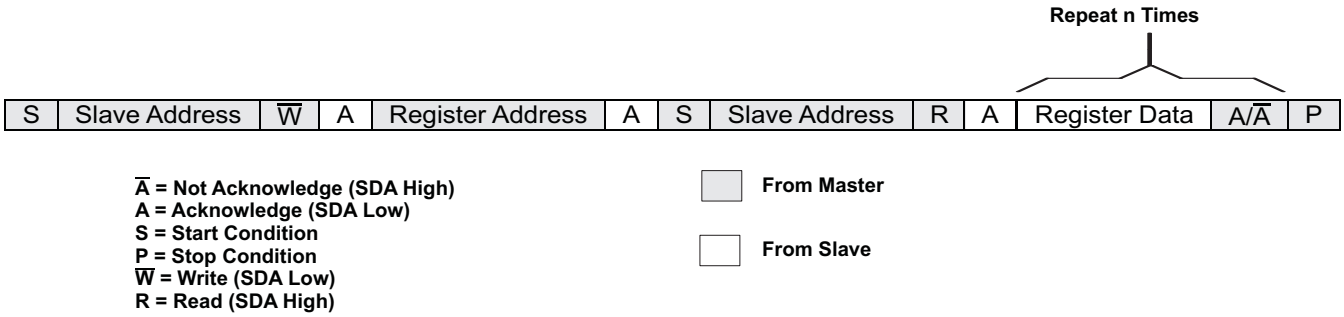


Figure 24. I²C Combined Format Write/Read Cycle

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The slave address is the first 7 bits received following the START condition from the master device. The first 5 Bits (MSBs) of the address are factory preset to 01011. The next two bits of the SN65LVCP408 address are controlled by the logic levels appearing on the ADDR2 and ADDR1 pins. The ADDR2 and ADDR1 address inputs can be connected to VCC for logic 1, GND for logic 0, or can be actively driven by TTL/CMOS logic levels. The device addresses are set by the state of these pins and are not latched. Thus a dynamic address control system could be utilized to incorporate several devices on the same system. Up to four SN65LVCP408 devices can be connected to the same I²C-Bus without requiring additional glue logic. Table 2 lists the possible addresses for the SN65LVCP408.

Table 2. Slave Addresses

Fixed Address			Fixed Address		Selectable with Address Pins		
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1 (addr2)	Bit 0 (addr1)
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1

Note: Following power up, this device must be reset.

Table 3. Port Register Addresses

Register Name	Register Address
Output Port 0	0000 0000
Output Port 1	0000 0001
Output Port 2	0000 0010
Output Port 3	0000 0011
Output Port 4	0000 0100
Output Port 5	0000 0101
Output Port 6	0000 0110
Output Port 7	0000 0111
Input Port 0	0000 1000
Input Port 1	0000 1001
Input Port 2	0000 1010
Input Port 3	0000 1011
Input Port 4	0000 1100
Input Port 5	0000 1101
Input Port 6	0000 1110
Input Port 7	0000 1111
Reserved for TI use only	0000 0001 to 0001 1001

Table 4. Output Port Control Registers

Bit	Function	Default	Note	ACCESS
7	RSVD	0	Reserved	R/W
6		0		
5		0		
4	Pre-Emphasis	00	Pre-emphasis setting. Valid values are: 00 = 0 dB; 01 = 3 dB; 10 = 6 dB, and 11= 10 dB. Note: When EN = 0, then the PRE pin is used to set the pre-emphasis setting rather than the I^2C register map.	
3				
2	Port 3-State	0	3-State Off = 0; 3-State On = 1	R/W
1	RSVD	0	Reserved	R
0	RSVD	0	Reserved	

Table 5. Input Port Control Registers

Bit	Function	Default	Note	Access
7	Rx Equalization Select	0	Rx Equalization Setting; 0 = 13 dB; 1=9dB; Note: When EN=0 then the EQ pin is used to set the Equalization setting rather than the I^2C register map.	R/W
6	RSVD	0	Reserved	
5	RSVD	0	Reserved	
4	RSVD	0	Reserved	
3	RSVD	0	Reserved	R
2	RSVD	0	Reserved	
1	RSVD	0	Reserved	
0	RSVD	0	Reserved	

Note: Following power up, this device must be reset.

Table 6. Reserved For TI Use (0001 0000)

Bit	Function	Default	Note	Access
5:6	RSVD	–	Reserved	R/W
5:1	RSVD	–	Reserved	R

Table 7. Reserved For TI Use (0001 0001 to 0001 1010)

Bit	Function	Default	Note	Access
7:0	RSVD	–	Read only. Value is indeterministic.	R

APPLICATION INFORMATION

BANDWIDTH REQUIREMENTS

Error free transmission of data over a transmission line has specific bandwidth demands. It is helpful to analyze the frequency spectrum of the transmit data first. For an 8B10B coded data stream at 3.75 Gbps of random data, the highest bit transition density occurs with a 1010 pattern (1.875 GHz). The least transition density in 8B10B allows for five consecutive ones or zeros. Hence, the lowest frequency of interest is 1.875 GHz/5 = 375 MHz. Real data signals consist of higher frequency components than sine waves due to the fast rise time. The faster the rise time, the more bandwidth becomes required. For 80-ps rise time, the highest important frequency component is at least 0.6/(π × 80 ps) = 2.4 GHz. Figure 25 shows the Fourier transformation of the 375-MHz and 1.875-GHz trapezoidal signal.

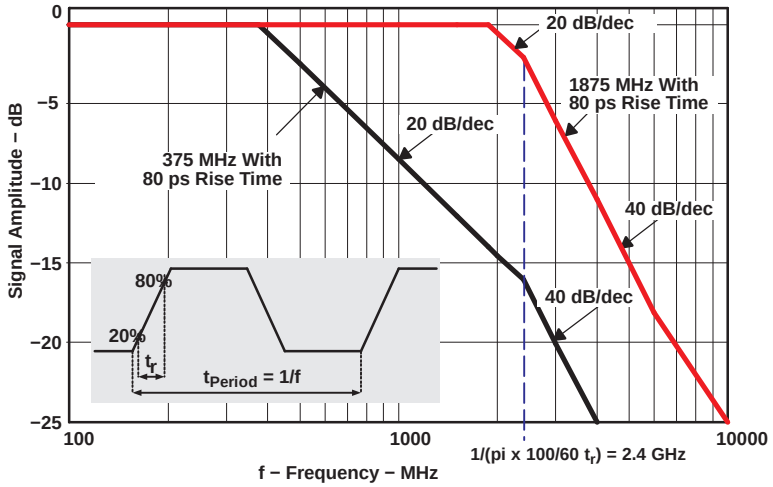


Figure 25. Approximate Frequency Spectrum of the Transmit Output Signal With 80 ps Rise Time

The spectrum analysis of the data signal suggests building a backplane with little frequency attenuation up to 2 GHz. This is achievable only with expensive, specialized PCB material. To support material like FR4, a compensation technique is necessary to compensate for backplane imperfections.

EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stack-up, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material and its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially – often ranging from 8 inches up to 40 inches. Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the frequency signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB while the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency dependent loss causes distortion jitter on the transmitted signal. Each LVCP418 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP418 equalizer provides 5 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches of FR4 material with 8-mil trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable pre-emphasis such as LVCP418) and the LVCP418 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the LVCP418 receiver output.
2. Increase the transmitter preemphasis until the data eye on the LVCP418 receiver output looks the cleanest.

REVISION HISTORY

Changes from Original (June 2009) to Revision A	Page
• Changed Table 4, row - Port 3-State From: Access = R To: Access = R/W	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVCP418PAPR	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP418	Samples
SN65LVCP418PAPT	ACTIVE	HTQFP	PAP	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP418	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

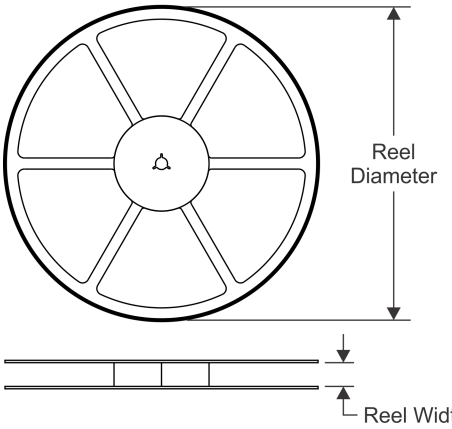
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

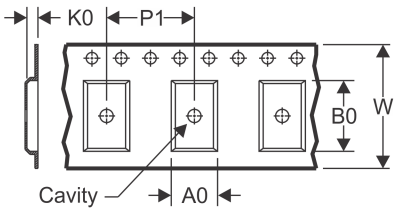
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

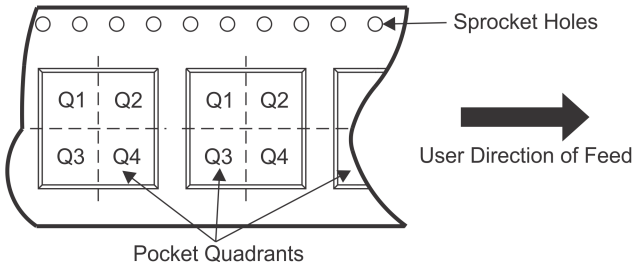


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

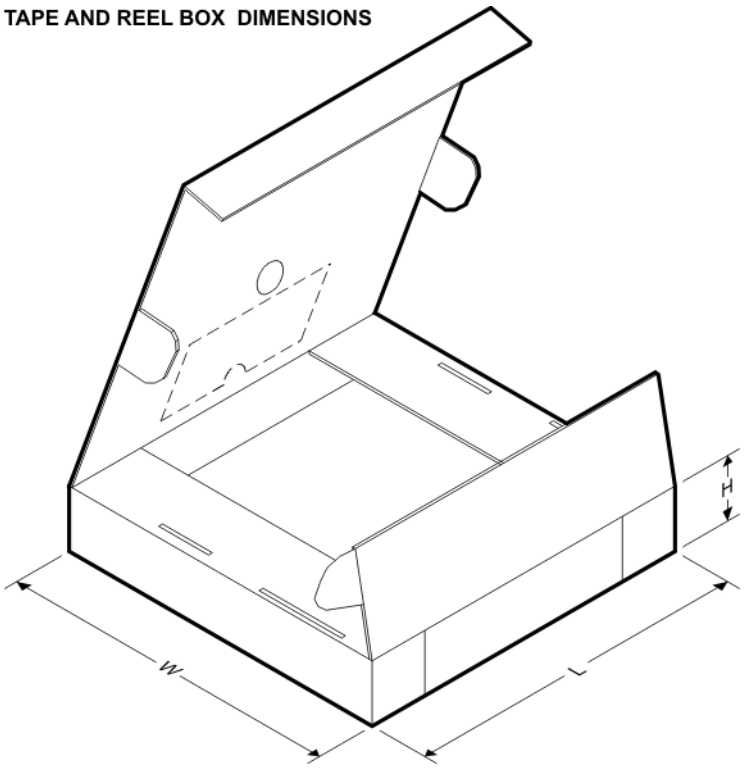
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP418PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
SN65LVCP418PAPT	HTQFP	PAP	64	250	180.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

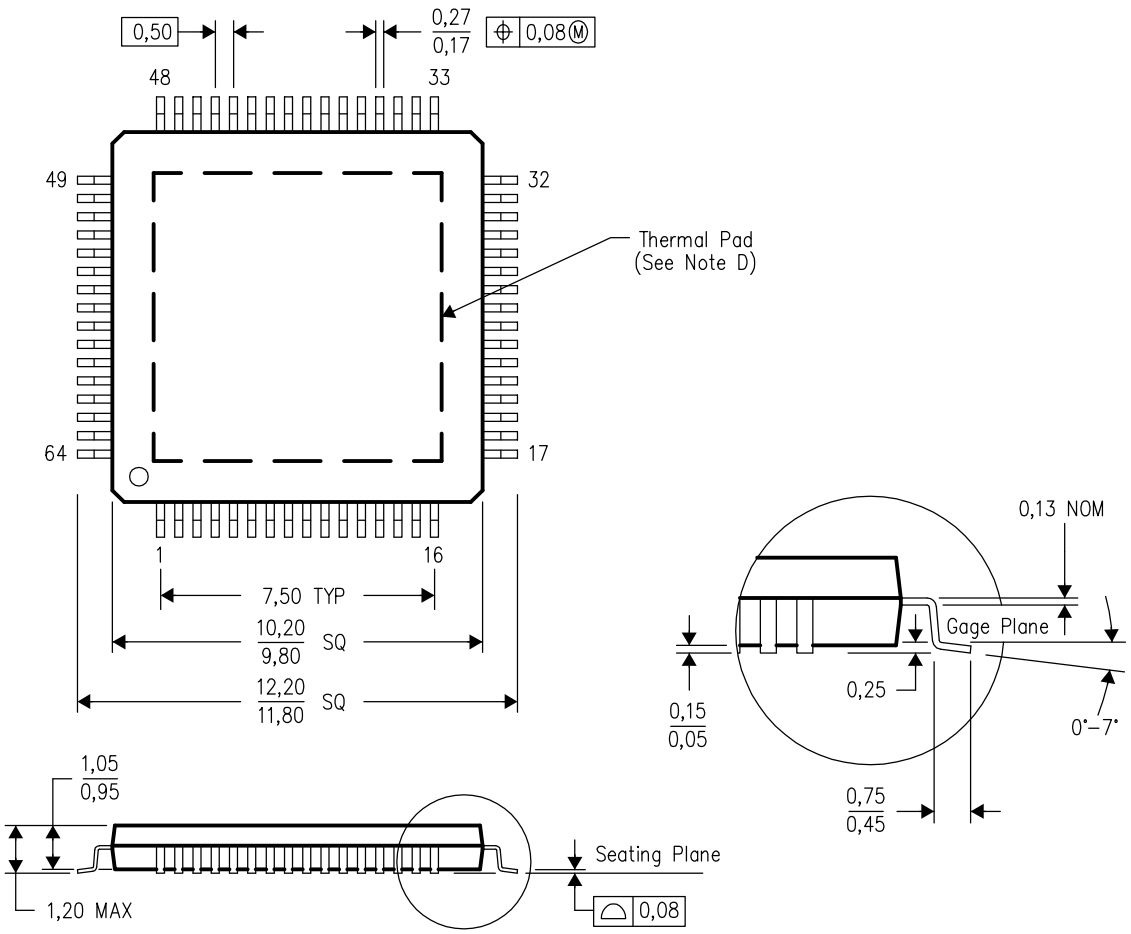
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP418PAPR	HTQFP	PAP	64	1000	367.0	367.0	45.0
SN65LVCP418PAPT	HTQFP	PAP	64	250	213.0	191.0	55.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

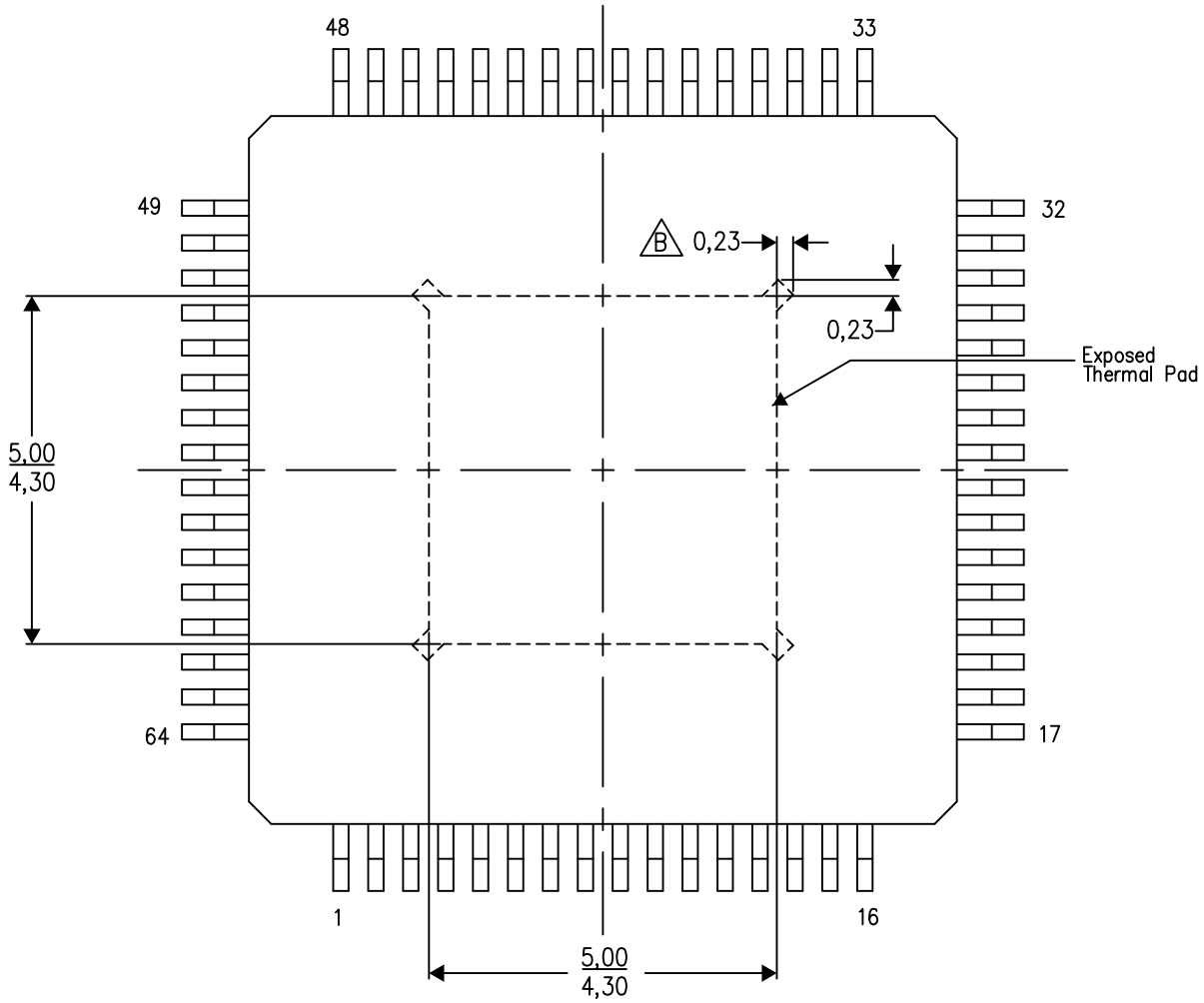
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–3/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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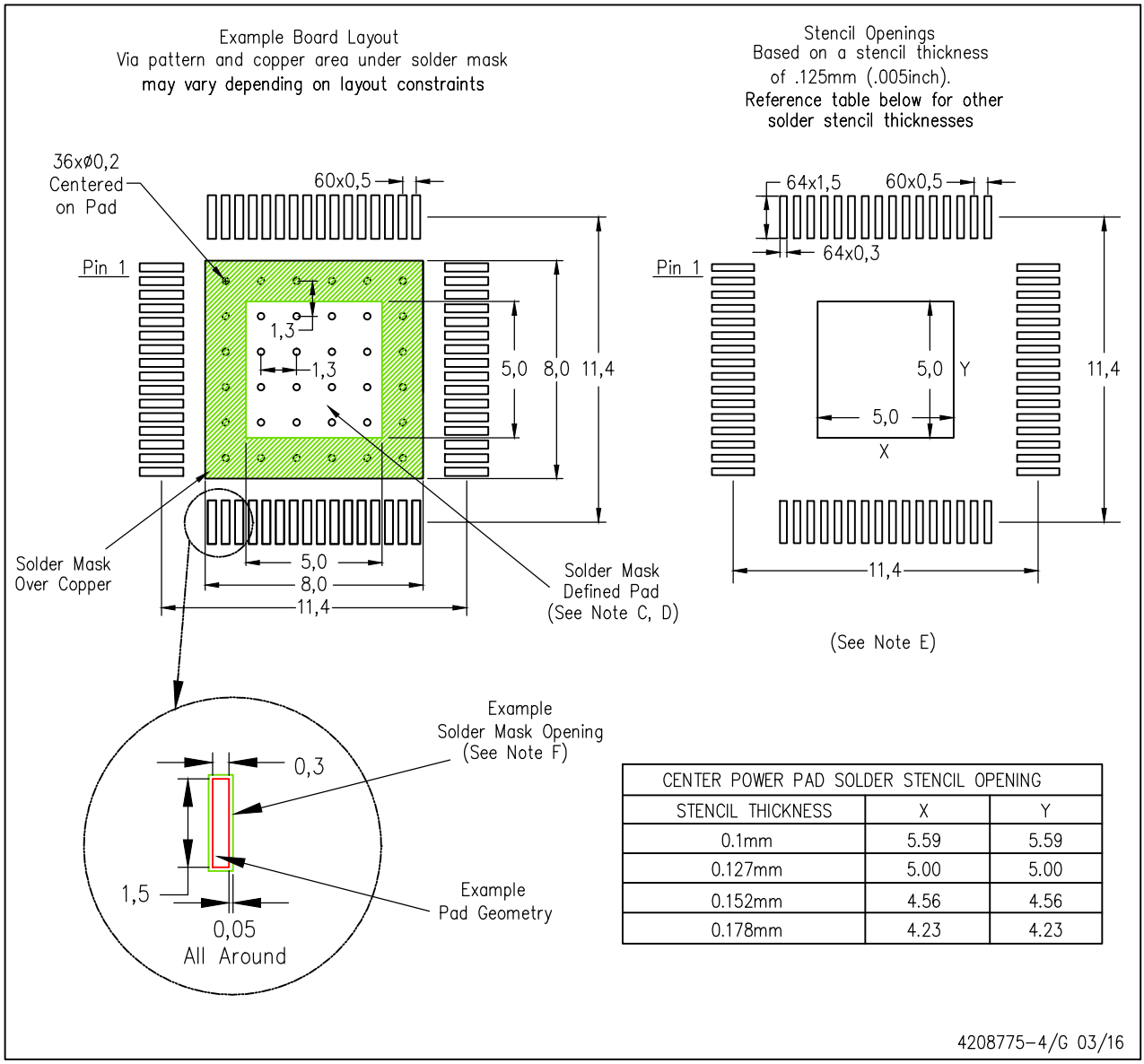
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	5.59	5.59
0.127mm	5.00	5.00
0.152mm	4.56	4.56
0.178mm	4.23	4.23

4208775–4/G 03/16

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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